

## MM5034/MM5035 Octal 80-Bit Static Shift Register

### General Description

The MM5034 octal 80-bit shift register is a monolithic MOS integrated circuit utilizing N-channel low threshold enhancement mode and ion-implanted depletion mode devices.

The MM5034 is designed for use in computer display peripherals. All inputs and outputs are TTL compatible. The clocks and recirculate logic are internal to reduce system component count, and TRI-STATE® output buffers provide bus interface. Because of its N-channel characteristics, single 5V power supply operation is required.

Simple interface to the NSC CRT DP8350 controller and character generator to incorporate an entire CRT terminal is feasible with the MM5034.

The MM5034 is available in a 22-lead dual-in-line package.

The MM5035 is a 20-pin version of the MM5034 with the TRI-STATE output select feature omitted, for a simple data in/data out operation.

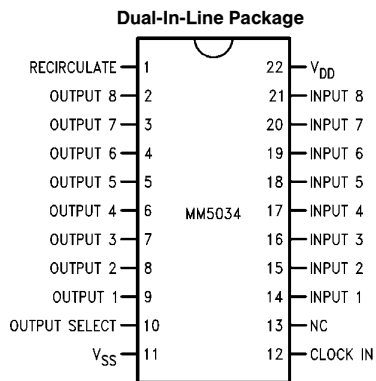
### Features

- Single 5V power supply
- Internal clocks
- High speed and static operation
- TRI-STATE output buffer
- Recirculate and output select independent
- TTL compatible

### Applications

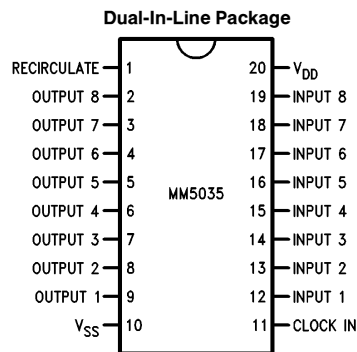
- CRT displays
- Computer peripherals

### Connection Diagrams



Order Number MM5034N  
See NS Package Number N22A

TL/F/10821-1



Order Number MM5035N  
See NS Package Number N20A

TL/F/10821-2

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## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7 V<sub>DC</sub>  
Input Voltage 7 V<sub>DC</sub>

Power Dissipation 750 mW  
Storage Temperature Range –65°C to +150°C  
Lead Temperature (Soldering, 10 sec.) 300°C

## Electrical Characteristics V<sub>DD</sub> = 5V ± 5%, T<sub>A</sub> = 0°C to +70°C

Parameter	Conditions	Min	Typ	Max	Units
Clock Input					
Logical “1” Input Voltage		2.2			V
Logical “0” Input Voltage				0.8	V
Data and Control Inputs					
Logical “1” Input Voltage		2.2			V
Logical “0” Input Voltage				0.8	V
Data, Clock and Control Inputs					
Logical “1” Input Current	V <sub>IN</sub> = 5V			5.0	μA
Input Capacitance	V <sub>IN</sub> = 2.5V		5.0	8.0	pF
Outputs					
Logical “1” Output Voltage	I <sub>OUT</sub> = 100 μA	2.4	2.8		V
Logical “0” Output Voltage	I <sub>OUT</sub> = 1.6 mA		0.25	0.4	V
TRI-STATE Output Current	V <sub>OUT</sub> = 5V			–5.0	μA
	V <sub>OUT</sub> = 0V			5.0	μA
Supply Current			60	90	mA
Timing					
Clock Frequency		0		3.0	MHz
Clock Pulse Width High	(Figure 1)	125		10,000	ns
Clock Pulse Width Low	(Note 1)	125		∞	ns
Output Rise and Fall Time (t <sub>r</sub> , t <sub>f</sub> )	(Figure 1)		40	50	ns
Set-Up Time	(Figure 1)	100			ns
Hold Time	(Figure 1)	0			ns
Output Enable Time	(Figure 1)			185	ns
Output Disable Time	(Figure 1)			185	ns
Clock Rise and Fall Time	(Figure 1)			5.0	μs
Output Delay, (t <sub>PD</sub> )			80	185	ns

**Note 1:** The clock input must be a low level for DC storage. Minimum width assumes 10 ns t<sub>r</sub> and t<sub>f</sub>.

## Recirculate and TRI-STATE Operation

Recirculate is used to maintain data in the shift register after it has been loaded. While the shift register is being loaded, Recirculate must be at a logical “0”. When the loading is completed, Recirculate should be brought to a logical “1”. This disables the data input and feeds the output of the last

shift cell back to the input of the first shift cell for each of the 8 registers.

For the output to be in the TRI-STATE mode output-select should be at the logical “1” level.

## AC Test Circuits and Switching Time Waveforms

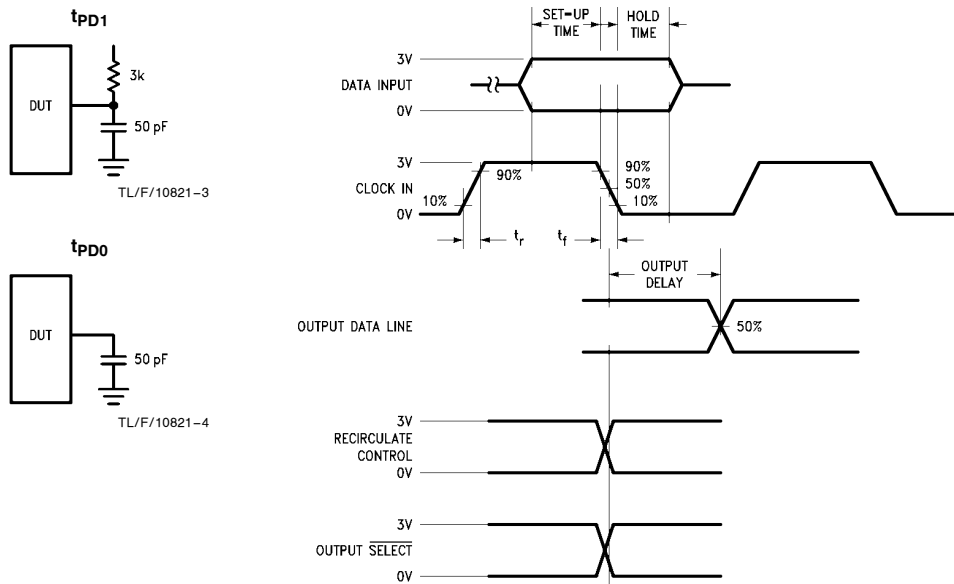


FIGURE 1

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## Typical Application

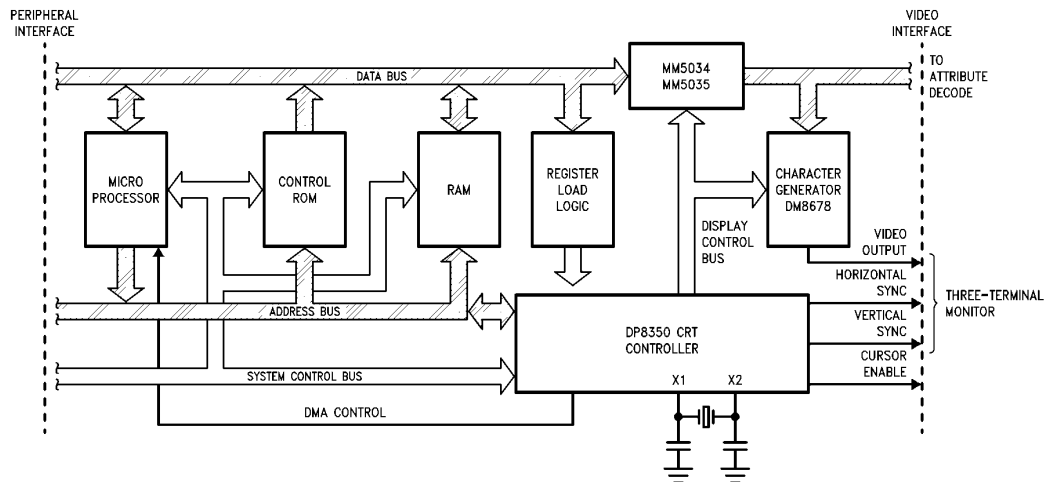
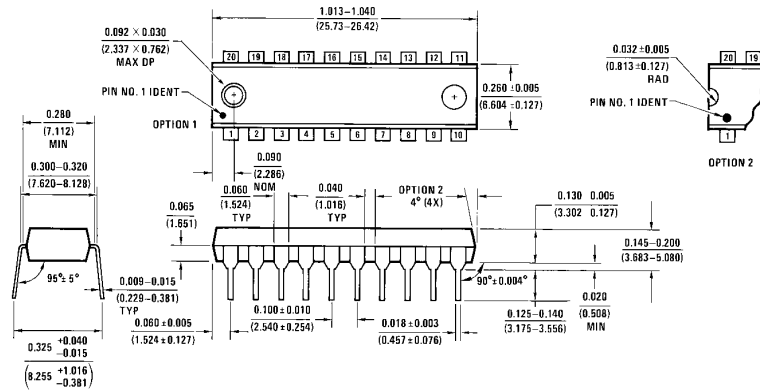
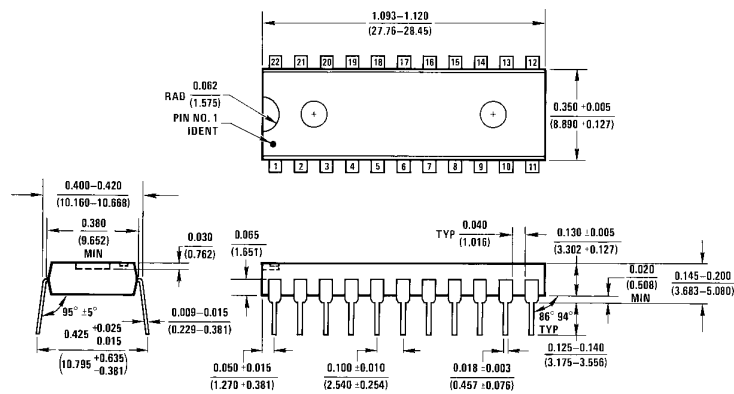


FIGURE 2. CRT System Diagram Using the MM5034, MM5035 as a Line Buffer with DMA

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**Physical Dimensions** inches (millimeters)

**20-Lead Molded Dual-In-Line Package (N)**  
**Order Number MM5035N**  
**NS Package Number N20A**



**22-Lead Molded Dual-In-Line Package (N)**  
**Order Number MM5034N**  
**NS Package Number N22A**

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**National Semiconductor Corporation**  
 1111 West Bardin Road  
 Arlington, TX 76017  
 Tel: 1(800) 272-9959  
 Fax: 1(800) 737-7018

**National Semiconductor Europe**

Fax: (+49) 0-180-530 85 86  
 Email: cnjwge@tevm2.nsc.com  
 Deutsch Tel: (+49) 0-180-530 85 85  
 English Tel: (+49) 0-180-532 78 32  
 Français Tel: (+49) 0-180-532 93 58  
 Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**

19th Floor, Straight Block,  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: (852) 2737-1600  
 Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**

Tel: 81-043-299-2309  
 Fax: 81-043-299-2408