November 2003

Features

- Supports AT&T TR62411 and Bellcore GR-1244-CORE, Stratum 4 Enhanced and Stratum 4 timing for DS1 interfaces
- Supports ETSI ETS 300 011, TBR 4, TBR 12 and TBR 13 timing for E1 interfaces
- Selectable 19.44 MHz, 1.544MHz, 2.048MHz or 8kHz input reference signals
- Provides C1.5, C2, $\overline{C4}$, C6, C8, $\overline{C16}$, and C19 (STS-3/OC3 clock divided by 8) output clock signals
- Provides 5 different styles of 8 KHz framing pulses
- Attenuates wander from 1.9Hz
- Fast lock mode
- Provides Time Interval Error (TIE) correction
- Accepts reference inputs from two independent sources
- JTAG Boundary Scan

Applications

- Synchronization and timing control for multitrunk T1,E1 and STS-3/OC3 systems
- ST-BUS clock and frame pulse sources

Ordering Information

MT9043AN 48 pin SSOP

-40°C to +85°C

Description

The MT9043 T1/E1 System Synchronizer contains a digital phase-locked loop (DPLL), which provides timing and synchronization signals for multitrunk T1 and E1 primary rate transmission links.

The MT9043 generates ST-BUS clock and framing signals that are phase locked to either a 19.44 MHz, 2.048MHz, 1.544MHz, or 8kHz input reference.

The MT9043 is compliant with AT&T TR62411 and Bellcore GR-1244-CORE, Stratum 4 Enhanced, and Stratum 4; and ETSI ETS 300 011. It will meet the jitter/wander tolerance, jitter transfer, intrinsic jitter, frequency accuracy, capture range, phase change slope, and MTIE requirements for these specifications.

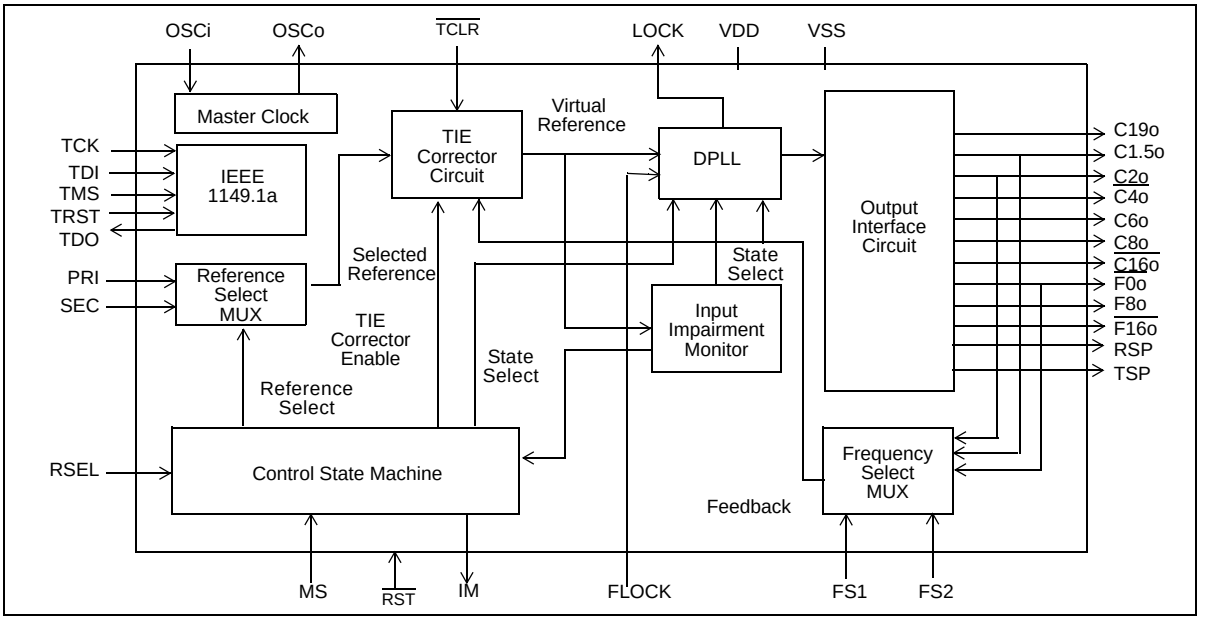


Figure 1 - Functional Block Diagram

Zarlink Semiconductor US Patent No. 5,602,884, UK Patent No. 0772912, France Brevete S.G.D.G. 0772912; Germany DBP No. 69502724.7-08

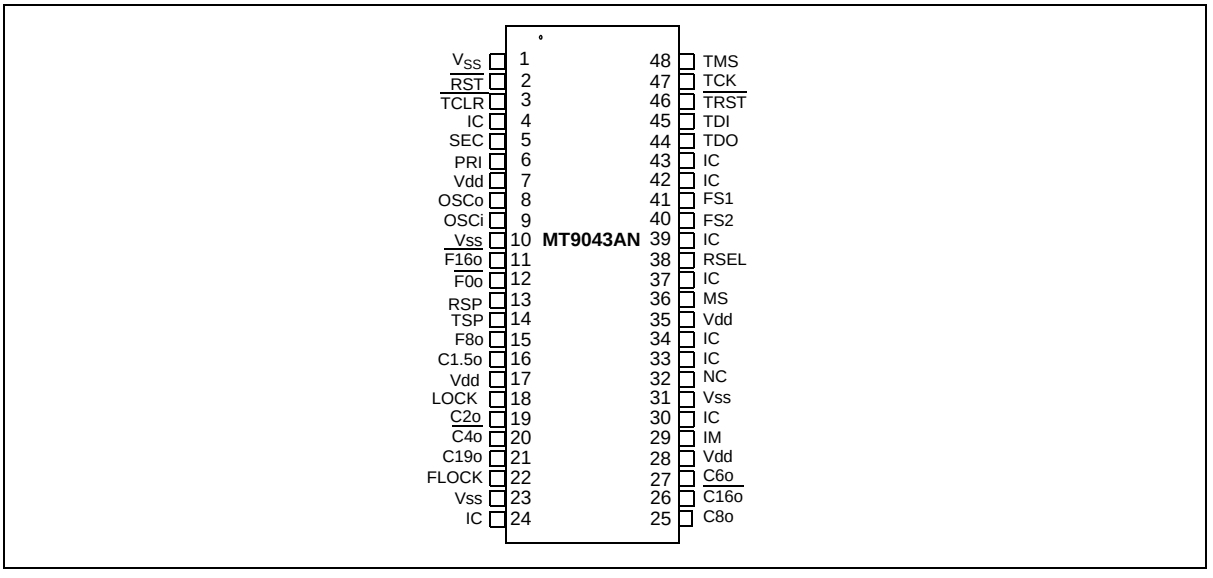


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1,10, 23,31	V_{SS}	**Ground.** 0 Volts. (Vss pads).
2	$\overline{RST}$	**Reset (Input).** A logic low at this input resets the MT9043. To ensure proper operation, the device must be reset after reference signal frequency changes and power-up. The RST pin should be held low for a minimum of 300ns. While the RST pin is low, all frame pulses except RST and TSP and all clock outputs except C6o, C16o and C19o are at logic high. The RST, TSP, C6o and C16o are at logic low during reset. The C19o is free-running during reset. Following a reset, the input reference source and output clocks and frame pulses are phase aligned as shown in Figure 12.
3	$\overline{TCLR}$	**TIE Circuit Reset (Input).** A logic low at this input resets the Time Interval Error (TIE) correction circuit resulting in a realignment of input phase with output phase as shown in Figure 13. The $\overline{TCLR}$ pin should be held low for a minimum of 300ns. This pin is internally pulled down to VSS.
4	IC	**Internal Connection.** Leave open circuit.
5	SEC	**Secondary Reference (Input).** This is one of two (PRI & SEC) input reference sources (falling edge) used for synchronization. One of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be used. The selection of the input reference is based upon the MS, and RSEL, control inputs.This pin is internally pulled up to V_{DD}.
6	PRI	**Primary Reference (Input).** See pin description for SEC. This pin is internally pulled up to V_{DD}.
7,17 28,35	V_{DD}	**Positive Supply Voltage.** +3.3V_{DC} nominal.
8	OSCo	**Oscillator Master Clock (CMOS Output).** For crystal operation, a 20MHz crystal is connected from this pin to OSCi, see Figure 9. Not suitable for driving other devices. For clock oscillator operation, this pin is left unconnected, see Figure 8.

Pin Description

Pin #	Name	Description
9	OSCi	**Oscillator Master Clock (CMOS Input).** For crystal operation, a 20MHz crystal is connected from this pin to OSCo, see Figure 9. For clock oscillator operation, this pin is connected to a clock source, see Figure 8.
11	$\overline{\text{F16o}}$	**Frame Pulse ST-BUS 8.192 Mb/s (CMOS Output).** This is an 8kHz 61ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mb/s. See Figure 14.
12	$\overline{\text{F0o}}$	**Frame Pulse ST-BUS 2.048Mb/s (CMOS Output).** This is an 8kHz 244ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048Mb/s and 4.096Mb/s. See Figure 14.
13	RSP	**Receive Sync Pulse (CMOS Output).** This is an 8kHz 488ns active high framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for connection to the Siemens MUNICH-32 device. See Figure 15.
14	TSP	**Transmit Sync Pulse (CMOS Output).** This is an 8kHz 488ns active high framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for connection to the Siemens MUNICH-32 device. See Figure 15.
15	F8o	**Frame Pulse (CMOS Output).** This is an 8kHz 122ns active high framing pulse, which marks the beginning of a frame. See Figure 14.
16	C1.5o	**Clock 1.544MHz (CMOS Output).** This output is used in T1 applications.
18	LOCK	**Lock Indicator (CMOS Output).** This output goes high when the PLL is frequency locked to the input reference.
19	C2o	**Clock 2.048MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048Mb/s.
20	$\overline{\text{C4o}}$	**Clock 4.096MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048Mb/s and 4.096Mb/s.
21	C19o	**Clock 19.44MHz (CMOS Output).** This output is used in OC3/STS3 applications.
22	FLOCK	**Fast Lock Mode (Input).** Set high to allow the PLL to quickly lock to the input reference (less than 500 ms locking time).
24	IC	**Internal Connection.** Tie low for normal operation.
25	C8o	**Clock 8.192MHz (CMOS Output).** This output is used for ST-BUS operation at 8.192Mb/s.
26	$\overline{\text{C16o}}$	**Clock 16.384MHz (CMOS Output).** This output is used for ST-BUS operation with a 16.384MHz clock.
27	C6o	**Clock 6.312 Mhz (CMOS Output).** This output is used for DS2 applications.
29	IM	**Impairment Monitor (CMOS Output).** A logic high on this pin indicates that the Input Impairment Monitor has automatically put the device into Freerun Mode.
30	IC	**Internal Connection.** Tie high for normal operation.
32	NC	**No Connection.** Leave open circuit**.**
33,34	IC	**Internal Connection.** Tie low for normal operation.
36	MS	**Mode/Control Select (Input).** This input determines the state (Normal or Freerun) of operation. The logic level at this input is gated in by the rising edge of F8o. See Table 3.
37	IC	**Internal Connection.** Tie low for normal operation.

Pin Description

Pin #	Name	Description
38	RSEL	**Reference Source Select (Input).** A logic low selects the PRI (primary) reference source as the input reference signal and a logic high selects the SEC (secondary) input. The logic level at this input is gated in by the rising edge of F8o. See Table 2. This pin is internally pulled down to VSS.
39	IC	**Internal Connection.** Tie low for normal operation.
40	FS2	**Frequency Select 2 (Input).** This input, in conjunction with FS1, selects which of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be input to the PRI and SEC inputs. See Table 1.
41	FS1	**Frequency Select 1 (Input).** See pin description for FS2.
42	IC	**Internal Connection.** Tie Low for Normal Operation.
43	IC	**Internal Connection.** Leave Open Circuit.
44	TDO	**Test Serial Data Out (CMOS Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
45	TDI	**Test Serial Data In (Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}.
46	$\overline{\text{TRST}}$	**Test Reset (Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. If not used, this pin should be held low.
47	TCK	**Test Clock (Input).** Provides the clock to the JTAG test logic. This pin is internally pulled up to V_{DD}.
48	TMS	**Test Mode Select (Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}.

Functional Description

The MT9043 is a Multitrunk System Synchronizer, providing timing (clock) and synchronization (frame) signals to interface circuits for T1 and E1 Primary Rate Digital Transmission links. Figure 1 is a functional block diagram which is described in the following sections.

Reference Select MUX Circuit

The MT9043 accepts two simultaneous reference input signals and operates on their falling edges. Either the primary reference (PRI) signal or the secondary reference (SEC) signal can be selected as input to the TIE Corrector Circuit. The selection is based on the Control, Mode and Reference Selection of the device. See Table 1 and Table 4.

Frequency Select MUX Circuit

The MT9043 operates with one of four possible input reference frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz). The frequency select inputs (FS1 and FS2) determine which of the four frequencies may be used at the reference inputs (PRI and SEC). Both inputs must have the same frequency applied to them. A reset ($\overline{\text{RST}}$) must be performed after every frequency select input change. See Table 1.

FS2	FS1	Input Frequency
0	0	19.44MHz
0	1	8kHz
1	0	1.544MHz
1	1	2.048MHz

Table 1 - Input Frequency Selection

Time Interval Error (TIE) Corrector Circuit

The TIE corrector circuit, when enabled, prevents a step change in phase on the input reference signals (PRI or SEC) from causing a step change in phase at the input of the DPLL block of Figure 1.

During reference input rearrangement, such as during a switch from the primary reference (PRI) to the secondary reference (SEC), a step change in phase on the input signals will occur. A phase step at the input of the DPLL would lead to unacceptable phase changes in the output signal.

As shown in Figure 3, the TIE Corrector Circuit receives one of the two reference (PRI or SEC) signals, passes the signal through a programmable delay line, and uses this delayed signal as an internal virtual reference, which is input to the DPLL. Therefore, the virtual reference is a delayed version of the selected reference.

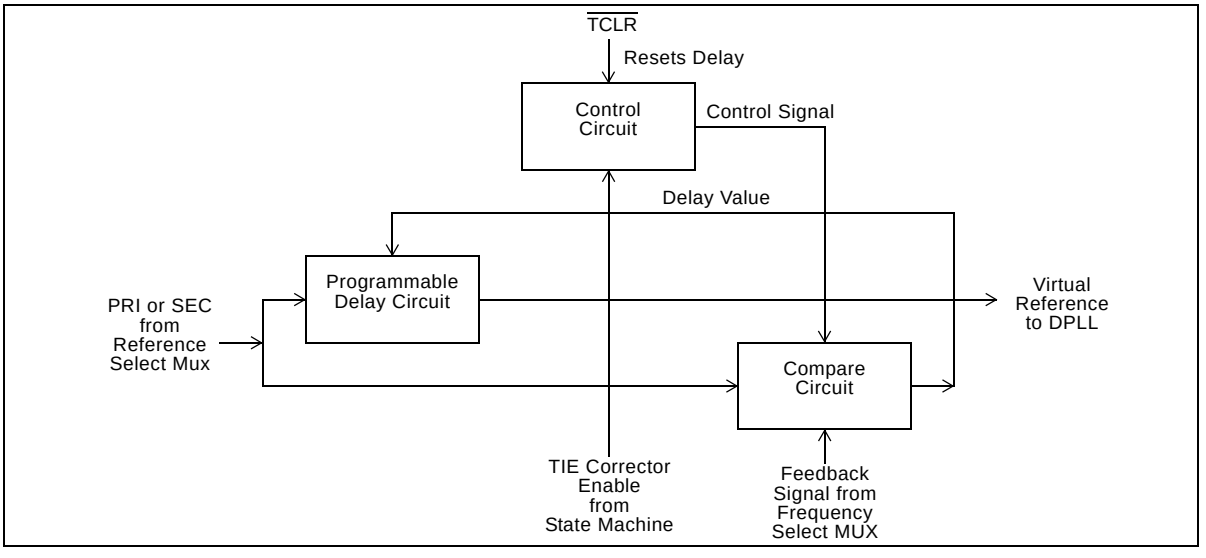


Figure 3 - TIE Corrector Circuit

During a switch from one reference to the other, the State Machine first changes the mode of the device

from Normal to Freerun. The Compare Circuit then measures the phase delay between the current phase (feedback signal) and the phase of the new reference signal. This delay value is passed to the Programmable Delay Circuit (See Figure 3). The state machine then returns the device to Normal Mode and the DPLL begins using the new virtual reference signal. The difference between the phase position of the new virtual reference and the previous reference is less than 1 μs.

Since internal delay circuitry maintains the alignment between the old virtual reference and the new virtual reference, a phase error may exist between the selected input reference signal and the output signal of the DPLL. This phase error is a function of the difference in phase between the two input reference signals during reference

rearrangements. Each time a reference switch is made, the delay between input signal and output signal will change. The value of this delay is the accumulation of the error measured during each reference switch.

The programmable delay circuit can be zeroed by applying a logic low pulse to the TIE Circuit Reset ($\overline{TCLR}$) pin. A minimum reset pulse width is 300ns. This results in a phase alignment between the input reference signal and the output signal as shown in Figure 13. The speed of the phase alignment correction is limited to 5ns per 125us, and convergence is in the direction of least phase travel.

The state diagram of Figure 7 indicates the state changes during which the TIE corrector circuit is activated.

Digital Phase Lock Loop (DPLL)

As shown in Figure 4, the DPLL of the MT9043 consists of a Phase Detector, Limiter, Loop Filter, Digitally Controlled Oscillator, and a Control Circuit.

Phase Detector - the Phase Detector compares the virtual reference signal from the TIE Corrector circuit with the feedback signal from the Frequency Select MUX circuit, and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Limiter circuit. The Frequency Select MUX allows the proper feedback signal to be externally selected (e.g., 8kHz, 1.544MHz, 2.048MHz or 19.44MHz).

Limiter - the Limiter receives the error signal from the Phase Detector and ensures that the DPLL responds to all input transient conditions with a maximum output phase slope of 5ns per 125us. This is well within the maximum phase slope of 7.6ns per 125us or 81ns per 1.326ms specified by AT&T TR62411 and Bellcore GR-1244-CORE, respectively.

Loop Filter - the Loop Filter is similar to a first order low pass filter with a 1.9 Hz cutoff frequency for all four reference frequency selections (8kHz, 1.544MHz, 2.048MHz or 19.44MHz). This filter ensures that the jitter transfer requirements in ETS 300 011 and AT&T TR62411 are met.

Control Circuit - the Control Circuit uses status and control information from the State Machine and the Input Impairment Circuit to set the mode of the DPLL. The two possible modes are Normal and Freerun.

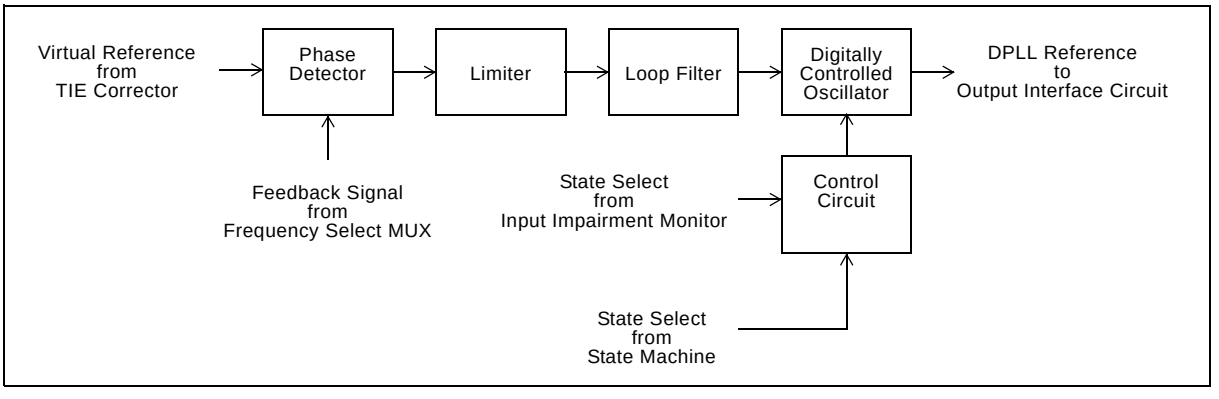


Figure 4 - DPLL Block Diagram

Digitally Controlled Oscillator (DCO) - the DCO receives the limited and filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the MT9043.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSCi 20MHz source.

Lock Indicator - If the PLL is in frequency lock (frequency lock means the center frequency of the PLL is identical to the line frequency), and the input phase offset is small enough such that no phase slope limiting is exhibited, then the lock signal will be set high. For specific Lock Indicator design recommendations see the Applications - Lock Indicator section.

Output Interface Circuit

The output of the DCO (DPLL) is used by the Output Interface Circuit to provide the output signals shown in Figure 5. The Output Interface Circuit uses four Tapped Delay Lines followed by a T1 Divider Circuit, an E1 Divider Circuit, and a DS2 Divider Circuit to generate the required output signals.

Four tapped delay lines are used to generate 16.384MHz, 12.352MHz, 12.624MHz and 19.44 MHz signals.

The E1 Divider Circuit uses the 16.384MHz signal to generate four clock outputs and five frame pulse outputs. The C8o, C4o and C2o clocks are generated by simply dividing the C16o clock by two, four and eight respectively. These outputs have a nominal 50% duty cycle.

The T1 Divider Circuit uses the 12.384MHz signal to generate the C1.5o clock by dividing the internal C12 clock by eight. This output has a nominal 50% duty cycle.

The DS2 Divider Circuit uses the 12.624 MHz signal to generate the clock output C6o. This output has a nominal 50% duty cycle.

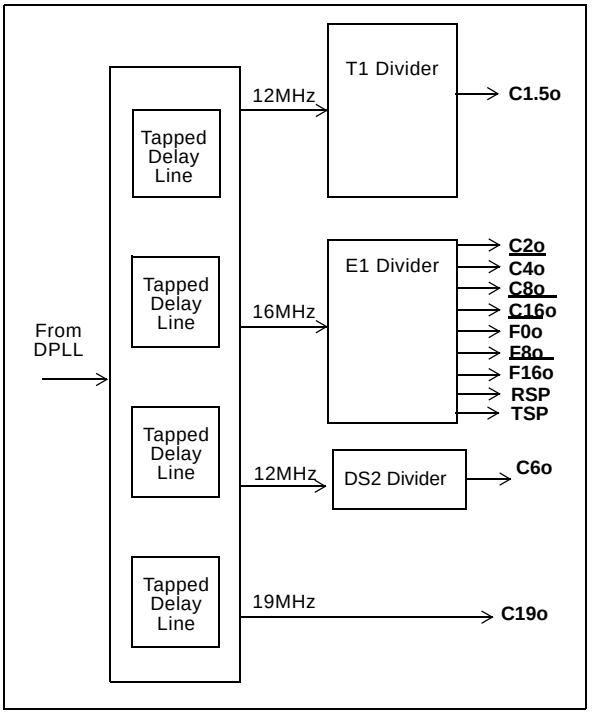


Figure 5 - Output Interface Circuit Block Diagram

The frame pulse outputs ($\overline{F0o}$, F8o, $\overline{F16o}$, TSP, and RSP) are generated directly from the C16 clock.

The T1 and E1 signals are generated from a common DPLL signal. Consequently, all frame pulse and clock outputs are locked to one another for all operating states, and are also locked to the selected input reference in Normal Mode. See Figures 14 & 15.

All frame pulse and clock outputs have limited driving capability, and should be buffered when driving high capacitance (e.g., 30pF) loads.

Input Impairment Monitor

This circuit monitors the input signal to the DPLL for a complete loss of incoming signal, or a large frequency shift in the incoming signal. If the input signal is outside the Impairment Monitor Capture Range the PLL automatically changes from Normal Mode to Free Run Mode. See AC Electrical Characteristics - Performance for the Impairment Monitor Capture Range. When the incoming signal returns to normal, the DPLL is returned to Normal Mode.

State Machine Control

As shown in Figure 1, this state machine controls the Reference Select MUX, the TIE Corrector Circuit and the DPLL. Control is based on the logic levels at the control inputs RSEL and MS (See Figure 6).

All state machine changes occur synchronously on the rising edge of F8o. See the Control and Mode of Operation section for full details.

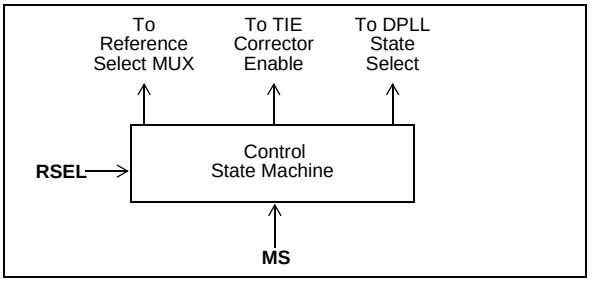


Figure 6 - Control State Machine Block Diagram

Master Clock

The MT9043 can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

Control and Mode of Operation

The active reference input (PRI or SEC) is selected by the RSEL pin as shown in Table 2.

RSEL	Input Reference
0	PRI
1	SEC

Table 2 - nput Reference Selection

MS	Mode
0	NORMAL
1	FREERUN

Table 3 - Operating Modes and States

The MT9043 has two possible modes of operation, Normal and Freerun.

As shown in Table 3, the Mode/Control Select pin MS selects the mode. Refer to Table 4 and Figure 7 for details of the state change sequences.

Normal Mode

Normal Mode is typically used when a slave clock source, synchronized to the network is required.

In Normal Mode, the MT9043 provides timing (C1.5o, C2o, $\overline{C4o}$, C8o, $\overline{C16o}$ and C19o) and frame synchronization ($\overline{F0o}$, F8o, $\overline{F16o}$, TSP and RSP) signals, which are synchronized to one of two reference inputs (PRI or SEC). The input reference signal may have a nominal frequency of 8kHz, 1.544MHz, 2.048MHz or 19.44MHz.

From a reset condition, the MT9043 will take up to 30 seconds (see AC Electrical Characteristics) of input reference signal to output signals which are synchronized (phase locked) to the reference input.

The selection of input references is control dependent as shown in state table 4. The reference frequencies are selected by the frequency control pins FS2 and FS1 as shown in Table 1.

Fast Lock Mode

Fast Lock Mode is a submode of Normal Mode, it is used to allow the MT9043 to lock to a reference more quickly than Normal mode will allow. Typically, the PLL will lock to the incoming reference within 500 ms if the FLOCK pin is set high.

Freerun Mode

Freerun Mode is typically used when a master clock source is required, or immediately following system power-up before network synchronization is achieved.

In Freerun Mode, the MT9043 provides timing and synchronization signals which are based on the master clock frequency (OSCi) only, and are not synchronized to the reference signals (PRI and SEC).

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±32ppm output clock is required, the master clock must also be ±32ppm. See Applications - Crystal and Clock Oscillator sections.

MT9043 Measures of Performance

The following are some synchronizer performance indicators and their corresponding definitions.

Intrinsic Jitter

Intrinsic jitter is the jitter produced by the synchronizing circuit and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is free running by measuring the output jitter of the device. Intrinsic jitter is usually measured with various bandlimiting filters depending on the applicable standards. In the MT9043, the intrinsic Jitter is limited to less than 0.02UI on the 2.048MHz and 1.544MHz clocks.

Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

For the MT9043, two internal elements determine the jitter attenuation. This includes the internal 1.9Hz low pass loop filter and the phase slope limiter. The phase slope limiter limits the output phase slope to 5ns/125us. Therefore, if the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited (i.e., attenuated) to 5ns/125us.

The MT9043 has twelve outputs with three possible input frequencies (except for 19.44MHz, which is internally divided to 8KHz) for a total of 36 possible jitter transfer functions. Since all outputs are derived from the same signal, the jitter transfer values for the four cases, 8kHz to 8kHz, 1.544MHz to 1.544MHz and 2.048MHz to 2.048MHz can be applied to all outputs.

It should be noted that 1UI at 1.544MHz is 644ns, which is not equal to 1UI at 2.048MHz, which is 488ns. Consequently, a transfer value using different input and output frequencies must be calculated in common units (e.g., seconds) as shown in the following example.

What is the T1 and E1 output jitter when the T1 input jitter is 20UI (T1 UI Units) and the T1 to T1 jitter attenuation is 18dB?

$$\mathrm{OutputT1} = \mathrm{InputT1} \times 10^{\left(\frac{-A}{20}\right)}$$

$$\mathrm{OutputT1} = 20 \times 10^{\left(\frac{-18}{20}\right)} = 2.5\mathrm{UI(T1)}$$

$$\mathrm{OutputE1} = \mathrm{OutputT1} \times \frac{(1\mathrm{UIT1})}{(1\mathrm{UIE1})}$$

$$\mathrm{OutputE1} = \mathrm{OutputT1} \times \frac{(644\mathrm{ns})}{(488\mathrm{ns})} = 3.3\mathrm{UI(T1)}$$

Using the above method, the jitter attenuation can be calculated for all combinations of inputs and outputs based on the three jitter transfer functions provided.

Note that the resulting jitter transfer functions for all combinations of inputs (8kHz, 1.544MHz, 2.048MHz) and outputs (8kHz, 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz, 19.44MHz) for a given input signal (jitter frequency and jitter amplitude) are the same.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

Frequency Accuracy

Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the MT9043, the Freerun accuracy is equal to the Master Clock (OSCi) accuracy.

Capture Range

Also referred to as pull-in range. This is the input frequency range over which the synchronizer must be able to pull into synchronization. The MT9043 capture range is equal to ±230 ppm minus the accuracy of the master clock (OSCi). For example, a 32 ppm master clock results in a capture range of 198 ppm.

Lock Range

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the MT9043.

Phase Slope

Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal.

Time Interval Error (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

Maximum Time Interval Error (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

$$MTIE(S) = TIEmax(t) - TIEmin(t)$$

Phase Continuity

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the synchronizer after a signal disturbance due to a reference switch or a mode change. The observation period is usually the time from the disturbance, to just after the synchronizer has settled to a steady state.

In the case of the MT9043, the output signal phase continuity is maintained to within ±5ns at the instance (over one frame) of all reference switches and all mode changes. The total phase shift, depending on the switch or type of mode change, may accumulate up to 200 ns over many frames. The rate of change of the 200 ns phase shift is limited to a maximum phase slope of approximately 5ns/125us. This meets the AT&T TR62411 maximum phase slope requirement of 7.6ns/125us and Bellcore GR-1244-CORE (81ns/1.326ms).

Phase Lock Time

This is the time it takes the synchronizer to phase lock to the input signal. Phase lock occurs when the input signal and output signal are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors which include:

- initial input to output phase difference
- initial input to output frequency difference
- synchronizer loop filter
- synchronizer limiter

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. And better (smaller) phase slope performance (limiter) results in longer lock times. The MT9043 loop filter and limiter were optimized to meet the AT&T TR62411 jitter transfer and phase slope requirements. Consequently, phase lock time, which is not a standards requirement, may be longer than in other applications. See AC Electrical Characteristics - Performance for Maximum Phase Lock Time.

MT9043 provides a fast lock pin (FLOCK), which, when set high enables the PLL to lock to an incoming reference within approximately 500 ms.

Description		State		
Input Controls		Freerun	Normal (PRI)	Normal (SEC)
MS	RSEL	S0	S1	S2
0	0	S1	-	S1 MTIE
0	1	S2	S2 MTIE	-
1	X	-	S0	S0

Legend:
- No Change
MTIE State change occurs with TIE Corrector Circuit
Refer to Control State Diagram for state changes to and from Auto-Freerun State

Table 4 - Control State Table

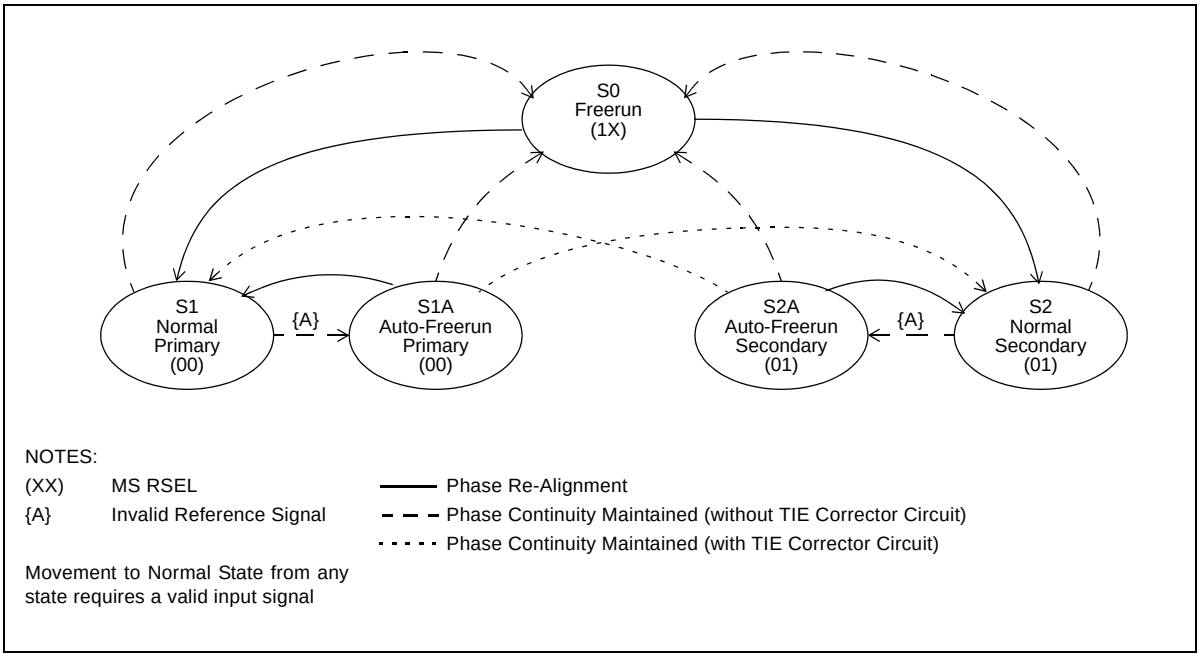


Figure 7 - Control State Diagram

MT9043 and Network Specifications

The MT9043 fully meets all applicable PLL requirements (intrinsic jitter, jitter/wander tolerance, jitter/wander transfer, frequency accuracy, capture range, phase change slope and MTIE during reference rearrangement) for the following specifications.

1. Bellcore GR-1244-CORE June 1995 for, Stratum 4 Enhanced and Stratum 4
2. AT&T TR62411 (DS1) December 1990 for, Stratum 4 Enhanced and Stratum 4
3. ANSI T1.101 (DS1) February 1994 for Stratum 4 Enhanced and Stratum 4
4. ETSI 300 011 (E1) April 1992 for Single Access and Multi Access

5. TBR 4 November 1995
6. TBR 12 December 1993
7. TBR 13 January 1996
8. ITU-T I.431 March 1993

Applications

This section contains MT9043 application specific details for clock and crystal operation, reset operation, power supply de coupling, and control operation.

Master Clock

The MT9043 can use either a clock or crystal as the master timing source.

In Freerun Mode, the frequency tolerance at the clock outputs is identical to the frequency tolerance of the source at the OSCi pin. For applications not requiring an accurate Freerun Mode, tolerance of the master timing source may be ±100ppm. For applications requiring an accurate Freerun Mode, such as AT&T TR62411, the tolerance of the master timing source must be no greater than ±32ppm.

Another consideration in determining the accuracy of the master timing source is the desired capture range. The sum of the accuracy of the master timing source and the capture range of the MT9043 will always equal 230ppm. For example, if the master timing source is 100ppm, then the capture range will be 130ppm.

Clock Oscillator - when selecting a Clock Oscillator, numerous parameters must be considered. This includes absolute frequency, frequency change over temperature, output rise and fall times, output levels and duty cycle.

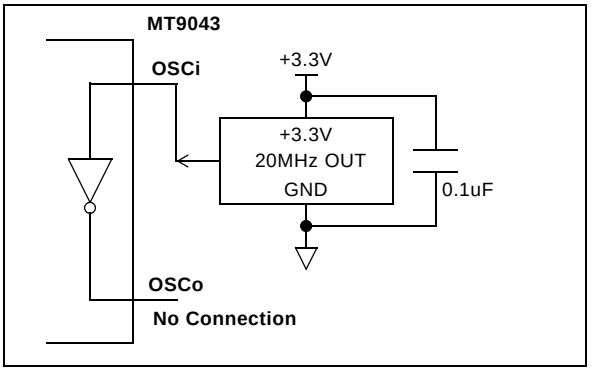


Figure 8 - Clock Oscillator Circuit

For applications requiring ±32ppm clock accuracy, the following clock oscillator module may be used.

FOX F7C-2E3-20.0MHz

Frequency:	*20MHz*
Tolerance:	*25ppm 0C to 70C*
Rise & Fall Time:	*10ns (0.33V 2.97V 15pF)*
Duty Cycle:	*40% to 60%*

CTS CB3LV-5I-20.0 MHz

Frequency:	*20MHz*
Tolerance:	*25ppm*
Rise & Fall Time:	*10ns*
Duty Cycle:	*45% to 55%*

The output clock should be connected directly (not AC coupled) to the OSCi input of the MT9043, and the OSCo output should be left open as shown in Figure 8.

Crystal Oscillator - Alternatively, a Crystal Oscillator may be used. A complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Figure 9.

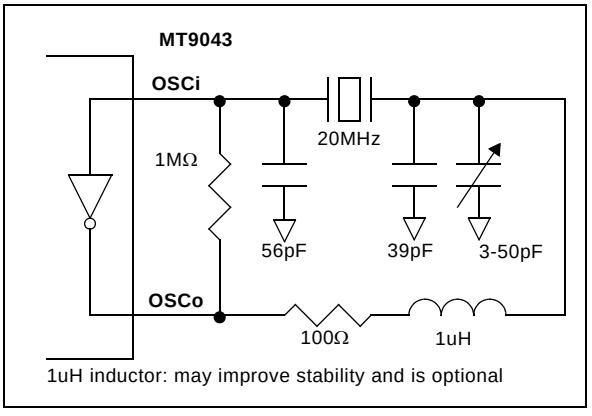


Figure 9 - Crystal Oscillator Circuit

The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20MHz crystal specified with a 32pF load capacitance, each 1pF change in load capacitance contributes approximately 9ppm to the frequency deviation. Consequently, capacitor tolerances, and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The trimmer capacitor shown in Figure 9 may be used to compensate for capacitive effects. If accuracy is not a concern, then the trimmer may be removed, the 39pF capacitor may be increased to 56pF, and a wider tolerance crystal may be substituted.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. The crystal specification is as follows.

Frequency:	*20MHz*
Tolerance:	*As required*
Oscillation Mode:	*Fundamental*
Resonance Mode:	*Parallel*
Load Capacitance:	*32pF*
Maximum Series Resistance:	*35Ω*
Approximate Drive Level:	*1mW*

e.g., R1B23B32-20.0MHz
(20ppm absolute, ±6ppm 0C to 50C, 32pF, 25Ω)

Reset Circuit

A simple power up reset circuit with about a 50us reset low time is shown in Figure 10. Resistor R_P is for protection only and limits current into the $\overline{RST}$ pin during power down conditions. The reset low time is not critical but should be greater than 300ns.

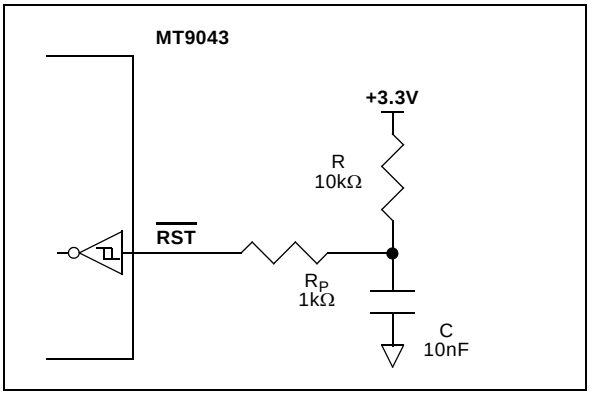


Figure 10 - Power-Up Reset Circuit

Lock Indicator

The LOCK pin toggles at a random rate when the PLL is frequency locked to the input reference. In Figure 11 the RC-time-constant circuit can be used to hold the high state of the LOCK pin.

Once the PLL is frequency locked to the input reference, the minimum duration of LOCK pin's high state would be 32ms and the maximum duration of LOCK pin's low state would not exceed 1 second. The following equations can be used to calculate the charge and discharge times of the capacitor.

$t_C = - R_D C \ln(1 - V_{T+}/V_{DD}) = 240\ \mu s$

t_C = Capacitor's charge time

R_D = Dynamic resistance of the diode (100 Ω)

C = Capacitor value (1μF)

V_{T+} = Positive going threshold voltage of the Schmitt Trigger (3.0 V)

V_{DD} = 3.3 V

$t_D = - R C \ln(V_{T-}/V_{DD}) = 1.65$ seconds

t_D = Capacitor's discharge time

R = Resistor value (3.3 MΩ)

C = Capacitor value (1μF)

V_{T-} = Negative going threshold voltage of the Schmitt Trigger (2.0 V)

V_{DD} = 3.3 V

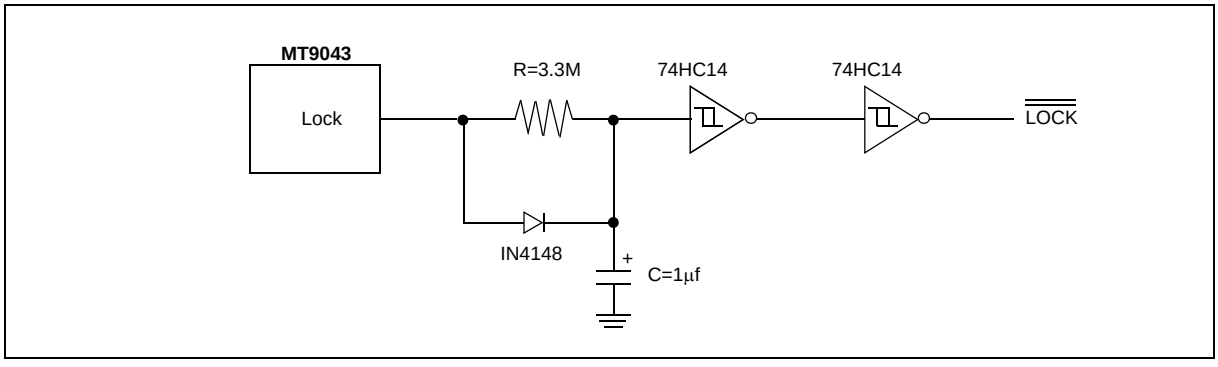


Figure 11 - Time-constant Circuit

A digital alternative to the RC-time-constant circuit is presented in Figure 12. The circuit in Figure 12 can be used to generate a steady lock signal. The circuit monitors the MT9043's LOCK pin, as long as it detects a positive pulse every 1.024 seconds or less, the Advanced Lock output will remain high. If no positive pulse is detected on the LOCK output within 1.024 seconds, the Advanced LOCK output will go low.

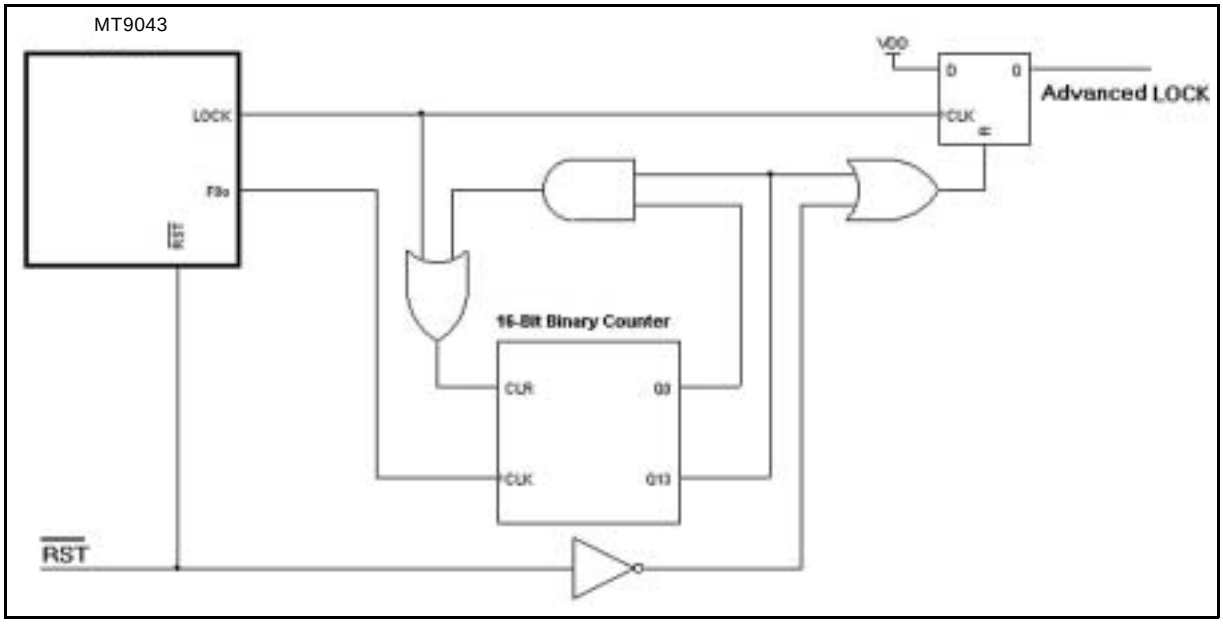


Figure 12 - Digital Lock Pin Circuit

Absolute Maximum Ratings* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any pin	V_{PIN}	-0.3	V_{DD}+ 0.3	V
3	Current on any pin	I_{PIN}		30	mA
4	Storage temperature	T_{ST}	-55	125	°C
5	48 SSOP package power dissipation	P_{PD}		200	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Max	Units
1	Supply voltage	V_{DD}	3.0	3.6	V
2	Operating temperature	T_A	-40	85	°C

DC Electrical Characteristics* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Max	Units	Conditions/Notes
1	Supply current with: OSCi = 0V	I_{DDS}		1.8	mA	Outputs unloaded
2	OSCi = Clock	I_{DD}		50	mA	Outputs unloaded
3	CMOS high-level input voltage	V_{CIH}	$0.7V_{DD}$		V	
4	CMOS low-level input voltage	V_{CIL}		$0.3V_{DD}$	V	
5	Input leakage current	I_{IL}		15	µA	V_I=V_{DD} or 0V
6	High-level output voltage	V_{OH}	2.4		V	I_{OH}= 10 mA
7	Low-level output voltage	V_{OL}		0.4	V	I_{OL}= 10 mA

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

AC Electrical Characteristics - Performance

	Characteristics	Sym	Min	Max	Units	Conditions/ Notes†
1	Freerun Mode accuracy with OSCi at: ±0ppm		-0	+0	ppm	4-8
2	±32ppm		-32	+32	ppm	4-8
3	±100ppm		-100	+100	ppm	4-8
4	Capture range with OSCi at: ±0ppm		-230	+230	ppm	1-3,5-8
5	±32ppm		-198	+198	ppm	1-3,5-8
6	±100ppm		-130	+130	ppm	1-3,5-8
7	Phase lock time			30	s	1-3,5-14
8	Output phase continuity with: reference switch			200	ns	1-3,5-14
9	mode switch to Normal			200	ns	1-2,4-14
10	mode switch to Freerun			200	ns	1-3,5-14
11	MTIE (maximum time interval error)			600	ns	1-14,27
12	Output phase slope			45	us/s	1-14,27
13	Impairment Monitor Capture Range at: 8kHz, 19.44MHz		-30k	+30k	ppm	1-3,5,8,9-11
14	1.544MHz		-30k	+30k	ppm	1-3,6,9-11
15	2.048MHz		-30k	+30k	ppm	1-3,7,9-11

† See “Notes” following AC Electrical Characteristics tables.

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels* - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	CMOS	Units
1	Threshold Voltage	V_T	$0.5V_{DD}$	V
2	Rise and Fall Threshold Voltage High	V_{HM}	$0.7V_{DD}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD}$	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Timing for input and output signals is based on the worst case result of the CMOS thresholds.
* See Figure 10.

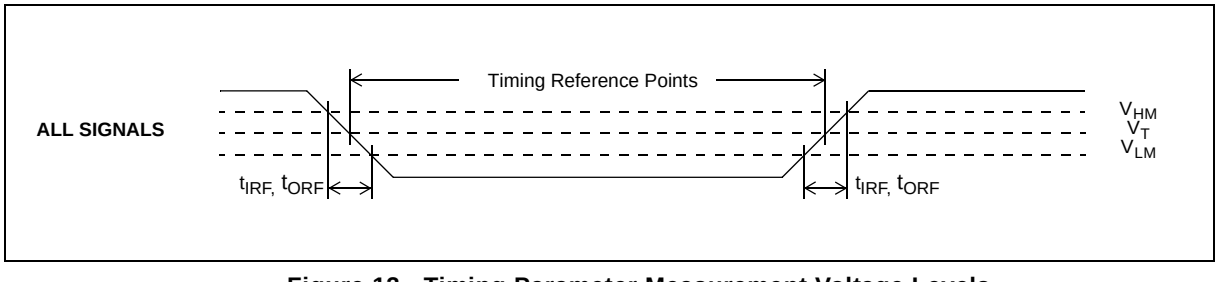
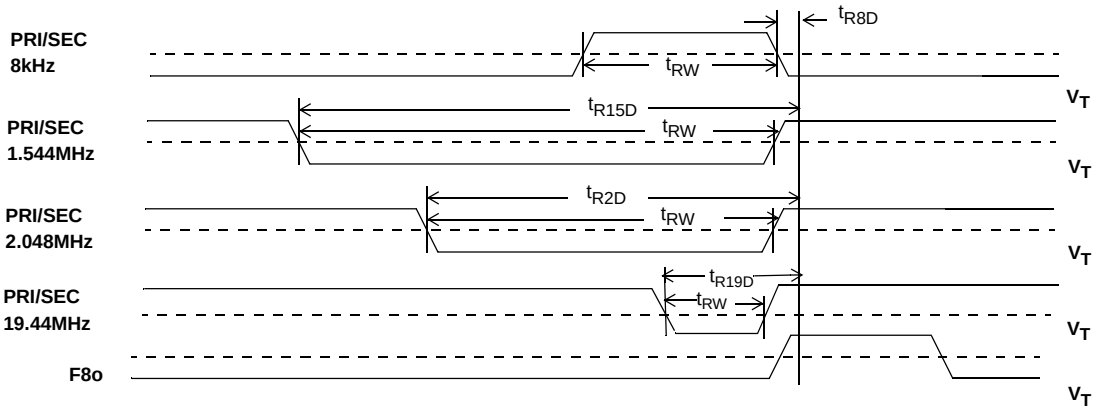


Figure 13 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics - Input/Output Timing

	Characteristics	Sym	Min	Max	Units
1	Reference input pulse width high or low	t_{RW}	100		ns
2	Reference input rise or fall time	t_{IRF}		10	ns
3	8kHz reference input to F8o delay	t_{R8D}	-21	6	ns
4	1.544MHz reference input to F8o delay	t_{R15D}	337	363	ns
5	2.048MHz reference input to F8o delay	t_{R2D}	222	238	ns
6	19.44MHz reference input to F8o delay	t_{R19D}	46	57	ns
7	F8o to $\overline{\text{F0o}}$ delay	t_{F0D}	111	130	ns
8	$\overline{\text{F16o}}$ setup to $\overline{\text{C16o}}$ falling	t_{F16S}	25	40	ns
9	$\overline{\text{F16o}}$ hold to $\overline{\text{C16o}}$ rising	t_{F16H}	-10	10	ns
10	F8o to C1.5o delay	t_{C15D}	-45	-25	ns
11	F8o to C6o delay	t_{C6D}	-10	10	ns
12	F8o to C2o delay	t_{C2D}	-11	5	ns
13	F8o to $\overline{\text{C4o}}$ delay	t_{C4D}	-11	5	ns
14	F8o to C8o delay	t_{C8D}	-11	5	ns
15	F8o to $\overline{\text{C16o}}$ delay	t_{C16D}	-11	5	ns
16	F8o to TSP delay	t_{TSPD}	-6	10	ns
17	F8o to RSP delay	t_{RSPD}	-8	8	ns
18	F8o to C19o delay	t_{C19D}	-15	5	ns
19	C1.5o pulse width high or low	t_{C15W}	309	339	ns
20	C6o pulse width high or low	t_{C6W}	70	86	ns
21	C2o pulse width high or low	t_{C2W}	230	258	ns
22	$\overline{\text{C4o}}$ pulse width high or low	t_{C4W}	111	133	ns
23	C8o pulse width high or low	t_{C8W}	52	70	ns
24	$\overline{\text{C16o}}$ pulse width high or low	t_{C16WL}	24	35	ns
25	TSP pulse width high	t_{TSPW}	478	494	ns
26	RSP pulse width high	t_{RSPW}	474	491	ns
27	C19o pulse width high	t_{C19WH}	25	35	ns
28	C19o pulse width low	t_{C19WL}	17	25	ns
29	$\overline{\text{F0o}}$ pulse width low	t_{F0WL}	234	254	ns
30	F8o pulse width high	t_{F8WH}	109	135	ns
31	$\overline{\text{F16o}}$ pulse width low	t_{F16WL}	47	75	ns
32	Output clock and frame pulse rise or fall time	t_{ORF}		9	ns
33	Input Controls Setup Time	t_S	100		ns
34	Input Controls Hold Time	t_H	100		ns



NOTES:

1. Input to output delay values are valid after a $\overline{TCLR}$ or $\overline{RST}$ with no further state changes

Figure 14 - Input to Output Timing (Normal Mode)

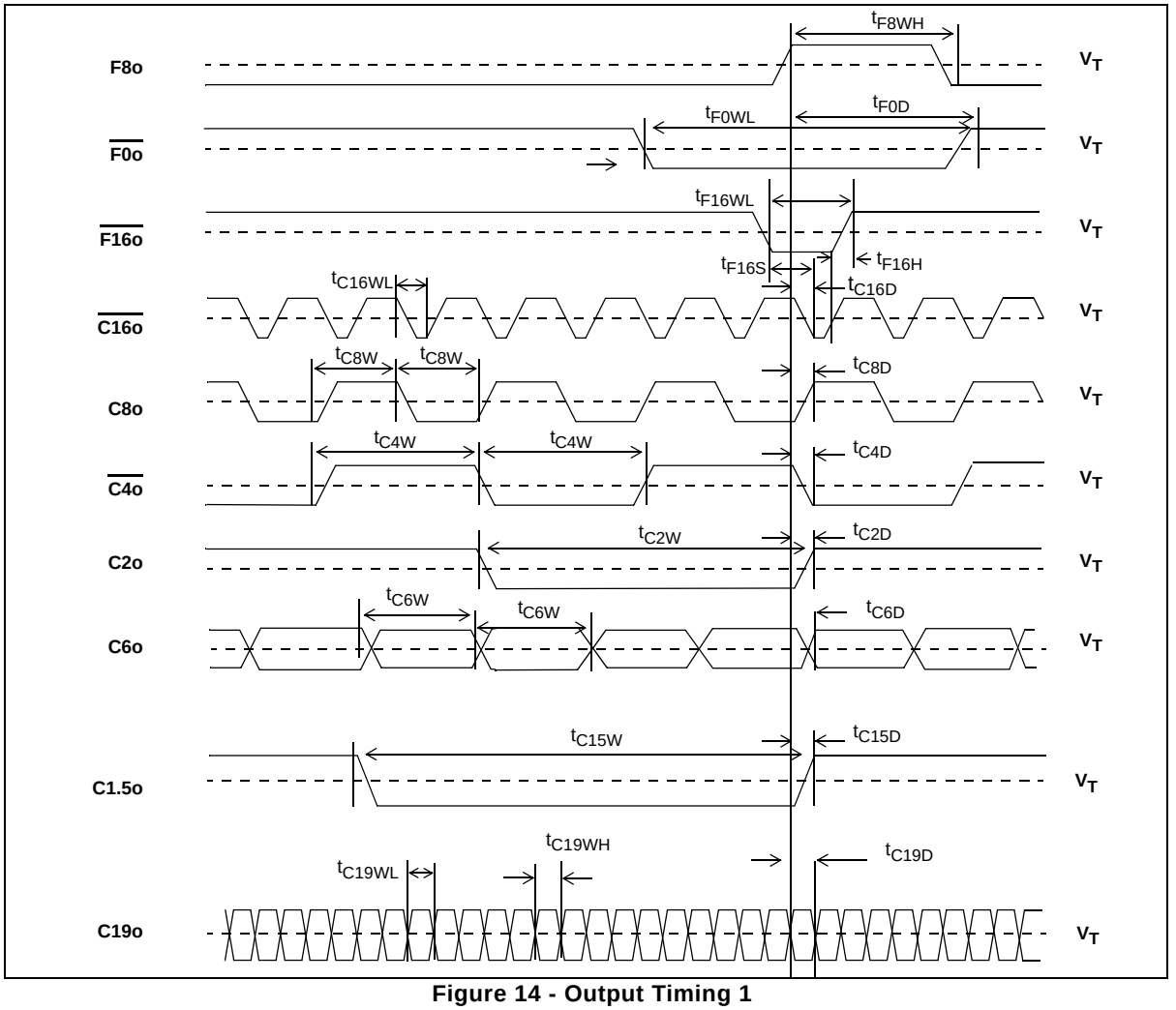


Figure 14 - Output Timing 1

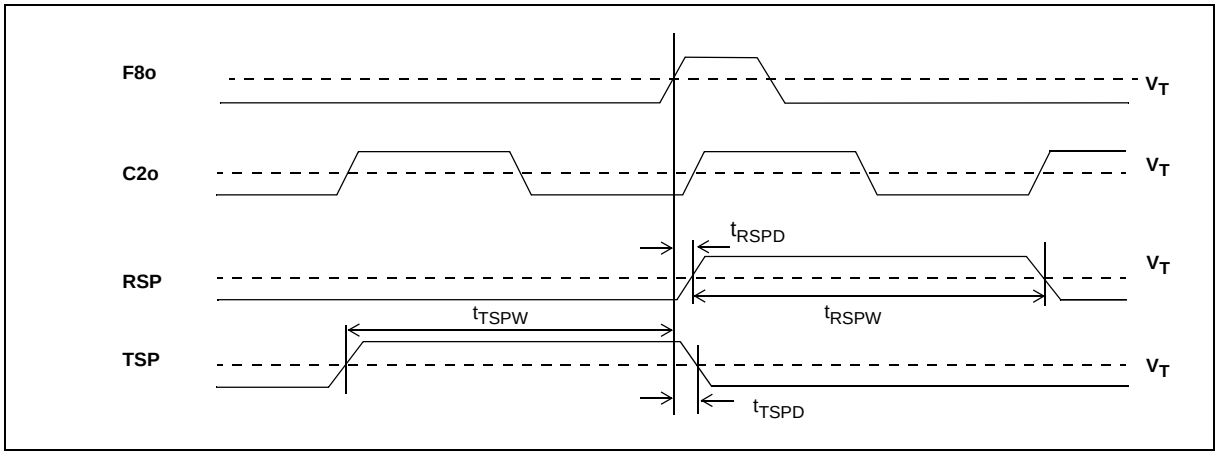


Figure 15 - Output Timing 2

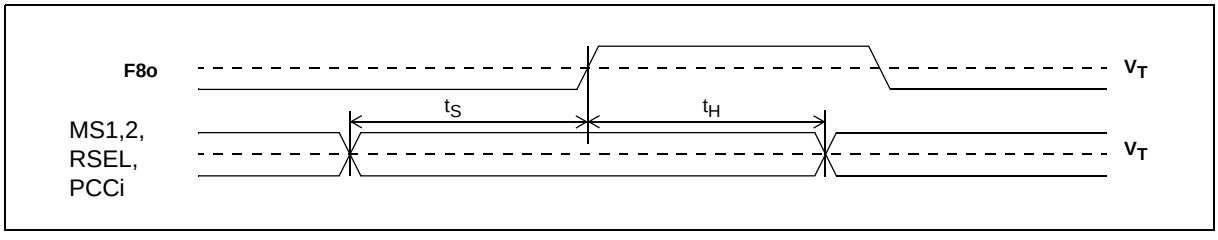


Figure 16 - Input Controls Setup and Hold Timing

AC Electrical Characteristics - Intrinsic Jitter Unfiltered

	Characteristics	Sym	Max	Units	Conditions/Notes†
1	Intrinsic jitter at F8o (8kHz)		0.0002	UIpp	1-14,21-24,28
2	Intrinsic jitter at $\overline{\text{F0o}}$ (8kHz)		0.0002	UIpp	1-14,21-24,28
3	Intrinsic jitter at $\overline{\text{F16o}}$ (8kHz)		0.0002	UIpp	1-14,21-24,28
4	Intrinsic jitter at C1.5o (1.544MHz)		0.030	UIpp	1-14,21-24,29
5	Intrinsic jitter at C2o (2.048MHz)		0.040	UIpp	1-14,21-24,30
6	Intrinsic jitter at C6o (6.312MHz)		0.120	UIpp	1-14,21-24,31
7	Intrinsic jitter at $\overline{\text{C4o}}$ (4.096MHz)		0.080	UIpp	1-14,21-24,32
8	Intrinsic jitter at C8o (8.192MHz)		0.104	UIpp	1-14,21-24,33
9	Intrinsic jitter at $\overline{\text{C16o}}$ (16.384MHz)		0.104	UIpp	1-14,21-24,34
10	Intrinsic jitter at TSP (8kHz)		0.0002	UIpp	1-14,21-24,34
11	Intrinsic jitter at RSP (8kHz)		0.0002	UIpp	1-14,21-24,34
12	Intrinsic jitter at C19o (19.44MHz)		0.27	UIpp	1-14,21-24,35

† See “Notes” following AC Electrical Characteristics tables.

AC Electrical Characteristics - C1.5o (1.544MHz) Intrinsic Jitter Filtered

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Intrinsic jitter (4Hz to 100kHz filter)			0.015	UIpp	1-14,21-24,29
2	Intrinsic jitter (10Hz to 40kHz filter)			0.010	UIpp	1-14,21-24,29
3	Intrinsic jitter (8kHz to 40kHz filter)			0.010	UIpp	1-14,21-24,29
4	Intrinsic jitter (10Hz to 8kHz filter)			0.005	UIpp	1-14,21-24,29

† See “Notes” following AC Electrical Characteristics tables.

AC Electrical Characteristics - C2o (2.048MHz) Intrinsic Jitter Filtered

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Intrinsic jitter (4Hz to 100kHz filter)			0.015	UIpp	1-14,21-24,30
2	Intrinsic jitter (10Hz to 40kHz filter)			0.010	UIpp	1-14,21-24,30
3	Intrinsic jitter (8kHz to 40kHz filter)			0.010	UIpp	1-14,21-24,30
4	Intrinsic jitter (10Hz to 8kHz filter)			0.005	UIpp	1-14,21-24,30

† See “Notes” following AC Electrical Characteristics tables.

AC Electrical Characteristics - 8kHz Input to 8kHz Output Jitter Transfer

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter attenuation for 1Hz@0.01UIpp input		0	6	dB	1-3, 5, 9-14, 21-22, 24, 28, 36
2	Jitter attenuation for 1Hz@0.54UIpp input		6	16	dB	1-3, 5, 9-14, 21-22, 24, 28, 36
3	Jitter attenuation for 10Hz@0.10UIpp input		12	22	dB	1-3, 5, 9-14, 21-22, 24, 28, 36
4	Jitter attenuation for 60Hz@0.10UIpp input		28	38	dB	1-3, 5, 9-14, 21-22, 24, 28, 36
5	Jitter attenuation for 300Hz@0.10UIpp input		42		dB	1-3, 5, 9-14, 21-22, 24, 28, 36
6	Jitter attenuation for 3600Hz@0.005UIpp input		45		dB	1-3, 5, 9-14, 21-22, 24, 28, 36

† See “Notes” following AC Electrical Characteristics tables.

AC Electrical Characteristics - 1.544MHz Input to 1.544MHz Output Jitter Transfer

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter attenuation for 1Hz@20UIpp input		0	6	dB	1-3,6,9-14, 21-22,24,29,36
2	Jitter attenuation for 1Hz@104UIpp input		6	16	dB	1-3,6,9-14, 21-22,24,29,36
3	Jitter attenuation for 10Hz@20UIpp input		12	22	dB	1-3,6,9-14, 21-22,24,29,36
4	Jitter attenuation for 60Hz@20UIpp input		28	38	dB	1-3,6,9-14, 21-22,24,29,36
5	Jitter attenuation for 300Hz@20UIpp input		42		dB	1-3,6,9-14, 21-22,24,29,36
6	Jitter attenuation for 10kHz@0.3UIpp input		45		dB	1-3,6,9-14, 21-22,24,29,36
7	Jitter attenuation for 100kHz@0.3UIpp input		45		dB	1-3,6,9-14, 21-22,24,29,36

† See “Notes” following AC Electrical Characteristics tables.

AC Electrical Characteristics - 2.048MHz Input to 2.048MHz Output Jitter Transfer

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter at output for 1Hz@3.00UIpp input with 40Hz to 100kHz filter			2.9	UIpp	1-3,7,9-14, 21-22,24,30,36
2				0.09	UIpp	1-3,7,9-14, 21-22,24,30,37
3	Jitter at output for 3Hz@2.33UIpp input with 40Hz to 100kHz filter			1.3	UIpp	1-3,7,9-14, 21-22,24,30,36
4				0.10	UIpp	1-3,7,9-14, 21-22,24,30,37
5	Jitter at output for 5Hz@2.07UIpp input with 40Hz to 100kHz filter			0.80	UIpp	1-3,7,9-14, 21-22,24,30,36
6				0.10	UIpp	1-3,7,9-14, 21-22,24,30,37
7	Jitter at output for 10Hz@1.76UIpp input with 40Hz to 100kHz filter			0.40	UIpp	1-3,7,9-14, 21-22,24,30,36
8				0.10	UIpp	1-3,7,9-14, 21-22,24,30,37
9	Jitter at output for 100Hz@1.50UIpp input with 40Hz to 100kHz filter			0.06	UIpp	1-3,7,9-14, 21-22,24,30,36
10				0.05	UIpp	1-3,7,9-14, 21-22,24,30,37
11	Jitter at output for 2400Hz@1.50UIpp input with 40Hz to 100kHz filter			0.04	UIpp	1-3,7,9-14, 21-22,24,30,36
12				0.03	UIpp	1-3,7,9-14, 21-22,24,30,37
13	Jitter at output for 100kHz@0.20UIpp input with 40Hz to 100kHz filter			0.04	UIpp	1-3,7,9-14, 21-22,24,30,36
14				0.02	UIpp	1-3,7,9-14, 21-22,24,30,35

† See “Notes” following AC Electrical Characteristics tables.

AC Electrical Characteristics - 8kHz Input Jitter Tolerance

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter tolerance for 1Hz input		0.80		UIpp	1-3,5,9 -14,21-22,24-26,28
2	Jitter tolerance for 5Hz input		0.70		UIpp	1-3,5,9 -14,21-22,24-26,28
3	Jitter tolerance for 20Hz input		0.60		UIpp	1-3,5,9 -14,21-22,24-26,28
4	Jitter tolerance for 300Hz input		0.20		UIpp	1-3,5,9 -14,21-22,24-26,28
5	Jitter tolerance for 400Hz input		0.15		UIpp	1-3,5,9 -14,21-22,24-26,28
6	Jitter tolerance for 700Hz input		0.08		UIpp	1-3,5,9 -14,21-22,24-26,28
7	Jitter tolerance for 2400Hz input		0.02		UIpp	1-3,5,9 -14,21-22,24-26,28
8	Jitter tolerance for 3600Hz input		0.01		UIpp	1-3,5,9 -14,21-22,24-26,28

† See “Notes” following AC Electrical Characteristics tables.

AC Electrical Characteristics - 1.544MHz Input Jitter Tolerance

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter tolerance for 1Hz input		150		UIpp	1-3,6,9 -14,21-22,24-26,29
2	Jitter tolerance for 5Hz input		140		UIpp	1-3,6,9 -14,21-22,24-26,29
3	Jitter tolerance for 20Hz input		130		UIpp	1-3,6,9 -14,21-22,24-26,29
4	Jitter tolerance for 300Hz input		35		UIpp	1-3,6,9 -14,21-22,24-26,29
5	Jitter tolerance for 400Hz input		25		UIpp	1-3,6,9 -14,21-22,24-26,29
6	Jitter tolerance for 700Hz input		15		UIpp	1-3,6,9 -14,21-22,24-26,29
7	Jitter tolerance for 2400Hz input		4		UIpp	1-3,6,9 -14,21-22,24-26,29
8	Jitter tolerance for 10kHz input		1		UIpp	1-3,6,9 -14,21-22,24-26,29
9	Jitter tolerance for 100kHz input		0.5		UIpp	1-3,6,9 -14,21-22,24-26,29

† See “Notes” following AC Electrical Characteristics tables.

AC Electrical Characteristics - 2.048MHz Input Jitter Tolerance

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter tolerance for 1Hz input		150		UIpp	1-3,7,9 -14,21-22,24-26,30
2	Jitter tolerance for 5Hz input		140		UIpp	1-3,7,9 -14,21-22,24-26,30
3	Jitter tolerance for 20Hz input		130		UIpp	1-3,7,9 -14,21-22,24-26,30
4	Jitter tolerance for 300Hz input		50		UIpp	1-3,7,9 -14,21-22,24-26,30
5	Jitter tolerance for 400Hz input		40		UIpp	1-3,7,9 -14,21-22,24-26,30
6	Jitter tolerance for 700Hz input		20		UIpp	1-3,7,9 -14,21-22,24-26,30
7	Jitter tolerance for 2400Hz input		5		UIpp	1-3,7,9 -14,21-22,24-26,30
8	Jitter tolerance for 10kHz input		1		UIpp	1-3,7,9 -14,21-22,24-26,30
9	Jitter tolerance for 100kHz input		1		UIpp	1-3,7,9 -14,21-22,24-26,30

† See “Notes” following AC Electrical Characteristics tables.

AC Electrical Characteristics - OSCi 20MHz Master Clock Input

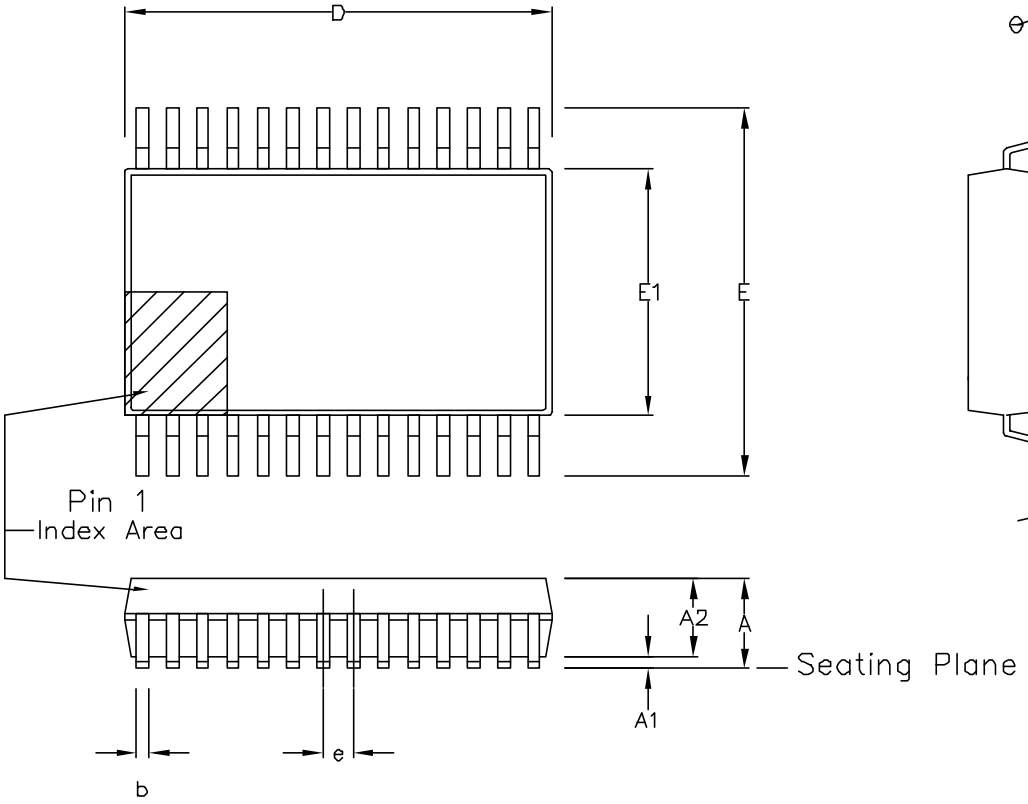
	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Tolerance		-0	+0	ppm	15,18
2			-32	+32	ppm	16,19
3			-100	+100	ppm	17,20
4	Duty cycle		40	60	%	
5	Rise time			10	ns	
6	Fall time			10	ns	

† See “Notes” following AC Electrical Characteristics tables.

† Notes:

Voltages are with respect to ground (V_{SS}) unless otherwise stated.
Supply voltage and operating temperature are as per Recommended Operating Conditions.
Timing parameters are as per AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

1. PRI reference input selected.
2. SEC reference input selected.
3. Normal Mode selected.
4. Freerun Mode selected.
5. 8kHz Frequency Mode selected.
6. 1.544MHz Frequency Mode selected.
7. 2.048MHz Frequency Mode selected.
8. 19.44MHz Frequency Mode selected.
9. Master clock input OSCi at 20MHz ±0ppm.
10. Master clock input OSCi at 20MHz ±32ppm.
11. Master clock input OSCi at 20MHz ±100ppm.
12. Selected reference input at ±0ppm.
13. Selected reference input at ±32ppm.
14. Selected reference input at ±100ppm.
15. For Freerun Mode of ±0ppm.
16. For Freerun Mode of ±32ppm.
17. For Freerun Mode of ±100ppm.
18. For capture range of ±230ppm.
19. For capture range of ±198ppm.
20. For capture range of ±130ppm.
21. 25pF capacitive load.
22. OSCi Master Clock jitter is less than 2nspp, or 0.04UIpp where1UIpp=1/20MHz.
23. Jitter on reference input is less than 7nspp.
24. Applied jitter is sinusoidal.
25. Minimum applied input jitter magnitude to regain synchronization.
26. Loss of synchronization is obtained at slightly higher input jitter amplitudes.
27. Within 10ms of the state, reference or input change.
28. 1UIpp = 125us for 8kHz signals.
29. 1UIpp = 648ns for 1.544MHz signals.
30. 1UIpp = 488ns for 2.048MHz signals.
31. 1UIpp = 323ns for 3.088MHz signals.
32. 1UIpp = 244ns for 4.096MHz signals.
33. 1UIpp = 122ns for 8.192MHz signals.
34. 1UIpp = 61ns for 16.384MHz signals.
35. 1UIpp = 51.44ns for 19.44MHz signals.
36. No filter.
37. 40Hz to 100kHz bandpass filter.
38. With respect to reference input signal frequency.
39. After a RST or TCLR.
40. Master clock duty cycle 40% to 60%.



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.41	2.59	2.79		0.095	0.102	0.110
A1	0.20	0.30	0.40		0.008	0.012	0.016
A2	2.26	2.39	2.52		0.089	0.094	0.099
D	15.75	15.88	16.00		0.620	0.625	0.630
E	10.03	10.31	10.67		0.395	0.406	0.420
E1	7.39	7.49	7.59		0.291	0.295	0.299
L	0.51	0.76	1.02		0.020	0.030	0.040
e	0.64 BSC.				0.025 BSC.		
b	0.20	0.25	0.34		0.008	0.010	0.0135
c	0.13	0.20	0.25		0.005	0.008	0.010
θ	0°		8°		0°		8°
	Pin features						
N	48						
Conforms to JEDEC MO-118 AA Iss. A							

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protrusion. Mould flash or protrusion shall not exceed 0.15 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.

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DATE	13-01-03			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for 48 lead SSOP (300 mil Body Width)

GPD00816

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