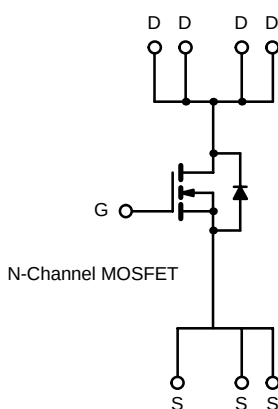
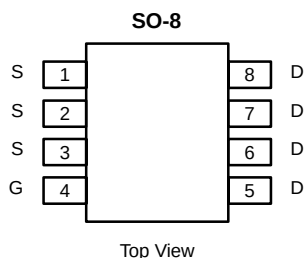




N-Channel Reduced Q_g , Fast Switching MOSFET

TrenchFET[®]
Power MOSFETs
High-Efficiency
PWM Optimized
100% R_G Tested

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.007 @ $V_{GS} = 10$ V	16
	0.010 @ $V_{GS} = 4.5$ V	13



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	10 secs	Steady State
Drain-Source Voltage		V_{DS}	30	
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	16	11
	$T_A = 70^\circ\text{C}$		13	8
Pulsed Drain Current		I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a		I_S	3.0	1.40
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	3.5	16
	$T_A = 70^\circ\text{C}$		2.2	1.0
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Typical	Maximum
Maximum Junction-to-Ambient (MOSFET) ^a	$t \leq 10$ sec	R_{thJA}	29	35
	Steady State		65	80
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	15	18

Notes

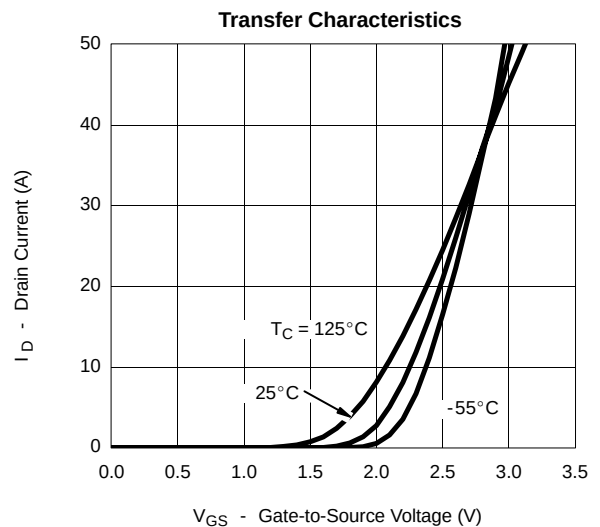
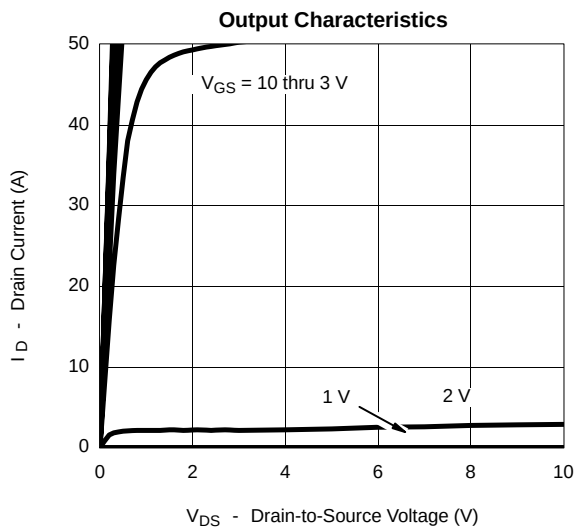
a. Surface Mounted on 1" x 1" FR4 Board.

MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.80		1.6	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 24\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 16\ \text{A}$		0.0058	0.007	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 13\ \text{A}$		0.008	0.010	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 16\ \text{A}$		38		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.74	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 5.0\ \text{V}$, $I_D = 16\ \text{A}$		16.3	24	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			5.9		
Gate Resistance	R_G		0.5	1.5	2.6	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		14	20	ns
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			44	70	
Fall Time	t_f			20	30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		40	70	

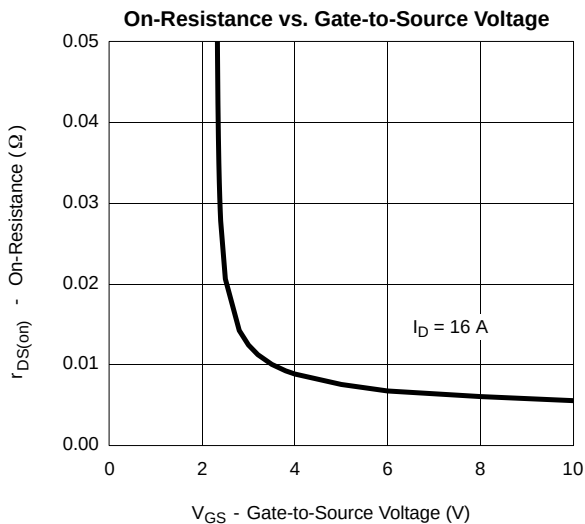
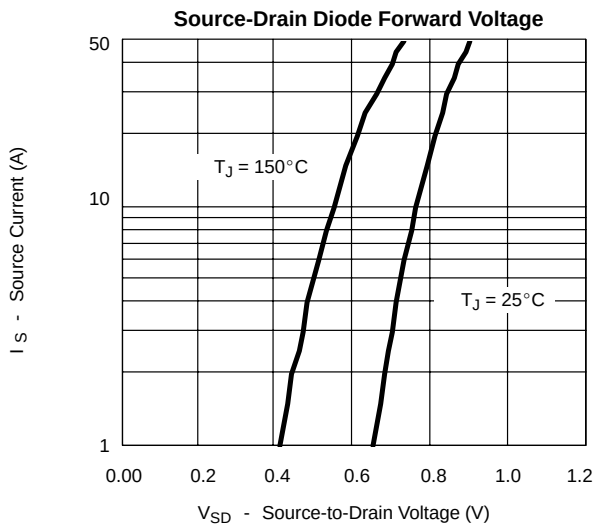
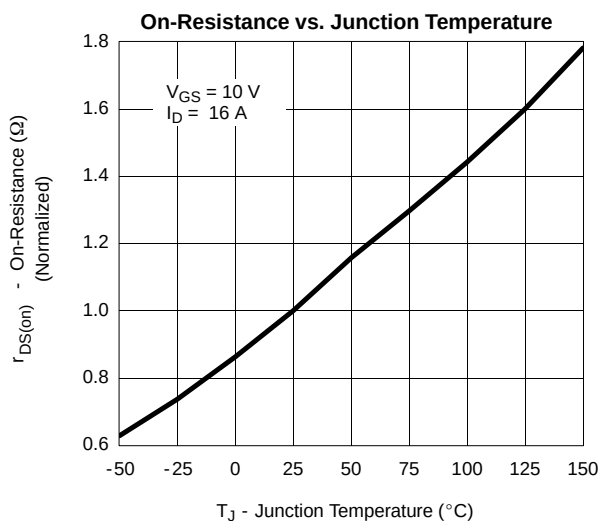
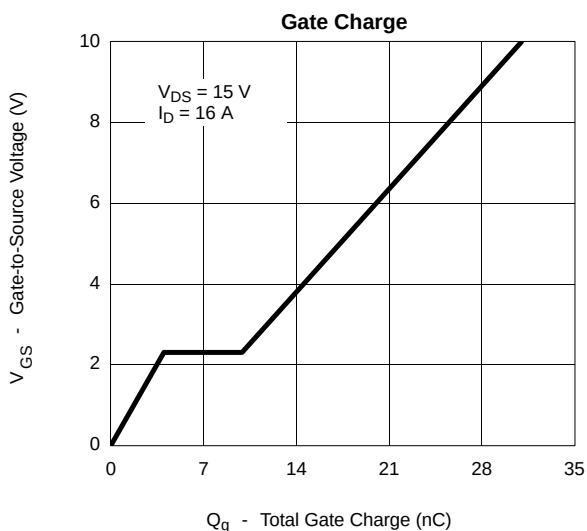
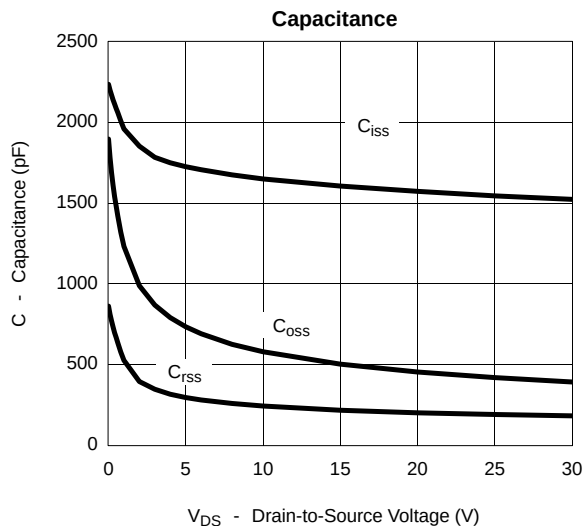
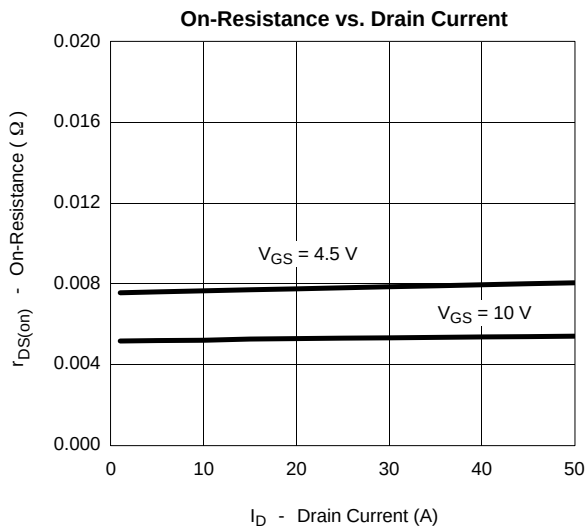
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

