

N-Channel 2.5-V (G-S) Battery Switch, ESD Protection

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
28	0.033 @ $V_{GS} = 4.5$ V	± 4.6
	0.038 @ $V_{GS} = 3.0$ V	± 4.3
	0.042 @ $V_{GS} = 2.5$ V	± 4.1



FEATURES

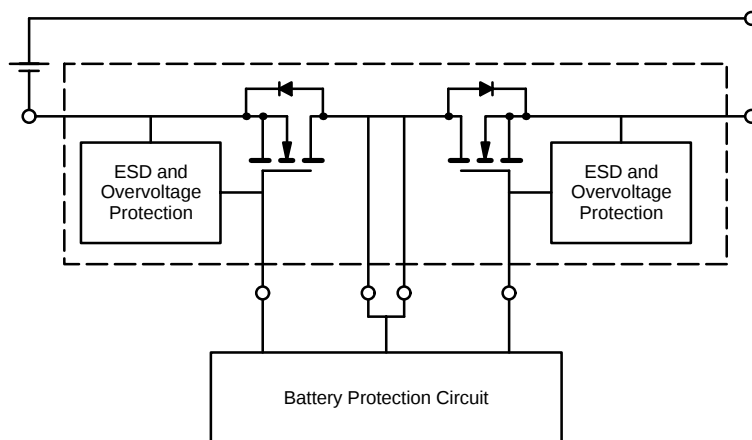
- Low $r_{DS(on)}$
- V_{GS} Max Rating: 14 V
- Exceeds 2-kV ESD Protection
- Low Profile TSSOP-8 Package
- $r_{DS(on)}$ Rating at 2.5-V V_{GS}
- 28-V V_{DS} Rated
- Symmetrical Voltage Blocking (Off Voltage)

DESCRIPTION

The Si6924EDQ is a dual n-channel MOSFET with ESD protection and gate over-voltage protection circuitry incorporated into the MOSFET. The device is designed for use in Lithium Ion battery pack circuits. The common-drain construction takes advantage of the typical battery pack topology, allowing a further reduction of the device's on-resistance. The 2-stage input protection circuit is a unique design, consisting of two stages of back-to-back zener diodes separated by a resistor. The first stage diode is designed to absorb most of the ESD energy. The second stage diode is

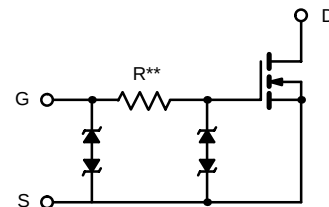
designed to protect the gate from any remaining ESD energy and over-voltages above the gates inherent safe operating range. The series resistor used to limit the current through the second stage diode during over voltage conditions has a maximum value which limits the input current to ≤ 10 mA @ 14 V and the maximum t_{off} to 12 μ s. The Si6924EDQ has been optimized as a battery or load switch in Lithium Ion applications with the advantage of both a 2.5-V $r_{DS(on)}$ rating and a safe 14-V gate-to-source maximum rating.

APPLICATION CIRCUITS



*Thermal connection to drain pins is required to achieve specific performance.

FIGURE 1. Typical Use In a Lithium Ion Battery Pack



**R typical value is 1.8 k Ω by design.

See Typical Characteristics,
Gate-Current vs. Gate-Source Voltage, Page 3.

FIGURE 2. Input ESD and Overvoltage Protection Circuit.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

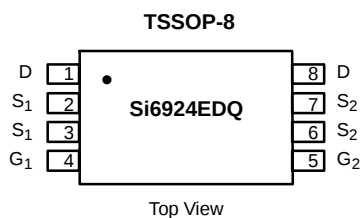
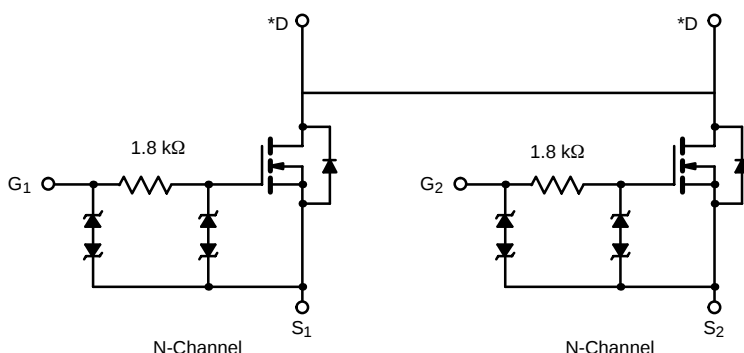


FIGURE 3.



*Thermal connection to drain pins is required to achieve specific performance.

FIGURE 4.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage, Source-Drain Voltage	V_{DS}	- to +	V
Gate-Source Voltage	V_{GS}	± 14	
Continuous Drain-to-Source Current ($T_J = 150^\circ\text{C}$) ^{a, b}	I_D	± 4.6	A
	I_D	± 3.7	
Pulsed Drain-to-Source Current	I_{DM}	± 20	
Pulsed Source Current (Diode Conduction) ^{a, b}	I_S	1.25	
Maximum Power Dissipation ^{a, b}	P_D	1.1	W
	P_D	0.72	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}		125	$^\circ\text{C/W}$
		115		

Notes

- a. Surface Mounted on FR4 Board.
b. $t \leq 10$ sec.



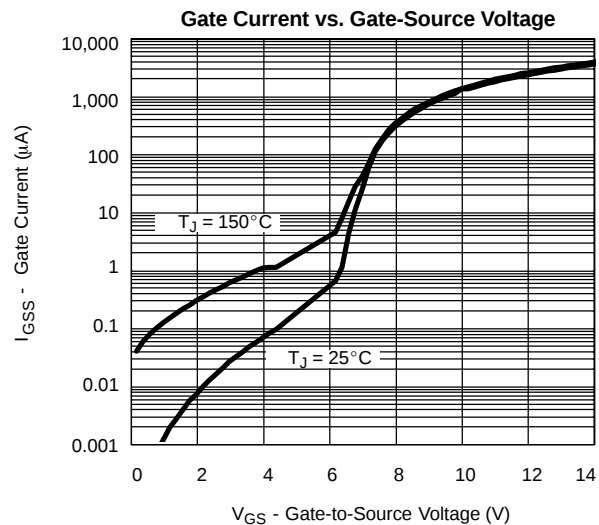
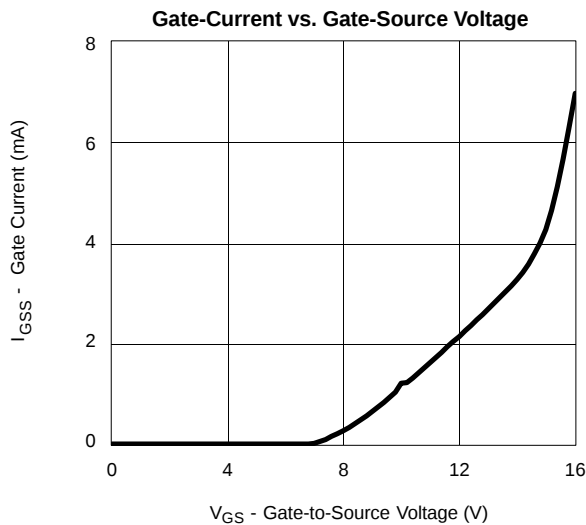
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.5			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 4.5\ \text{V}$			± 1	μA
		$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 14\ \text{V}$			± 10	mA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 22.4\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 22.4\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 5\ \text{V}$	10			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}$, $I_D = 4.6\ \text{A}$		0.026	0.033	Ω
		$V_{GS} = 3.0\ \text{V}$, $I_D = 4.3\ \text{A}$		0.029	0.038	
		$V_{GS} = 2.5\ \text{V}$, $I_D = 4.1\ \text{A}$		0.031	0.042	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\ \text{V}$, $I_D = 4.6\ \text{A}$		18		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.25\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.7	1.1	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 4.6\ \text{A}$		14	20	nC
Gate-Source Charge	Q_{gs}			2.1		
Gate-Drain Charge	Q_{gd}			4.2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \approx 1\ \text{A}$, $V_{GEN} = 4.5\ \text{V}$, $R_G = 6\ \Omega$		0.55	1.0	μs
Rise Time	t_r			2.0	4.0	
Turn-Off Delay Time	$t_{d(off)}$			7.0	12	
Fall Time	t_f			4.5	8	

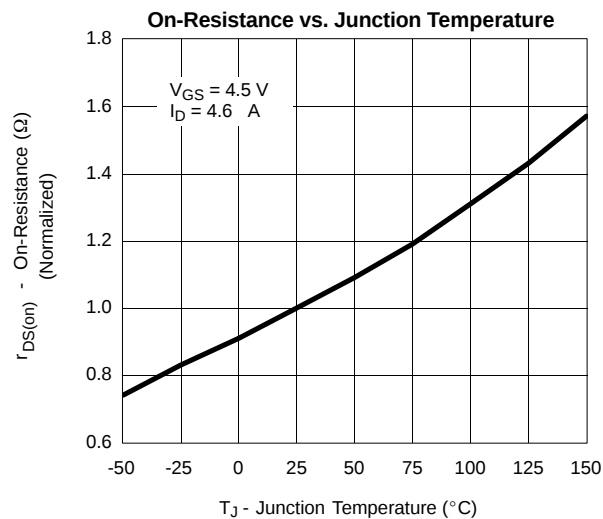
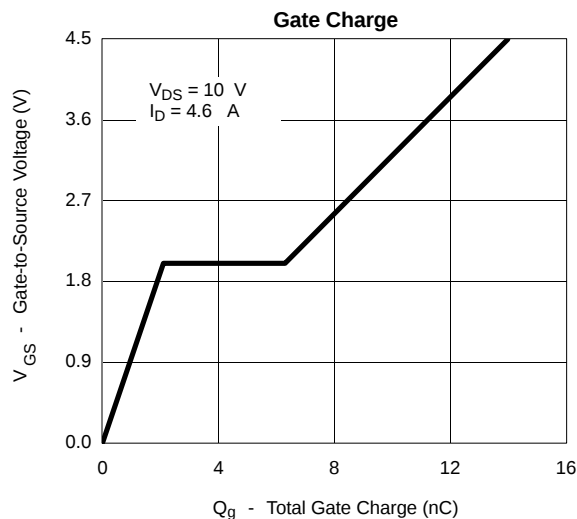
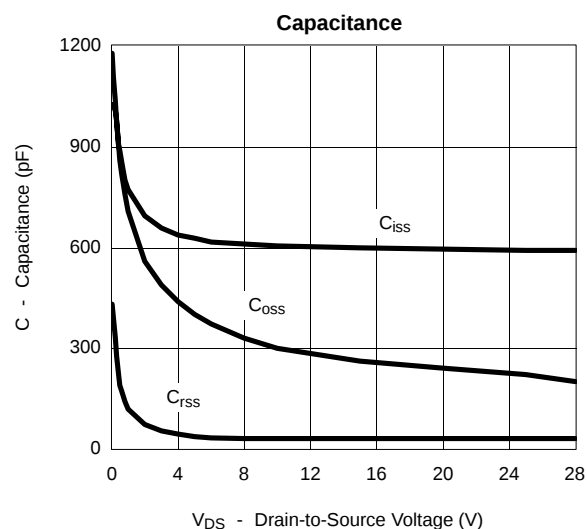
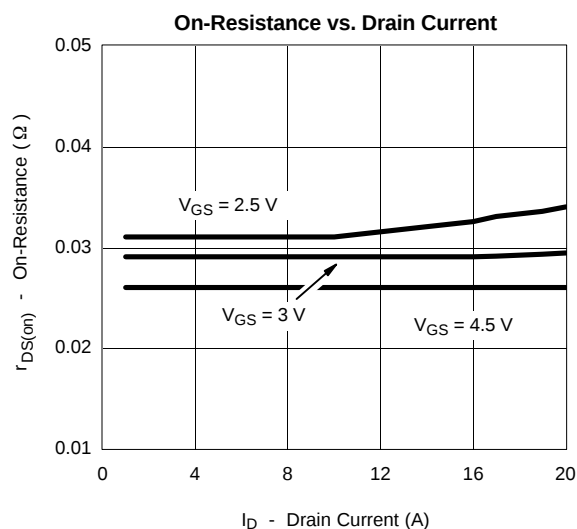
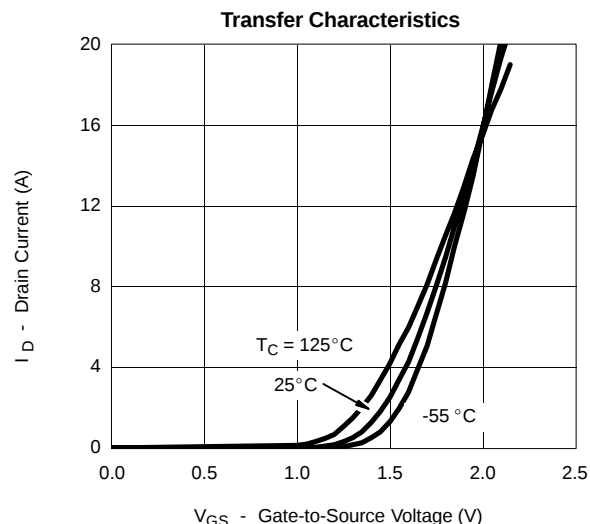
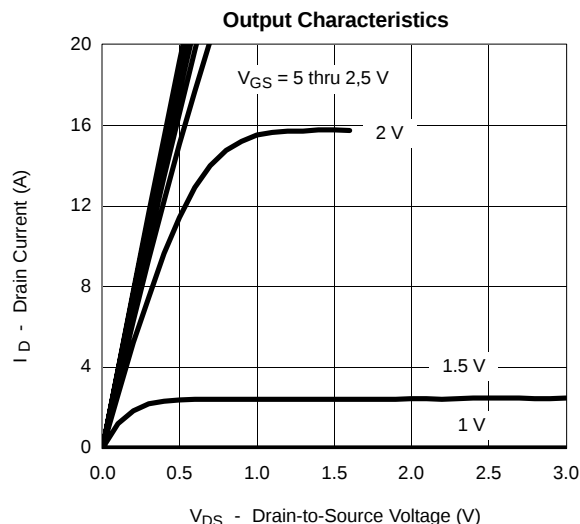
Notes

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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