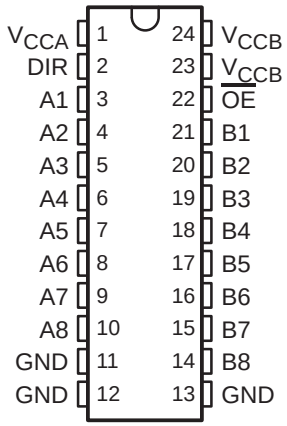
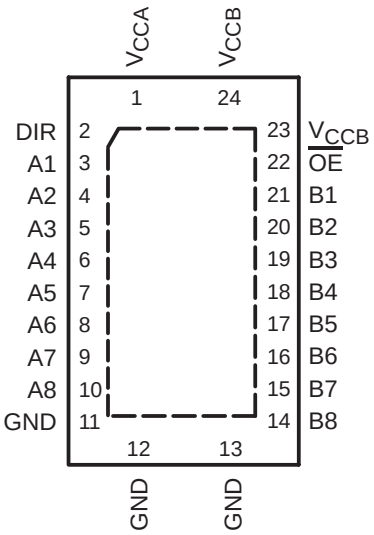
- **Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage**
- **V_{CC} Isolation Feature − If Either V_{CC} Input Is at GND, All I/O Ports Are in the High-Impedance State**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.4-V to 3.6-V Power-Supply Range**
- **I/Os Are 4.6-V Tolerant**
- **Max Data Rates:**
  - **170 Mbps (1.2 V ≤ (V_{CCA} or V_{CCB}) ≤ 3.3 V)**
  - **320 Mbps (1.8 V ≤ (V_{CCA} or V_{CCB}) ≤ 3.3 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGV OR PW PACKAGE
(TOP VIEW)



RHL PACKAGE
(TOP VIEW)



description/ordering information

This 8-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVC8T245 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RHL	Tape and reel	SN74AVC8T245RHLR	WE245
	TSSOP − PW	Tube	SN74AVC8T245PW	WE245
		Tape and reel	SN74AVC8T245PWR	
	TVSOP − DGV	Tape and reel	SN74AVC8T245DGVR	WE245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description/ordering information (continued)

The SN74AVC8T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVC8T245 is designed so the control pins (DIR and $\overline{OE}$) are supplied by V_{CCA}.

The SN74AVC8T245 solution is compatible with a single-supply system and can be replaced later with a ’245 function, with minimal printed circuit board redesign.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

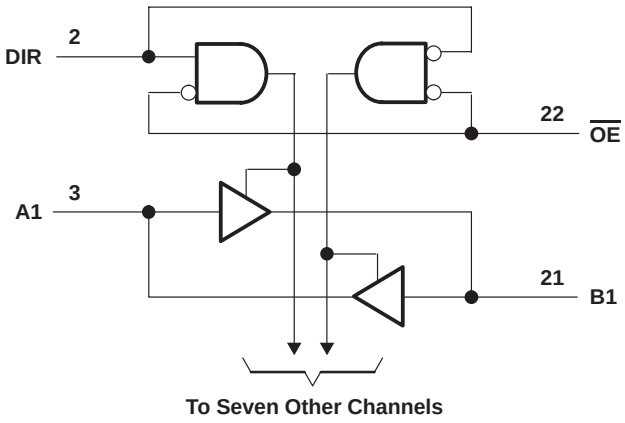
The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	All outputs Hi-Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): I/O ports (A port)	−0.5 V to 4.6 V
I/O ports (B port)	−0.5 V to 4.6 V
Control inputs	−0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	−0.5 V to 4.6 V
B port	−0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2): A port	−0.5 V to V_{CCA} + 0.5 V
B port	−0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−50 mA
Output clamp current, I_{OK} (V_O < 0)	−50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CCA}, V_{CCB}, or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGV package	86°C/W
PW package	88°C/W
RHL package	43°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 6)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs	1.2 V to 1.95 V		$V_{CCI} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 1.95 V			$V_{CCI} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V		$V_{CCA} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V			$V_{CCA} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		−3	mA
				1.4 V to 1.6 V		−6	
				1.65 V to 1.95 V		−8	
				2.3 V to 2.7 V		−9	
				3 V to 3.6 V		−12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				−40	85	°C

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.
5. V_{CCO} is the V_{CC} associated with the output port.
6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 7 and 8)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = −100 μA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} − 0.2 V		V
		I_{OH} = −3 mA		1.2 V	1.2 V		0.95				
		I_{OH} = −6 mA		1.4 V	1.4 V				1.05		
		I_{OH} = −8 mA		1.65 V	1.65 V				1.2		
		I_{OH} = −9 mA		2.3 V	2.3 V				1.75		
		I_{OH} = −12 mA		3 V	3 V				2.3		
V_{OL}		I_{OL} = 100 μA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.15				
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	μA
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 to 3.6 V		±0.1	±1		±5	μA
	A or B port			0 to 3.6 V	0 V		±0.1	±1		±5	
I_{OZ}†	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	$\overline{OE} = V_{IH}$	3.6 V	3.6 V		±0.5	±2.5		±5	μA
I_{CCA}		$V_I = V_{CCI}$ or GND	I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					15	μA
				0 V	3.6 V					−2	
				3.6 V	0 V					15	
I_{CCB}		$V_I = V_{CCI}$ or GND	I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					15	μA
				0 V	3.6 V					15	
				3.6 V	0 V					−2	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND	I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					25	μA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		3.5			4.5	pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		6			7	pF

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

NOTES: 7. V_{CCO} is the V_{CC} associated with the output port.
8. V_{CCI} is the V_{CC} associated with the input port.

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.1	2.6	2.5	3	3.5	ns
t_{PHL}			3.1	2.6	2.5	3	3.5	
t_{PLH}	B	A	3.1	2.7	2.5	2.4	2.3	ns
t_{PHL}			3.1	2.7	2.5	2.4	2.3	
t_{PZH}	$\overline{OE}$	A	5.3	5.3	5.3	5.3	5.3	ns
t_{PZL}			5.3	5.3	5.3	5.3	5.3	
t_{PZH}	$\overline{OE}$	B	5.1	4	3.5	3.2	3.1	ns
t_{PZL}			5.1	4	3.5	3.2	3.1	
t_{PHZ}	$\overline{OE}$	A	4.8	4.8	4.8	4.8	4.8	ns
t_{PLZ}			4.8	4.8	4.8	4.8	4.8	
t_{PHZ}	$\overline{OE}$	B	4.7	4	4.1	4.3	5.1	ns
t_{PLZ}			4.7	4	4.1	4.3	5.1	

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.7	0.5	5.4	0.5	4.6	0.5	4.9	0.5	6.8	ns
t_{PHL}			2.7	0.5	5.4	0.5	4.6	0.5	4.9	0.5	6.8	
t_{PLH}	B	A	2.6	0.5	5.4	0.5	5.1	0.5	4.7	0.5	4.5	ns
t_{PHL}			2.6	0.5	5.4	0.5	5.1	0.5	4.7	0.5	4.5	
t_{PZH}	$\overline{OE}$	A	3.7	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	ns
t_{PZL}			3.7	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	
t_{PZH}	$\overline{OE}$	B	4.8	1.1	7.6	1.1	7.1	1	5.6	1	5.2	ns
t_{PZL}			4.8	1.1	7.6	1.1	7.1	1	5.6	1	5.2	
t_{PHZ}	$\overline{OE}$	A	3.1	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	ns
t_{PLZ}			3.1	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	
t_{PHZ}	$\overline{OE}$	B	4.1	0.5	8.4	0.5	7.6	0.5	7.2	0.5	7.8	ns
t_{PLZ}			4.1	0.5	8.4	0.5	7.6	0.5	7.2	0.5	7.8	

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.5	0.5	5.1	0.5	4.4	0.5	4	0.5	3.9	ns
t_{PHL}			2.5	0.5	5.1	0.5	4.4	0.5	4	0.5	3.9	
t_{PLH}	B	A	2.5	0.5	4.6	0.5	4.4	0.5	3.9	0.5	3.7	ns
t_{PHL}			2.5	0.5	4.6	0.5	4.4	0.5	3.9	0.5	3.7	
t_{PZH}	$\overline{OE}$	A	3	1	6.8	1	6.8	1	6.8	1	6.8	ns
t_{PZL}			3	1	6.8	1	6.8	1	6.8	1	6.8	
t_{PZH}	$\overline{OE}$	B	4.6	1.1	8.2	1	6.7	0.5	5.1	0.5	4.5	ns
t_{PZL}			4.6	1.1	8.2	1	6.7	0.5	5.1	0.5	4.5	
t_{PHZ}	$\overline{OE}$	A	2.8	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	ns
t_{PLZ}			2.8	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	
t_{PHZ}	$\overline{OE}$	B	3.9	0.5	7.8	0.5	6.9	0.5	6	0.5	5.8	ns
t_{PLZ}			3.9	0.5	7.8	0.5	6.9	0.5	6	0.5	5.8	

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.4	0.5	4.7	0.5	3.9	0.5	3.1	0.5	2.8	ns
t_{PHL}			2.4	0.5	4.7	0.5	3.9	0.5	3.1	0.5	2.8	
t_{PLH}	B	A	3	0.5	4.9	0.5	4	0.5	3.1	0.5	2.9	ns
t_{PHL}			3	0.5	4.9	0.5	4	0.5	3.1	0.5	2.9	
t_{PZH}	$\overline{OE}$	A	2.2	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	ns
t_{PZL}			2.2	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	
t_{PZH}	$\overline{OE}$	B	4.5	1.1	7.9	0.5	6.4	0.5	4.6	0.5	4	ns
t_{PZL}			4.5	1.1	7.9	0.5	6.4	0.5	4.6	0.5	4	
t_{PHZ}	$\overline{OE}$	A	1.8	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	ns
t_{PLZ}			1.8	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	
t_{PHZ}	$\overline{OE}$	B	3.6	0.5	7.1	0.5	6.3	0.5	5.1	0.5	3.9	ns
t_{PLZ}			3.6	0.5	7.1	0.5	6.3	0.5	5.1	0.5	3.9	

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	0.5	4.5	0.5	3.7	0.5	2.9	0.5	2.5	ns
t_{PHL}			2.3	0.5	4.5	0.5	3.7	0.5	2.9	0.5	2.5	
t_{PLH}	B	A	3.5	0.5	6.8	0.5	3.9	0.5	2.8	0.5	2.5	ns
t_{PHL}			3.5	0.5	6.8	0.5	3.9	0.5	2.8	0.5	2.5	
t_{PZH}	$\overline{OE}$	A	2	0.5	4	0.5	4	0.5	4	0.5	4	ns
t_{PZL}			2	0.5	4	0.5	4	0.5	4	0.5	4	
t_{PZH}	$\overline{OE}$	B	4.5	1.1	7.8	0.5	6.2	0.5	4.5	0.5	3.9	ns
t_{PZL}			4.5	1.1	7.8	0.5	6.2	0.5	4.5	0.5	3.9	
t_{PHZ}	$\overline{OE}$	A	1.7	0.5	4	0.5	4	0.5	4	0.5	4	ns
t_{PLZ}			1.7	0.5	4	0.5	4	0.5	4	0.5	4	
t_{PHZ}	$\overline{OE}$	B	3.4	0.5	6.9	0.5	6	0.5	4.8	0.5	4.2	ns
t_{PLZ}			3.4	0.5	6.9	0.5	6	0.5	4.8	0.5	4.2	

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pdA}†	A to B	Outputs Enabled	C_L = 0, f = 10 MHz, $t_r = t_f$ =1 ns	1	1	1	1	1	pF
		Outputs Disabled		1	1	1	1	1	
	B to A	Outputs Enabled		12	12	12	13	14	
		Outputs Disabled		1	1	1	1	1	
C_{pdB}†	A to B	Outputs Enabled	C_L = 0, f = 10 MHz, $t_r = t_f$ =1 ns	12	12	12	13	14	pF
		Outputs Disabled		1	1	1	1	1	
	B to A	Outputs Enabled		1	1	1	1	1	
		Outputs Disabled		1	1	1	1	1	

† Power-dissipation capacitance per transceiver

typical total static power consumption (I_{CCA} + I_{CCB})

Table 1

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 1.2$ V

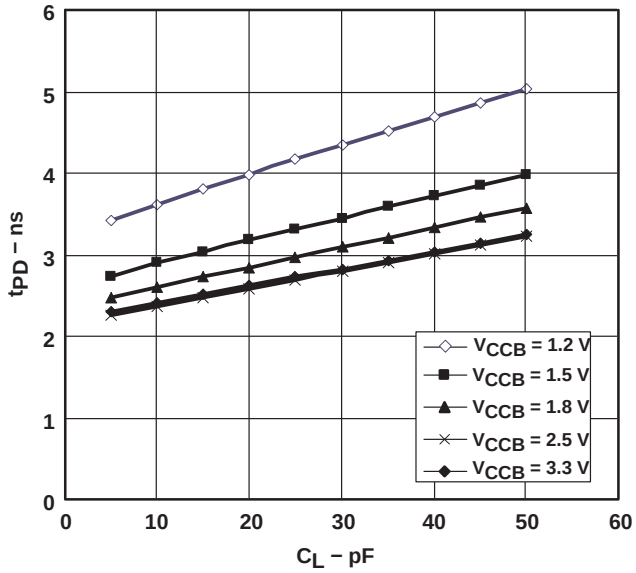


Figure 1

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 1.5$ V

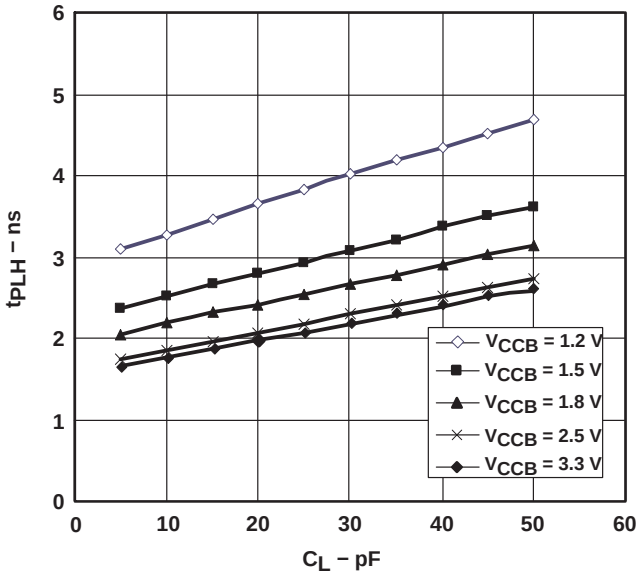


Figure 2

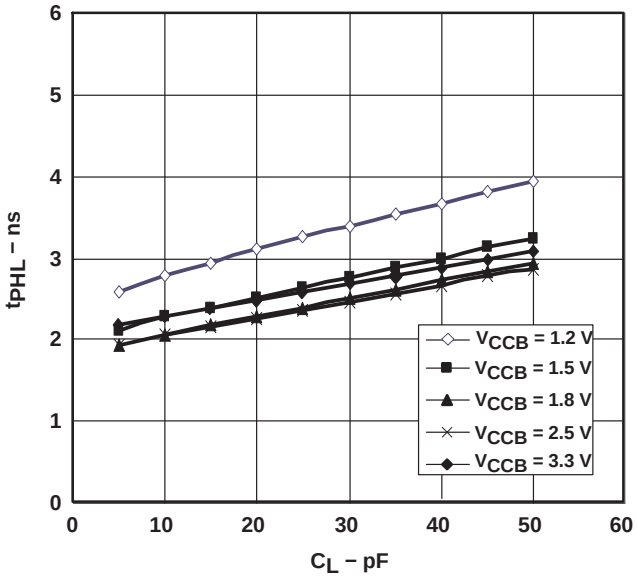


Figure 3

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
T_A = 25°C, V_{CCA} = 1.8 V

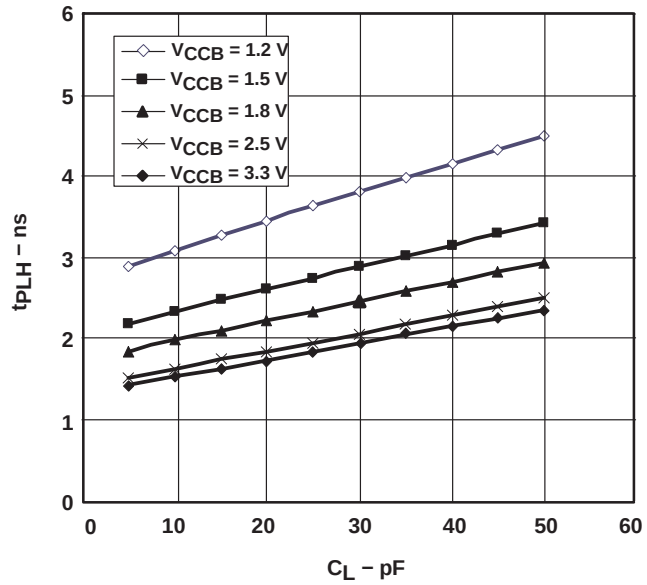


Figure 4

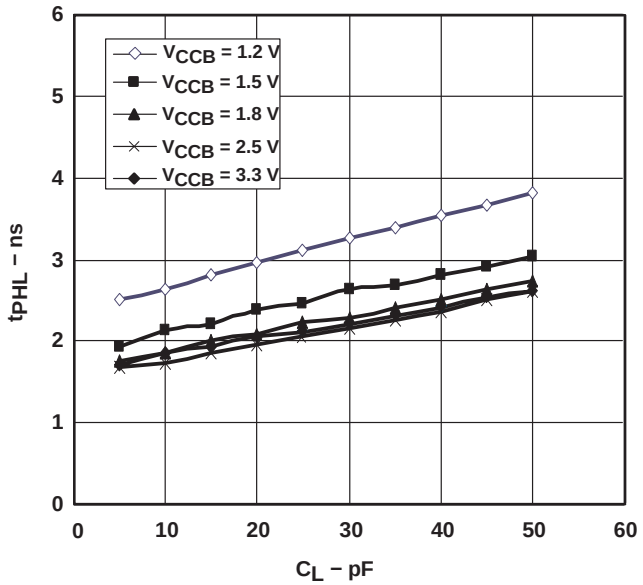


Figure 5

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
T_A = 25°C, V_{CCA} = 2.5 V

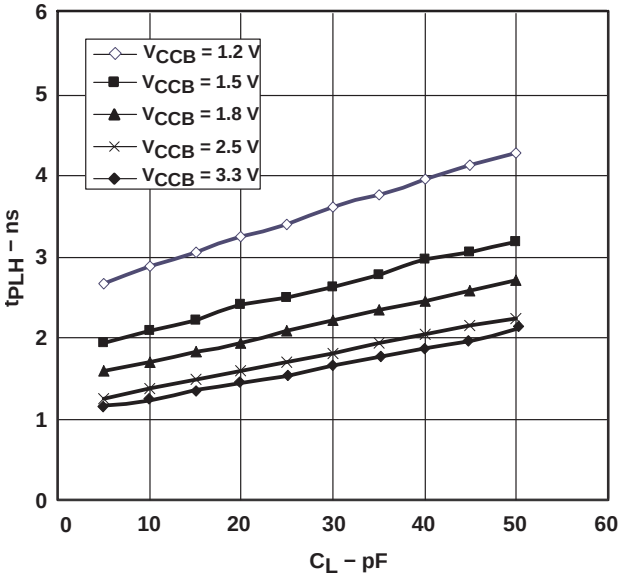


Figure 6

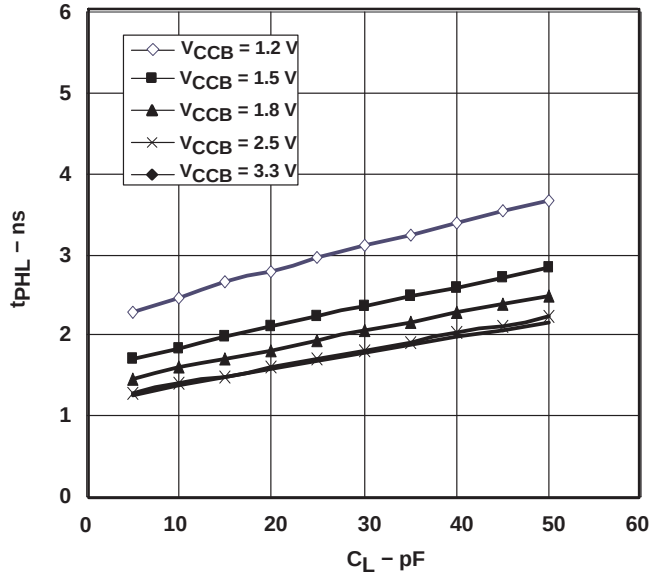


Figure 7

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
T_A = 25°C, V_{CCA} = 3.3 V

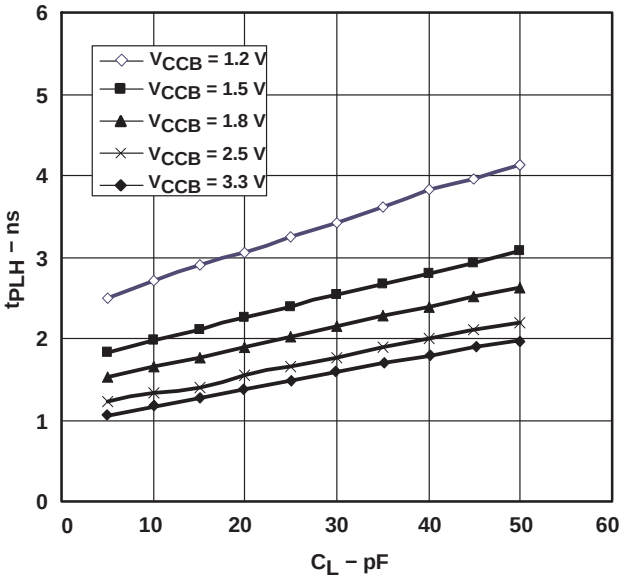


Figure 8

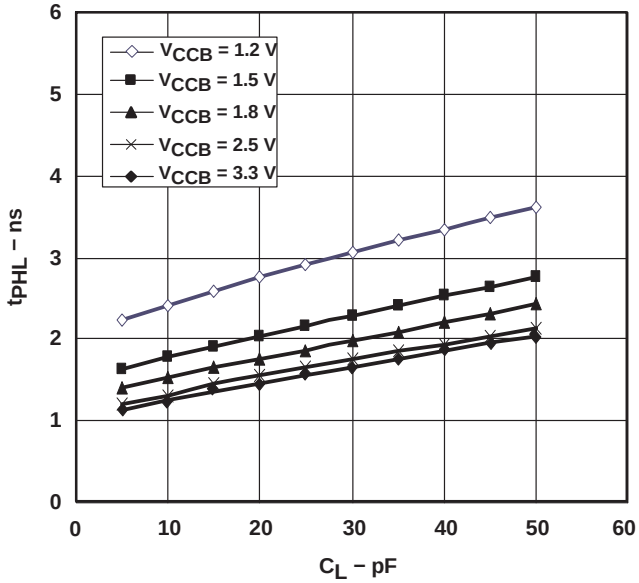
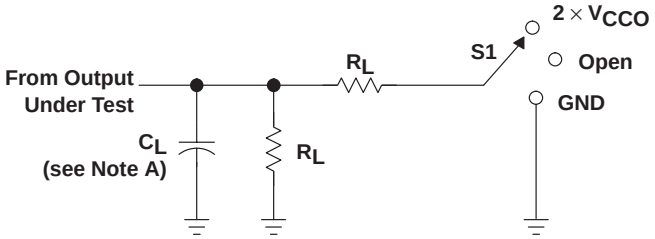


Figure 9

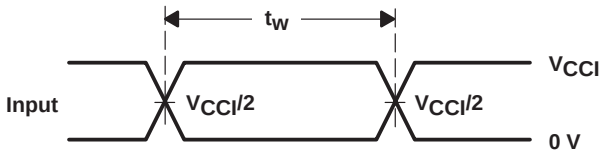
PARAMETER MEASUREMENT INFORMATION



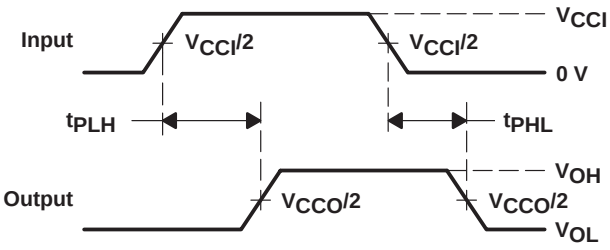
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

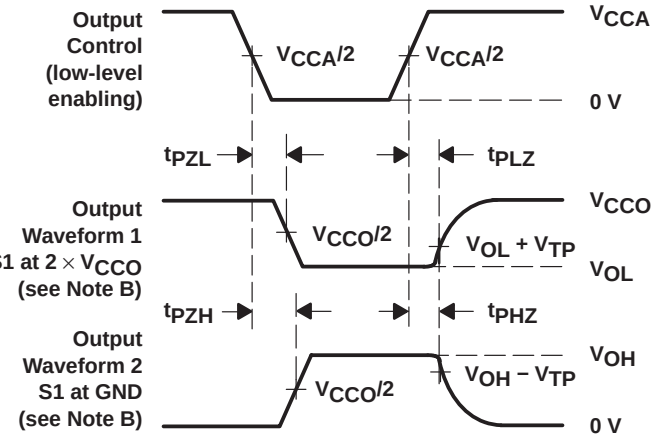
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



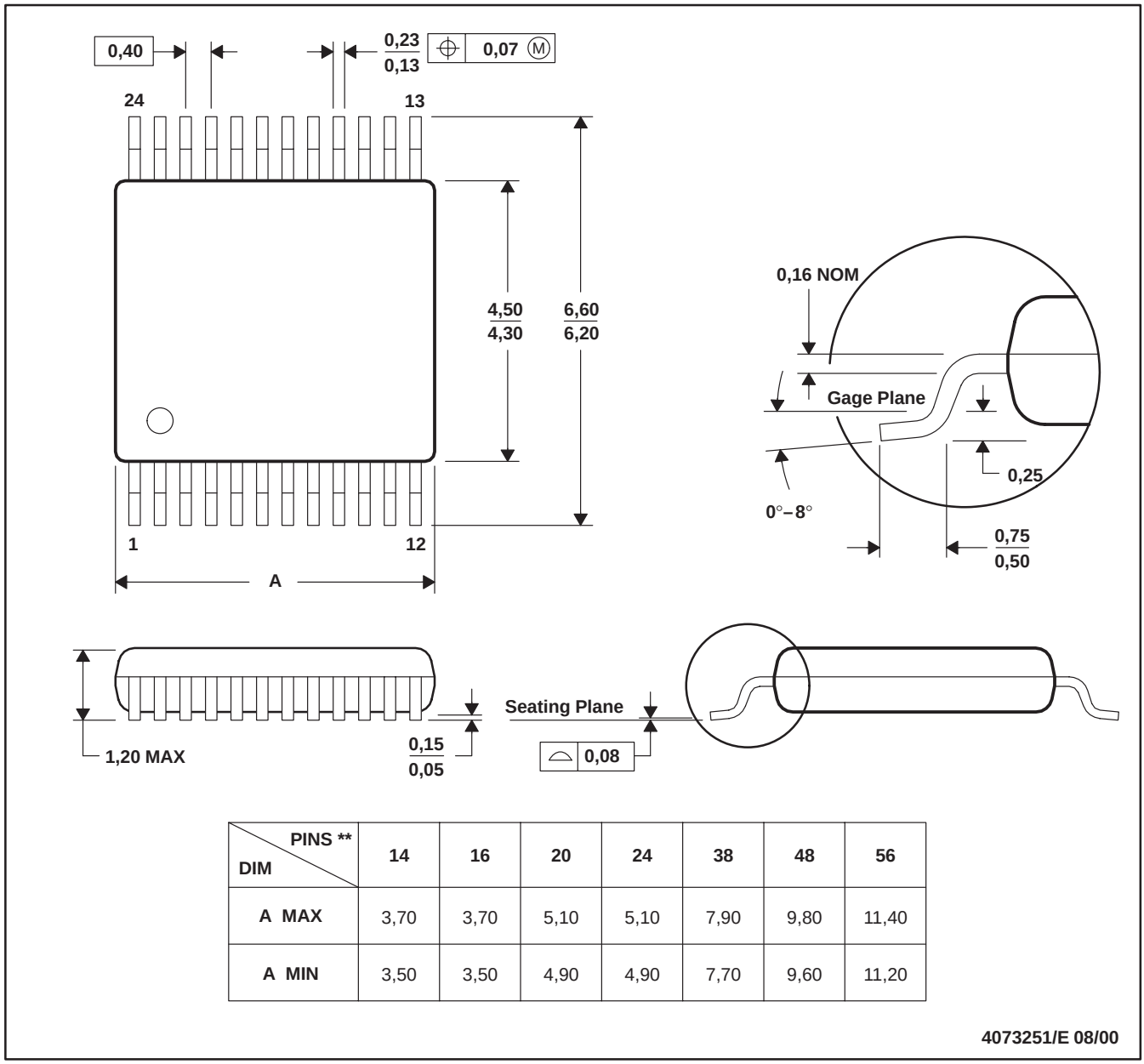
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 10. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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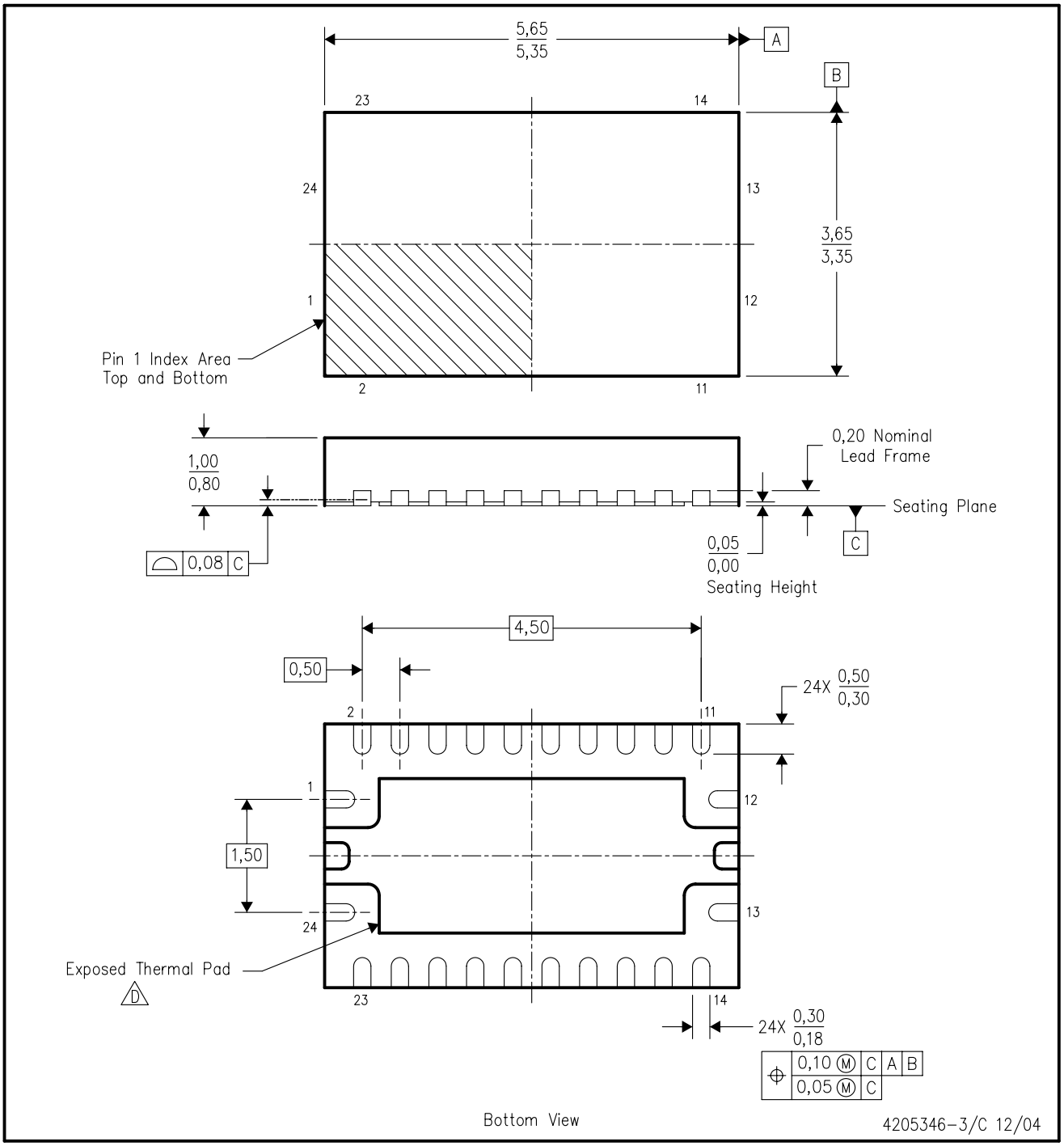
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

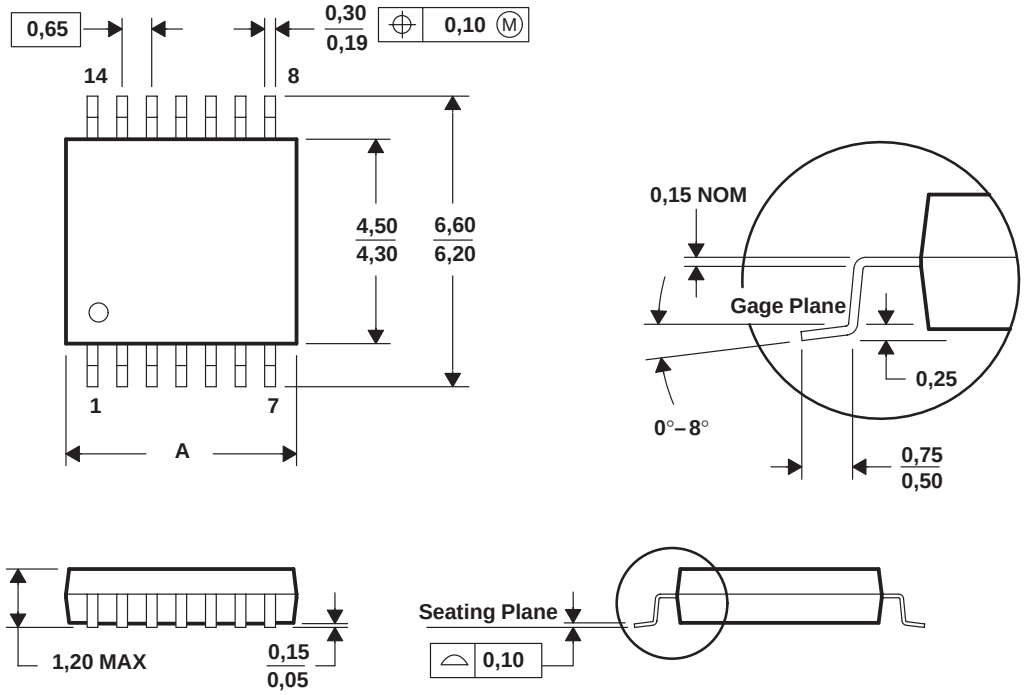
RHL (R–PQFP–N24) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–241 package registration pending.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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