UCC283-3/-5/-ADJ
UCC383-3/-5/-ADJ

UNITRODE

Low Dropout 3 Ampere Linear Regulator Family

FEATURES

- Precision Positive Series Pass Voltage Regulation
- 0.45V Dropout at 3A
- 50mV Dropout at 10mA
- Quiescent Current Under 650µA Irrespective of Load
- Adjustable (5 Lead) Output Voltage Version
- Fixed (3 Lead) Versions for 3.3V and 5V Outputs
- Logic Shutdown Capability
- Short Circuit Power Limit of $3\% \cdot V_{IN} \cdot I_{SHORT}$
- Low V_{OUT} to V_{IN} Reverse Leakage
- Thermal Shutdown

DESCRIPTION

The UCC283-3/-5/-ADJ family of positive linear series pass regulators are tailored for low drop out applications where low quiescent power is important. Fabricated with a BiCMOS technology ideally suited for low input to output differential applications, the UCC283-5 will pass 3A while requiring only 0.45V of typical input voltage headroom (guaranteed 0.6V dropout). These regulators include reverse voltage sensing that prevents current in the reverse direction. Quiescent current is always less than 650µA. These devices have been internally compensated in such a manner that the need for a minimum output capacitor has been eliminated.

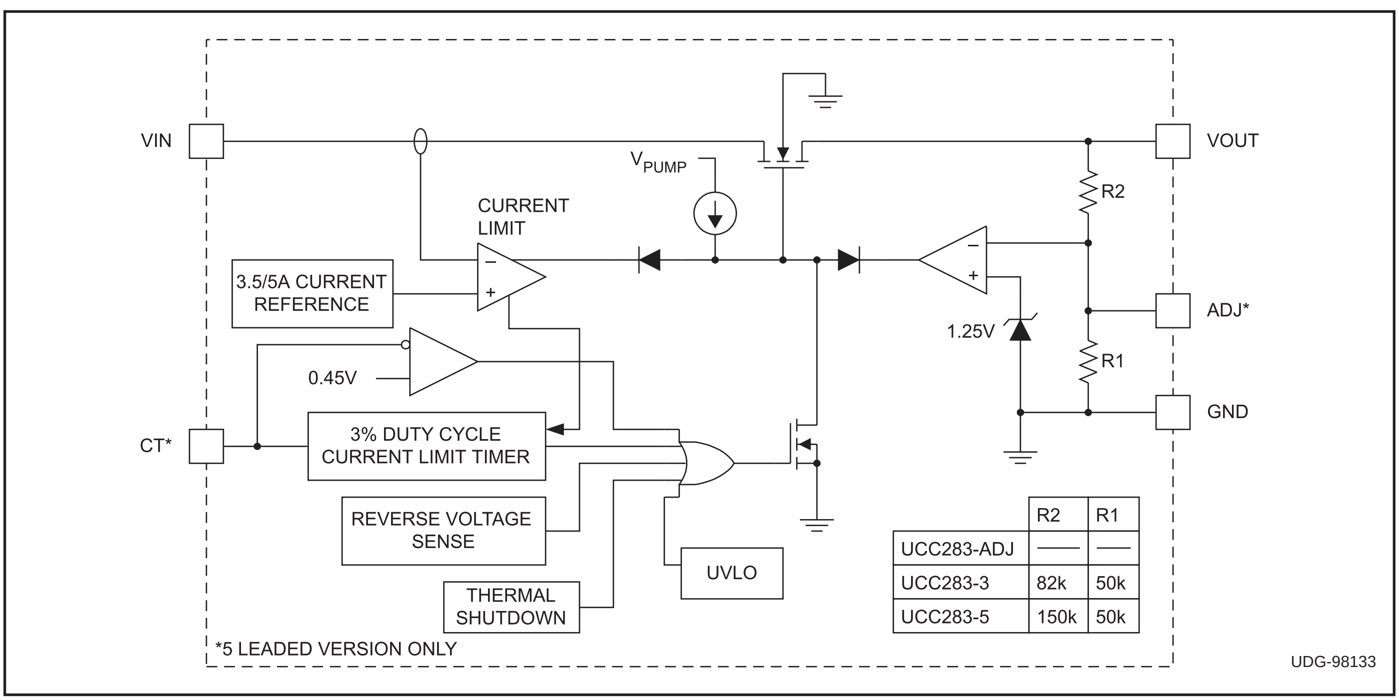
UCC283-3 and UCC283-5 versions are in 3 lead packages and have preset outputs at 3.3V and 5.0V respectively. The output voltage is regulated to 1.5% at room temperature. The UCC283-ADJ version, in a 5 lead package, regulates the output voltage programmed by an external resistor ratio.

Short circuit current is internally limited. The device responds to a sustained overcurrent condition by turning off after a T_{ON} delay. The device then stays off for a period, T_{OFF}, that is 32 times the T_{ON} delay. The device then begins pulsing on and off at the $T_{ON}/(T_{ON}+T_{OFF})$ duty cycle of 3%. This drastically reduces the power dissipation during short circuit and means heat sinks need only accommodate normal operation. On the 3 leaded versions of the device T_{ON} is fixed at 750µs, on the adjustable 5 leaded versions an external capacitor sets the on time — the off time is always 32 times T_{ON}. The external timing control pin, CT, on the five leaded versions also serves as a shutdown input when pulled low.

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 165°C. The chip will remain off until the temperature has dropped 20°C.

The UCC283 series is specified for operation over the industrial range of –40°C to +85°C, and the UCC383 series is specified from 0°C to +70°C. These devices are available in 3 and 5 pin TO-220 and TO-263 power packages.

BLOCK DIAGRAM



	R2	R1
UCC283-ADJ	——	——
UCC283-3	82k	50k
UCC283-5	150k	50k

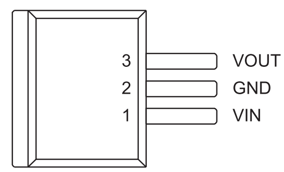
ABSOLUTE MAXIMUM RATINGS

VIN 9V
CT . . . . –0.3 to 3V
ADJ . . . . –0.3 to 9V
Storage Temperature . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . +300°C

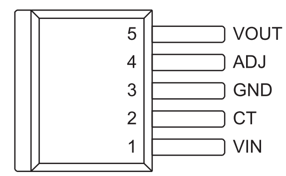
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

TO-263-3 (Front View)
TD Package

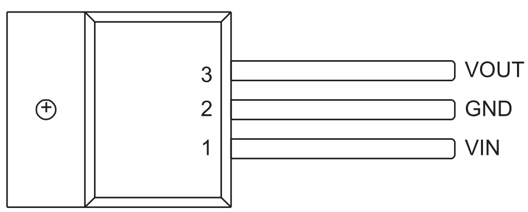


TO-263-5 (Front View)
TD Package



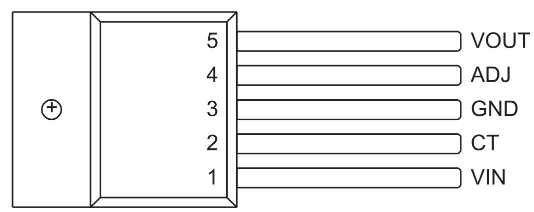
See Note 1

TO-220-3 (Front View)
T Package



See Note 1

TO-220-5 (Front View)
T Package



See Note 1

Note 1: Tab = GND

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC383-X series, –40°C to +85°C for the UCC283-X, $V_{VIN} = V_{VOUT}$ + 1.5V, I_{OUT} = 10mA, C_{IN} = 10µF, C_{OUT} = 22µF. For the 283-ADJ, V_{VIN} = 6.5V, CT = 750pF, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC283-5 Fixed 5V, 3A Family					
Output Voltage	T_J = 25°C	4.925	5	5.075	V
	Over Temperature	4.875		5.125	V
Line Regulation	V_{VIN} = 5.15V to 9V		2	10	mV
Load Regulation	I_{OUT} = 10mA to 3A		10	20	mV
Dropout Voltage, $V_{DROPOUT} = V_{VIN} - V_{VOUT}$	I_{OUT} = 3A, VOUT = 4.85V		0.4	0.6	V
	I_{OUT} = 1.5A, VOUT = 4.85V		0.2	0.45	V
	I_{OUT} = 10mA, VOUT = 4.85V		50	150	mV
Peak Current Limit	V_{VOUT} = 0V	4	5	6.5	A
Overcurrent Threshold		3	4	5.5	A
Current Limit Duty Cycle	V_{VOUT} = 0V		3	5	%
Overcurrent Time Out, T_{ON}	V_{VOUT} = 0V	400	750	1400	µs
Quiescent Current	No load		400	650	µA
Reverse Leakage Current	0V < V_{VIN} < V_{VOUT}, V_{VOUT} ≤ 5.1V, at V_{VOUT}		0	75	µA
UVLO	VIN where VOUT passes current	2.6	2.8	3	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC383-X series, –40°C to +85°C for the UCC283-X, V_{VIN} = V_{VOUT} + 1.5V, I_{OUT} = 10mA, C_{IN} = 10µF, C_{OUT} = 22µF. For the 283-ADJ, V_{VIN} = 6.5V, CT = 750pF, T_J = T_A.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC283-3 Fixed 3.3V, 3A Family					
Output Voltage	T_J = 25°C	3.25	3.3	3.35	V
	Over Temperature	3.22		3.38	V
Line Regulation	V_{VIN} = 3.45V to 9V		2	7	mV
Load Regulation	I_{OUT} = 10mA to 3A		7	15	mV
Dropout Voltage, $V_{DROPOUT}$ = V_{VIN} – V_{VOUT}	I_{OUT} = 3A, VOUT = 3.15V		0.5	1	V
	I_{OUT} = 1.5A, VOUT = 3.15V		0.25	0.6	V
	I_{OUT} = 10mA, VOUT = 3.15V		50	150	mV
Peak Current Limit	V_{VOUT} = 0V	4	5	6.5	A
Overcurrent Threshold		3	4	5.5	A
Current Limit Duty Cycle	V_{VOUT} = 0V		3	5	%
Overcurrent Time Out, T_{ON}	V_{VOUT} = 0V	400	750	1400	µs
Quiescent Current	No load		400	650	µA
Reverse Leakage Current	0V < V_{VIN} < V_{VOUT}, V_{VOUT} ≤ 3.35V, at V_{VOUT}		0	75	µA
UVLO	VIN where VOUT passes current	2.6	2.8	3	V
UCC283-ADJ Adjustable Output, 3A Family					
Regulating Voltage at ADJ Pin	T_J = 25°C	1.23	1.25	1.27	V
	Over Temperature	1.22		1.28	V
Line Regulation, at ADJ Input	V_{VIN} = V_{VOUT} + 150mV to 9V		1	3	mV
Load Regulation, at ADJ Input	I_{OUT} = 10mA to 3A		2	5	mV
Dropout Voltage, $V_{DROPOUT}$ = VIN – VOUT	V_{VIN} > 4V, I_{OUT} = 3A		0.4	0.6	V
	V_{VIN} > 3V, I_{OUT} = 1.5A		0.2	0.45	V
	V_{VIN} > 3V, I_{OUT} = 10mA		50	150	mV
Peak Current Limit	V_{VOUT} = 0V, VIN = 6.5V	4	5	6.5	A
Overcurrent Threshold	V_{VIN} = 6.5V	3	4	5.5	A
Current Limit Duty Cycle	V_{VOUT} = 0V		3	5	%
Overcurrent Time Out, T_{ON}	V_{VOUT} = 0V, CT = 1500pF		750		µs
Reverse Leakage Current	0V < V_{VIN} < V_{VOUT}, V_{VOUT} ≤ 9V, at V_{VOUT}		0	100	µA
Bias current at ADJ Input			100	250	nA
Quiescent Current	No load		400	650	µA
Shutdown Threshold	At CT Input	0.25	0.45		V
Quiescent Current in Shutdown	V_{VIN} = 10V		40	75	µA
UVLO	VIN where VOUT passes current	2.6	2.8	3	V

PIN DESCRIPTIONS

ADJ: Adjust pin for the UCC283-ADJ version only. Feedback pin for the linear regulator. Program the output voltage with R1 connected from ADJ to GND and R2 connected from VOUT to ADJ. Output voltage is given by:

$$VOUT = \frac{1.25V \bullet (R1 + R2)}{R1}$$

CT: Short circuit timing capacitor and shutdown input for the UCC283-ADJ version. Pulling CT below 0.25V turns off the regulator and places it in a low quiescent current mode. A timing capacitor, C, from CT to GND programs the duration of the pulsed short circuit on-time. On-time, T_{ON}, is approximately given by: $T_{ON} = 500k \bullet C$.

GND: Reference ground.

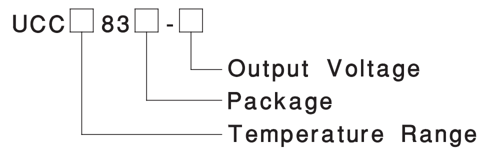
VIN: Input voltage, This pin must be bypassed with a low ESL/ESR 1µF or larger capacitor to GND. VIN can range from (VOUT + $V_{DROPOUT}$) to 9V. If VIN is reduced to zero while VOUT is held high, the reverse leakage from VOUT to VIN is less than 75µA.

VOUT: Regulated output voltage. A bypass capacitor is not required at VOUT, but may be desired for good transient response. The bypass capacitor must not exceed a maximum value in order to insure the regulator can start.

Table I. Package Information

Temperature Range	Package	Output Voltage
2: –40°C to +85°C	T: TO-220	3: 3.3V
3: 0°C to +70°C	TD: TO-263	5: 5V
		ADJ: Adjustable

ORDERING INFORMATION



APPLICATION INFORMATION

Overview

The UCC383 family of low dropout linear (LDO) regulators provide a regulated output voltage for applications with up to 3A of load current. The regulators feature a low dropout voltage and short circuit protection, making their use ideal for demanding high current applications requiring fault protection.

Short Circuit Protection

The UCC383 provides unique short circuit protection circuitry that reduces power dissipation during a fault. When an overload situation is detected, the device enters a pulsed mode of operation at 3% duty cycle reducing the heat sink requirements during a fault. The UCC383 has two current thresholds that determine its behavior during a fault as shown in Figure 1.When the regulator current exceeds the **overcurrent threshold** for a period longer than T_{ON}, the UCC383 shuts off for a period (T_{OFF}) which is 32 times T_{ON}. During an overload, the regulator actively limits the maximum current to the **peak current limit** value. The peak current limit is nominally 1 Amp greater than the overcurrent threshold. The regulator will continue in pulsed mode until the fault is cleared as illustrated in Figure 1.

Short Circuit Protection

A capacitive load on the regulator's output will appear as a short circuit during start-up. If the capacitance is too large, the output voltage will not come into regulation during the initial T_{ON} period and the UCC383 will enter pulsed mode operation. The peak current limit, T_{ON} period, and load characteristics determine the maximum value of output capacitor that can be charged. For a constant current load the maximum output capacitance is given as follows:

$$C_{OUT(max)} = (I_{CL} - I_{LOAD}) \bullet \frac{T_{ON}}{V_{OUT}} \ Farads \quad (1)$$

For worst case calculations the minimum values of on time (T_{ON}) and peak current limit (I_{CL}) should be used. The adjustable version allows the T_{ON} time to be adjusted with a capacitor on the CT pin:

$$T_{ON(ADJ)} = 500,000 \bullet C(\mu Farad)\ microseconds \quad (2)$$

$$T_{ON(\mu sec)} = 500,000 \bullet C(\mu Farads)$$

For a resistive load (R_{LOAD}) the maximum output capacitor can be estimated from:

$$C_{OUT(max)} = \frac{T_{ON(sec)}}{R_{LOAD} \bullet \ell n\left(\frac{1}{1 - \frac{V_{OUT}}{I_{CL} \bullet R_{LOAD}}}\right)} \ Farads \quad (3)$$

APPLICATION INFORMATION (cont.)

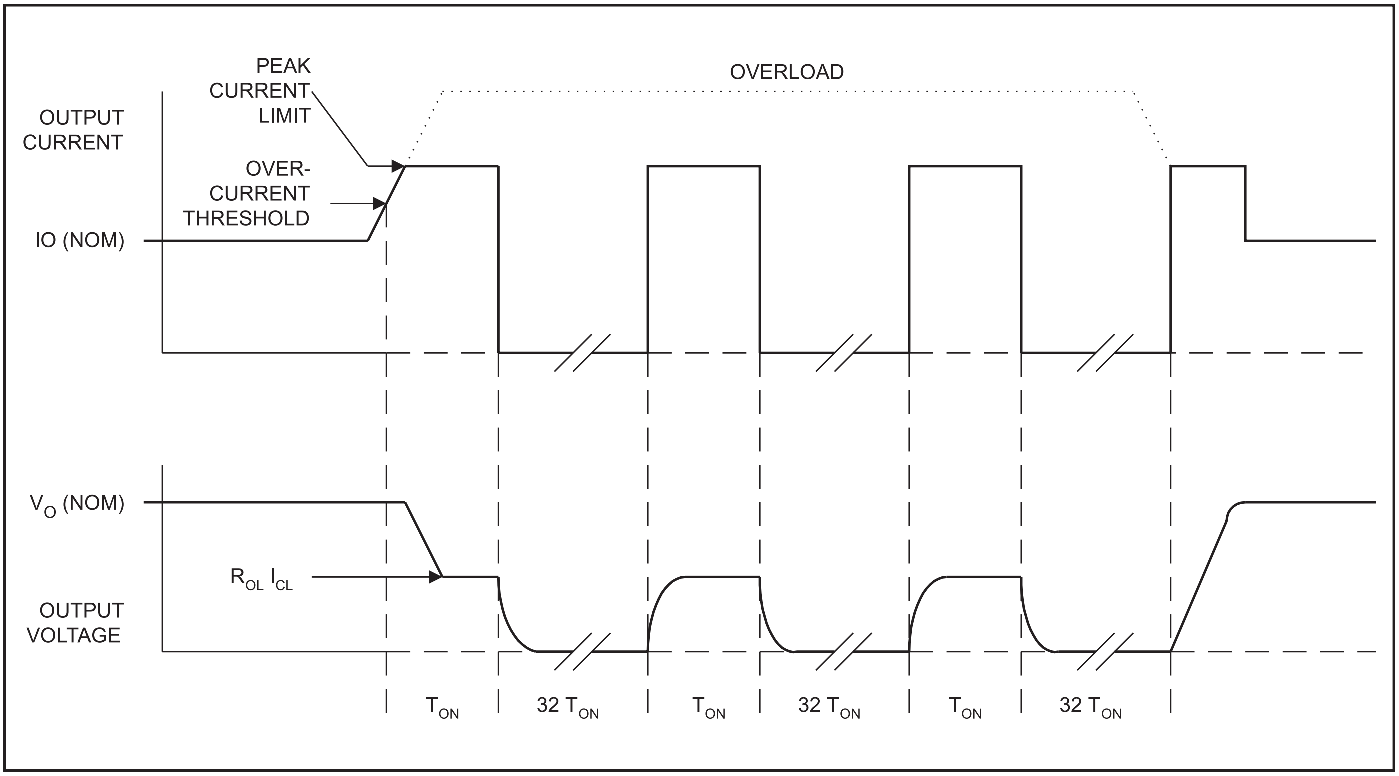


Figure 1. UCC383 Short Circuit Timing

Dropout Performance

Referring to the Block Diagram, the dropout voltage of the UCC383 is equal to the minimum voltage drop (V_{IN} to V_{OUT}) across the N-Channel MOSFET. The dropout voltage is dependent on operating conditions such as load current, input and load voltages, as well as temperature. The UCC383 achieves a low $RDS_{(ON)}$ through the use of an internal charge-pump (V_{PUMP}) that drives the MOSFET gate. Figure 2 depicts typical dropout voltages versus load current for the 3.3V and 5V versions of the part, as well as the adjustable version programmed to 3.0V.

Figure 3. depicts the typical dropout performance of the adjustable version with various output voltages and load currents.

Operating temperatures also effect the $RDS_{(ON)}$ and dropout voltage of the UCC383. Figure 4. graphs the typical dropout for the 3.3V and 5V versions with a 3A load over temperature.

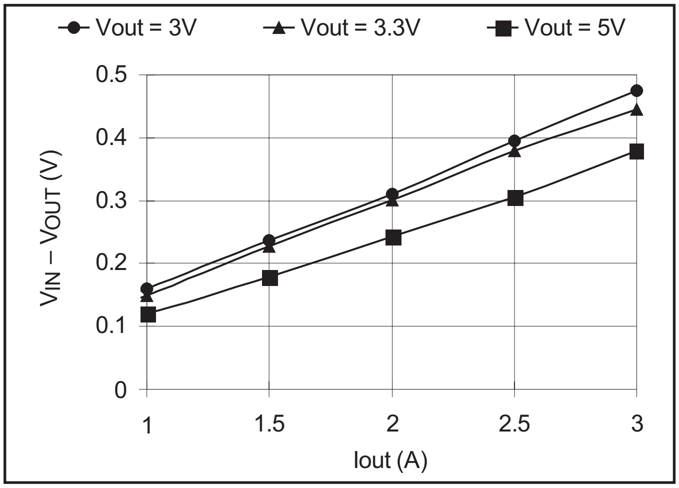


Figure 2. UCC383 Typical Dropout vs. Load Current

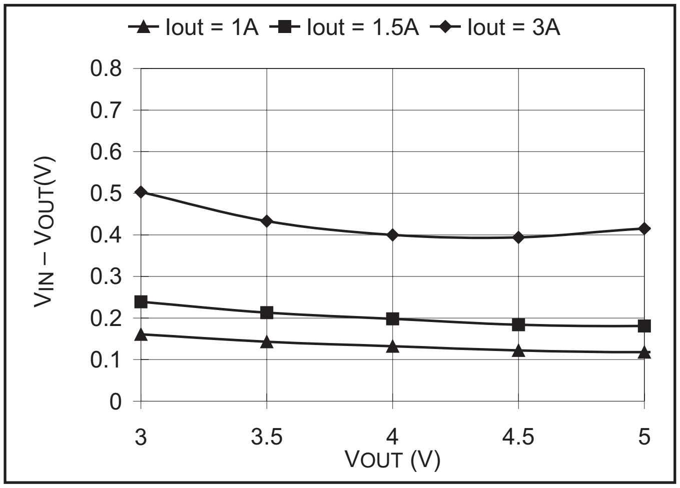


Figure 3. Typical Dropout Voltage vs. I_{OUT} and V_{VOUT}

Voltage Programming and Shutdown Feature for Adjustable Version

A typical application circuit based on the UCC383 adjustable version is shown in Figure 5. The output voltage is externally programmed through a resistive divider at the ADJ pin.

$$V_{OUT} = 1.25 \bullet \left(1 + \frac{R2}{R1}\right) volts \tag{4}$$

The maximum programmed output voltage is constrained by the 9V absolute rating of the IC (this includes the charge pump voltage) and its ability to enhance the N-Channel MOSFET. Unless the load current is below the 3A rating of the device, output voltages above 7V are not recommended. The minimum output voltage can be programmed down to 1.25V, however, the input voltage must always be greater than the UVLO of the part.

The adjustable version includes a shutdown feature, limiting quiescent current to 40uA typical. The UCC383 is shutdown by pulling the CT pin to below 0.25V. As shown in Figure 4, a small logic level MOSFET or BJT transistor in parallel with the timing capacitor can be driven with a digital signal, putting the device in shutdown. If the CT pin is not pulled low, the IC will internally pull up on the pin enabling the regulator. The CT pin should not be forced high, as this will interfere with the short circuit protection feature. Selection of the timing capacitor is explained in *Short Circuit Protection*.

The adjustable version can be used in applications requiring remote voltage sensing (i.e. monitoring a voltage other than or not directly tied to the VOUT pin). This is possible since the inverting input of the voltage amplifier (see Block Diagram) is brought out to the ADJ pin.

Thermal Design

The Packing Information section of the data book contains reference material for the thermal ratings of various packages. The section also includes an excellent article *Thermal Characteristics of Surface Mount Packages*, that is the basis of the following discussion.

Thermal design for the UCC383 includes two modes of operation, normal and pulsed mode. In normal operation, the linear regulator and heat sink must dissipate power equal to the maximum forward voltage drop multiplied by the maximum load current. Assuming a constant current load, the expected heat rise at the regulator's junction can be calculated as follows:

$$T_{RISE}(\theta) = P_{DISS} \bullet \left(\theta_{jc} + \theta_{ca}\right) \ °C \tag{5}$$

Where theta, (θ) is thermal resistance and P_{DISS} is the power dissipated. The thermal resistance of both the TO-220 and TO-263 packages (junction to case) is 3 degrees Celsius per Watt. In order to prevent the regulator from going into thermal shutdown, the case to ambient theta must keep the junction temperature below 150°C. If the LDO is mounted on a 5 square inch pad of 1 ounce copper, for example, the thermal resistance from junction to ambient becomes 60 degrees Celsius per Watt. If a lower thermal resistance is required by the application, the device heat sinking would need to be improved.

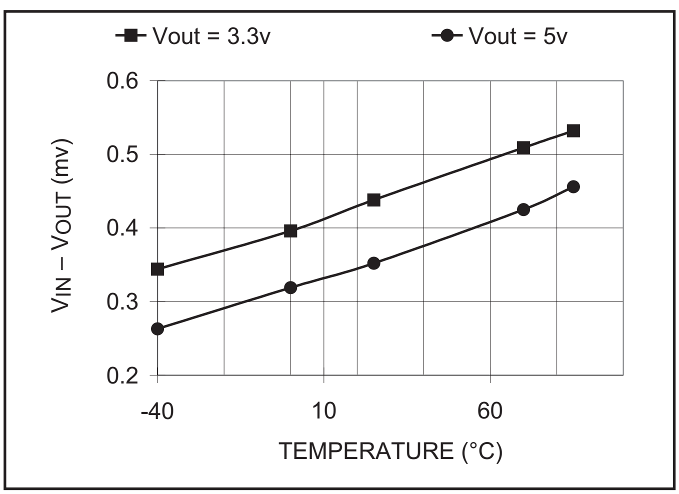


Figure 4. Typical dropout voltage vs. case temperature with a 3A load

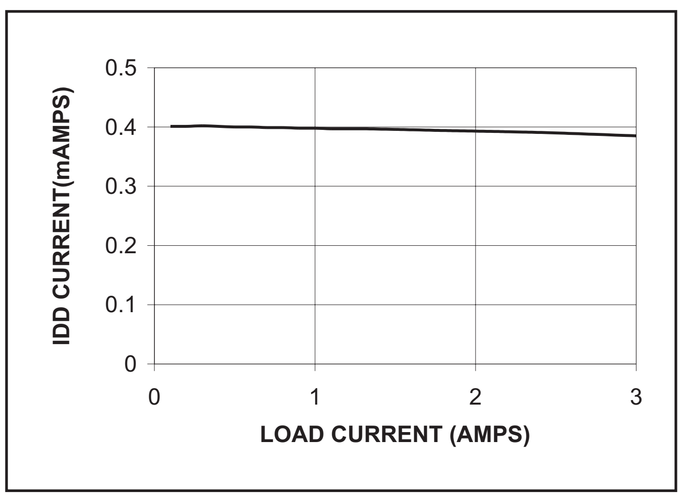


Figure 5. Typical application for the 5 pin adjustable version.

When the UCC383 regulator is in pulsed mode due to an overload or short circuit in the application, the maximum *average* power dissipation is calculated as follows:

$$P_{PULSE\_AVE} = \left(V_{IN} - V_{OUT}\right) \bullet I_{CL} \bullet \frac{T_{ON}}{33 \bullet T_{ON}} Watts \quad (6)$$

As seen in equation 6, the average power during a fault is reduced dramatically by the duty cycle, allowing the heat sink to be sized for normal operation. Although the peak power in the regulator during the T_{ON} period can be significant, the thermal mass of the package will generally keep the junction temperature from rising unless the T_{ON} period is increased to tens of milliseconds.

Ripple Rejection

Even though the UCC383 family of linear regulators are not optimized for fast transient applications (Refer to UC182 Fast LDO Linear Regulator), they do offer significant power supply rejection at lower frequencies. Figure 6 depicts ripple rejection performance in a typical application. The performance can be improved with additional filtering.

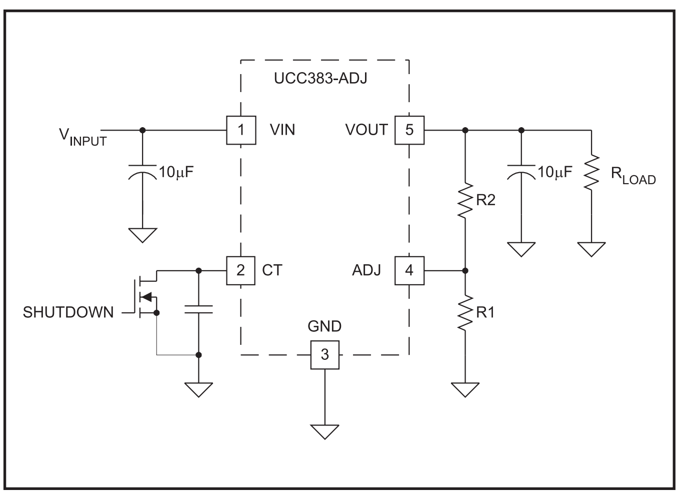


Figure 6. Typical supply current vs. load current.

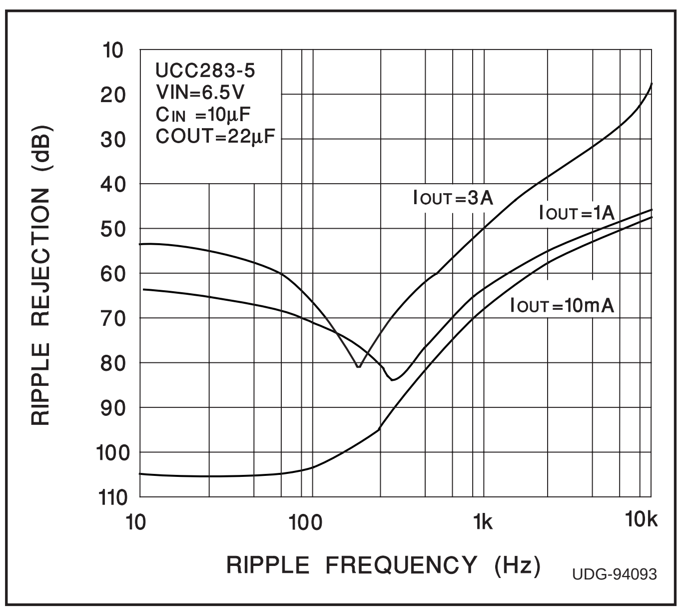


Figure 7. Ripple rejection vs. frequency.

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