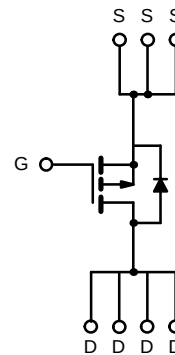
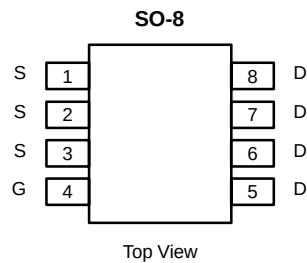


**P-Channel Enhancement-Mode MOSFET****PRODUCT SUMMARY**

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	I_D (A)
-20	0.040 @ $V_{GS} = -4.5$ V	± 6.4
	0.060 @ $V_{GS} = -2.5$ V	± 5.1

Recommended upgrade: Si9424DY



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^A	I_D	± 6.4	A
		± 5.1	
Pulsed Drain Current	I_{DM}	± 10	
Continuous Source Current (Diode Conduction) ^A	I_S	-2.5	
Maximum Power Dissipation ^A	P_D	2.5	W
		1.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Maximum Junction-to-Ambient ^A	R_{thJA}	50	$^\circ\text{C/W}$

Notes

A. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70147.

A SPICE Model data sheet is available for this product (FaxBack document #70528).

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

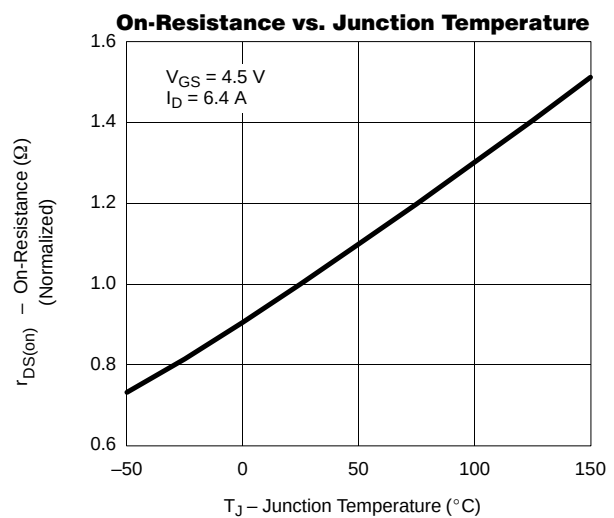
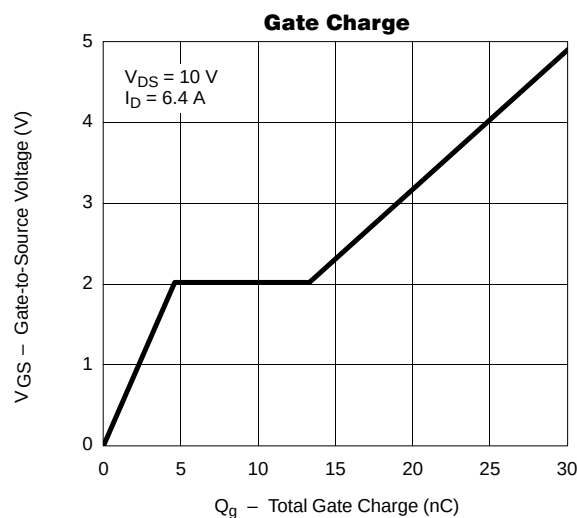
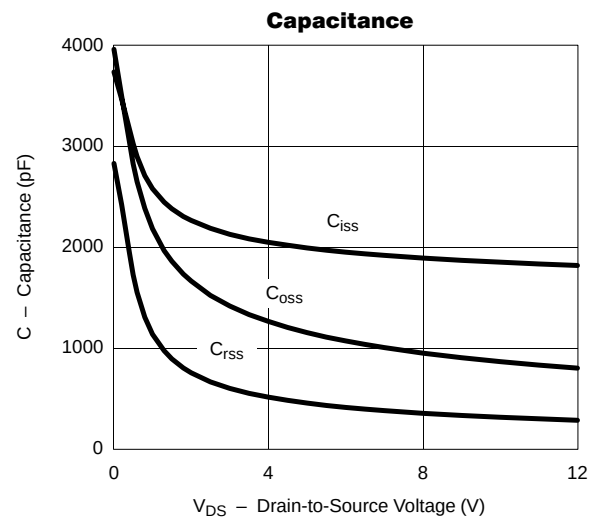
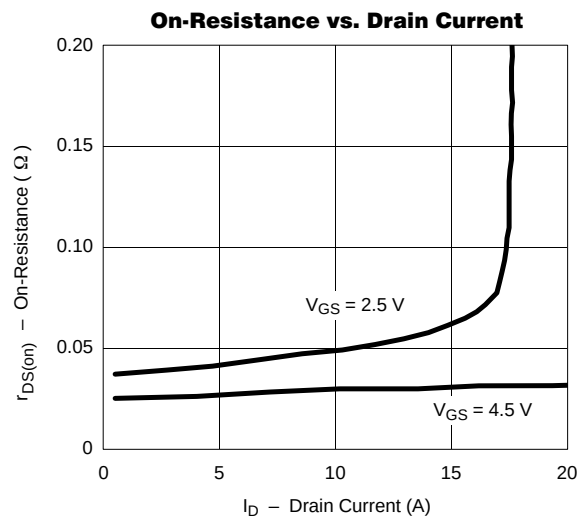
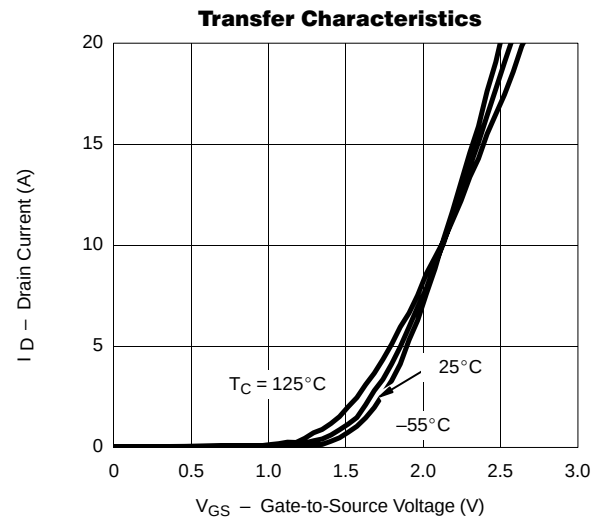
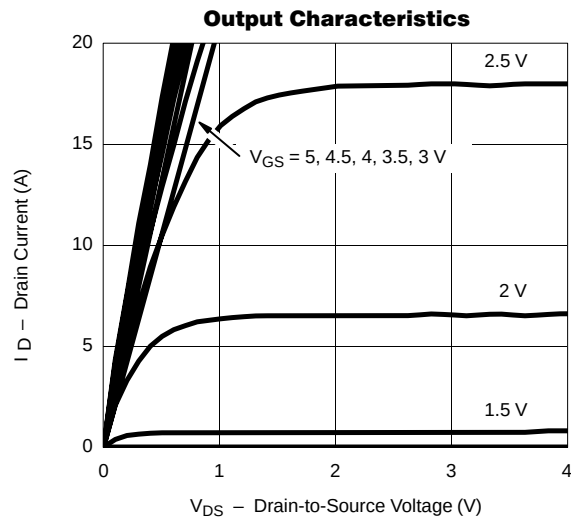
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
STATIC						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.6			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 70°C			-5	
On-State Drain Current ^A	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-10			A
		V _{DS} ≤ -5 V, V _{GS} = -2.5 V	-5			
Drain-Source On-State Resistance ^A	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -6.4 A		0.031	0.040	Ω
		V _{GS} = -2.5 V, I _D = -5.1 A		0.045	0.060	
Forward Transconductance ^A	g _{fs}	V _{DS} = -9 V, I _D = -6.4 A		14		S
Diode Forward Voltage ^A	V _{SD}	I _S = -2.5 A, V _{GS} = 0 V		-0.9	-1.2	V
Dynamic^B						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -6.4 A		30	50	nC
Gate-Source Charge	Q _{gs}			5		
Gate-Drain Charge	Q _{gd}			9		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 6 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		25	50	ns
Rise Time	t _r			42	80	
Turn-Off Delay Time	t _{d(off)}			160	200	
Fall Time	t _f			75	120	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -2.5 A, di/dt = 100 A/μs		50	100	

Notes

- A. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
 B. Guaranteed by design, not subject to production testing.



Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

