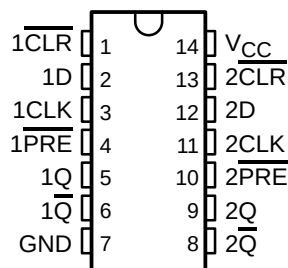


CD54AC74, CD74AC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ± 24 -mA Output Drive Current
– Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54AC74 . . . F PACKAGE
CD74AC74 . . . E OR M PACKAGE
(TOP VIEW)



description/ordering information

The 'AC74 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74AC74E	CD74AC74E
	SOIC – M	Tube	CD74AC74M	AC74M
		Tape and reel	CD74AC74M96	
	CDIP – F	Tube	CD54AC74F3A	CD54AC74F3A

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each flip-flop)

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [‡]	H [‡]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	$\overline{\text{Q}}_0$

[‡] This configuration is nonstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

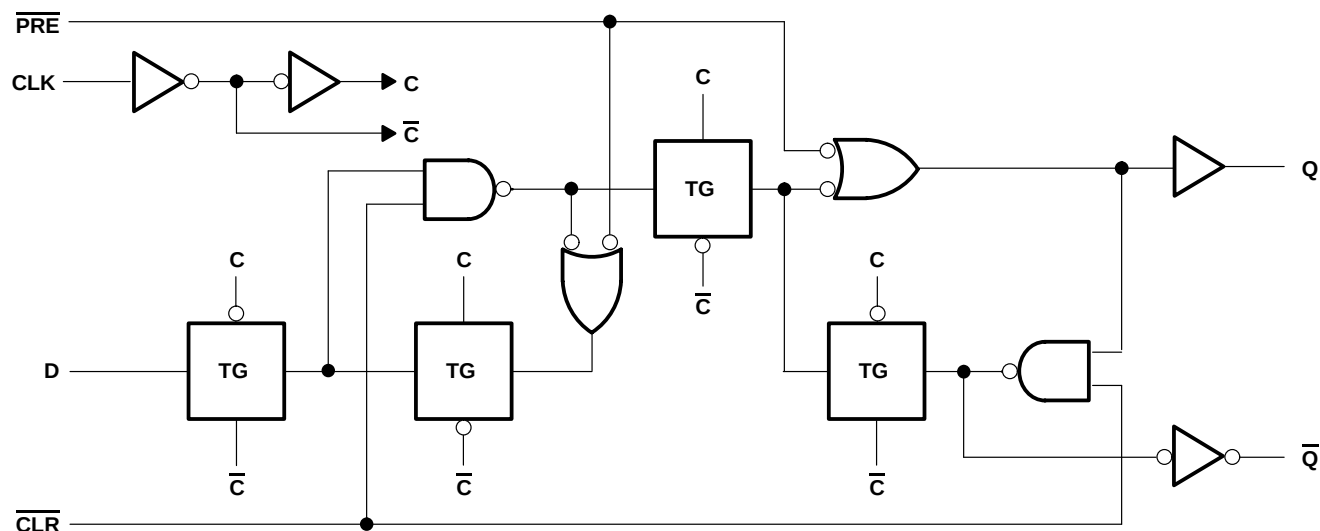
CD54AC74, CD74AC74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

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logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	80°C/W
M package	86°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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recommended operating conditions (see Note 3)

			$T_A = 25^\circ\text{C}$		$-55^\circ\text{C to } 125^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 1.5\text{ V}$	1.2		1.2		1.2		V
		$V_{CC} = 3\text{ V}$	2.1		2.1		2.1		
		$V_{CC} = 5.5\text{ V}$	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 1.5\text{ V}$		0.3		0.3		0.3	V
		$V_{CC} = 3\text{ V}$		0.9		0.9		0.9	
		$V_{CC} = 5.5\text{ V}$		1.65		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$		-24		-24		-24	mA
I_{OL}	Low-level output current	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.5\text{ V to } 3\text{ V}$		50		50		50	ns/V
		$V_{CC} = 3.6\text{ V to } 5.5\text{ V}$		20		20		20	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25^\circ\text{C}$		$-55^\circ\text{C to } 125^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	1.5 V	1.4		1.4		1.4		V
			3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
		$I_{OH} = -4\text{ mA}$	3 V	2.58		2.4		2.48		
		$I_{OH} = -24\text{ mA}$	4.5 V	3.94		3.7		3.8		
		$I_{OH} = -50\text{ mA}^\dagger$	5.5 V			3.85				
		$I_{OH} = -75\text{ mA}^\dagger$	5.5 V					3.85		
V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	1.5 V		0.1		0.1		0.1	V
			3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
		$I_{OL} = 12\text{ mA}$	3 V		0.36		0.5		0.44	
		$I_{OL} = 24\text{ mA}$	4.5 V		0.36		0.5		0.44	
		$I_{OL} = 50\text{ mA}^\dagger$	5.5 V				1.65			
		$I_{OL} = 75\text{ mA}^\dagger$	5.5 V						1.65	
I_I	$V_I = V_{CC} \text{ or } \text{GND}$		5.5 V		± 0.1		± 1		± 1	μA
I_{CC}	$V_I = V_{CC} \text{ or } \text{GND}, I_O = 0$		5.5 V		4		80		40	μA
C_i					10		10		10	pF

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50- Ω transmission-line drive capability at 85°C and 75- Ω transmission-line drive capability at 125°C.



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DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 1.5\text{ V}$ (unless otherwise noted)

			–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		9		10		MHz
t _w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	50		44		ns
		CLK	56		49		
t _{su}	Setup time	Data	44		39		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive					ns
t _h	Hold time	Data after CLK↑	0		0		ns
t _{rec}	Recovery time, before CLK↑	$\overline{\text{CLR}}$ ↑ or $\overline{\text{PRE}}$ ↑	34		30		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

			–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		79		90		MHz
t _w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	5.6		4.9		ns
		CLK	6.3		5.5		
t _{su}	Setup time	Data	4.9		4.3		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive					ns
t _h	Hold time	Data after CLK↑	0		0		ns
t _{rec}	Recovery time, before CLK↑	CLR↑ or PRE↑	4.7		4.1		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		110		125		MHz
t _w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4		3.5		ns
		CLK	4.5		3.9		
t _{su}	Setup time	Data	3.5		3.1		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive					ns
t _h	Hold time	Data after CLK↑	0		0		ns
t _{rec}	Recovery time, before CLK↑	$\overline{\text{CLR}}$ ↑ or $\overline{\text{PRE}}$ ↑	2.7		2.4		ns

CD54AC74, CD74AC74
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH CLEAR AND PRESET

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 1.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{\max}$			9		10		MHz
t_{PLH}	CLK	Q or $\bar{Q}$	125		114		ns
t_{PHL}			125		114		
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\bar{Q}$	132		120		ns
t_{PHL}			144		131		

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{\max}$			79		90		MHz
t_{PLH}	CLK	Q or $\bar{Q}$	3.5	14	3.6	12.7	ns
t_{PHL}			3.5	14	3.6	12.7	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\bar{Q}$	3.7	14.7	3.8	13.4	ns
t_{PHL}			4	16.1	4.1	14.6	

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{\max}$			110		125		MHz
t_{PLH}	CLK	Q or $\bar{Q}$	2.5	10	2.6	9.1	ns
t_{PHL}			2.5	10	2.6	9.1	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\bar{Q}$	2.6	10.5	2.7	9.5	ns
t_{PHL}			2.9	11.5	3	10.4	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	55	pF

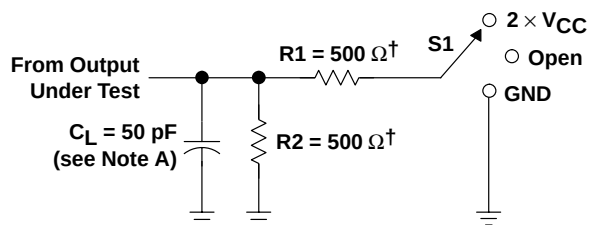
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DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

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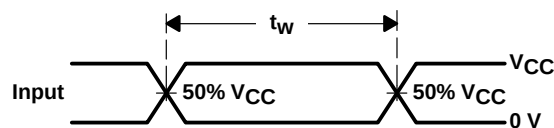
PARAMETER MEASUREMENT INFORMATION



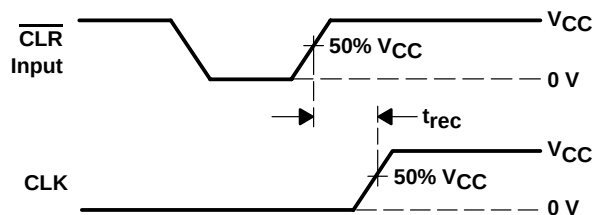
† When $V_{CC} = 1.5\text{ V}$, $R1 = R2 = 1\text{ k}\Omega$

LOAD CIRCUIT

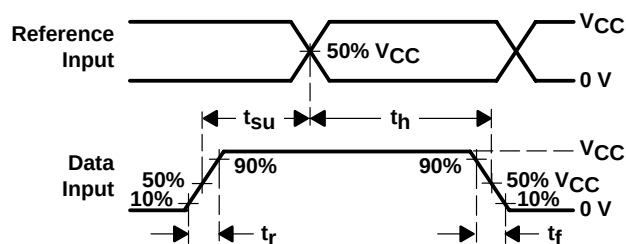
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



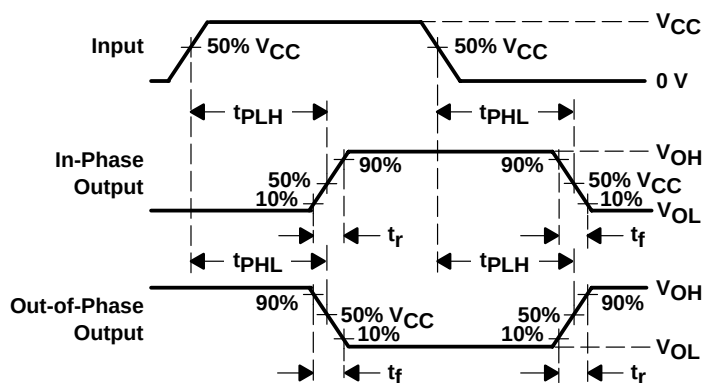
VOLTAGE WAVEFORMS
PULSE DURATION



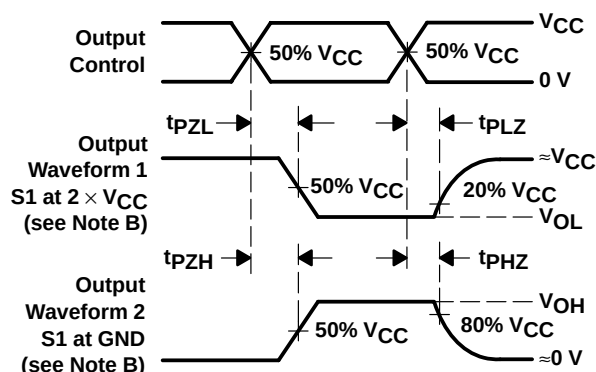
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

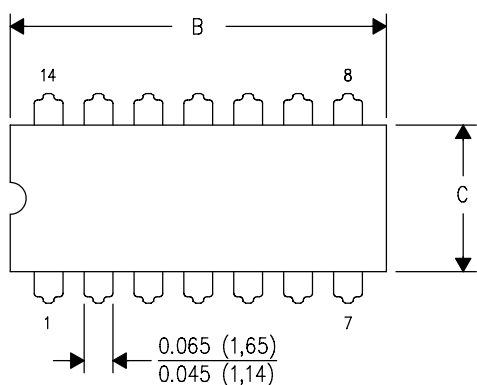
- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$. Phase relationships between waveforms are arbitrary.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time with one input transition per measurement.
 - F. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

Figure 1. Load Circuit and Voltage Waveforms

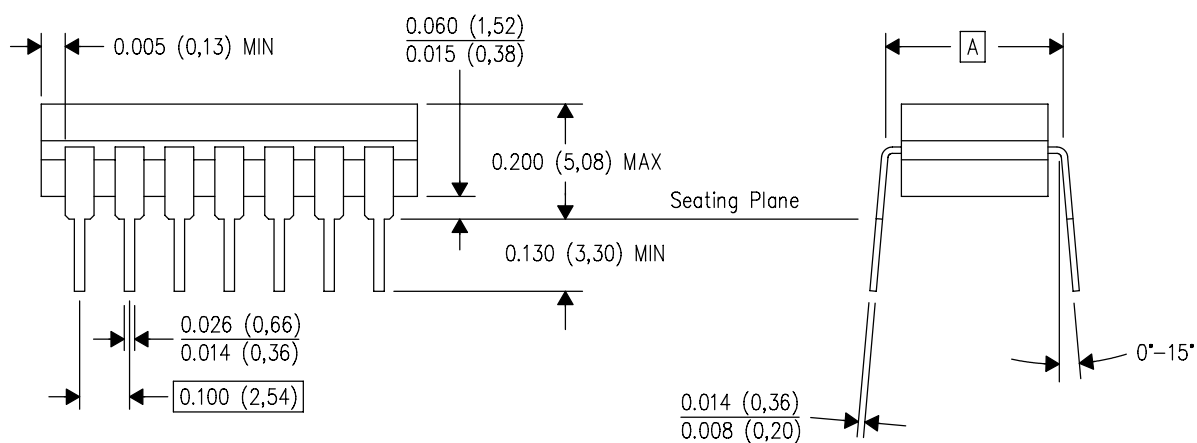
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



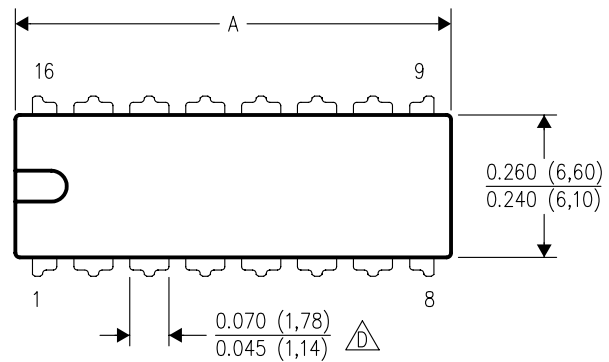
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

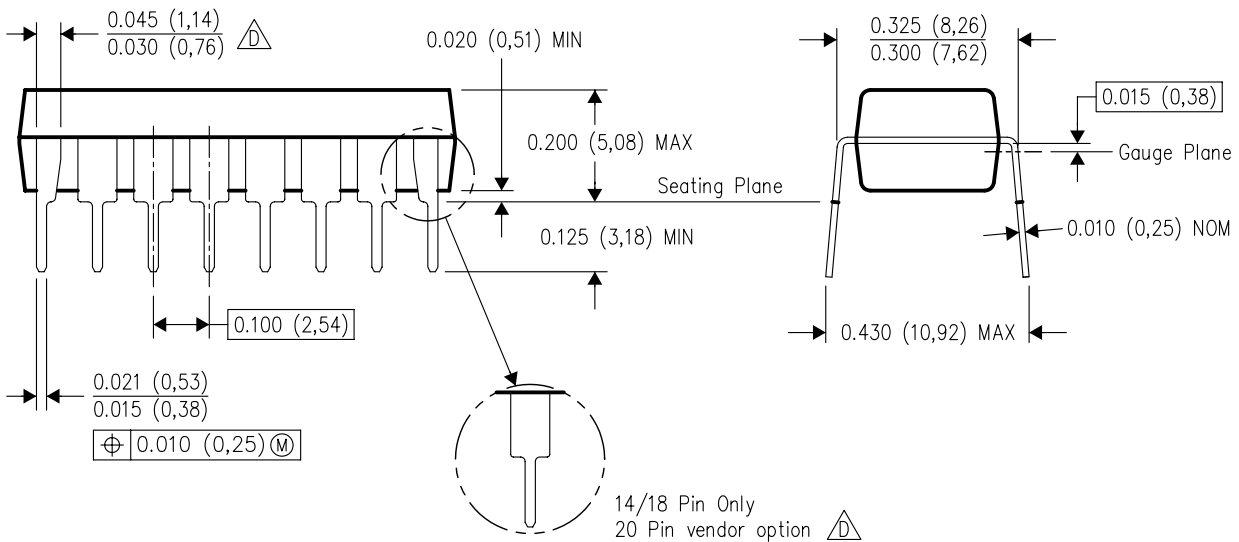
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



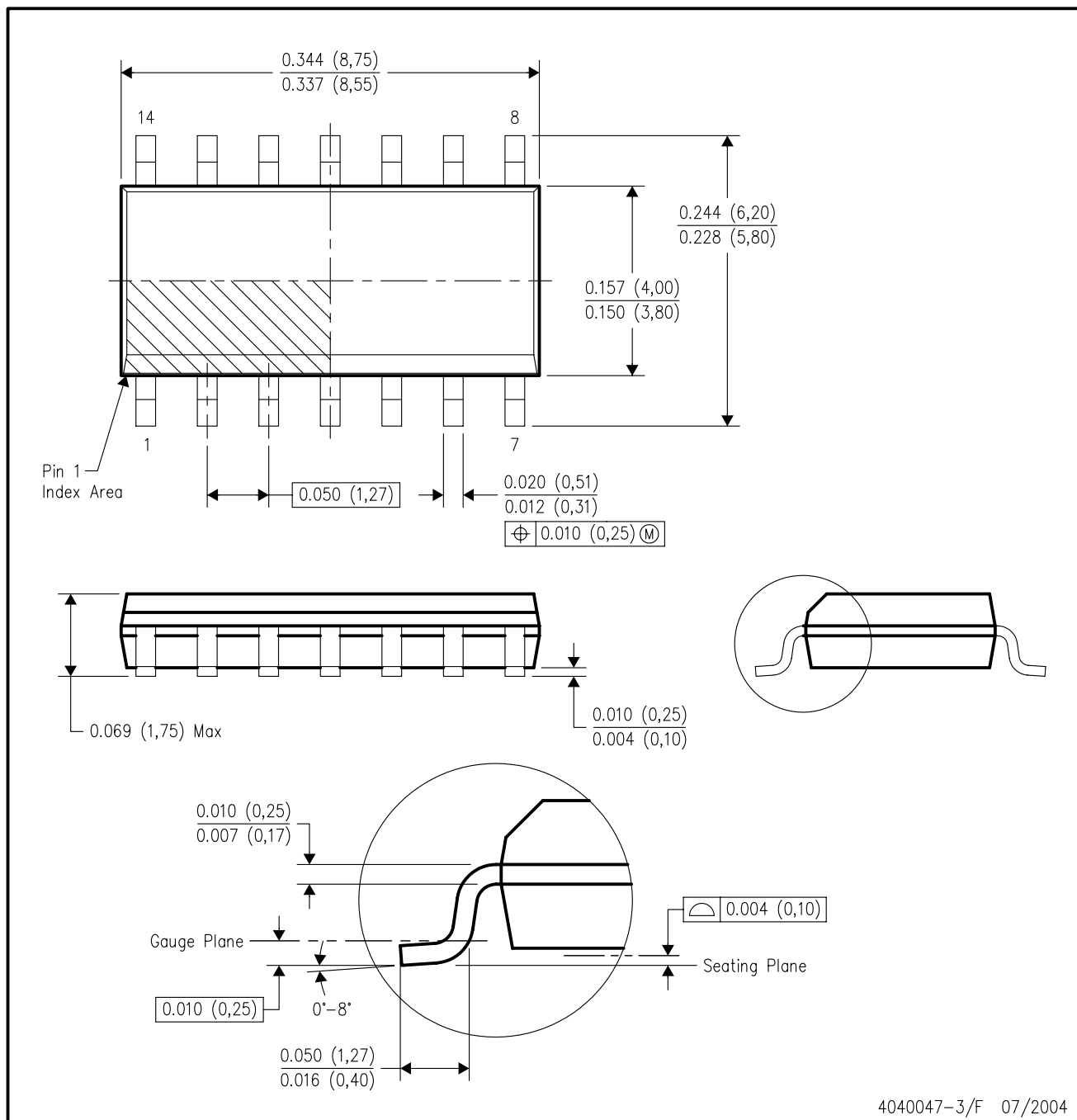
14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AB.

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