TSB43CA43A/TSB43CB43A/TSB43CA42
iceLynx-Micro

IEEE 1394a-2000
Consumer Electronics Solution
ABBREVIATED DATA MANUAL

SLLS546F – September 2004

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References

The following sources of information were used in the generation of this document:

- IEEE Standard for a High Performance Serial Bus, IEEE Standard 1394-1995
- IEEE 1394a-2000 Serial Bus Supplement
- Digital Interface for consumer audio/video equipment, IEC Document 61883
- Home Digital Network Interface Specification, Revision 1.1
- 5C Digital Transmission Content Protection Specification

Acronyms

The acronyms used in this document are defined below.

5C	Five Company (Intel, Sony, Matsushita, Hitachi, Toshiba)
CFR	Configuration Register
DSS	Direct Satellite System
DV	Digital Video
DVB	Digital Video Broadcasting
DVD	Digital Versatile Disc
HSDI	High Speed Data Interface
IEC	International Electrotechnical Commission
IEEE	Institute of Electronics and Electrical Engineers
IP	Internet Protocol
MPEG	Motion Pictures Experts Group

Device Ordering Information

Ordering Number	Name	Package
TSB43CA43APGF	iceM 5C	PQFP 176
TSB43CB43APGF	iceM non-5C	PQFP 176
TSB43CA43AGGW	iceM 5C	µ *BGA 176
TSB43CB43AIGGW	iceM non-5C, I temperature	µ *BGA 176
TSB43CA43AZGW	iceM 5C	µ *BGA 176
TSB43CA42PGF	iceM 5C (2 Port)	PQFP 176
TSB43CA42GGW	iceM 5C (2 Port)	µ *BGA 176
TSB43CA42ZGW	iceM 5C (2 Port)	µ *BGA 176

The ZGW package is similar to the GGW package with the added benefits of lead-free balls and the use of environmentally-friendly (green) mold compound.

1 Hardware IC Characteristics

iceLynx-Micro Overview

The iceLynx-Micro (consumer electronics link with integrated microcontroller and physical layer (PHY)) is a high performance 1394 link-layer device designed as a total solution for digitally interfacing advanced audio/video consumer electronics applications. The device is offered in both a DTCP encryption/decryption version (TSB43CA43A and TSB43CA42) and a non-DTCP encryption/decryption version (TSB43CB43).

In addition to supporting transmit and receive of MPEG2 and DSS formatted transport streams with encryption and decryption, the iceLynx-Micro supports the IEC 61883-6 and audio music protocol standards for audio format and packetizing and asynchronous and asynchronous stream (as defined by 1394).

The device also features an embedded ARM7TDMI microprocessor core with access to 256K bytes of internal program memory. The ARM7 is embedded to process 1394 specific transactions, thus significantly reducing the processing power required by the host CPU and the development time required by the user. The ARM7 is accessed from the 16/1-bit host CPU interface, from a UART communication port, or from a JTAG debug port.

The iceLynx-Micro integrated 3-port PHY allows the user enhanced flexibility as two additional devices can be utilized in a system application. The PHY's speeds are capable of running at 100 Mbps, 200 Mbps, or 400 Mbps. The PHY follows all requirements as stated in the IEEE 1394-1995 and IEEE 1394a-2000 standards.

The TSB43CA43A and TSB43CA42 version of iceLynx-Micro incorporates two M6 baseline ciphers (one per HSDI port) per the 5C specification to support transmit and receive of MPEG2 formatted transport streams with encryption and decryption. The TSB43CB43 version of iceLynx-Micro is identical to the TSB43CA43A without implementation of the encryption/decryption features. The TSB43CB43 device allows customers that do not require the encryption/decryption features to incorporate iceLynx-Micro without becoming DTLA licensees. Both devices support the IEC 61883-6 and audio music protocol standards for audio format and packetizing.

1.1 Feature List

1.1.1 1394 Features

- ❑ Integrated 400 Mbps 3-port PHY
- ❑ Compliant with IEEE 1394-1995 and IEEE 1394a-2000 standards
- ❑ Supports bus manager functions and automatic 1394 self-ID verification.
- ❑ Separate Async Ack FIFO decreases the ack-tracking burden on in-CPU and ex-CPU

1.1.2 DTLA Encryption Support for MPEG2-DVB, DSS, DV, and Audio (TSB43CA43A and TSB43CA42 Only)

- ❑ Two M6 baseline ciphers (one per HSDI port)
  - Content key generation from exchange key
- ❑ AKE acceleration features in hardware
  - Random Number Generator
  - Secure Hash Algorithm, Revision 1 (SHA-1)
- ❑ Other AKE acceleration features
  - Elliptical curve digital signature algorithm (EC-DCA) both signature and verification
  - Elliptical curve Diffie-Hellman (EC-DH), first phase value and shared secret calculation
  - 160-bit math functions

1.1.3 High Speed Data Interface (HSDI)

Two configurable high speed data interfaces support the following audio and video modes:

- MPEG2-DVB interface
- MPEG2-DSS interface
- DV codec interface
- IEC60958 interface
- Audio DAC interface
- SACD interface

1.1.4 External CPU Interface

- 16-bit parallel asynchronous I/O-type
- 16-bit parallel synchronous I/O-type
- 16-bit parallel synchronous memory type

1.1.5 Internal ARM7

- 50-MHz operating frequency
- 32-bit and thumb (16-bit) mode support
- UART included for communication
- 256K bytes of program memory included on chip
- ARM JTAG included for software debug

1.1.6 Data Buffers

- Large 16.5K byte total FIFO
- Programmable data/space available indicators for buffer flow control

1.1.7 Hardware Packet Formatting for the Following Standards

- DVB MPEG2 transport stream (IEC61883-4)
- DSS MPEG2 transport stream per standard
- DV Stream (IEC 61883-2) SD-DV
- Audio over 1394 (IEC 61883-6)
- Audio Music Protocol (version 1.0 and enhancements)
- Asynchronous and asynchronous stream (as defined by IEEE 1394)

1.1.8 Additional Features

- PID filtering for transmit function (up to 16 separate PIDs per HSDI)
- Packet insertion – two insertion buffers per HSDI
- 11 general-purpose inputs/outputs (GPIOs)
- Interrupt driven to minimize CPU polling.
- Single 3.3-V supply
- JTAG interface to support post-assembly scan of device I/O – boundary scan

1.2 Application Diagram

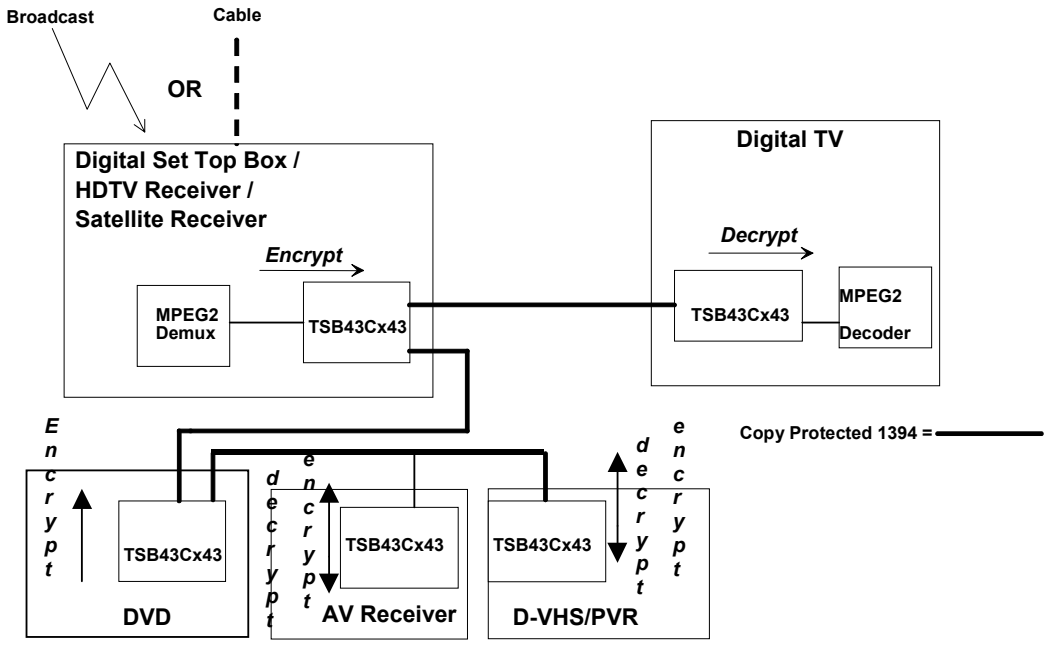
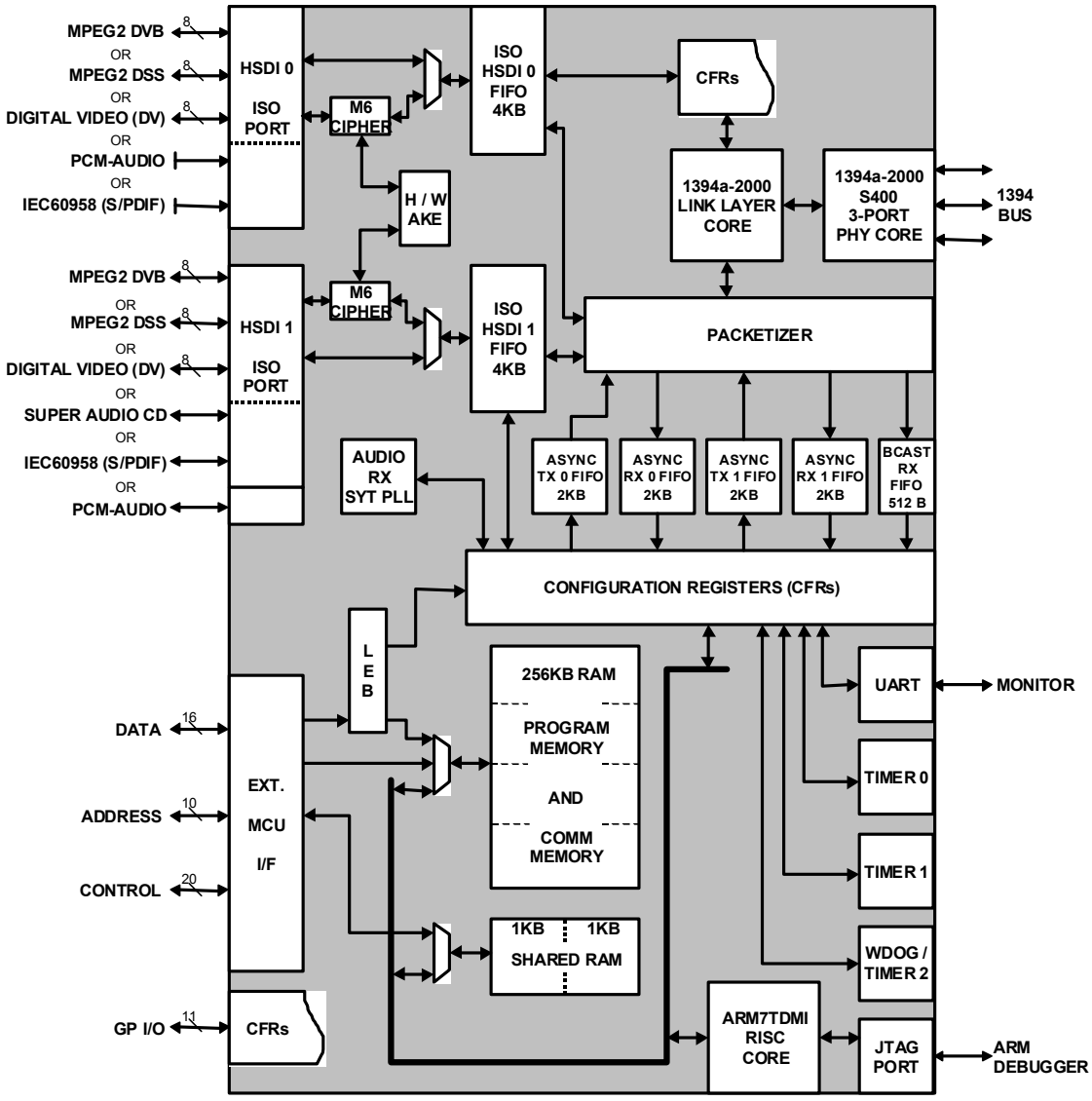


Figure 1. TSB43Cx43 Typical Application

1.3 Block Diagram

1.3.1 TSB43Cx43A Block Diagram

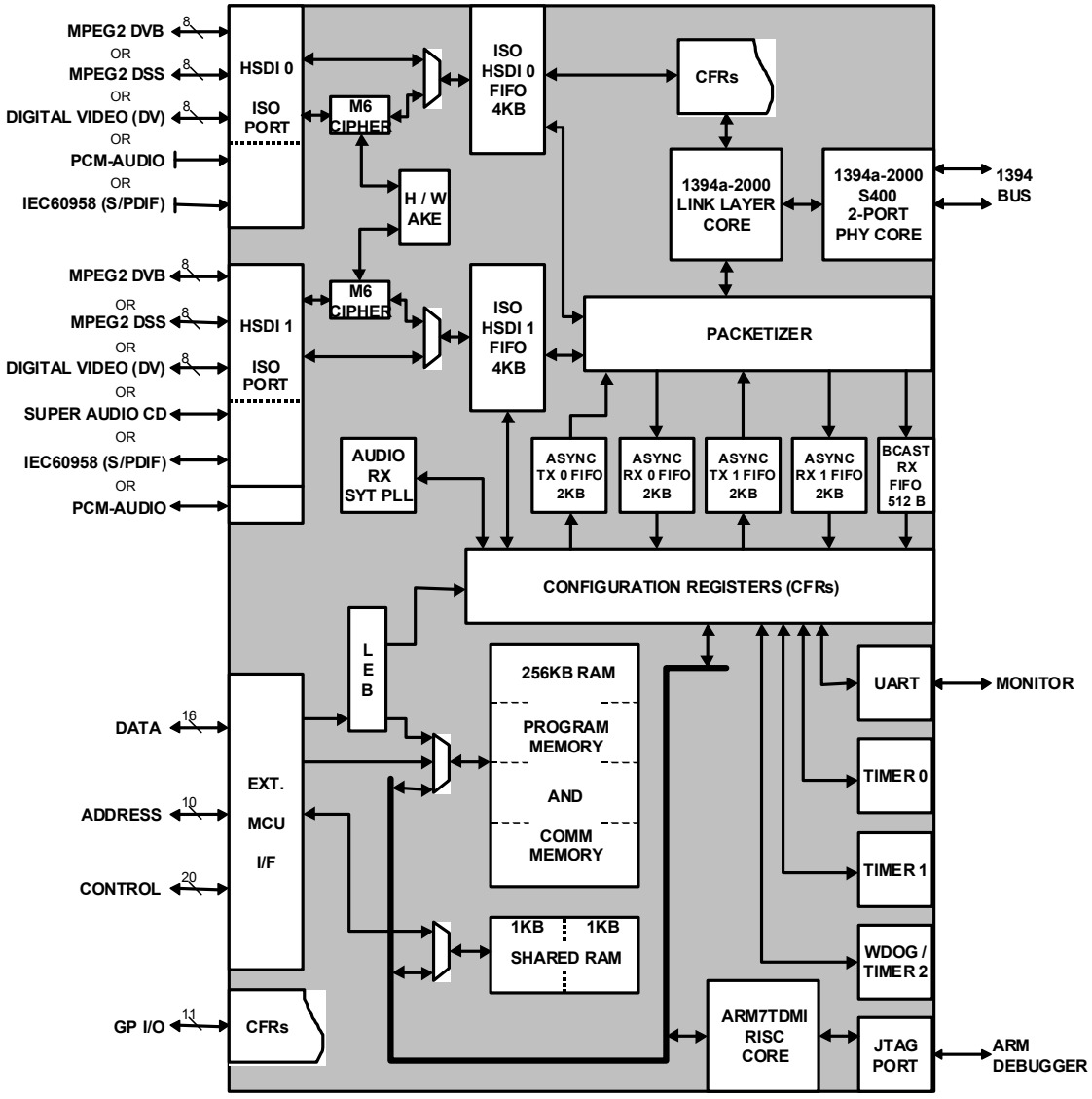


† LEB is an acronym for local encryption block (**Note:** only included in the TSB43CA43)

Figure 2. TSB43Cx43 System Block Diagram

Note: The M6 Cipher is only included in the TSB43CA43.

1.3.2 TSB43CA42 Block Diagram



† LEB is an acronym for local encryption block (**Note:** only included in the TSB43CA42)

Figure 3. TSB43CA42 System Block Diagram

1.4 Pin Out

1.4.1 TSB43CA43A/TSB43CB43A Plastic Quad Flat Pack (PQFP)

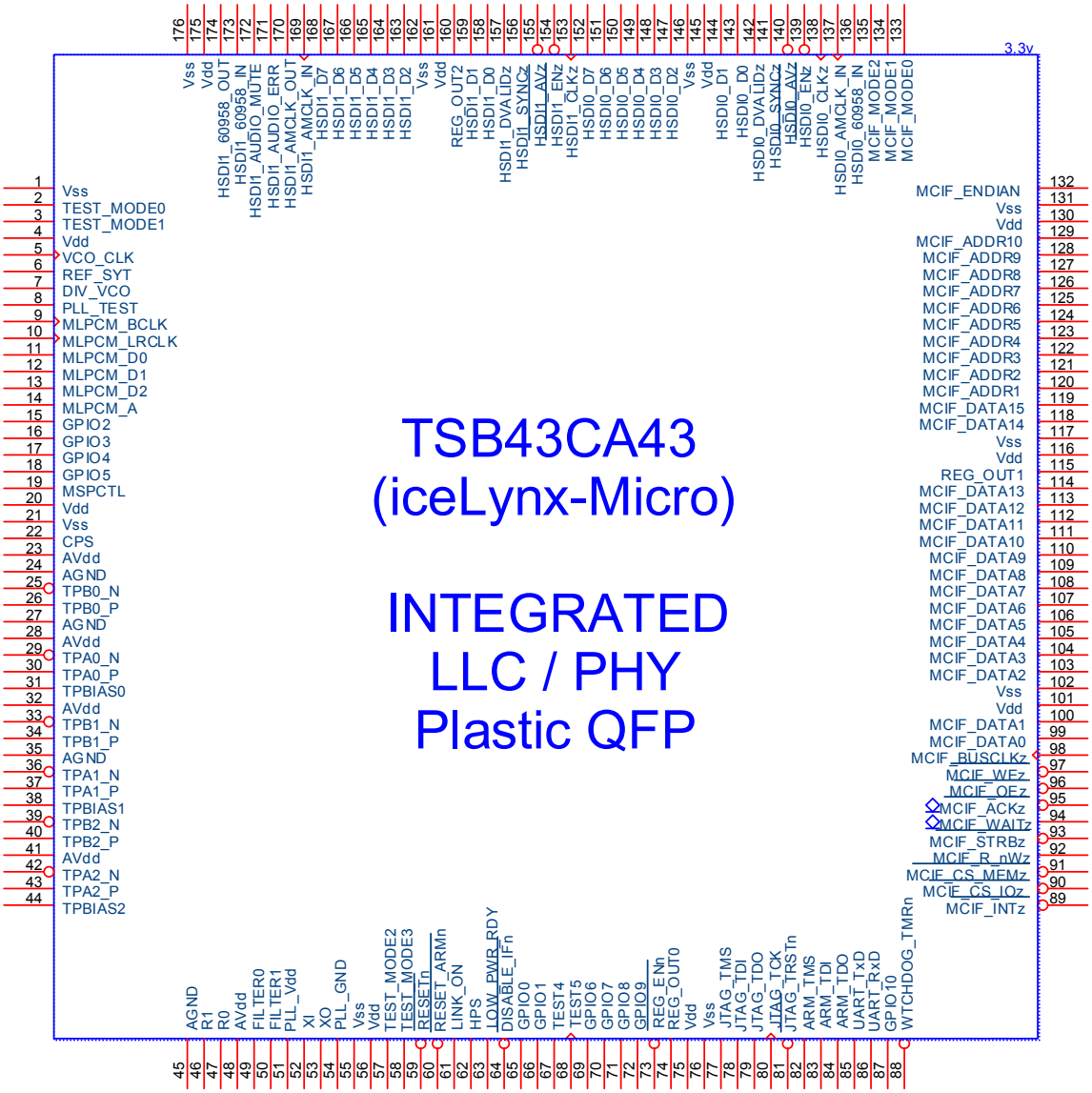


Figure 4. TSB43CA43A Plastic QFP Pin Out

1.4.2 TSB43CA43A/TSB43CB43A Micro-Star Ball Grid Array (μ*BGA)

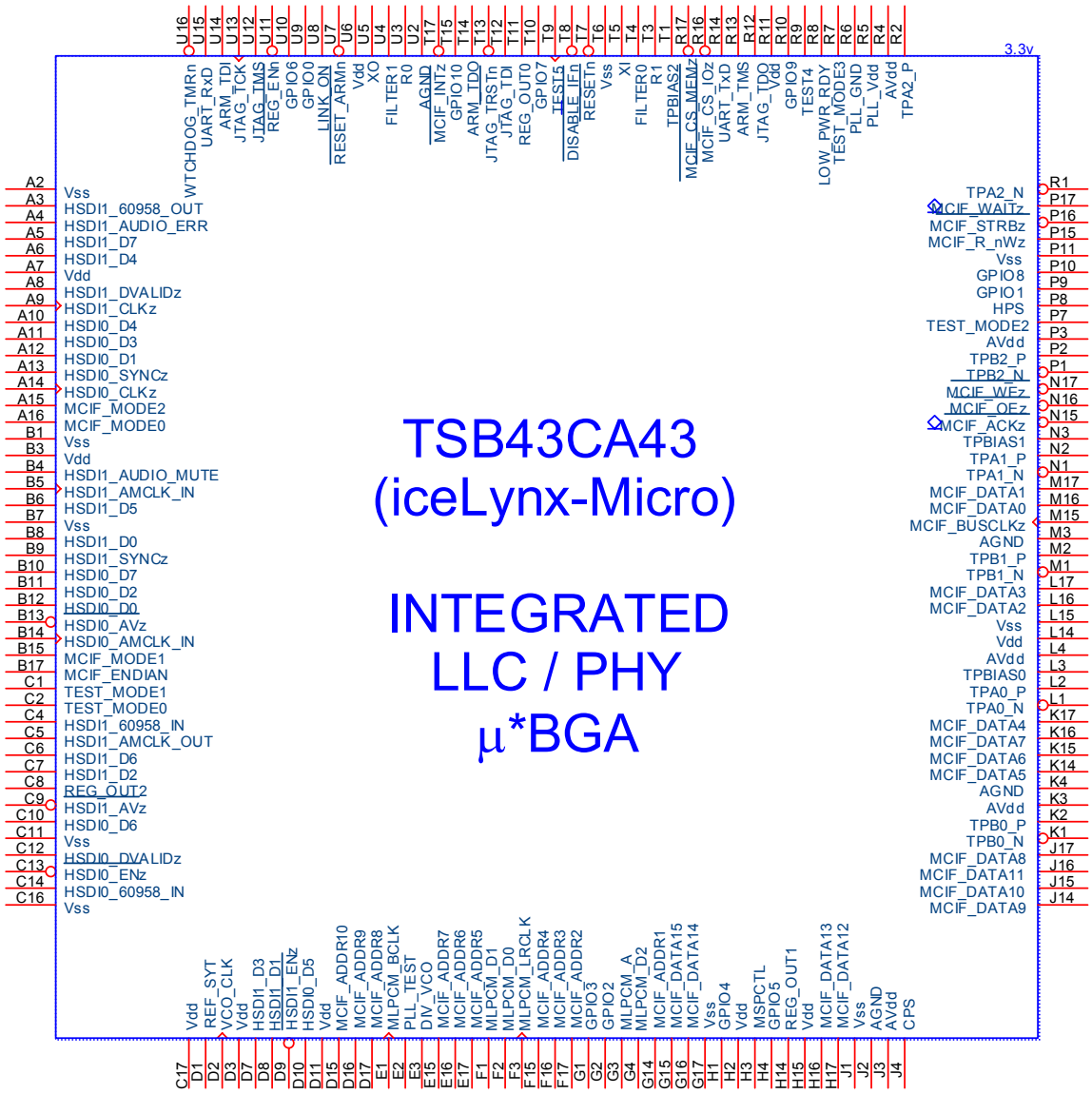


Figure 5. TSB43CA43A μ*BGA Pin Out

1.4.3 TSB43CA42 Plastic Quad Flat Pack (PQFP)

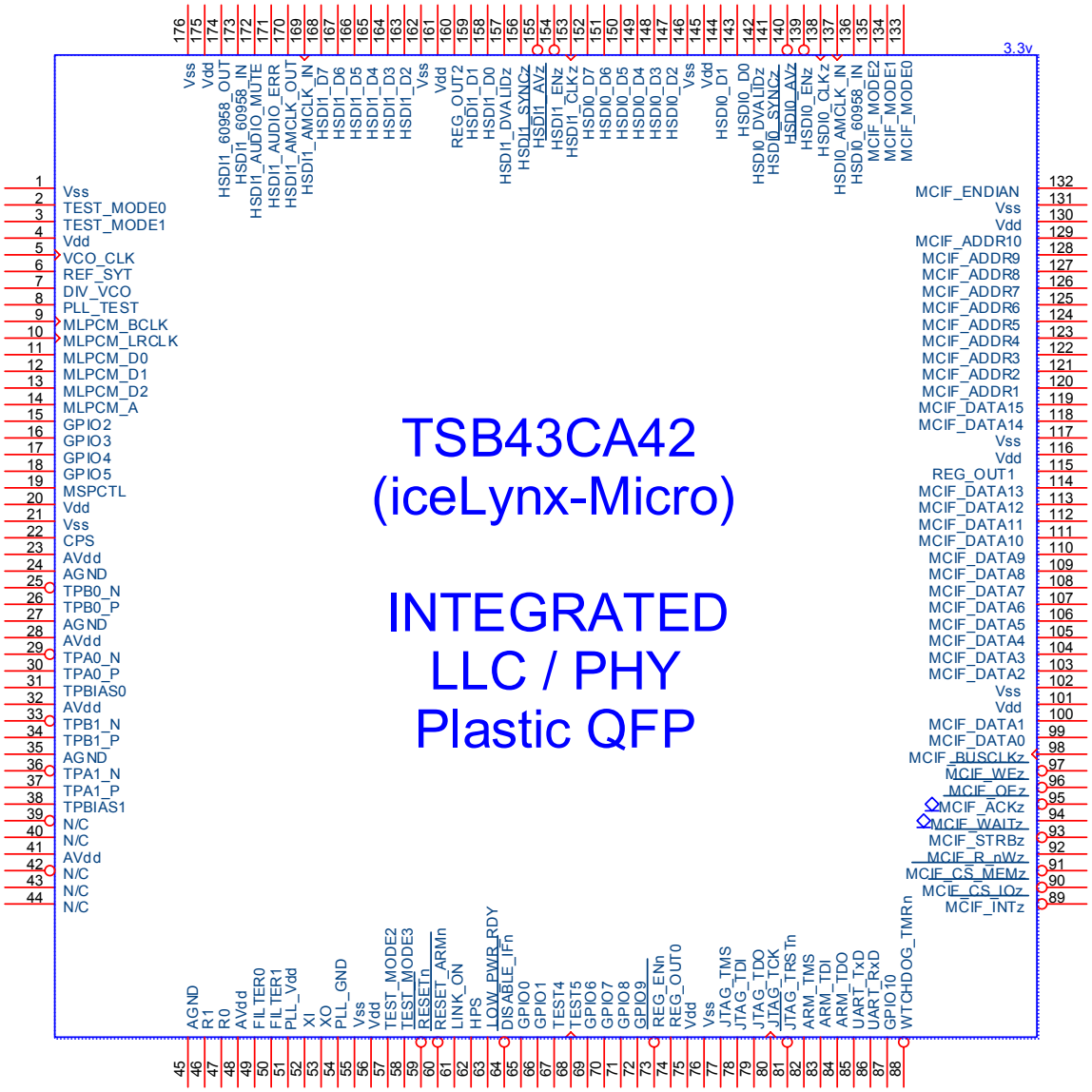


Figure 6. TSB43CA42 Plastic QFP Pin Out

1.4.4 TSB43CA42 Micro-Star Ball Grid Array (μ*BGA)

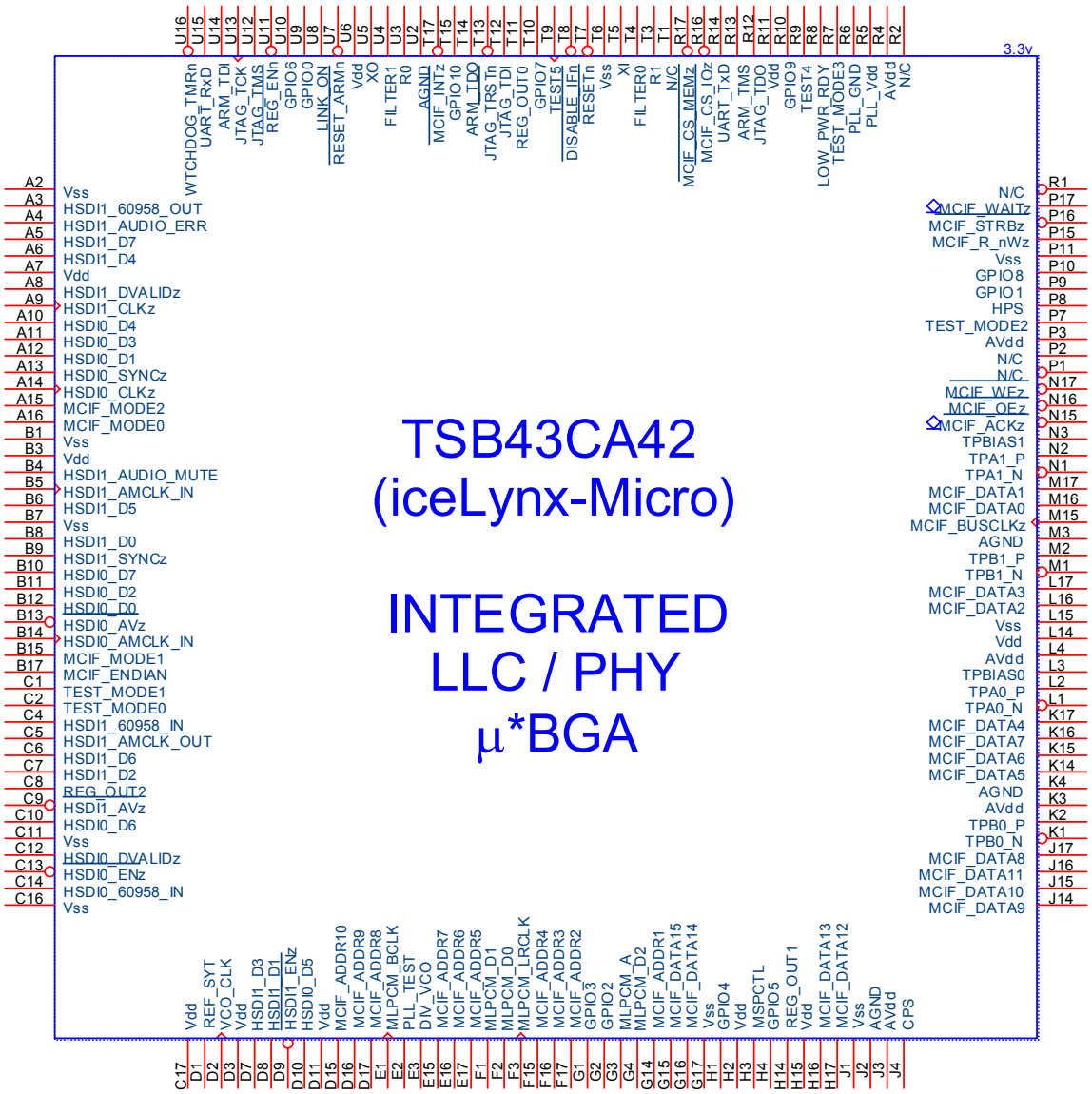


Figure 7. TSB43CA42 μ*BGA Pin Out

1.5 Pin Description

Terminal Name	Terminal Number		I/O	Description
	BGA	QFP		
Miscellanous Pins				
DISABLE_IFn	T8	64	I	Interface disable. When asserted, the interfaces are put into a high-Z state. Interfaces include: ex-CPU, HSDI, GPIO, and WTCH_DG_TMRn.
HPS	P8	62	I	Host power status. This indicates the power status of the external system to iceLynx-Micro. A rising edge indicates the system CPU has been turned ON. (The internal ARM must wake up.) A falling edge indicates the system CPU has been turned OFF. (The internal ARM decides if power down is necessary.)
LOW_PWR_RDY	R8	63	O	Output to system to indicate iceLynx-Micro is ready to go into a low power state. The ARM and WTCH_DG_TMRn control this pin.
WTCH_DG_TMRn	U16	88	O	Watch dog timer (for the ARM). iceLynx-Micro hardware asserts this pin whenever ARM software has not updated the Timer2 register within the allowed time period.
RESET_ARMn	U7	60	I	ARM reset. This signal resets the internal ARM processor.
RESETn	T7	59	I	Device reset. This signal resets all logic. This includes the PHY, link core, memory, the ARM, and random logic.
Power and Ground Pins				
VSS	A2, B1, B7, C11, C16, G17, J1, L15, P11, T6	1, 21, 55, 76, 102, 117, 131, 146, 162, 176		Digital ground
AGND	J2, K4, M3, U2	24, 27, 35, 45,		Analog ground
PLL_GND	R6	54		PLL ground
VDD	A7, B3, C17, D3, D11, H2, H15, L14, R11, U6	4, 20, 56, 75, 101, 116, 130, 145, 161, 175		Digital power supply. Must be set to 3.3-V nominal.
AVDD	J3, K3, L4, P3, R4	23, 28, 32, 41, 48		Analog power supply. Must be set to 3.3-V nominal.
PLL_VDD	R5	51		PLL power supply. Must be set to 3.3-V nominal.
Regulator Pins				
REG_ENn	U11	73	I	Internal regulator enable. The iceLynx-Micro core voltage is 1.8 V. Internal regulators are used to regulate the 3.3-V VDD inputs to 1.8 V. This pin enables the regulators.

Terminal Name	Terminal Number		I/O	Description
	BGA	QFP		
REG_OUT0	T11	74	O	1.8-V regulator output. This pin must be connected to ground using a 0.1-μF capacitor.
REG_OUT1	H14	115	O	1.8-V regulator output. This pin must be connected to ground using a 0.1-μF capacitor.
REG_OUT2	C8	160	O	1.8-V regulator output. This pin must be connected to ground using a 0.1-μF capacitor.
External CPU Interface Pins				
MCIF_ACKz	N15	95	I/O	MCIF acknowledge pin. Default active low. iceLynx-Micro asserts this signal if it has completed the MCIF request. This signal is driven when chip select (CS) is asserted. This signal is used for the following modes: ▪ 68000 + wait I/O access ▪ I/O Type-3 MPC850
MCIF_ADDR1	G14	120	I	MCIF address 1 pin. This data pin is the least significant bit of the MCIF address bus. MCIF_ADDR0 is internally grounded. Only 16-bit addressing is allowed. MCIF_ADDR1 must be connected to the Address1 signal of the system CPU.
MCIF_ADDR2	F17	121	I	MCIF address 2 pin
MCIF_ADDR3	F16	122	I	MCIF address 3 pin
MCIF_ADDR4	F15	123	I	MCIF address 4 pin
MCIF_ADDR5	E17	124	I	MCIF address 5 pin
MCIF_ADDR6	E16	125	I	MCIF address 6 pin
MCIF_ADDR7	E15	126	I	MCIF address 7 pin
MCIF_ADDR8	D17	127	I	MCIF address 8 pin
MCIF_ADDR9	D16	128	I	MCIF address 9 pin
MCIF_ADDR10	D15	129	I	MCIF address 10 pin. This data pin is the most significant bit of the MCIF address bus.
MCIF_BUSCLKz	M15	98	I	MCIF bus clock. This pin is only used for the MCIF synchronous mode. I/O Type-3 MPC850 and the memory access. This signal must be pulled high if not used.
MCIF_CS_IOz	R16	90	I	MCIF chip select for all I/O MCIF modes.
MCIF_CS_MEMz	R17	91	I	MCIF chip select for the memory MCIF mode.
MCIF_DATA0	M16	99	I/O	MCIF data 0 pin. This data pin is the least significant bit of the MCIF data bus.
MCIF_DATA1	M17	100	I/O	MCIF data 1 pin
MCIF_DATA2	L16	103	I/O	MCIF data 2 pin
MCIF_DATA3	L17	104	I/O	MCIF data 3 pin
MCIF_DATA4	K17	105	I/O	MCIF data 4 pin
MCIF_DATA5	K14	106	I/O	MCIF data 5 pin
MCIF_DATA6	K15	107	I/O	MCIF data 6 pin
MCIF_DATA7	K16	108	I/O	MCIF data 7 pin
MCIF_DATA8	J17	109	I/O	MCIF data 8 pin
MCIF_DATA9	J14	110	I/O	MCIF data 9 pin
MCIF_DATA10	J15	111	I/O	MCIF data 10 pin
MCIF_DATA11	J16	112	I/O	MCIF data 11 pin
MCIF_DATA12	H17	113	I/O	MCIF data 12 pin
MCIF_DATA13	H16	114	I/O	MCIF data 13 pin
MCIF_DATA14	G16	118	I/O	MCIF data 14 pin

Terminal Name	Terminal Number		I/O	Description
	BGA	QFP		
MCIF_DATA15	G15	119	I/O	MCIF data 15 pin. This data pin is the most significant bit of the MCIF data bus.
MCIF_ENDIAN	B17	132	I	MCIF endian pin. This sets the endianness for accesses between the external CPU and the internal iceLynx-Micro memory. This pin sets endianness for all MCIF modes. When set to 0, data is read/written to the ex-CPU exactly as it is stored in iceLynx-Micro memory. (Big endian) When set to 1, data is swapped on half-word and byte boundaries before it is read/written to the ex-CPU. (Little endian)
MCIF_INTz	T17	89	O	MCIF Interrupt. This signal is push-pull (always asserted). It does not require a pullup resistor.
MCIF_MODE0	A16	133	I	MCIF mode 0. Used to select MCIF mode.
MCIF_MODE1	B15	134	I	MCIF mode 1. Used to select MCIF mode.
MCIF_MODE2	A15	135	I	MCIF mode 2. Used to select MCIF mode.
MCIF_OEz	N16	96	I	MCIF output enable. Default active low. This input pin indicates if the system CPU wants to perform a MCIF read access. This signal is used for the following modes: ▪ SH-3 I/O access ▪ M16C/62 I/O access ▪ Memory access This signal must be pulled high if not used.
MCIF_R_nWz	P15	92	I	MCIF read/write pin. Default value for a read is 1. Default value for a write is 0.
MCIF_STRBz	P16	93	I	MCIF strobe pin. Default active low. This pin is used (along with MCIF_CS_IOz) to validate the MCIF access. This signal is used for the following modes: ▪ 68000 + wait I/O access ▪ MPC850 I/O access When not used, this pin must be pulled high.
MCIF_WAITz	P17	94	O	MCIF wait pin. Default active high. iceLynx-Micro asserts this signal if it is not ready to service an MCIF request. When not asserted, this signal is in a high-Z state. This signal is used for the following modes: ▪ 68000 + wait I/O access ▪ SH-3 I/O access ▪ M16C/62 I/O access
MCIF_WEz	N17	97	I	MCIF Write Enable. Default active low. This input pin indicates if the system CPU wants to perform a MCIF write access. This signal is used for the following modes: • SH-3 I/O access • M16C/62 I/O access • Memory access This signal must be pulled high if not used.
Universal Asynchronous Receiver Transmitter Pins				
UART_RxD	U15	86	I	UART receive port. Data from the system is input to the UART buffer using this pin.
UART_TxD	R14	85	O	UART transmit port. Data from the UART buffer is output to the system using this pin.
Joint Test Action Group (JTAG) and ARM Pins				
JTAG_TCK	U13	80	I	JTAG clock pin. Both the boundary scan and ARM JTAG uses this input for the JTAG clock.
JTAG_TDI	T12	78	I	JTAG test data input pin

Terminal Name	Terminal Number		I/O	Description
	BGA	QFP		
JTAG_TDO	R12	79	O	JTAG test data output pin
JTAG_TMS	U12	77	I	JTAG test mode selector pin
JTAG_TRSTn	T13	81	I	JTAG reset pin. Both the boundary scan and ARM JTAG uses this input for the JTAG clock. **Note 1**: TSB43Cx43A/TSB43CA42 must have JTAG_TRSTn=0 for correct ARM interrupt operation. **Note 2**: JTAG_TRST must be asserted once after power-up for correct operation of the iceLynx-Micro.
ARM_TDI	U14	83	I	ARM JTAG test data input pin
ARM_TDO	T14	84	O	ARM JTAG test data output pin
ARM_TMS	R13	82	I	ARM JTAG test mode selector pin
General-Purpose Input/Out Pins (GPIO)				
GPIO0	U9	65	I/O	GPIO0. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO1	P9	66	I/O	GPIO1. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO2	G2	15	I/O	GPIO2. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO3	G1	16	I/O	GPIO3. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO4	H1	17	I/O	GPIO 4. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO5	H4	18	I/O	GPIO 5. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO6	U10	69	I/O	GPIO6. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO7	T10	70	I/O	GPIO7. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO8	P10	71	I/O	GPIO8. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO9	R10	72	I/O	GPIO9. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO10	T15	87	I/O	GPIO10. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
Physical Layer Pins				
TPA0_N TPA1_N TPA2_N TPA0_P TPA1_P TPA2_P	L1, N1, R1, L2, N2, R2	29, 36, 42, 30, 37, 43	I/O	Twisted pair A differential signal terminals. For an unused port, TPAN and TPAP signals are left open (i.e., TSB43CA42 for Port 2).
TPB0_N TPB1_N TPB2_N TPB0_P TPB1_P TPB2_P	K1, M1, P1, K2, M2, P2	25, 33, 39, 26, 34, 40	I/O	Twisted pair B differential signal terminals. For an unused port, TPBN and TPBP signals are left open (i.e., TSB43CA42 for Port 2).
TPBIAS0 TPBIAS1 TPBIAS2	L3, N3, T1	31, 38, 44	I/O	Twisted pair bias output. These signals provide the 1.86-V nominal bias voltage needed for proper operation of the twisted pair driver and receivers for signaling an active connection to a remote node. For an unused port, TPBIAS is left unconnected (i.e., TSB43CA42 for Port 2).

Terminal Name	Terminal Number		I/O	Description
	BGA	QFP		
R1 R0	T3, U3	46, 47	-	Current setting resistors. These pins are connected to external resistors to set the internal operating currents and cable driver output currents. A resistance of 6.34 kΩ ± 1% is required to meet the IEEE 1394-1995 output voltage limits.
FILTER0 FILTER1	T4, U4	49, 50	I/O	PLL filter terminals. These terminals are connected to an external capacitor to form a lag-lead filter required for stable operation of the internal frequency-multiplier PLL, which is using the crystal oscillator. A 0.1-μF ±10% capacitor is the only external component required to complete this filter.
XI X0	T5, U5	52, 53	-	Crystal oscillator inputs. These terminals connect to a 24.576-MHz parallel resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the crystal used.
CPS	J4	22	I	Cable power status. This input to iceLynx-Micro detects if cable power is present. This pin must be connected to the cable power through 390-kΩ resistor.
MSPCTL	H3	19	I	Maximum speed of PHY. When this signal is high; S100 and S200 operation. When this signal is low; S100, S200, and S400 operation.
LINKON	U8	61	O	Link-on output. This signal is asserted whenever LPS is low and a link-on packet is received from the 1394 bus.
High Speed Data Interface (HSDI) Port 0 Pins				
HSDI0_60958_IN	C14	136	I	60958 data input
HSDI0_AMCLK_IN	B14	137	I	Audio master clock input. This clock is used to decode the bi-phase encoding of 60958 data. This pin is also used to input the 1.5 x BCLK for flow control mode.
HSDI0_AVz	B13	140	O	HSDI port 0 available. Programmable. Default active low. For receive from 1394, this signal indicates if a 1394 packet is available in the receive buffer for reading. The HSDI_AV signal for MPEG2 data also depends on time stamp based release. For transmit to 1394, this signal indicates buffer level in HSDI TX modes 8 and 9 by programming a CFR. If the buffer level is above a programmed level, HSDI_AV will be asserted.
HSDI0_CLKz	A14	138	I	HSDI port 0 clock. Programmable. Default rising edge sample. This clock is used to operate the HSDI port 0 logic. In parallel mode the maximum clock is 27 MHz. in serial mode, the maximum clock is 70 MHz. This signal is output to HSDI1_CLKz in pass-through mode. This signal is used as HSDI0_MLPCM_BCLK for DVD-audio transmit.
HSDI0_D0	B12	143	I/O	HSDI port 0 data 0 pin. Data 0 is the least significant bit on the HSDI data bus. In serial mode, only HSDI0_D0 is used. This signal is output to HSDI1_D0 in pass-through mode. This signal is used as HSDI0_MLPCM_D0 for DVD-audio transmit.
HSDI0_D1	A12	144	I/O	HSDI port 0 Data 1 pin This signal is output to HSDI1_D1 in pass-through mode. This signal is used as HSDI0_MLPCM_D1 for DVD-audio transmit.
HSDI0_D2	B11	147	I/O	HSDI port 0 Data 2 pin This signal is output to HSDI1_D2 in pass-through mode. This signal is used as HSDI0_MLPCM_D2 for DVD-audio transmit.
HSDI0_D3	A11	148	I/O	HSDI port 0 Data 3 pin This signal is output to HSDI1_D3 in pass-through mode. This signal is used as HSDI0_MLPCM_A for DVD-audio transmit.

Terminal Name	Terminal Number		I/O	Description
	BGA	QFP		
HSDI0_D4	A10	149	I/O	HSDI port 0 data 4 pin This signal is output to HSDI1_D4 in pass-through mode.
HSDI0_D5	D10	150	I/O	HSDI port 0 data 5 pin This signal is output to HSDI1_D5 in pass-through mode.
HSDI0_D6	C10	151	I/O	HSDI port 0 data 6 pin This signal is output to HSDI1_D6 in pass-through mode.
HSDI0_D7	B10	152	I/O	HSDI port 0 data 7 pin. Data 0 is the most significant bit on the HSDI data bus. This signal is output to HSDI1_D7 in pass-through mode.
HSDI0_DVALIDz	C12	142	I/O	HSDI port 0 data valid pin. Programmable. Default active high. This pin indicates if data on the HSDI data bus valid for reading or writing. For transmit to 1394, this signal is provided by the system with the data. For receive from 1394, iceLynx-Micro provides this signal with the data. For HSDI DV modes, this signal is used as HSDI0_FrameSync indicating DV frame boundary. This signal is output to HSDI1_DVALIDz in pass-through mode If not used in transmit mode, this signal is pulled low.
HSDI0_ENz	C13	139	I	HSDI port 0 enable. Programmable. Default active low. Input by the system to enable the HSDI for both transmit to and receive from 1394. If not used, this signal is pulled enabled (low or high depending on the polarity set). The application can use HSDI_DVALID or HSDI_SYNC to validate the HSDI data. This signal is used as HSDI0_MLPCM_LRCLK for DVD-audio transmit.
HSDI0_SYNCz	A13	141	I/O	HSDI port 0 sync signal. Programmable. Default active high. This signal indicates the start of packet. For transmit to 1394, this signal is provided by the system with the data. For receive from 1394, iceLynx-Micro provides this signal with the data. This signal is output to HSDI1_SYNCz in pass-through mode. If not used in transmit mode, this signal is pulled low or high depending on the polarity.
High Speed Data Interface (HSDI) Port 1 Pins				
HSDI1_AMCLK_IN	B5	169	I	Audio master clock input. This clock is used to decode the bi-phase encoding of 60958 data. This pin also inputs the 1.5 x BCK for flow control mode. MLPCM interface, HSDI1 audio port, and HSDI1 video port share IsoPathBuffer 1. Only one interface can access the buffer at a time.
HSDI1_AMCLK_OUT	C5	170	O	Audio master clock output. This clock is derived from the VCO_CLK input. 60958 data output from iceLynx-Micro is bi-phase encoded using this clock.
HSDI1_AUDIO_ERR	A4	171	O	Audio error signal. iceLynx-Micro asserts this signal whenever an audio error condition occurs. (Receive from 1394 only.)
HSDI1_AUDIO_MUTE	B4	172	O	Audio mute status. iceLynx-Micro asserts this signal whenever an audio mute condition has occurred, and hardware has muted the HSDI1 audio interface. (Receive from 1394 only.)
HSDI1_60958_IN	C4	173	I	60958 data input
HSDI1_60958_OUT	A3	174	O	60958 data output This signal is also used as FLWCTRL_DVALID in flow control data valid mode.

Terminal Name	Terminal Number		I/O	Description
	BGA	QFP		
HSDI1_AVz	C9	155	O	HSDI port 1 available. Programmable. Default active low. For receive from 1394, this signal indicates if a 1394 packet is available in the receive buffer for reading. The HSDI_AV signal for MPEG2 data also depends on time stamp based release. For transmit to 1394, this signal indicates the buffer level in HSDI TX modes 8 and 9 by programming a CFR. This pin indicates buffer level in transmit mode by programming a CFR. If the buffer level is above a programmed level, HSDI_AV is asserted.
HSDI1_CLKz	A9	153	I/O	HSDI port 1 clock. Programmable. Default rising edge sample. This clock is used to operate the HSDI port 1 logic. In parallel mode, the maximum clock is 27 MHz. In serial mode, the maximum clock is 70 MHz. This signal is used as HSDI1_SACD_BCLK for SACD transmit and receive. MLPCM interface, HSDI1 audio port, and HSDI1 video port share IsoPathBuffer 1. Only one interface can access the buffer at a time.
HSDI1_D0	B8	158	I/O	HSDI port 1 data 0 pin. Data 0 is the least significant bit on the HSDI data bus. In serial mode, only HSDI0_D0 is used. This signal is used as HSDI1_SACD_D0 for SACD transmit and receive.
HSDI1_D1	D8	159	I/O	HSDI port 1 data 1 pin This signal is used as HSDI1_SACD_D1 for SACD transmit and receive.
HSDI1_D2	C7	163	I/O	HSDI port 1 data 2 pin This signal is used as HSDI1_SACD_D2 for SACD transmit and receive.
HSDI1_D3	D7	164	I/O	HSDI port 1 data 3 pin This signal is used as HSDI1_SACD_D3 for SACD transmit and receive.
HSDI1_D4	A6	165	I/O	HSDI port 1 data 4 pin This signal is used as HSDI1_SACD_D4 for SACD transmit and receive.
HSDI1_D5	B6	166	I/O	HSDI port 1 data 5 pin This signal is used as HSDI1_SACD_D5 for SACD transmit and receive.
HSDI1_D6	C6	167	I/O	HSDI port 1 data 6 pin This signal is used as HSDI1_SACD_A for SACD transmit and receive.
HSDI1_D7	A5	168	I/O	HSDI port 1 data 7 pin. Data 0 is the most significant bit on the HSDI data bus.
HSDI1_DVALIDz	A8	157	I/O	HSDI port 1 data valid pin. Programmable. Default active high. This pin indicates if data on the HSDI data bus valid for reading or writing. For transmit to 1394, this signal is provided by the system with the data. For receive from 1394, iceLynx-Micro provides this signal with the data. For HSDI DV modes, this signal is used as HSDI0_FrameSync indicating DV frame boundary. If not used in transmit mode, this signal is pulled low.
HSDI1_ENz	D9	154	I	HSDI port 1 enable. Programmable. Default active low. Input by the system to enable the HSDI for both transmit to and receive from 1394. If not used, this signal is pulled enabled (low or high depending on the polarity set). The application can use HSDI_DVALID or HSDI_SYNC to validate the HSDI data.

Terminal Name	Terminal Number		I/O	Description
	BGA	QFP		
HSDI1_SYNCz	B9	156	I/O	HSDI port 1 sync signal. Programmable. Default active high. This signal indicates the start of a packet. For transmit to 1394, this signal is provided by the system with the data. For receive from 1394, iceLynx-Micro provides this signal with the data. If not used in transmit mode, this signal is pulled low or high depending on the polarity. This signal is used as HSDI1_SACD_FRAME for SACD transmit and receive.
DVD-Audio Interface Pins				
MLPCM_A	G3	14	I/O	Audio MLPCM interface ancillary data. Ancillary data is input/output using this pin. For DVD-Audio, MLPCM_LRCLK determines if ancillary left or ancillary right data is present. This signal also functions as FLWCTL_A in flow control mode.
MLPCM_BCLK	E1	9	I/O	Audio MLPCM interface bit clock. Multiple functions: ▪ DVD audio BCK (I) ▪ DVD audio BCK (O) ▪ Flow control BCK (I/O) MLPCM interface, HSDI1 audio port, and HSDI1 video port share IsoPathBuffer 1. Only one interface can access the buffer at a time.
MLPCM_D0	F2	11	I/O	Audio MLPCM interface D0. Contains channel 1 and channel 2 information. MLPCM_LRCLK determines which channel is present. This signal also functions as FLWCTL_D0 in flow control mode.
MLPCM_D1	F1	12	I/O	Audio MLPCM interface D1. Contains channel 3 and channel 4 information. MLPCM_LRCLK determines which channel is present. This signal also functions as FLWCTL_D0 in flow control mode.
MLPCM_D2	G4	13	I/O	Audio MLPCM interface D2. Contains channel 5 and channel 6 information. MLPCM_LRCLK determines which channel is present. This signal also functions as FLWCTL_D0 in flow control mode
MLPCM_LRCLK	F3	10	I/O	Audio MLPCM interface left-right clock. Multiple functions: ▪ DVD audio LRCLK (I) ▪ DVD audio LRCLK (O) ▪ Flow control LRCLK (I/O)
Audio Phase Lock Loops Pins				
DIV_VCO	E3	7	O	Output for external phase detector. This signal is the divided VCO_CLK. It used by the external phase detector to compare with the REF_SYT signal. The divide ratios are setup in CFR.
PLL_TEST	E2	8	O	PLL test. This signal is used for internal Texas Instruments testing and must be unconnected for normal operation.
REF_SYT	D1	6	O	Output for external phase detector. This signal represents the SYT match for received audio or DV packets. The phase detector uses it as input to detect differences between the SYT match and the VCO clock.
VCO_CLK	D2	5	I	Input from VCO. This signal generates internal audio and DV clocks for receive clock recovery. Audio frequency: 33.868 MHz or 36.864 MHz. DV frequency: 30.72 MHz, 27 MHz
Test Mode Pins				
TEST_MODE0	C2	2	I/O	Test mode. Used for internal Texas Instruments testing. Must be pulled low for normal operation.
TEST_MODE1	C1	3	I/O	Test mode. Used for internal Texas Instruments testing. Must be pulled low for normal operation.

Terminal Name	Terminal Number		I/O	Description
	BGA	QFP		
TEST_MODE2	P7	57	I/O	Test mode. Used for internal Texas Instruments testing. Must be pulled low for normal operation.
TEST_MODE3	R7	58	I/O	Test mode. Used for internal Texas Instruments testing. Must be pulled low for normal operation.
TEST4	R9	67	I/O	Factory test pin. Must tie to low for normal operation. Recommend connection to ground through a 1-kΩ resistor.
TEST5	T9	68	I/O	Factory test pin. Must tie to low for normal operation. Recommend connection to ground through a 1-kΩ resistor.

1.6 Memory Map

Figure 8 shows the memory map for iceLynx-Micro.

- The program memory (256K bytes) includes the communication memory for transactions between the internal and external CPU. The boundaries of the communication memory are programmable. (Refer to the register address)
- Two 1024-byte RAMs are included for ex-CPU memory access functions.
- The configuration registers start at offset 0x 0010 0000.

Note: The program memory is divided into physical blocks. (For example, four blocks of 64K each.) Each memory block is accessed by the ARM or ex-CPU independently. The ARM could access program memory in block 1 at the same time as the ex-CPU accesses comm memory in block 4. Because of this, software must program the comm memory pointers into the highest memory block (the last 64K of block 4). Noncritical program code can also be loaded into this block.

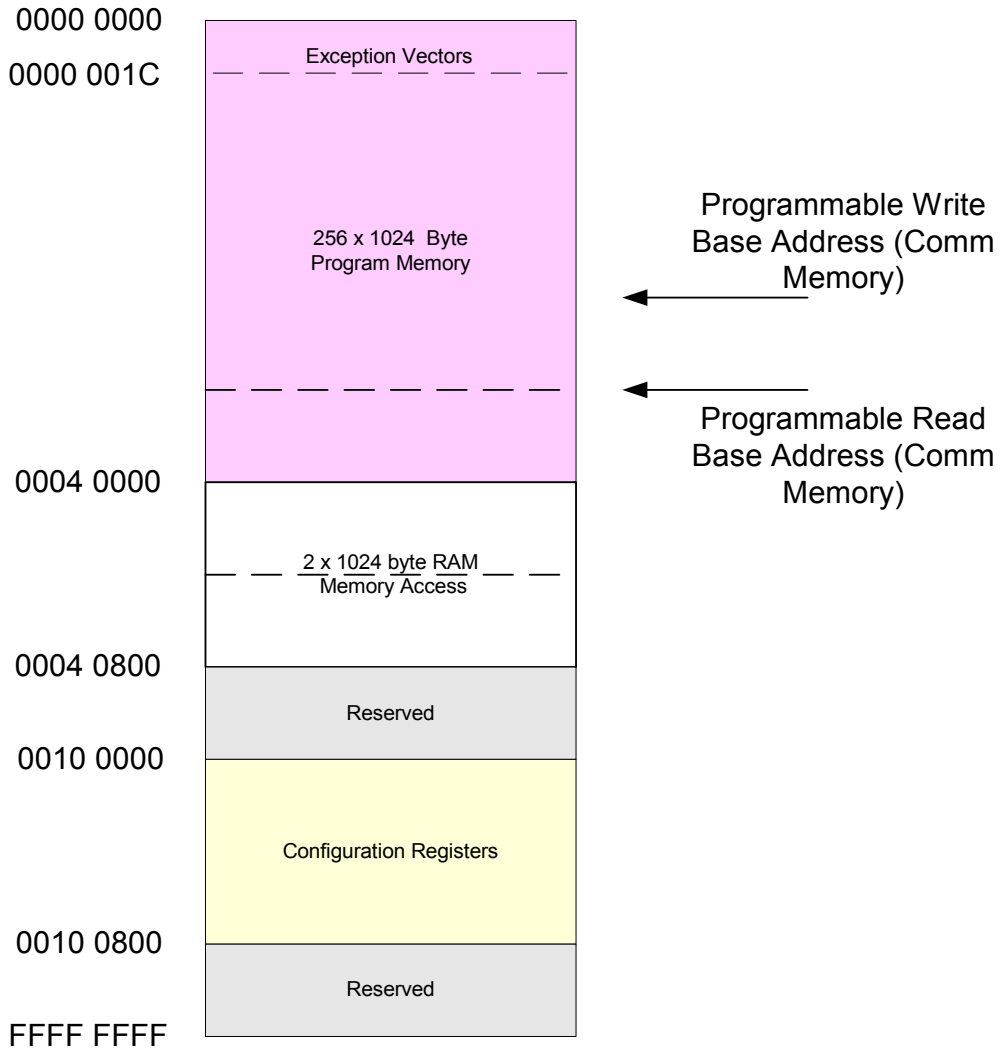


Figure 8. TSB43Cx43 Memory Map

1.7 DTCP Encryption – Hardware Implementation (TSB43CA43A and TSB43CA42 Only)

The TSB43CA43A and TSB43CA42 version of iceLynx-Micro is fully compliant with the DTCP method of digital content protection. iceLynx-Micro supports the baseline M6 cipher, content key creation, and key updates in iceLynx-Micro hardware. iceLynx-Micro has the capability to encrypt or decrypt MPEG2-DVB, DSS, DV, or audio. The authentication and key exchange (AKE) is also implemented in hardware. Customers requiring the DTCP version of iceLynx-Micro must have signed an NDA with Texas Instruments and be a current DTLA licensee. Information on the DTCP implementation within the TSB43CA43A and TSB43CA42 devices are found in the following document provided by Texas Instruments:

Note: Recipients must have signed Texas Instruments NDA and be a current DTLA licensee to receive this document.

1.8 Program Memory

1.8.1 Overview/Description

The iceLynx-Micro provides 256K bytes of internal program RAM. The program memory is loaded by the external CPU interface. The external CPU cannot read the program memory.

Anytime the RESET_ARMn pin is asserted (transitions from high to low), the cipher and AKE registers are cleared.

1.8.2 External CPU (Parallel Mode)

Steps for loading program memory:

1) ARM is placed in reset (using RESET_ARMn pin) and ex-CPU initiates write to the program memory CFR (Sys.IntMemLoad at 0x5C).If the ARM is only put into reset, there is no change in the program memory.
2) The program must contain a 2-quadlet header. The 2-quadlet header specifies if the program is LEB encrypted. See Section 1.9.5 for more information on LEB.
3) The program is loaded into program memory through the Sys.IntMemLoad CFR. The program is placed in memory starting at address 0x 0000 0000. The ex-CPU indicates the end of program load by deasserting the RESET_ARMn signal. When the RESET_ARMn signal is deasserted, the iceLynx-Micro hardware pads the rest of program memory with zeros.
4) The ARM is executing code as soon as RESET_ARMn signal is deasserted and all 256K bytes of program memory are loaded.

1.9 External CPU Interface

1.9.1 Overview/Description

The ex-CPU accesses iceLynx-Micro configuration registers and FIFOs using 32-bit addressing. The quadlet-aligned address is provided for the first 16-bit access. The iceLynx-Micro internally increments the address for the second 16-bit access. All 32 bits of a register or FIFO must be read using back-to-back transactions. An access to address N must be followed by address N+2.

A 16-bit processor can be used with iceLynx-Micro. However, the processor must access the entire quadlet address (all 32 bits) in order. For example, for a register address N, the ex-CPU must first access register address N and then address N+2. It cannot access address N+2 first. If the ex-CPU accesses the 32-bit address incorrectly, the ExCPUInt.ExCPUErr interrupt occurs.

The Ex-CPU can access to iceLynx-Micro by I/O- or memory-type methods. The iceLynx-Micro supports four memory types of processor interfaces: Type-1, Type-2, I/O Type-1 SH3, and I/O Type-2 M16C. The ex-CPU I/Fs and access types are categorized as follows:

1. Asynchronous I/O-type

Bus clock is not provided.

- I/O Type-0 68K + wait
- I/O Type-1 SH3 SRAM-like + wait
- I/O Type-2 M16C SRAM-like + wait

2. Synchronous I/O-type

Bus clock is provided.

- I/O Type-3 MPC850

3. Memory-type

Access to single port RAM. Timing matches for I/O type except bus clock are provided and a special memory chip select signal is used.

- Type-1 memory access
- Type-2 memory access
- SH3-type memory access
- M16C/62 memory access

Users can select the ex-CPU by setting the external pin MCIF_MODE[2:0]. Table 1 shows the pin assignments.

Table 1. External CPU MCIF Pin Assignment Modes

				External MCU Interface Method†	
MCIF_MODE[2:0]				I/O Type	Memory Type
0x0	0	0	0	I/O Type-0: 68K+ wait	Memory access available
0x1	0	0	1	I/O Type-1: SH3 + wait	
0x2	0	1	0	I/O Type-2: M16C + wait	
0x3	0	1	1	I/O Type-3: MPC850	
0x4	1	0	0	I/O types reserved	Memory access invalid
0x5	1	0	1		
0x6	1	1	0		
0x7	1	1	1		

† External MCU access type (I/O or memory) is dependent on the chip select signal used, MCIF_CS_IOz or MCIF_CS_MEMz, respectively.

With regard to the above four types of processors, Table 2 shows the relation between the signals of the iceLynx-Micro and those of the ex-CPU.

‡**Note:** ARM must be in reset to load program memory.

Table 2. Ex-CPU I/F Signals

Signal Name	Port Type	External Interface Method			
		Type-0 (68K)	Type-1 (SH3)	Type-2 (M16C)	Type-3 (MPC850)
I/O Type					
MCIF_CS_IOz	I	CSn	CSn	CSn	CSn
MCIF_RW	I	R_nW	----	----	R_nW
MCIF_STRBz	I	STRBz	----	----	TSn
MCIF_ACKz	O (3S)	NA	----	----	TAn
MCIF_WAITz	O (3S)	WAITz	WAITz	WAITz	----
MCIF_OEz	I	----	RDn	RDn	----
MCIF_WEz	I	----	WRn	WRn	----
MCIF_BUSCLKz	I	----	----	----	BUSCLKz
Memory Type					
MCIF_CS_MEMz	I	CSn			
MCIF_OEz	I	RDn			
MCIF_WEz	I	WRn			
MCIF_BUSCLKz	I	BUSCLKz			

1.9.2 Endian Setting (Parallel and Memory Accesses)

The iceLynx-Micro registers in the CFR map are structured as (byte 0, byte 1, byte 2, and byte 3). The iceLynx-Micro has an endian pin (MCIF_ENDIAN) that controls the byte order between the ex-CPU interface and internal iceLynx-Micro memory (including CFRs, FIFOs, and RAM for memory access). The status of the MCIF_ENDIAN pin is shown at ExCPUCfg.Endian CFR.

Note: In I/O mode, the MCIF_ENDIAN pin is asserted or deasserted for individual 32-bit accesses.

MCIF_A[1] = 0, Data = ABCD
MCIF_A[1] = 1, Data = EF01

If MCIF_ENDIAN is set to 0, the data written to the FIFO is ABCD EF01.
If MCIF_ENDIAN is set to 1, the data written to the FIFO is EF01 ABCD.

1.9.2.1 Parallel Mode and Memory Access

- In I/O mode, the ex-CPU has access to program memory, comm memory, and CFRs through registers. The ex-CPU only has write access to the program memory. It can only perform writes while the ARM is in reset.
- In memory mode, the ex-CPU directly accesses the two 1024-byte single port RAMs. The two RAMs are used individually (1024 bytes each) and are randomly accessed by the ARM (32-bit) and ex-CPU (16-bit). The MCIF_ADDR signals indicate where the ex-CPU is accessing. The MCIF_ADDR range to address the single port RAMs is 0x000 through 0x7FF. The ex-CPU has priority access to the RAM. The software must assure there are no collisions. (Use GPInts)

1.9.3 Ex-CPU Access

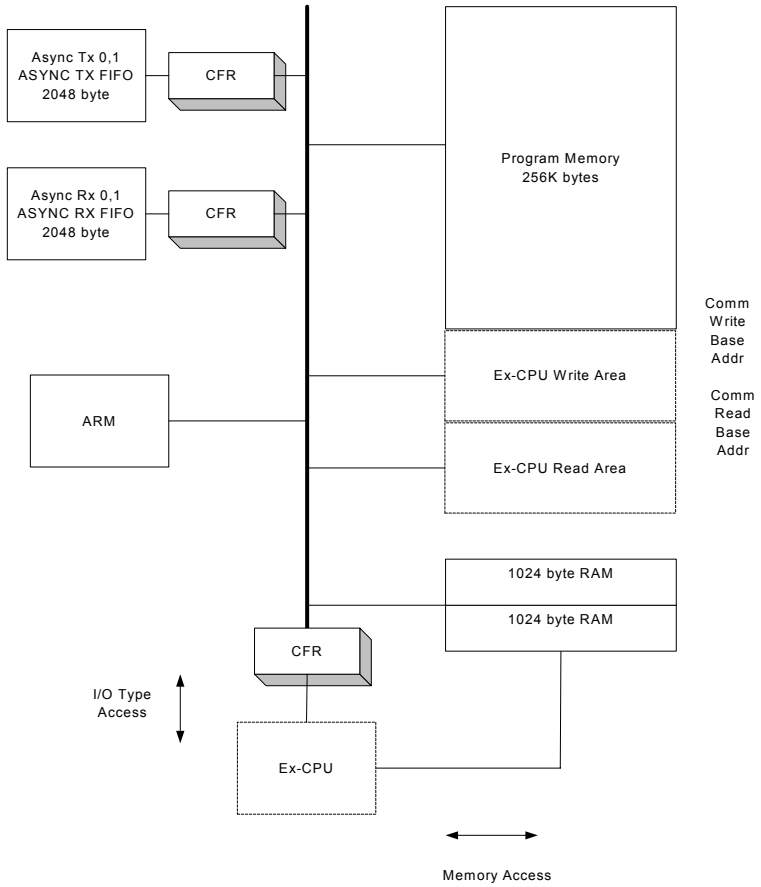
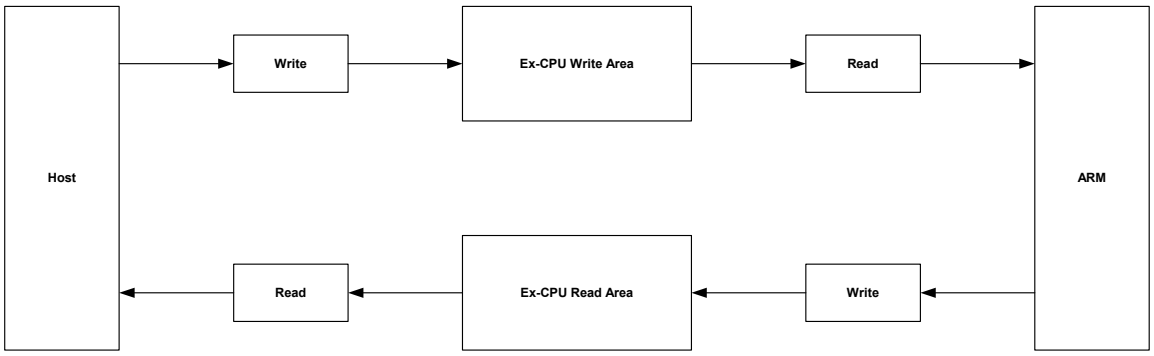


Figure 9. Ex-CPU Access

The communication area is part of the 256K-byte memory. This area is used for data communication between Ex-CPU and ARM. CFR CommWrBase and CommRdBase define the top address of the area. The communication area consists of an ex-CPU write area and ex-CPU read area.



Upon the chip reset, CommWrBase and CommRdBase are 0x 0000 FFFF. When set to this default value, the ex-CPU is not allowed to access the communication memory.

The ARM manages the communication area between the ex-CPU and ARM. General interrupts share the access time for the areas. The ARM has full random access of the communication memory area. The parallel ex-CPU can access the communication memory through the CommData CFR.

The ARM can know how much data was read or written into the communication area by reading the Sys.CommStat.RdCnt and Sys.CommStat.WrCnt bits in CFR. The ARM can also reset the internal address counters using Sys.CommStat.RdCnt and Sys.CommStat.WrCnt bits in CFR.

Note: Only the ARM can set the Comm (read/write) base addresses.

1.9.3.1 Ex-CPU and ARM Communication Sequence in Parallel Ex-CPU I/F Mode

The Ex-CPU and ARM use GPInts (general-purpose interrupts) for communication. Any reference to interrupt in the following sections refers to the GPInts. GPInts are available in the Sys.InCPUCommInt and Sys.ExCPUCommInt CFRs.

1.9.3.1.1 Ex-CPU Read

- ARM sends an interrupt to ex-CPU as READ ENABLE.
- Ex-CPU sends an interrupt to ARM as READ REQUEST. ARM invokes a timer to watch access timeout and can't access read communication area memory ex-CPU access end.
- Ex-CPU reads data from communication area.
- Ex-CPU sends an interrupt to ARM as READ ACCESS END. ARM stops the timer. ARM sends an interrupt to Ex-CPU as READ DISABLE" Sys.*
- CPUInt.GPInt bits and the associated Sys.*CPUCommInt CFRs are used for this communication.

1.9.3.1.2 Ex-CPU Write

- ARM sends an interrupt to ex-CPU as WRITE ENABLE.
- Ex-CPU sends an interrupt to ARM as WRITE REQUEST. ARM invokes a timer to watch access timeout and can't access write communication memory until ex-CPU access end.
- Ex-CPU writes data into communication area.
- Ex-CPU sends an interrupt to ARM as WRITE ACCESS END. ARM stops the timer.
- ARM sends an interrupt toeEx-CPU as WRITE DISABLE.
- Sys.*CPUInt.GPInt bits and the associated Sys.*CPUCommInt CFRs are used for this communication.

1.9.3.1.3 Ex-CPU Access Limitation

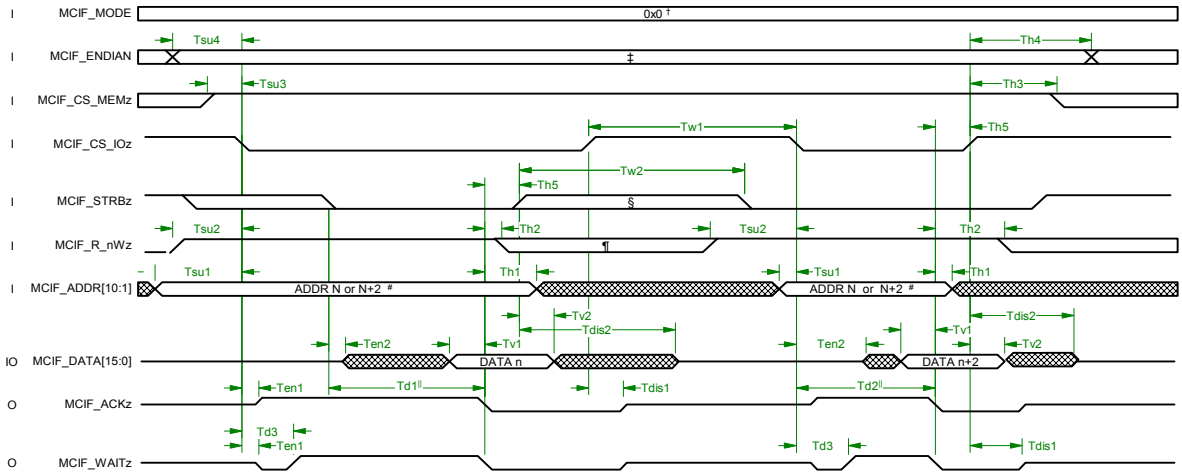
Table 3. Ex-CPU Access Limitation

Addr	Bit	Bit Name	Read Access	Write Access	Condition
018h	16	InCPUCfg.DbgRegUnlock	Yes	Yes	
018h	8	InCPUCfg.DebugEn	Yes	No	
018h	**N/A**	**RSVD**	**N/A**	**N/A**	
048h	15:0	CommWrBase.Addr	No	No	
04Ch	15:0	CommRdBase.Addr	No	No	
05Ch	31:0	IntMemLoad.IntMemLoad	Conditional	Conditional	**Write access only** while ARM_RESET = LOW in normal operation mode: IntMemDiag.ProtectDis = 0. **Read and write access** in diagnostic mode: IntMemDiag.ProtectDis = 1
060h	25	IntMemDiag.EncryptDis	Yes	No	
060h	24	IntMemDiag.ProtectDis	Yes	No	
03Ch	31:0	InCPUComIntEn.*	Yes	No	
024h	31:0	InCPUInt.*	Yes	No	
028h, 02Ch	31:0	InCPUIntEn.*	Yes	No	
1FAh -1FCh, 324h – 32Ch	**N/A**	**RSVD**	**N/A**	**N/A**	
200h - 204h, 330h – 334h	**N/A**	**RSVD**	**N/A**	**N/A**	
208h - 20Ch, 338h – 33Ch	**N/A**	**RSVD**	**N/A**	**N/A**	
630h – 774h	**N/A**	**RSVD**	**N/A**	**N/A**	

Note: The **BOLD** coded CFRs are reserved (RSVD).

1.9.4 Ex-CPU Timing

1.9.4.1 I/O Type-0 68K + Wait



NOTES: A. The timing diagram assumes MCIF signals used their default polarities. The MCIF_WAITz defaults to the active high polarity in the MCIF I/O Type-0 68K mode.

B. MCIF_OEz, MCIF_WEz and MCIF_BUSCLKz are "Don't Care" for the MCIF I/O Type-0 68K mode.

C. Single 16-bit read accesses will not result in an error or an interrupt.

D. For a read access to occur both MCIF_CS_IOz and MCIF_STRBz must be asserted.

† MCIF_MODE may be changed during device operation but is not recommended. MCIF_MODE should not change during a quadlet access cycle.

‡ MCIF_ENDIAN may change during device operation. It should not change during a quadlet access or data corruption may result.

§ The MCIF_STRBz is not required to deassert between accesses.

¶ MCIF_R_nWz may change between accesses.

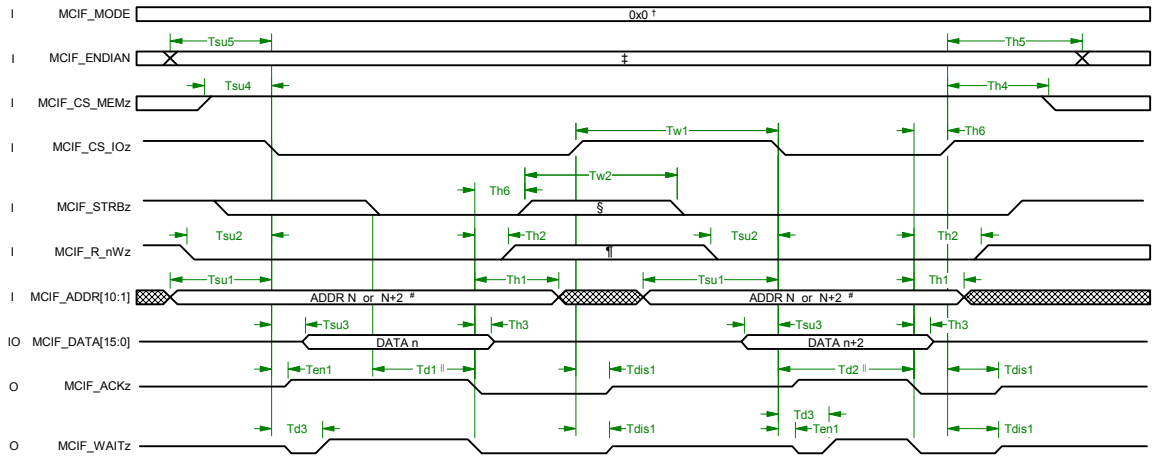
CFR accesses must be quadlet aligned. The MCIF_ADDR[1] bit is immaterial and the MCIF_ADDR may be of value "N" or "N+2" when considered as a byte address (ADDR[10:0]). MCIF_ADDR[1] is internally grounded. MCIF_ADDR[1] is used in the Memory MCIF mode.

|| The MCIF_ACKz / MCIF_WAITz assert delays Td1 and Td2 are measured from the MCIF_CS_IOz or MCIF_STRBz assert, whichever occurs last in the access.

Figure 10. I/O Type-0 68K + Wait Read

Table 4. I/O Type-0 68K + Wait Read MCIF AC-Timing Parameters

	Description	Min	Max	Units
Tsu1	Setup time, MCIF_ADDR valid before MCIF_CS_IOz asserted	0		ns
Tsu2	Setup time, MCIF_R_nWz before MCIF_CS_IOz asserted	0		ns
Tsu3	Setup time, MCIF_CS_MEMz deasserted before MCIF_CS_IOz asserted	0		ns
Tsu4	Setup time, MCIF_ENDIAN before MCIF_CS_IOz asserted	0		ns
Th1	Hold time, MCIF_ADDR valid after MCIF_ACKz asserted	0		ns
Th2	Hold time, MCIF_R_nWz after MCIF_ACKz asserted	0		ns
Th3	Hold time, MCIF_CS_MEMz deasserted after MCIF_CS_IOz deasserted	0		ns
Th4	Hold time, MCIF_ENDIAN after MCIF_CS_IOz deasserted	0		ns
Th5	Hold time, MCIF_CS_IOz or MCIF_STRBz after MCIF_ACKz asserted / MCIF_WAITz deasserted	0		ns
Td1	Delay time, read access, MCIF_ACKz asserted / MCIF_WAITz deasserted after MCIF_STRBz asserted		260	ns
Td2	Delay time, read access, MCIF_ACKz asserted / MCIF_WAITz deasserted after MCIF_CS_IOz asserted		260	ns
Td3	Delay time, MCIF_WAITz asserted after MCIF_CS_IOz asserted		15	ns
Tv1	Valid time, MCIF_DATA before MCIF_ACKz asserted / MCIF_WAITz deasserted	0		ns
Tv2	Valid time, MCIF_DATA after MCIF_CS_IOz or MCIF_STRBz deasserted	0		ns
Ten1	Enable time, MCIF_CS_IOz asserted to MCIF_ACKz / MCIF_WAITz driven		15	ns
Ten2	Enable time, MCIF_CS_IOz and MCIF_STRBz asserted to MCIF_DATA driven		15	ns
Tdis1	Disable time, MCIF_ACKz / MCIF_WAITz high impedance from MCIF_CS_IOz deasserted		15	ns
Tdis2	Disable time, MCIF_DATA high impedance from MCIF_CS_IOz or MCIF_STRBz deasserted		15	ns
Tw1	Access width, MCIF_CS_IOz deasserted to MCIF_CS_IOz asserted	25		ns
Tw2	Access width, MCIF_STRBz deasserted to MCIF_STRBz asserted	0		ns



NOTES: A. The timing diagram assumes MCIF signals used their default polarities. The MCIF_WAITz defaults to the active high polarity in the MCIF I/O Type-0 68K mode.

B. MCIF_OEz, MCIF_WEz and MCIF_BUSCLK are "Don't Care" for the MCIF I/O Type-0 68K mode.

C. Single 16-bit write accesses are not allowed, resulting in the ExCPUErr interrupt bit being set.

D. For a write access to occur both MCIF_CS_IOz and MCIF_STRBz must be asserted.

† MCIF_MODE may be changed during device operation but is not recommended. MCIF_MODE should not change during a quadlet write cycle.

‡ MCIF_ENDIAN may change during device operation. It should not change during a quadlet access or data corruption may result.

§ MCIF_STRBz is not required to deassert between accesses.

¶ MCIF_R_nWz may change between accesses.

CFR accesses must be quadlet aligned. The MCIF_ADDR[1] bit is immaterial and the MCIF_ADDR may be of value "N" or "N+2" when considered as a byte address (ADDR[10:0]). MCIF_ADDR[0] is internally grounded. MCIF_ADDR[1] is used in the Memory MCIF mode.

|| The MCIF_ACKz / MCIF_WAITz assert delays Td1 and Td2 are measured from the MCIF_CS_IOz or MCIF_STRBz assert, whichever occurs last in the access.

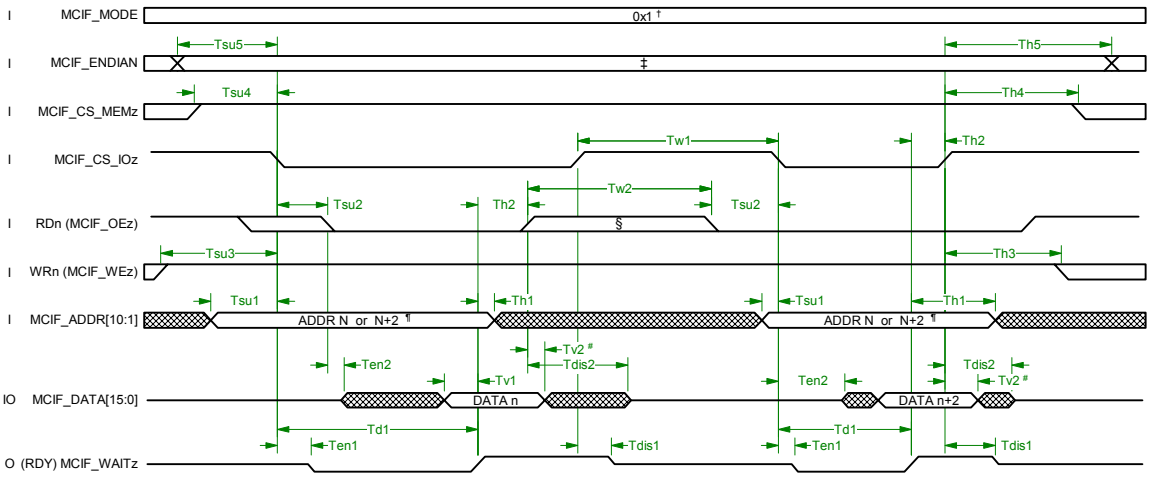
Figure 11. I/O Type-0 68K + Wait Write

Table 5. I/O Type-0 68K + Wait Write MCIF AC Timing Parameters

	Description	Min	Max	Units
Tsu1	Setup time, MCIF_ADDR valid before MCIF_CS_IOz asserted	0		ns
Tsu2	Setup time, MCIF_R_nWz before MCIF_CS_IOz asserted	0		ns
Tsu3	Setup time, MCIF_DATA valid before MCIF_CS_IOz asserted	-40		ns
Tsu4	Setup time, MCIF_CS_MEMz deasserted before MCIF_CS_IOz asserted	0		ns
Tsu5	Setup time, MCIF_ENDIAN before MCIF_CS_IOz asserted	0		ns
Th1	Hold time, MCIF_ADDR valid after MCIF_CS_IOz asserted	0		ns
Th2	Hold time, MCIF_R_nWz after MCIF_CS_IOz asserted	0		ns
Th3	Hold time, MCIF_DATA valid after MCIF_ACKz asserted / MCIF_WAITz deasserted	0		ns
Th4	Hold time, MCIF_CS_MEMz deasserted after MCIF_CS_IOz deasserted	0		ns
Th5	Hold time, MCIF_ENDIAN after MCIF_CS_IOz deasserted	0		ns
Th6	Hold time, MCIF_CS_IOz or MCIF_STRBz after MCIF_ACKz asserted / MCIF_WAITz deasserted	0		ns
Td1	Delay time, first write access, MCIF_ACKz asserted / MCIF_WAITz deasserted after MCIF_CS_IOz / MCIF_STRBz asserted		140	ns
Td2	Delay time, second write access, MCIF_ACKz asserted / MCIF_WAITz deasserted after MCIF_CS_IOz / MCIF_STRBz asserted		100	ns
Td3	Delay time, MCIF_WAITz asserted after MCIF_CS_IOz asserted		15	ns
Ten1	Enable time, MCIF_CS_IOz asserted to MCIF_ACKz / MCIF_WAITz driven		15	ns
Tdis1	Disable time, MCIF_ACKz / MCIF_WAITz high impedance from MCIF_CS_IOz deasserted		15	ns
Tw1	Access width, MCIF_CS_IOz deasserted to MCIF_CS_IOz asserted	25		ns
Tw2	Access width, MCIF_STRBz deasserted to MCIF_STRBz asserted	0		ns
Tsu1	Setup time, MCIF_ADDR valid before MCIF_CS_IOz asserted	0		ns

1.9.4.2 I/O Type-1 SH3 SRAM-Like + Wait

This I/O interface type supports SH3(HD6417709A) bus state controller specification.



NOTES: A. The timing diagram assumes MCIF signals used their default polarities. The RDY (MCIF_WAITz) defaults to the active low polarity in the MCIF I/O Type-1 SH3 mode.

B. The MCIF_STRBz, MCIF_R_nWz and MCIF_BUSCLKz inputs are "Don't Care" and the MCIF_ACKz output is not used in the MCIF I/O Type-1 SH3 mode.

C. Single 16-bit read accesses will not result in an error or an interrupt.

† MCIF_MODE may be changed during device operation but is not recommended. MCIF_MODE should not change during a quadlet access cycle.

‡ MCIF_ENDIAN may change during device operation. It should not change during a quadlet access or data corruption may result.

§ For a read access to occur, both MCIF_CS_IOz and RDn (MCIF_OEz) must be asserted. The RDn (MCIF_OEz) is not required to deassert between accesses.

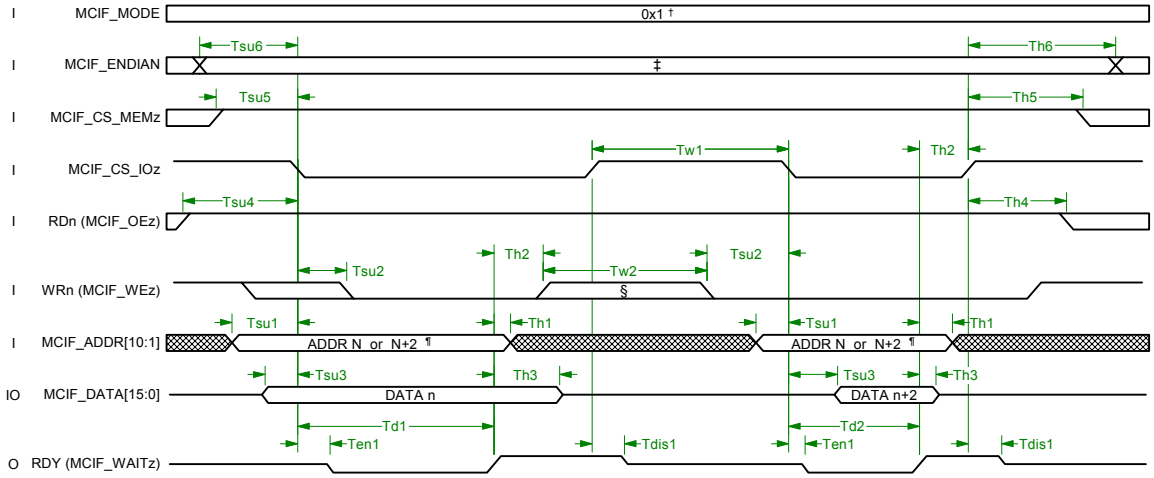
¶ CFR accesses must be quadlet aligned. The MCIF_ADDR[1] bit is immaterial and the MCIF_ADDR may be of value "N" or "N+2" when considered as a byte address (ADDR[10:0]). MCIF_ADDR[0] is internally grounded. MCIF_ADDR[1] is used in the Memory MCIF mode.

Valid time Tv2 is from RDn (MCIF_OEz) or MCIF_CS_IOz, whichever deasserts first in the access.

Figure 12. I/O Type-1 SH3 Read

Table 6. I/O Type-1 SH3 Critical Timing (Read)

	Description	Min	Max	Units
Tsu1	Setup time, MCIF_ADDR valid before MCIF_CS_IOz asserted	0		ns
Tsu2	Setup time, RDn (MCIF_OEz) asserted before MCIF_CS_IOz asserted	-40		ns
Tsu3	Setup time, WRn (MCIF_WEz) deasserted before MCIF_CS_IOz asserted	0		ns
Tsu4	Setup time, MCIF_CS_MEMz deasserted before MCIF_CS_IOz asserted	0		ns
Tsu5	Setup time, MCIF_ENDIAN before MCIF_CS_IOz asserted	0		ns
Th1	Hold time, MCIF_ADDR valid after RDY (MCIF_WAITz) asserted	0		ns
Th2	Hold time, RDn (MCIF_OEz) or MCIF_CS_IOz asserted after RDY (MCIF_WAITz) asserted	0		ns
Th3	Hold time, WRn (MCIF_WEz) deasserted after MCIF_CS_IOz deasserted	0		ns
Th4	Hold time, MCIF_CS_MEMz deasserted after MCIF_CS_IOz deasserted	0		ns
Th5	Hold time, MCIF_ENDIAN after MCIF_CS_IOz deasserted	0		ns
Td1	Delay time, read access, RDY (MCIF_WAITz) asserted after MCIF_CS_IOz asserted		260	ns
Tv1	Valid time, MCIF_DATA before RDY (MCIF_WAITz) asserted	0		ns
Tv2	Valid time, MCIF_DATA after MCIF_CS_IOz or RDn (MCIF_OEz) deasserted	0		ns
Ten1	Enable time, MCIF_CS_IOz asserted to RDY (MCIF_WAITz) driven		15	ns
Ten2	Enable time, MCIF_CS_IOz and RDn (MCIF_OEz) asserted to MCIF_DATA driven		15	ns
Tdis1	Disable time, RDY (MCIF_WAITz) high impedance after MCIF_CS_IOz deasserted		15	ns
Tdis2	Disable time, MCIF_DATA high impedance after MCIF_CS_IOz or RDn (MCIF_OEz) deasserted		15	ns
Tw1	Access width, MCIF_CS_IOz deasserted to MCIF_CS_IOz asserted	25		ns
Tw2	Access width, RDn (MCIF_OEz) deasserted to RDn (MCIF_OEz) asserted	0		ns



NOTES: A. The timing diagram assumes MCIF signals used their default polarities. The RDY (MCIF_WAITz) defaults to the active low polarity in the MCIF I/O Type-1 SH3 mode.

B. The MCIF_STRBz, MCIF_R_nWz and MCIF_BUSCLKz inputs are "Don't Care" and the MCIF_ACKz output is not used in the MCIF I/O Type-1 SH3 mode.

C. Single 16-bit write accesses are not allowed, resulting in the ExCPUErr interrupt bit being set.

† MCIF_MODE may be changed during device operation but is not recommended. MCIF_MODE should not change during a quadlet access cycle.

‡ MCIF_ENDIAN may change during device operation. It should not change during a quadlet access or data corruption may result.

§ For a write access to occur, both MCIF_CS_IOz and MCIF_WEz must be asserted. The WRn (MCIF_WEz) is not required to deassert between accesses.

¶ CFR accesses must be quadlet aligned. The MCIF_ADDR[1] bit is immaterial and the MCIF_ADDR may be of value "N" or "N+2" when considered as a byte address (ADDR[10:0]). MCIF_ADDR[0] is internally grounded. MCIF_ADDR[1] is used in the Memory MCIF mode.

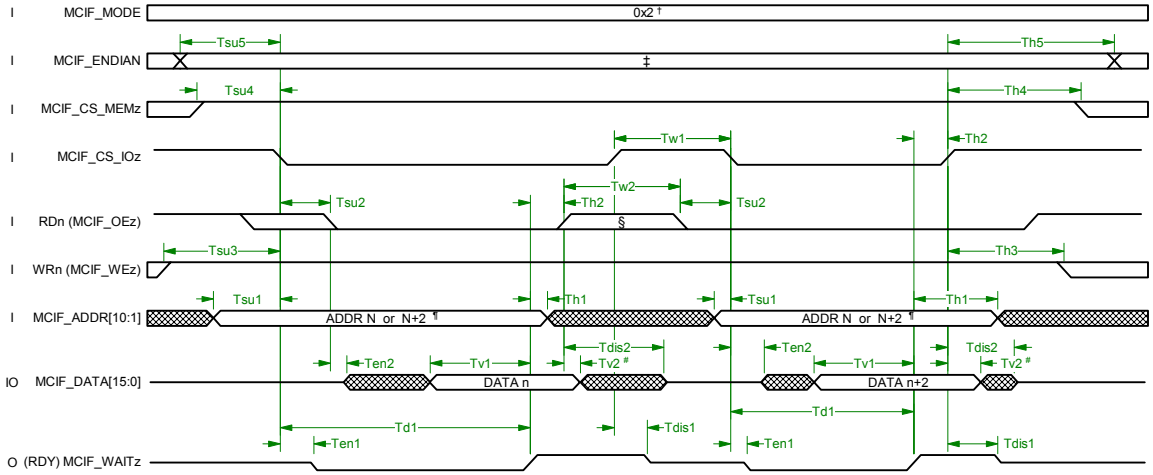
Figure 13. I/O Type-1 SH3 Write

Table 7. I/O Type-1 SH3 AC Timing (Write)

	Description	Min	Max	Units
Tsu1	Setup time, MCIF_ADDR valid before MCIF_CS_IOz asserted	0		ns
Tsu2	Setup time, WRn (MCIF_WEz) asserted before MCIF_CS_IOz asserted	-40		ns
Tsu3	Setup time, MCIF_DATA valid before MCIF_CS_IOz asserted	-40		ns
Tsu4	Setup time, RDn (MCIF_OEz) deasserted before MCIF_CS_IOz asserted	0		ns
Tsu5	Setup time, MCIF_CS_MEMz deasserted before MCIF_CS_IOz asserted	0		ns
Tsu6	Setup time, MCIF_ENDIAN before MCIF_CS_IOz asserted	0		ns
Th1	Hold time, MCIF_ADDR valid after RDY (MCIF_WAITz) asserted	0		ns
Th2	Hold time, WRn (MCIF_WEz) or MCIF_CS_IOz asserted after RDY (MCIF_WAITz) asserted	0		ns
Th3	Hold time, MCIF_DATA valid after RDY (MCIF_WAITz) asserted	0		ns
Th4	Hold time, RDn (MCIF_OEz) deasserted after MCIF_CS_IOz deasserted	0		ns
Th5	Hold time, MCIF_CS_MEMz deasserted after MCIF_CS_IOz deasserted	0		ns
Th6	Hold time, MCIF_ENDIAN after MCIF_CS_IOz deasserted	0		ns
Td1	Delay time, first write access, RDY (MCIF_WAITz) asserted after MCIF_CS_IOz asserted		120	ns
Td2	Delay time, second write access, RDY (MCIF_WAITz) asserted after MCIF_CS_IOz asserted		120	ns
Ten1	Enable time, MCIF_CS_IOz asserted to RDY (MCIF_WAITz) driven		15	ns
Tdis1	Disable time, RDY (MCIF_WAITz) high impedance after MCIF_CS_IOz deasserted		15	ns
Tw1	Access width, MCIF_CS_IOz deasserted to MCIF_CS_IOz asserted	25		ns
Tw2	Access width, WRn (MCIF_WEz) deasserted to WRn (MCIF_WEz) asserted	0		ns

1.9.4.3 I/O Type-2 M16C SRAM-Like + Wait

This type supports the M16C/62-compatible interface timing.



NOTES: A. The timing diagram assumes MCIF signals used their default polarities. The RDY (MCIF_WAITz) defaults to the active low polarity in the MCIF I/O Type-2 M16C mode.

B. The MCIF_STRBz, MCIF_R_nWz and MCIF_BUSCLKz inputs are "Don't Care" and the MCIF_ACKz output is not used in the MCIF I/O Type-2 M16C mode.

C. Single 16-bit read accesses will not result in an error or an interrupt.

† MCIF_MODE may be changed during device operation but is not recommended. MCIF_MODE should not change during a quadlet access cycle.

‡ MCIF_ENDIAN may change during device operation. It should not change during a quadlet access or data corruption may result.

§ For a read access to occur, both MCIF_CS_IOz and RDz (MCIF_OEz) must be asserted. The RDn (MCIF_OEz) is not required to deassert between accesses.

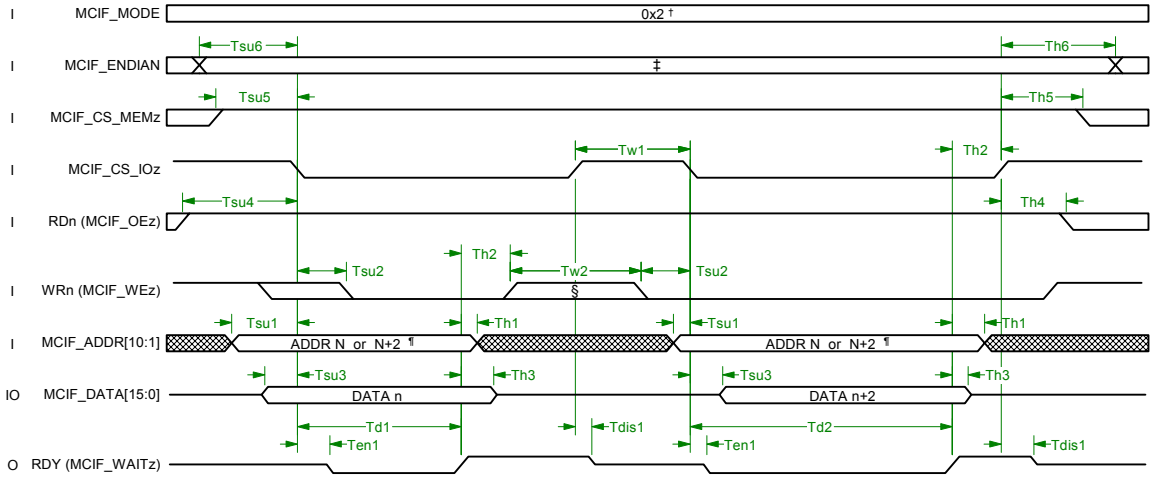
¶ CFR accesses must be quadlet aligned. The MCIF_ADDR[1] bit is immaterial and the MCIF_ADDR may be of value "N" or "N+2" when considered as a byte address (ADDR[10:0]). MCIF_ADDR[0] is internally grounded. MCIF_ADDR[1] is used in the Memory MCIF mode.

Valid time Tv2 is from RDn (MCIF_OEz) or MCIF_CS_IOz, whichever deasserts first in the access.

Figure 14. I/O Type-2 M16C SRAM-Like + Wait Read

Table 8. I/O Type-2 M16C SRAM-Like + Wait AC Timing Parameters (Read)

	Description	Min	Max	Units
Tsu1	Setup time, MCIF_ADDR valid before MCIF_CS_IOz asserted	0		ns
Tsu2	Setup time, RDn (MCIF_OEz) asserted before MCIF_CS_IOz asserted	-40		ns
Tsu3	Setup time, WRn (MCIF_WEz) deasserted before MCIF_CS_IOz asserted	0		ns
Tsu4	Setup time, MCIF_CS_MEMz deasserted before MCIF_CS_IOz asserted	0		ns
Tsu5	Setup time, MCIF_ENDIAN before MCIF_CS_IOz asserted	0		ns
Th1	Hold time, MCIF_ADDR valid after RDY (MCIF_WAITz) asserted	0		ns
Th2	Hold time, RDn (MCIF_OEz) or MCIF_CS_IOz asserted after RDY (MCIF_WAITz) asserted	0		ns
Th3	Hold time, WRn (MCIF_WEz) deasserted after MCIF_CS_IOz deasserted	0		ns
Th4	Hold time, MCIF_CS_MEMz deasserted after MCIF_CS_IOz deasserted	0		ns
Th5	Hold time, MCIF_ENDIAN after MCIF_CS_IOz deasserted	0		ns
Td1	Delay time, read access, RDY (MCIF_WAITz) asserted after MCIF_CS_IOz asserted	210	340	ns
Tv1	Valid time, MCIF_DATA before RDY (MCIF_WAITz) asserted	30		ns
Tv2	Valid time, MCIF_DATA after MCIF_CS_IOz or RDn (MCIF_OEz) deasserted	0		ns
Ten1	Enable time, MCIF_CS_IOz asserted to RDY (MCIF_WAITz) driven		15	ns
Ten2	Enable time, MCIF_CS_IOz and RDn (MCIF_OEz) asserted to MCIF_DATA driven		15	ns
Tdis1	Disable time, RDY (MCIF_WAITz) high impedance after MCIF_CS_IOz deasserted		15	ns
Tdis2	Disable time, MCIF_DATA high impedance after MCIF_CS_IOz or RDn (MCIF_OEz) deasserted		15	ns
Tw1	Access width, MCIF_CS_IOz deasserted to MCIF_CS_IOz asserted	25		ns
Tw2	Access width, RDn (MCIF_OEz) deasserted to RDn (MCIF_OEz) asserted	0		ns



NOTES: A. The timing diagram assumes MCIF signals used their default polarities. The RDY (MCIF_WAITz) defaults to the active low polarity in the MCIF I/O Type-2 M16C mode.

B. The MCIF_STRBz, MCIF_R_nWz and MCIF_BUSCLK inputs are "Don't Care" and the MCIF_ACKz output is not used in the MCIF I/O Type-2 M16C mode.

C. Single 16-bit write accesses are not allowed, resulting in the ExCPUErr interrupt bit being set.

† MCIF_MODE may be changed during device operation but is not recommended. MCIF_MODE should not change during a quadlet access cycle.

‡ MCIF_ENDIAN may change during device operation. It should not change during a quadlet access or data corruption may result.

§ For a write access to occur, both MCIF_CS_IOz and WRn (MCIF_WEz) must be asserted. The WRn (MCIF_WEz) is not required to deassert between accesses.

¶ CFR accesses must be quadlet aligned. The MCIF_ADDR[1] bit is immaterial and the MCIF_ADDR may be of value "N" or "N+2" when considered as a byte address (ADDR[10:0]). MCIF_ADDR[0] is internally grounded. MCIF_ADDR[1] is used in the Memory MCIF mode.

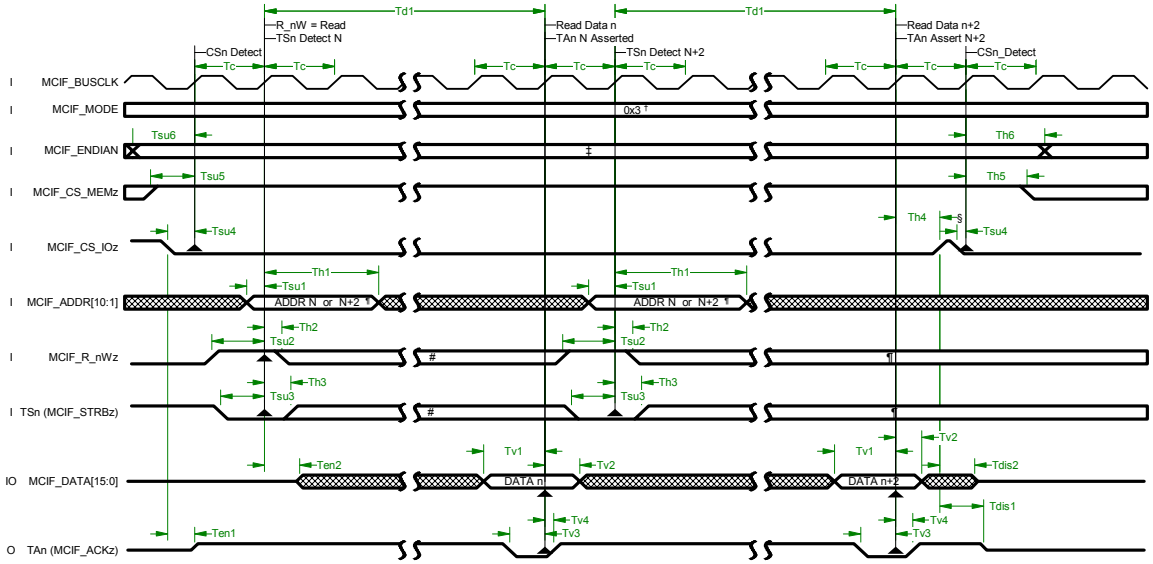
Figure 15. I/O Type-2 M16C SRAM-Like + Wait Write

Table 9. I/O Type-2 M16C SRAM-Like + Wait AC Timing Parameters (Write)

	Description	Min	Max	Units
Tsu1	Setup time, MCIF_ADDR valid before MCIF_CS_IOz asserted	0		ns
Tsu2	Setup time, WRn (MCIF_WEz) asserted before MCIF_CS_IOz asserted	-40		ns
Tsu3	Setup time, MCIF_DATA valid before MCIF_CS_IOz asserted	-40		ns
Tsu4	Setup time, RDn (MCIF_OEz) deasserted before MCIF_CS_IOz asserted	0		ns
Tsu5	Setup time, MCIF_CS_MEMz deasserted before MCIF_CS_IOz asserted	0		ns
Tsu6	Setup time, MCIF_ENDIAN before MCIF_CS_IOz asserted	0		ns
Th1	Hold time, MCIF_ADDR valid after RDY (MCIF_WAITz) asserted	0		ns
Th2	Hold time, WRn (MCIF_WEz) or MCIF_CS_IOz asserted after RDY (MCIF_WAITz) asserted	0		ns
Th3	Hold time, MCIF_DATA valid after RDY (MCIF_WAITz) asserted	0		ns
Th4	Hold time, RDn (MCIF_OEz) deasserted after MCIF_CS_IOz deasserted	0		ns
Th5	Hold time, MCIF_CS_MEMz deasserted after MCIF_CS_IOz deasserted	0		ns
Th6	Hold time, MCIF_ENDIAN after MCIF_CS_IOz deasserted	0		ns
Td1	Delay time, first write access, RDY (MCIF_WAITz) asserted after MCIF_CS_IOz asserted	80	340	ns
Td2	Delay time, second write access, RDY (MCIF_WAITz) asserted after MCIF_CS_IOz asserted	80	340	ns
Ten1	Enable time, MCIF_CS_IOz asserted to RDY (MCIF_WAITz) driven		15	ns
Tdis1	Disable time, RDY (MCIF_WAITz) high impedance after MCIF_CS_IOz deasserted		15	ns
Tw1	Access width, MCIF_CS_IOz deasserted to MCIF_CS_IOz asserted	25		ns
Tw2	Access width, WRn (MCIF_WEz) deasserted to WRn (MCIF_WEz) asserted	0		ns

1.9.4.4 I/O Type-3 MPC850

Supports Motorola MPC850 external bus.



NOTES: A. The timing diagram assumes MCIF signals used their default polarities.

B. MCIF_OEz, MCIF_WEz and MCIF_WAITz are "Don't Care" for the MCIF I/O Type-3 MPC850 mode.

C. Single 16-bit read accesses will not result in an error or an interrupt.

† MCIF_MODE may be changed during device operation but is not recommended. MCIF_MODE should not change during a quadlet access cycle.

‡ MCIF_ENDIAN may change during device operation. It should not change during a quadlet access or data corruption may result.

§ MCIF_CS_IOz may deassert after TAn (MCIF_ACKz) is detected as long as Th5 is met. In synchronous designs it may be better to allow at least one clock period delay between TAn (MCIF_ACKz) detect and the next MCIF_CS_IOz access cycle.

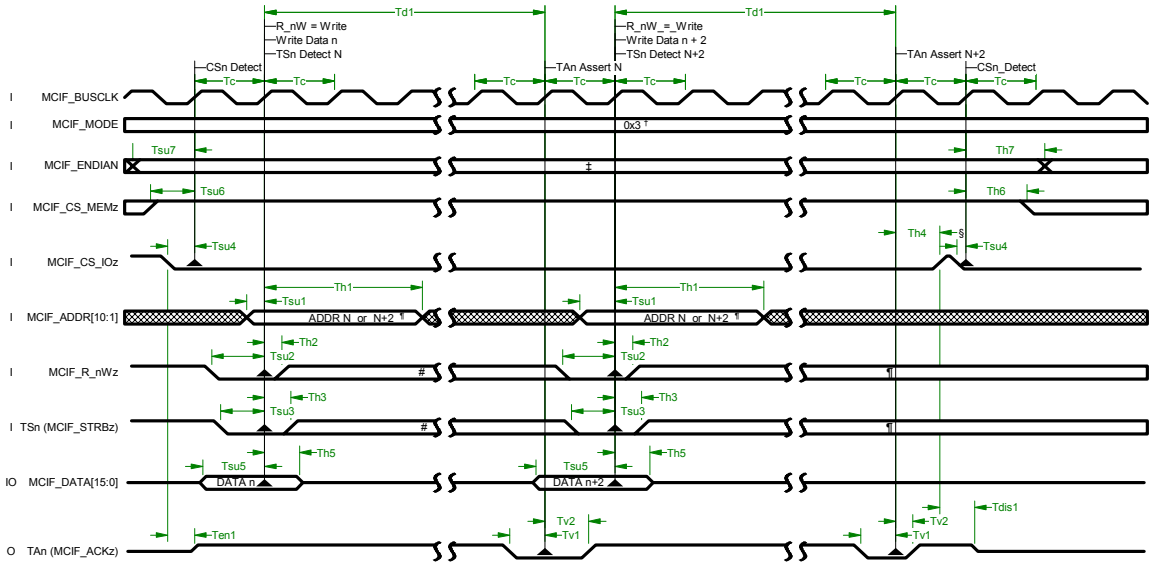
¶ CFR accesses must be quadlet aligned. The MCIF_ADDR[1] bit is immaterial and the MCIF_ADDR may be of value "N" or "N+2" when considered as a byte address (ADDR[10:0]). MCIF_ADDR[0] is internally grounded. MCIF_ADDR[1] is used in the Memory MCIF mode.

MCIF_R_nWz and TSn (MCIF_STRBz) may remain valid / asserted or become invalid /deasserted during the access.

Figure 16. I/O Type-3 MPC850 Read

Table 10. I/O Type-3 MPC850 Read AC Timing Parameters

	Description	Min	Max	Units
Tc	Cycle time, MCIF_BUSCLKz	24		ns
Tsu1	Setup time, MCIF_ADDR valid before MCIF_BUSCLKz rising edge [TSn (MCIF_STRBz) assert cycle]	2		ns
Tsu2	Setup time, MCIF_R_nWz before MCIF_BUSCLKz rising edge [TSn (MCIF_STRBz) assert cycle]	16		ns
Tsu3	Setup time, TSn (MCIF_STRBz) asserted before MCIF_BUSCLKz rising edge	15		ns
Tsu4	Setup time, MCIF_CS_IOz asserted before MCIF_BUSCLKz rising edge	4		ns
Tsu5	Setup time, MCIF_CS_MEMz deasserted before MCIF_BUSCLKz rising edge (MCIF_CS_IOz assert cycle)	4		ns
Tsu6	Setup time, MCIF_ENDIAN before MCIF_BUSCLKz rising edge (MCIF_CS_IOz assert cycle)	4		ns
Th1	Hold time, MCIF_ADDR valid after MCIF_BUSCLKz rising edge [TSn (MCIF_ACKz) assert cycle]	14		ns
Th2	Hold time, MCIF_R_nWz after MCIF_BUSCLKz rising edge [TSn (MCIF_ACKz) assert cycle]	2		ns
Th3	Hold time, TSn (MCIF_STRBz) asserted after MCIF_BUSCLKz rising edge	2		ns
Th4	Hold time, MCIF_CS_IOz asserted after MCIF_BUSCLKz rising edge [TAn (MCIF_ACKz) assert cycle]	14		ns
Th5	Hold time, MCIF_CS_MEMz deasserted after MCIF_BUSCLKz rising edge [MCIF_CS_IOz deassert cycle]	0		ns
Th6	Hold time, MCIF_ENDIAN after MCIF_BUSCLKz rising edge [MCIF_CS_IOz deassert cycle]	0		ns
Td1	Delay time, read access, TSn (MCIF_STRBz) assert cycle to TAn (MCIF_ACKz) assert cycle		150	ns
Tv1	Valid time, MCIF_DATA before MCIF_BUSCLKz rising edge [TAn (MCIF_ACKz) asserted cycle]	10		ns
Tv2	Valid time, MCIF_DATA after MCIF_BUSCLKz rising edge [TAn (MCIF_ACKz) asserted cycle]	2		ns
Tv3	Valid time, TAn (MCIF_ACKz) asserted before MCIF_BUSCLKz rising edge	11		ns
Tv4	Valid time, TAn (MCIF_ACKz) asserted after MCIF_BUSCLKz rising edge	0		ns
Ten1	Enable time, MCIF_CS_IOz asserted to TAn (MCIF_ACKz) driven		15	ns
Ten2	Enable time, MCIF_BUSCLKz rising edge to MCIF_DATA driven [TSn (MCIF_ACKz) assert cycle]		15	ns
Tdis1	Disable time, TAn (MCIF_ACKz) high impedance after MCIF_CS_IOz deasserted		15	ns
Tdis2	Disable time, MCIF_DATA high impedance after MCIF_CS_IOz deasserted		15	ns



NOTES: A. The timing diagram assumes MCIF signals used their default polarities.

B. MCIF_OEz, MCIF_WEz and MCIF_WAITz are "Don't Care" for the MCIF I/O Type-3 MPC850 mode.

C. Single 16-bit write accesses are not allowed, resulting in the ExCPUErr interrupt bit being set.

† MCIF_MODE may be changed during device operation but is not recommended. MCIF_MODE should not change during a quadlet access cycle.

‡ MCIF_ENDIAN may change during device operation. It should not change during a quadlet access or data corruption may result.

§ MCIF_CS_IOz may deassert after TAn (MCIF_ACKz) is detected as long as Th5 is met. In synchronous designs it may be better to allow at least one clock period delay between TAn (MCIF_ACKz) detect and the next MCIF_CS_IOz access cycle.

¶ CFR accesses must be quadlet aligned. The MCIF_ADDR[1] bit is immaterial and the MCIF_ADDR may be of value "N" or "N+2" when considered as a byte address (ADDR[10:0]). MCIF_ADDR[0] is internally grounded. MCIF_ADDR[1] is used in the Memory MCIF mode.

MCIF_R_nWz and TSn (MCIF_STRBz) may remain valid / asserted or become invalid /deasserted during the access.

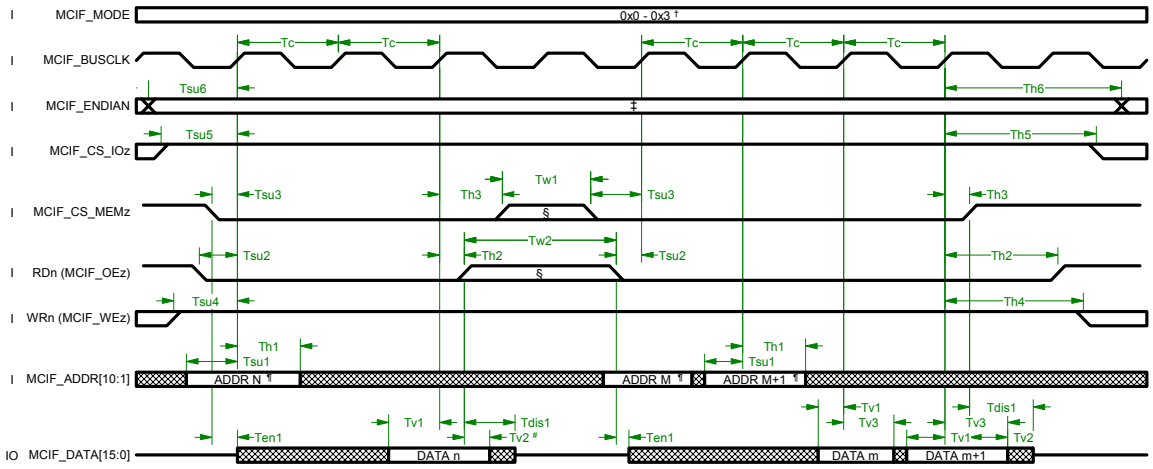
Figure 17. I/O Type-3 MPC850 Write

Table 11. I/O Type-3 MPC850 Write AC Timing Parameters

	Description	Min	Max	Units
Tsu1	Setup time, MCIF_ADDR valid before MCIF_BUSCLKz rising edge [TSn (MCIF_STRBz) assert cycle]	2		ns
Tsu2	Setup time, MCIF_R_nWz before MCIF_BUSCLKz rising edge [TSn (MCIF_STRBz) assert cycle]	16		ns
Tsu3	Setup time, TSn (MCIF_STRBz) asserted before MCIF_BUSCLKz rising edge	15		ns
Tsu4	Setup time, MCIF_CS_IOz asserted before MCIF_BUSCLKz rising edge	4		ns
Tsu5	Setup time, MCIF_DATA valid before MCIF_BUSCLKz rising edge [TSn (MCIF_ACKz) assert cycle]	16		ns
Tsu6	Setup time, MCIF_CS_MEMz deasserted before MCIF_BUSCLKz rising edge (MCIF_CS_IOz assert cycle)	4		ns
Tsu7	Setup time, MCIF_ENDIAN before MCIF_BUSCLKz rising edge (MCIF_CS_IOz assert cycle)	4		ns
Th1	Hold time, MCIF_ADDR valid after MCIF_BUSCLKz rising edge [TSn (MCIF_ACKz) assert cycle]	14		ns
Th2	Hold time, TSn (MCIF_STRBz) asserted after MCIF_BUSCLKz rising edge	2		ns
Th3	Hold time, TAn (MCIF_ACKz) asserted after MCIF_BUSCLKz rising edge	0		ns
Th4	Hold time, MCIF_CS_IOz asserted after MCIF_BUSCLKz rising edge [TAn (MCIF_ACKz) assert cycle]	14		ns
Th5	Hold time, MCIF_DATA valid after MCIF_BUSCLKz rising edge [TSn (MCIF_ACKz) assert cycle]	2		ns
Th6	Hold time, MCIF_CS_MEMz deasserted after MCIF_BUSCLKz rising edge [MCIF_CS_IOz deassert cycle]	0		ns
Th7	Delay time, read access, TSn (MCIF_STRBz) assert cycle to TAn (MCIF_ACKz) assert cycle	0		ns
Td1	Delay time, read access, TSn (MCIF_STRBz) assert cycle to TAn (MCIF_ACKz) assert cycle		130	ns
Tv1	Valid time, TAn (MCIF_ACKz) asserted before MCIF_BUSCLKz rising edge	11		ns
Tv2	Valid time, TAn (MCIF_ACKz) asserted after MCIF_BUSCLKz rising edge	2		ns
Ten1	Enable time, MCIF_BUSCLKz rising edge to TAn (MCIF_ACKz) driven (MCIF_CS_IOz assert cycle)		15	ns
Tdis1	Disable time, TAn (MCIF_ACKz) high impedance after MCIF_BUSCLKz rising edge (MCIF_CS_IOz deassert cycle)		15	ns

1.9.4.5 Memory Type

All ex-CPU modes (Type-0 (68K) and Type-2 (M16C/62)) use the same timing for memory access. The ex-CPU provides the bus clock (MCIF_BUSCLKz) in all modes.



NOTES: A. The timing diagram assumes MCIF signals used their default polarities.

B. The MCIF_STRBz and MCIF_R_nWz inputs are "Don't Care". The MCIF_ACKz and MCIF_WAITz outputs are not used in the MCIF Memory Access mode.

C. Single 16-bit read accesses will not result in an error or an interrupt.

D. MCIF Memory Mode read access latency is two clock cycles.

† MCIF_MODE may be changed during device operation but is not recommended. MCIF_MODE should not change during an MCIF Memory Access cycle. Memory accesses may only occur if MCIF_MODE is valid (0x0 through 0x3).

‡ MCIF_ENDIAN may change during device operation. It should not change during an access or data corruption may result.

§ For a read access to occur, both MCIF_CS_MEMz and RDn (MCIF_OEz) must be asserted. The MCIF_CS_MEMz and RDn (MCIF_OEz) are not required to deassert between accesses.

¶ Memory accesses are not required to be quadlet aligned. The MCIF_ADDR[1] bit is used along with the MCIF_ENDIAN to determine which 16-bit word is read. Addressing should be considered as byte addressing (ADDR[10:0]) with MCIF_ADDR[0] internally grounded.

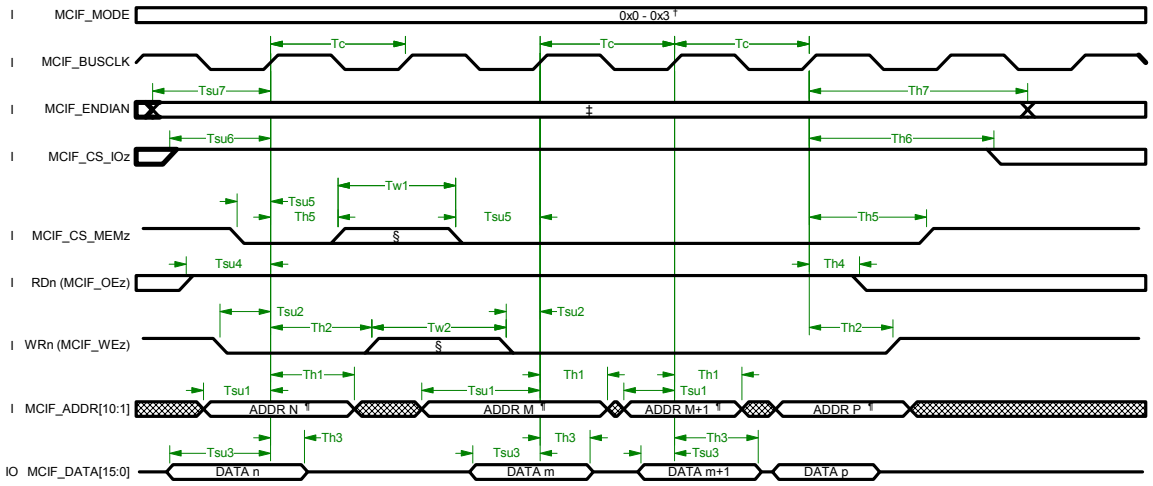
Valid time Tv2 is from MCIF_CS_MEMz or RDn (MCIF_OEz), whichever deasserts first in the access.

Figure 18. Memory Type

Table 12. Memory Type Read AC Timing Parameters

	Description	Min	Max	Units
Tc	Cycle time, MCIF_BUSCLKz [Assume 20-pF loading]	8.33	142.86	ns
Tsu1	Setup time, MCIF_ADDR valid before MCIF_BUSCLKz rising edge (MCIF_CS_MEMz assert cycle)	8		ns
Tsu2	Setup time, RDn (MCIF_OEz) asserted before MCIF_BUSCLKz rising edge (MCIF_CS_MEMz assert cycle)	8		ns
Tsu3	Setup time, MCIF_CS_MEMz asserted before MCIF_BUSCLKz rising edge	8		ns
Tsu4	Setup time, WRn (MCIF_WEz) deasserted before MCIF_BUSCLKz rising edge (MCIF_CS_MEMz assert cycle)	8		ns
Tsu5	Setup time, MCIF_CS_IOz deasserted before MCIF_BUSCLKz rising edge (MCIF_CS_MEMz assert cycle)	8		ns
Tsu6	Setup time, MCIF_ENDIAN before MCIF_BUSCLKz rising edge (MCIF_CS_MEMz assert cycle)	8		ns
Th1	Hold time, MCIF_ADDR valid after MCIF_BUSCLKz rising edge (MCIF_CS_MEMz assert cycle)	0		ns
Th2	Hold time, RDn (MCIF_OEz) asserted after MCIF_BUSCLKz rising edge (data read cycle)	0		ns
Th3	Hold time, MCIF_CS_MEMz asserted after MCIF_BUSCLKz rising edge (data read cycle)	0		ns
Th4	Hold time, WRn (MCIF_WEz) deasserted after MCIF_BUSCLKz rising edge (data read cycle)	0		ns
Th5	Hold time, MCIF_CS_IOz deasserted after MCIF_BUSCLKz rising edge (data read cycle)	0		ns
Th6	Hold time, MCIF_ENDIAN after MCIF_BUSCLKz rising edge (data read cycle)	0		ns
Tv1	Valid time, MCIF_DATA before MCIF_BUSCLKz rising edge (data read cycle)	8		ns
Tv2	Valid time, MCIF_DATA after MCIF_CS_MEMz or RDn (MCIF_OEz) deasserted	8		ns
Tv3	Valid time, MCIF_DATA after MCIF_BUSCLKz rising edge (data read cycle)	2		ns
Ten1	Enable time, MCIF_CS_MEMz and RDn (MCIF_OEz) asserted to MCIF_DATA driven		15	ns
Tdis1	Disable time, MCIF_DATA high impedance after MCIF_CS_MEMz deasserted		15	ns
Tw1	Access width, MCIF_CS_MEMz deasserted to MCIF_CS_MEMz asserted	0		ns
Tw2	Access width, RDn (MCIF_OEz) deasserted to RDn (MCIF_OEz) asserted	0		ns

Note: Measurements are based on a 20-pF loading.



NOTES: A. The timing diagram assumes MCIF signals used their default polarities.

B. The MCIF_STRBz and MCIF_R_nWz inputs are "Don't Care". The MCIF_ACKz and MCIF_WAITz outputs are not used in the MCIF Memory Access mode.

C. Single 16-bit write accesses are allowed and will not result in an error or an interrupt.

D. MCIF Memory Mode write access latency is zero clock cycles.

† MCIF_MODE may be changed during device operation but is not recommended. MCIF_MODE should not change during an MCIF Memory Access cycle. Memory accesses may only occur if MCIF_MODE is valid (0x0 through 0x3).

‡ MCIF_ENDIAN may change during device operation. It should not change during an access or data corruption may result.

§ For a write access to occur, both MCIF_CS_MEMz and WRn (MCIF_WEz) must be asserted. The MCIF_CS_MEMz and WRn (MCIF_WEz) are not required to deassert between accesses.

¶ Memory accesses are not required to be quadlet aligned. The MCIF_ADDR[1] bit is used along with the MCIF_ENDIAN to determine which 16-bit word is written. Addressing should be considered as byte addressing (ADDR[10:0]) with MCIF_ADDR[0] internally grounded.

Figure 19. Memory Write

Table 13. Memory Type Write AC Timing Parameters

	Description	Min	Max	Units
Tsu1	Setup time, MCIF_ADDR valid before MCIF_BUSCLKz rising edge	8		ns
Tsu2	Setup time, WRn (MCIF_WEz) asserted before MCIF_BUSCLKz rising edge	8		ns
Tsu3	Setup time, MCIF_DATA valid before MCIF_BUSCLKz rising edge	8		ns
Tsu4	Setup time, RDn (MCIF_OEz) deasserted before MCIF_BUSCLKz rising edge (data write cycle)	8		ns
Tsu5	Setup time, MCIF_CS_MEMz asserted before MCIF_BUSCLKz rising edge	8		ns
Tsu6	Setup time, MCIF_CS_IOz deasserted before MCIF_BUSCLKz rising edge (data write cycle)	8		ns
Tsu7	Setup time, MCIF_ENDIAN before MCIF_BUSCLKz rising edge (data write cycle)	8		ns
Th1	Hold time, MCIF_ADDR valid after MCIF_BUSCLKz rising edge	0		ns
Th2	Hold time, WRn (MCIF_WEz) asserted after MCIF_BUSCLKz rising edge	0		ns
Th3	Hold time, MCIF_DATA valid after MCIF_BUSCLKz rising edge	0		ns
Th4	Hold time, RDn (MCIF_OEz) deasserted after MCIF_BUSCLKz rising edge (data write cycle)	0		ns
Th5	Hold time, MCIF_CS_MEMz asserted after MCIF_BUSCLKz rising edge (data write cycle)	0		ns
Th6	Hold time, MCIF_CS_IOz deasserted after MCIF_BUSCLKz rising edge (data write cycle)	0		ns
Th7	Hold time, MCIF_ENDIAN after MCIF_BUSCLKz rising edge (data write cycle)	0		ns
Tw1	Access width, MCIF_CS_MEMz deasserted to MCIF_CS_MEMz asserted	0		ns
Tw2	Access width, WRn (MCIF_WEz) deasserted to WRn (MCIF_WEz) asserted	0		ns

Note: Measurements are based on a 20-pF loading.

1.9.5 LEB Encryption

The external CPU interface contains an option for encryption. The encryption protects DTLA key transfer over the external CPU interface. The parallel external CPU mode uses this method.

1) The external CPU starts the program load to the iceLynx-Micro. The code is loaded starting at address 0h. The first two quadlets have encryption information. The other quadlets are the encrypted download program (up to 256K bytes). The program code must always contain these two header quadlets, even if the data is not encrypted. The C bits indicate if data must be decrypted.

The first two quadlets have the following format:

Table 14. Ex-CPU Encryption First Quadlet

31 29	28 24	23 0
C	Key No	Key Seed
Key Seed		

2) The iceLynx-Micro uses the values in the first quadlet to determine how to decrypt the data.

Table 15. Ex-CPU Encryption Reference

Field	Description	Purpose	
C	Three bit encryption indicator	Indicates encryption mode. Values from 000 to 111 are valid. If value is 111, the hardware stops LEB decryption. The program is loaded to program memory without being decrypted. If value is any other than 111, the hardware performs LEB decryption on the data loaded into program memory.	
Key No	Key Number (see Note 1)	Used to indicate which 56-bit key the iceLynx-Micro uses for LEB decryption. The keys are available in a Device Key ROM table. There are 32 separate 56-bit entries. Each key corresponds to a specific Key No.	
		Key No	Single LEB
		0	AAAA AAAA AAAA AA
		1	BBBB BBBB BBBB BB
		2	CCCC CCCC CCCC CC
		31	6666 6666 6666 66
Key Seed	Seed value provided by ex-CPU	This 56-bit number is used as an input to the Single LEB decryption hardware.	

Note 1: Contact Texas Instruments for actual key numbers and key data.

3) LEB decryption hardware

An XOR operation is performed on the Key Seed provided by the ex-CPU and the Device Key (selected from the Device Key ROM table by Key No). If the C values are any value except 111, the hardware decrypts the program code.

The maximum throughput for the program load using LEB is 20 Mbytes per second.

1.10 Integrated CPU

1.10.1 Description/Overview

The iceLynx-Micro has an integrated ARM7TDMI processor. The operating frequency is 50 MHz. The processor is intended to handle all 1394 transactions as well as DTCP related software. It operates in 16-bit mode in addition to 32-bit mode.

Access to CFRs requires three clock cycles for reads and writes. All other internal memory locations are accessed in a single cycle.

1.10.2 Interaction With External CPU

Only one CPU (internal or external) can access memory locations at one time. This includes configuration registers and FIFOs. The integrated CPU has access to program memory and communication memory in byte mode, 16-bit mode, or 32-bit mode. The external CPU has priority over the internal CPU. While the ex-CPU performs a memory access (2x1024-byte RAMs), the ARM can use the internal bus freely.

1.10.3 External Interrupts

The GPIO pins are configured as IRQ and/or FIQ interrupts used to signal interrupts for the ARM. GPIO pins can also be configured as other types of interrupts as specified in GPIOIntCfg CFR. General-purpose interrupts can also be used for communication between the internal and external processors. These interrupts are available in InCPUComInt and ExCPUComInt CFRs.

1.10.4 Timer

The iceLynx-Micro has three general timers. One of these timers, Timer2, is configured as the watchdog timer. The WTCH_DG_TMRn (watchdog timer output) port detects any internal ARM software failure. If the watchdog timer expires, hardware sets WTCH_DG_TMRn = low, Low_Pwr_Rdy = low.

The value for CFR and output are as follows:

- Low_Pwr_Rdy = low (hardware sets)
- WTCH_DG_TMRn = low (hardware sets)
- HPS = high (external application sets)
- LPS = high
- RESET_ARMn = low (external application sets)
- PHYNoticeEn = high or low
- The following describes the WTCH_DG_TMRn behavior whenever PinCfg.WtchDgTmrN is set to 0. The WTCH_DG_TMRn pin reflects the value of Timer2.Enable.

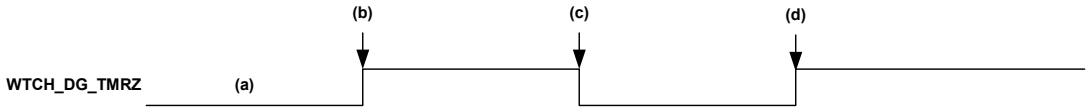


Figure 20. Watchdog Timer Waveform

At phase (a), the iceLynx-Micro is in the power-up stage. The ARM has not been programmed and is not operating. Sys.Timer2.Enable bit is 0, and the WTCH_DG_TMRn pin is asserted (low).

At phase (b), the iceLynx-Micro is in the active stage. The ARM is executing code and has set Sys.Timer2.Enable = 1. The ARM clears the Timer2 counter by periodically writing a 1 to Sys.Timer2.Enable bit to keep Sys.Timer2.Counter from equaling Sys.Timer2.Period. The WTCH_DG_TMRn pin reflects the status of Sys.Timer2.Enable and is deasserted (high).

At phase (c), the iceLynx-Micro is still in the active stage. However, the ARM has failed to clear the Timer2 counter in time. Sys.Timer2.Counter = Sys.Timer2.Period. At this point, iceLynx-Micro hardware clears Sys.Timer2.Enable. The WTCH_DG_TMRn pin is asserted (low). If Sys.Timer2.RstInCPU == 1, the ARM gets a reset. The Sys.*CPUInt.Timer2 interrupt indicates what happened to the ARM after it comes out of reset.

The system decides to perform a device reset and reload program code according to system conditions.

At phase (d), the ARM (or Ex-CPU) has set Sys.Timer2.Enable == 1. The WTCH_DG_TMRn signal is deasserted (goes high).

Note: WTCH_DG_TMRn function is independent of Sys.InCPUCfg.Reset function. If the ARM is placed in reset by setting Sys.InCPUCfg.Reset = 1, WTCH_DG_TMRn is still active as long as Sys.Timer2.Enable = 1.

1.11 High Speed Data Interface

1.11.1 Overview/Description

The high speed data interface (HSDI) is used for transmitting and receiving high-speed video data. The HSDI is connected to the isochronous buffers. HSDI0 is connected to ISO FIFO 0 and HSDI1 is connected to ISO FIFO 1. The HSDI ports can be configured as transmit or receive. A single port cannot transmit and receive at the same time. The buffer direction, HSDI mode, and stream type are all set by CFR. See Table 16 for a description of the HSDI signals.

Table 16. HSDI Signals

Signal	Polarity	Tx Direction	Rx Direction	Description
HSDI*_CLK	Programmable Defaults to rising edge	Input	Input	All activity on HSDI uses this clock. The clock must be always provided by an external codec in read and write mode *except* for TX mode 3. In TX mode 3, the clock is only available during data transmit.
HSDI*_EN	Programmable Defaults to active low	Input	Input	Enables the HSDI interface. This signal must be enabled all the time by tying it low or high for modes that do not provide an enable signal.
HSDI*_SYNC (See Note1)	Programmable Defaults to active high	Input	Output	HSDI*_SYNC indicates the start of the packet. The rising edge (or falling edge, depending on polarity setting) of this signal indicates first byte of data. An internal packet counter[note2] keeps track of the packet end. For TX operations of all data types, the packet counter must be programmed by software in HSDI*Cfg.TxDatBlkSz. On TX operation, the width of the HSDI*_SYNC pulse can vary. On RX operation, HSDI*_SYNC is an output from iceLynx-Micro. It is the width of one HSDI*_CLK cycle. For DVB TX, if the application chooses to use the modes that do not provide the HSDI*_Sync signal, the frame sync detection circuitry must be enabled by setting HSDI*Cfg.FrmSyncDetEn = 1.
HSDI*_AV	Programmable Defaults to active low	Output for HSDI TX modes 8 and 9 (DV)	Output	Indicates data is available in FIFO for reading. For MPEG2 RX, data is available once SPH=cycle timer (timestamp). For DV, data is available once the entire 480-byte cell has been received into the FIFO. For HSDI TX modes 8 and 9, it indicates the number of quadlets in the TX ISO buffer is over the programmed limit. The limit is programmed at CFR.
HSDI*_Data		Input	Output	Byte wide data bus. HSDI*_D7 is MSB. For serial mode, only HSDI*_D0 is used.
HSDI*_DVALID HSDI*_FrameSync	Programmable Defaults to active high	Input	Output	For transmit, this signal is input and indicates data is valid and is written to TX ISO buffer. For receive, this signal is output and indicates data is valid on HSDI. On RX operation, this signal is not deasserted for back to back packets. In DV I/F mode (HSDI TX mode 9, RX mode 4), HSDI*_DVALID is used as HSDI*_FrameSync.

Notes:

1) HSDI*SYNC
Data on HSDI is ignored until the HSDI*_SYNC signal is detected. In frame sync detection mode, data is ignored until the SyncLock event occurs.

The SyncLock event is signaled by an interrupt in CFR-Iso*CPUInt.SyncLock when the HSDI*_Sync signal is activated as programmed in CFR–or in frame sync detection mode when the MPEG2-DVB synchronization byte 0x47 are detected 188 bytes apart.

The Iso*TxCfg.SyncLock status bit is also asserted. The Iso*TxCfg.SyncLock status bit stays asserted until a Sync violation event occurs. If a sync violation occurs (such as a synchronization byte occurs too soon or too late), the Iso*InCPUInt.SyncUnlock interrupt occurs and the current packet is flushed.

2) Packet Counter
Once the HSDI*_SYNC edge or SyncLock event is detected, the counter starts. The packet is written into the FIFO once the counter value is reached. Data on the HSDI is ignored until the next HSDI*_SYNC or SyncLock event when the frame sync detection circuitry is enabled. If another HSDI*_SYNC occurs before the end of the counter, the packet is aborted. More details on the frame sync detection circuit provided in Section 1.12.2. Table 17 shows the counter values to be programmed for the applications shown below:

Table 17. Application Counter Values

Application	Counter Value
MPEG2-DVB	188 bytes
MPEG2-DSS-130	130 bytes
MPEG2-DSS-140	140 bytes
DV-SD	480 bytes

1.11.2 Frame Sync Detection Circuit

The iceLynx-Micro supports the frame sync detection feature for MPEG2-DVB applications that do not provide a sync signal (=byte start) to the HSDI. It is enabled in CFR using HSDI*Cfg.FrmSyncDetEn. The frame detection circuit looks for the MPEG2-DVB transport stream synchronization byte, (0x47). The iceLynx-Micro detects synchronization bytes that are 188 bytes apart and signal a SyncLock event. The number of sync bytes detected for a lock condition is programmable in HSDICfg.SyncLockDetNum (the range is 2-7).

For example, if HSDICfg.SyncLockDetNum is set to 2, the iceLynx-Micro searches for two synchronization bytes 188 bytes apart. The second synchronization byte must be marked as start of packet and assert the Iso*CPUInt.SyncLock Interrupt. The first packet is confirmed into the TX FIFO when the second synchronization byte is detected. Otherwise, the first packet is flushed from the FIFO. After the last byte is input to HSDI (188^{th} byte), the iceLynx-Micro does not capture any packet data until the next MPEG2 transport stream synchronization byte.

Note: The frame sync detection circuit can only be used for MPEG2-DVB (188-byte) data.

1.11.3 HSDI Pass-Through Function

This function is enable/disabled by a CFR setting (HSDI*Cfg.PassThru). Both the HSDI0 and HSDI1 ports support the data pass-through function in accordance with the following conditions:

- The MPEG2-TS data for HSDI TX modes 1-7.
- The pass through direction is input to HSDI0 and output HSDI1.

1. In this case, HSDI*Cfg.PassThru and Iso*Cfg.Enable must both be set. The DVD MPEG2-TS data is transmitted to 1394 as well as passed through to HSDI1. The audio interface, which uses ISO PATH1 (data buffer 1), can also be used at the same time.
2. The direction is only HSDI0->HSDI1 available.
3. When the data pass through function is enabled, the signals shown in Table 18 are handled.

Table 18. HSDI Pass-Through Function

HSDI0 -> HSDI1				
Signal Name of HSDI0	**I/O**	**Direction**	**Signal Name of HSDI1**	**I/O**
Data CLK	I	->	Data CLK	O
SYNC	I	->	SYNC	O
Data valid	I	->	Data Valid	O

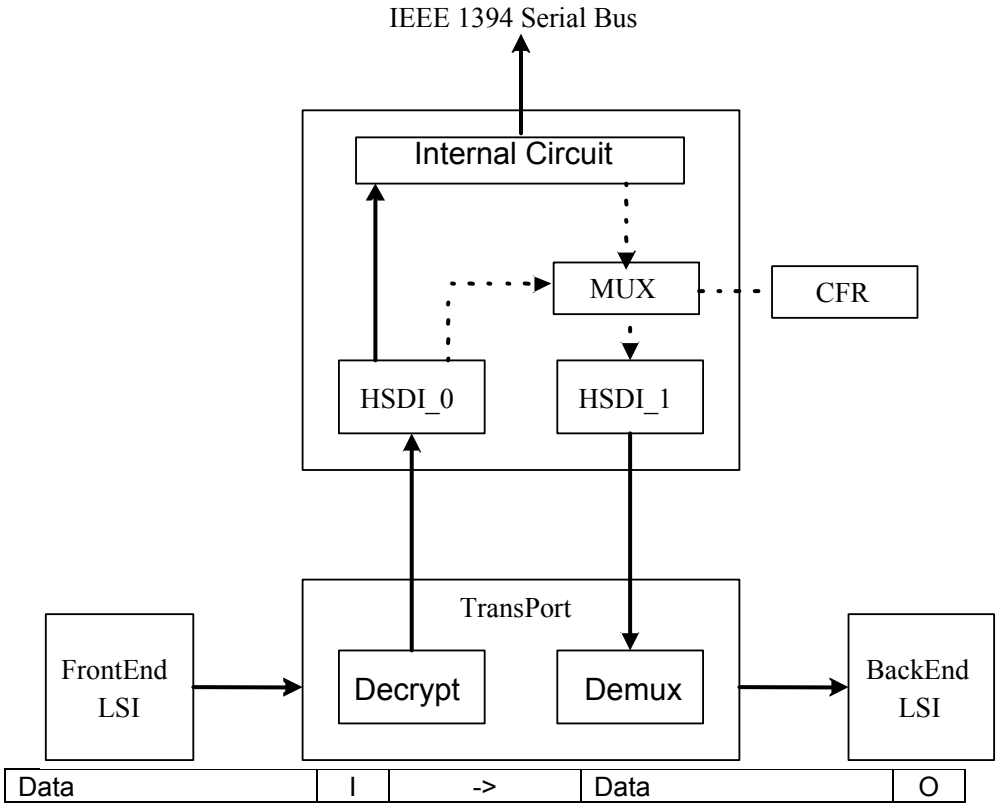


Figure 21. Example for Data Pass-Through Function

1.11.4 HSDI Maximum Clock Rates and Throughput

See Table 19 for the maximum clock rates and throughput on the HSDI interface.

Table 19. HSDI Maximum Clock Rates and Throughput

HSDI Format	Maximum Clock Rate	Maximum Throughput
Serial	70 MHz	8.75 Mbytes/sec
Parallel	27 MHz	27 Mbytes/sec

1.11.5 HSDI Mode Settings

The HSDI modes, for both transmit and receive, are set by CFR bits (HSDI*Cfg.Mode) as shown below. See Table 20 for general mode settings.

Table 20. General HSDI Mode Settings

Mode Setting At HSDI*Cfg.Mode	Description
Video Modes	
0000b	Serial video burst I/F (MPEG2, DSS)
0001b	Serial video burst I/F (MPEG2, DSS) clock active only when data is valid
0010b	Parallel fideo burst I/F (MPEG2, DSS)
0011b	MPEG2 I/F mode
0100b	DV I/F mode
Audio Modes	
0101b	60958 interface
	For HSDI0, uses HSDI0_AMCLK_IN and HSDI0_60958_IN signals. For transmit only.
	For HSDI1, uses HSDI1_AMCLK_IN and HSDI1_60958_IN for transmit. Uses HSDI1_AMCLK_OUT and HSDI1_60958_OUT for receive.
0110b	60958 data with MLPCM Interface
	For HSDI0, uses DVD-Audio-In pins muxed on HSDI0 interface (D0 only). For transmit only.
	For HSDI1, uses DVD-Audio I/F for receive only, defined as: MLPCM_BCLK MLPCM_LRCLK MLPCM_D0
0111b	MLPCM I/F
	For HSDI0, uses DVD-Audio-In pins muxed on HSDI0 interface. For transmit only.
	For HSDI1, uses DVD-Audio I/F for transmit and receive defined as: MLPCM_BCLK MLPCM_LRCLK MLPCM_D0-D2 MLPCM_A
1000b	SACD I/F
	For HSDI0, there is no SACD I/F.
	For HSDI1, uses SACD-IN and SACD-OUT signal multiplexed on HSDI1 signals. For flow control mode, uses DVD-Audio I/F signals.

Other bits also determine the HSDI operations. Table 21 summarizes all HSDI video modes available in the iceLynx-micro.

Table 21. HSDI Video Modes

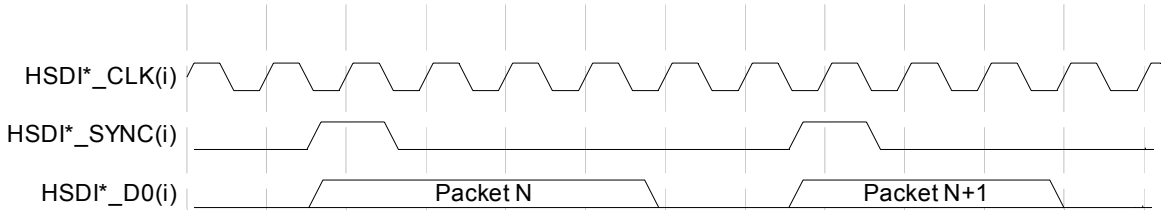
HSDI*Cfg.Mode Setting	HSDI*.FrmSyncDetEn Setting	HSDI*.ValidEn Setting	Corresponding Transmit Modes (see Timing Diagrams in Section 1.12.6)	Corresponding Receive Modes (see Timing Diagrams in Section 1.12.7)	Description
0000	0	0	TX mode 1	None	Serial video burst I/F (MPEG2, DSS)
0000	1	0	TX mode 2	None	Serial video burst I/F (MPEG2, DSS) with frame sync detect circuit
0000	0	1	TX mode 4	RX mode 1	Serial video burst I/F (MPEG2, DSS) with data valid signal
0001	1	0	TX mode 3	--none**--	Serial video burst I/F (MPEG2-DVB) clock active only when data is valid
0010	0	0	TX mode 5	None	Parallel video burst I/F (MPEG2, DSS)
0010	1	1	TX mode 6	None	Parallel video burst I/F (MPEG2-DVB) with frame sync detect circuit
0010	0	1	TX mode 7	RX mode 2	Parallel video burst I/F (MPEG2, DSS) with data valid signal
0011	0	0	TX mode 8	RX mode 3	MPEG2 I/F mode
0100	0	NA (see Note 1)	TX mode 9	RX mode 4	DV I/F mode

Note 1: DV I/F mode (TX mode 9, RX mode 4).

1.11.6 HSDI Transmit Modes

The following MPEG2-TS and DV write function timing diagrams are with the polarity of data CLK, sync, data valid, HSDI*_FrameSync, enable, and available signals at their default setting.

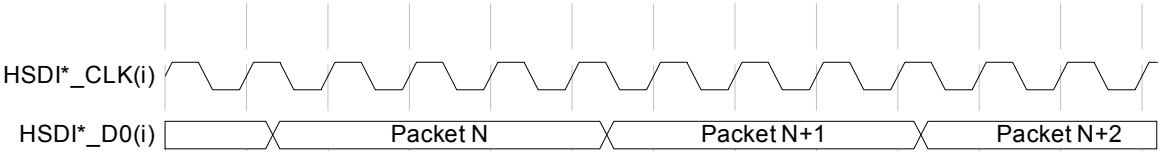
1.11.6.1 TX Mode 1: Serial Burst I/F (MPEG2)



Notes:
1. HSDI*_EN must be pulled low for this mode (HSDI*_EN defaults to active low).
2. HSDI*_DVALID is a don't care for this mode. It is pulled low.

Figure 22. MPEG2 Serial Burst I/F (TX Mode 1)

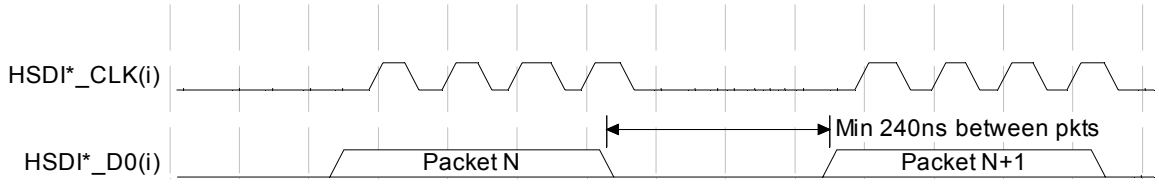
1.11.6.2 TX Mode 2: Serial Video Burst I/F (MPEG2) With Frame Sync Detect Circuit



Notes:
1. HSDI*_EN must be pulled low for this mode (HSDI*_EN defaults to active low).
2. HSDI*_DVALID is a don't care for this mode. It is pulled low.

Figure 23. MPEG2 Serial Video Burst I/F With Frame Sync Detect Circuit (TX Mode 2)

1.11.6.3 TX Mode 3: Serial Video Burst I/F (MPEG2) Clock Active Only When Data Is Valid

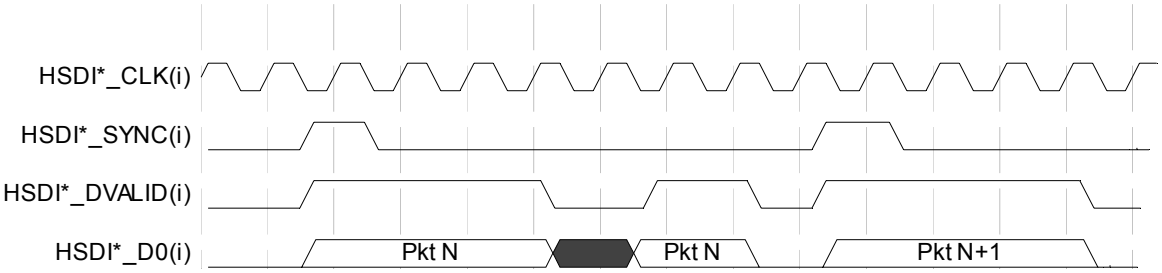


Notes:

1. HSDI*_EN must be pulled low for this mode (HSDI*_EN defaults to active low) and stay active at all times. HSDI*_EN must not be toggled.
2. HSDI*_DVAILD is a don't care for this mode. It is pulled low.
3. Frame sync detect circuit is used.

Figure 24. MPEG2 Serial Video Burst I/F Clock Active Only When Data Is Valid (TX Mode 3)

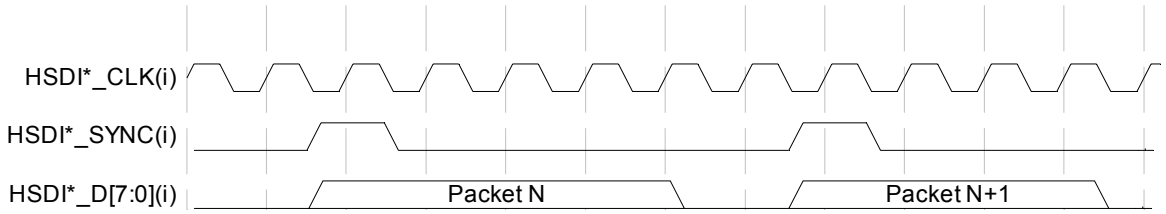
1.11.6.4 TX Mode 4: Serial Video Burst I/F (MPEG2) With Data Valid



Note: HSDI*_EN must be pulled low for this mode (HSDI*_EN defaults to active low).

Figure 25. MPEG2 Serial Video Burst I/F With Data Valid (TX Mode 4)

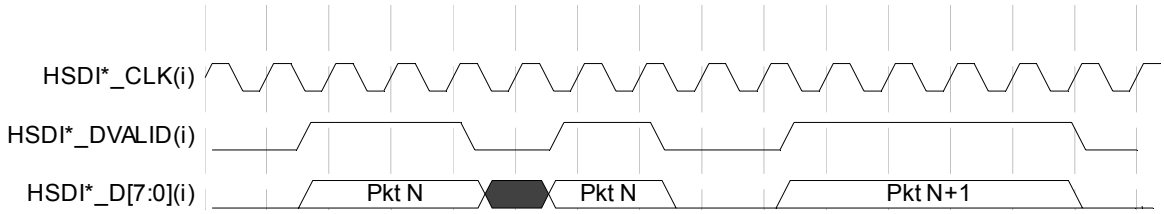
1.11.6.5 TX Mode 5: Parallel Burst Video I/F (MPEG2)



Notes:
1. HSDI*_EN must be pulled low for this mode (HSDI*_EN defaults to active low).
2. HSDI*_DVALID is a don't care for this mode. It is pulled low.

Figure 26. MPEG2 Parallel Burst Video I/F (TX Mode 5)

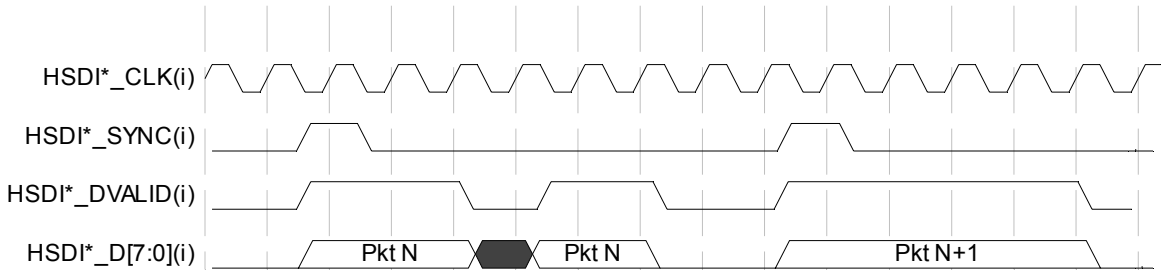
1.11.6.6 TX Mode 6: Parallel Video Burst I/F (MPEG2) With Frame Sync Detect Circuit



Note: HSDI*_EN must be pulled low for this mode (HSDI*_EN defaults to active low).

Figure 27. MEPG2 Parallel Video Burst I/F With Frame Sync Detect Circuit (TX Mode 6)

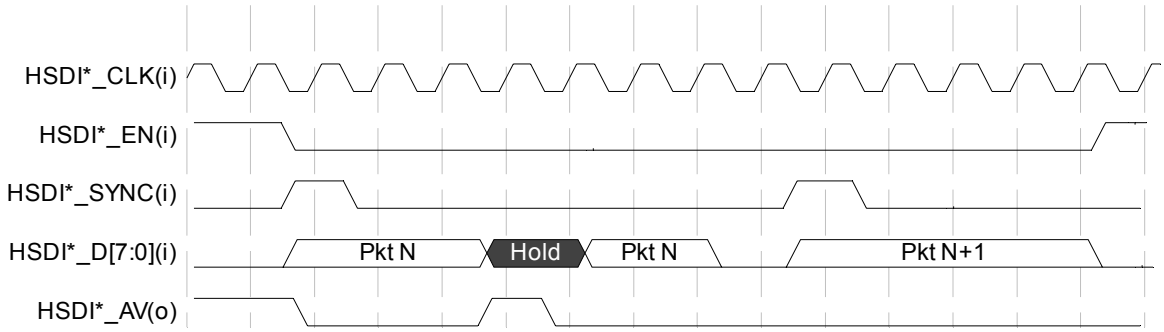
1.11.6.7 TX Mode 7: Parallel Video Burst I/F (MPEG2) With Data Valid



Note: HSDI*_EN must be pulled low for this mode (HSDI*_EN defaults to active low).

Figure 28. MPEG2 Parallel Video Burst I/F With Data Valid (TX Mode 7)

1.11.6.8 TX Mode 8: MPEG2 I/F Mode

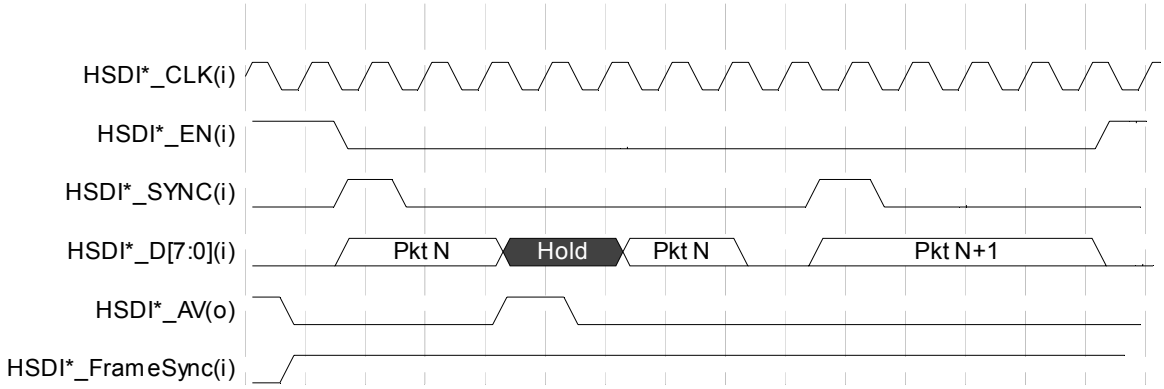


Note:

1. HSDI*_DVALID is a don't care for this mode. It is pulled low.
2. HSDI*_AV is an output in this mode. It indicates if the number of quadlets in the ISO transmit buffer is over a programmed limit. The watermark control must be programmed for the watermark high. If Iso*WtrMrk.HSDIAvailEn is set to 1, the limit is programmed in Iso*WtrMrk.Level0. The watermark must be programmed less than BUFFER SIZE – (packet length + packet header).

Figure 29. MPEG2 I/F (TX Mode 8)

1.11.6.9 TX Mode 9: DV I/F Mode



Notes:

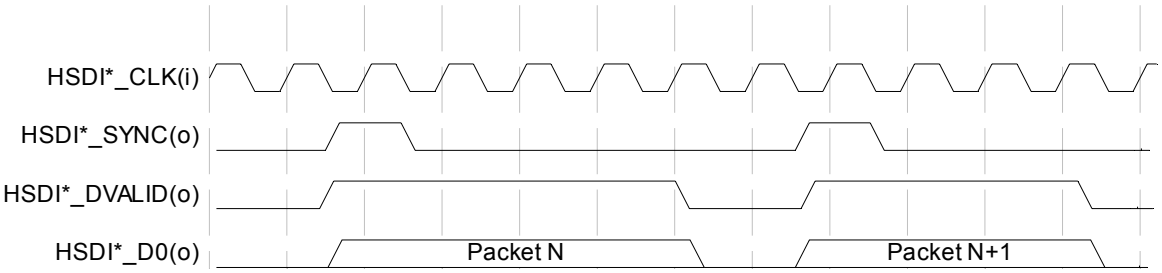
1. The HSDI*_FrameSync signal and SYT circuit are independent of the HSDI*Data [7:0].
2. HSDI*_FrameSync is multiplexed with HSDI*_DVALID. HSDI*_AV is an output in this mode. It indicates if the number of quadlets in the transmit buffer is over a programmed limit. The watermark control must be programmed for the watermark high. If Iso*WtrMrk.HSDIAvailEn is set to 1, the limit is programmed in Iso*WtrMrk.Level0. The watermark must be programmed less than BUFFER SIZE – (packet length + packet header).

Figure 30. DV I/F (TX Mode 9)

1.11.7 HSDI Receive Modes

The following MPEG2-TS and DV read function timing diagrams are with the polarity of data CLK, sync, data valid, HSDI*_FrameSync, enable, and available signals are default setting.

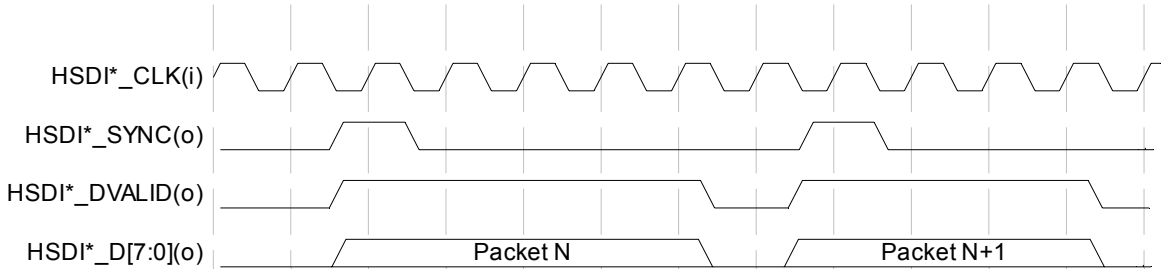
1.11.7.1 RX Mode 1: Serial Burst Video I/F (MPEG2)



Note: HSDI*_EN must be pulled low for this mode (HSDI*_EN defaults to active low).

Figure 31. MPEG2 Serial Burst Video I/F (RX Mode 1)

1.11.7.2 RX Mode 2: Parallel Burst Video I/F (MPEG2)



Note: HSDI*_EN must be pulled low for this mode (HSDI*_EN defaults to active low).

Figure 32. MPEG2 Parallel Burst Video I/F (RX Mode 2)

1.11.7.3 RX Mode 3: Parallel Burst Video I/F (MPEG2) Mode

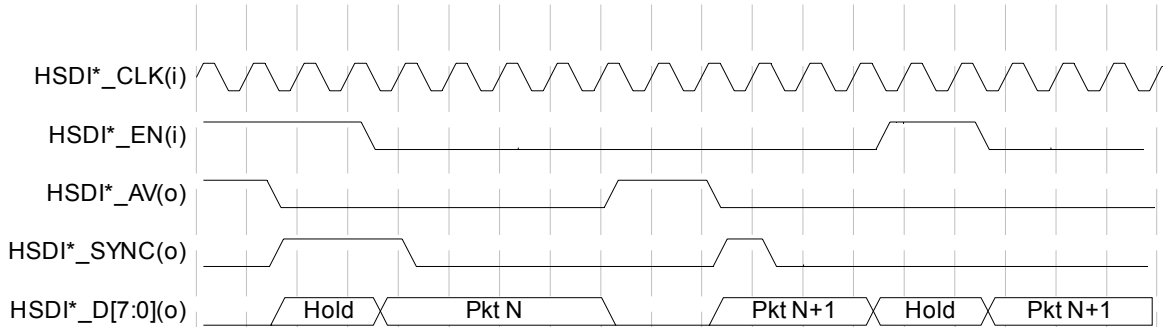
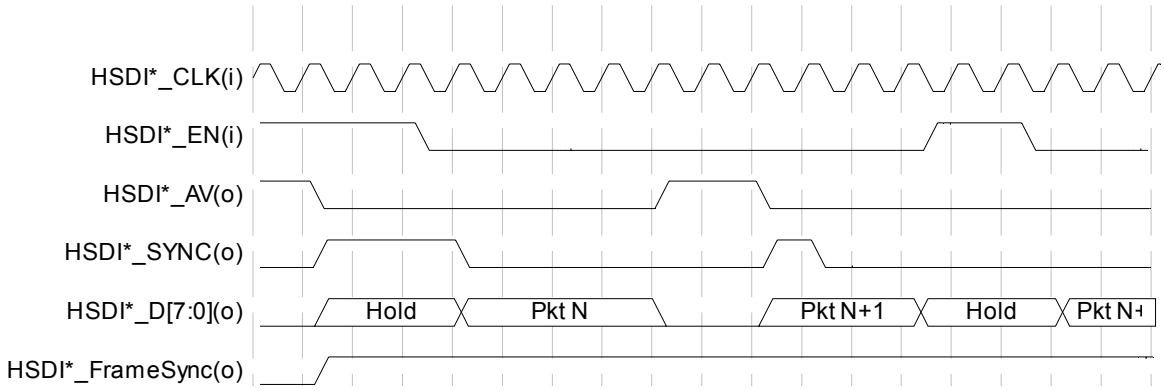


Figure 33. MPEG2 Parallel Burst Video I/F (RX Mode 3)

1.11.7.4 RX Mode 4: Parallel Burst Video I/F (DV) Mode



Notes:
1. The HSDI*_FrameSync signal and the SYT circuit are independent of the HSDI*_D [7:0].
2. HSDI*_FrameSync is multiplexed with HSDI*_DVALID.

Figure 34. DV Parallel Burst Video I/F (RX Mode 4)

1.11.7.5 HSDI A/C Timing

1.11.7.5.1 Transmit HSDI AC Timing

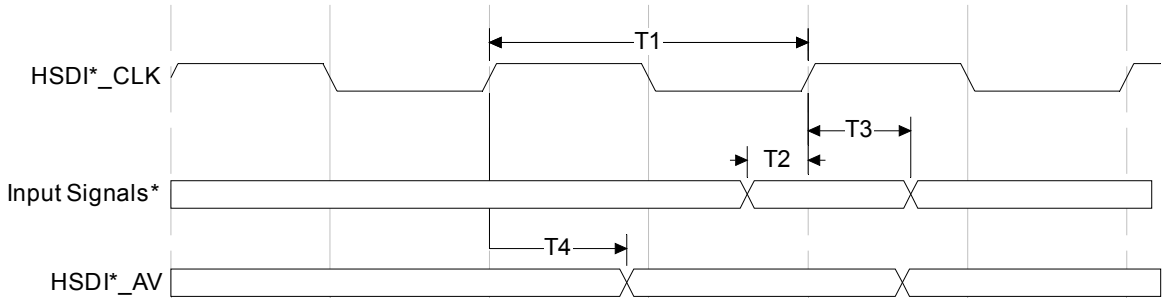


Figure 35. Transmit HSDI AC Timing

Input signals include the following: HSDI*_SYNC, HSDI*_DVALID, HSDI*_D [7:0], HSDI*_EN, and HSDI*_FrameSync.

Table 22. AC Timing Parameters for Serial I/F (Modes 1 and 4)

	Description	Min	Max	Units
T1	Data CLK period	14.3		ns
T2	Signals setup to rising edge of data CLK	2.2		ns
T3	Signals hold to rising edge of data CLK	0		ns

Table 23. AC Timing Parameters for Serial I/F (Modes 2 and 3)

	Description	Min	Max	Units
T1	Data CLK period	12.5		ns
T2	Signals setup to rising edge of data CLK	2.2		ns
T3	Signals hold to rising edge of data CLK	0		ns

Table 24. AC Timing Parameters for Parallel I/F (Modes 5, 6, and 7)

	Description	Min	Max	Units
T1	Data CLK period	37		ns
T2	Signals setup to rising edge of data CLK	11		ns
T3	Signals hold to rising edge of data CLK	0		ns

Table 25. AC Timing Parameters for Parallel I/F (Modes 8 and 9)

	Description	Min	Max	Units
T1	Data CLK period	37		ns
T2	Signals setup to rising edge of data CLK	15		ns
T3	Signals hold to rising edge of data CLK	0		ns
T4	Signals delay from rising edge of data CLK		7	ns

Note: Measurements based on a 20-pF loading.

1.11.7.5.2 Receive HSDI AC Timing

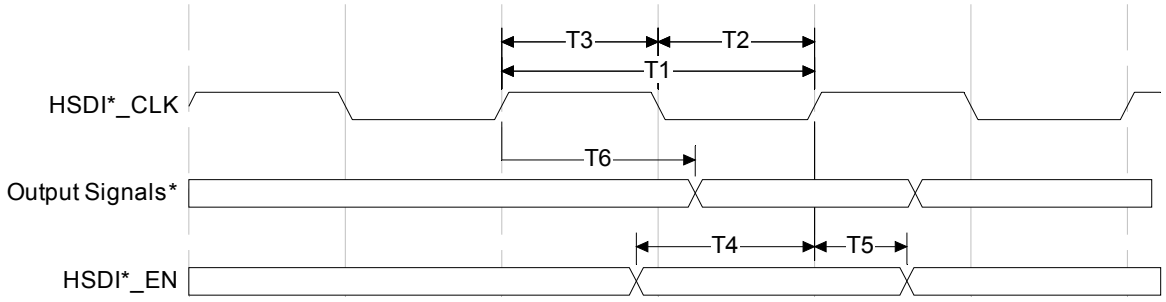


Figure 36. Receive HSDI AC Timing

Output signals include the following: HSDI*_SYNC, HSDI*_DVALID, HSDI*_D[7:0], HSDI*_AV, and HSDI*_FrameSync.

Table 26. AC Timing Parameters for Serial I/F (Mode 1)

	Description	Min	Max	Units
T1	Data CLK period	14.3		ns
T2	CLK low width	4		ns
T3	CLK high width	4		ns
T4	Signals setup to rising edge of data CLK	2.2		ns
T5	Signals hold to rising edge of data CLK	0		ns
T6	Signals delay from rising edge of data CLK		7	ns

Table 27. AC Timing Parameters for Parallel I/F (Mode 2)

	Description	Min	Max	Units
T1	Data CLK period	37		ns
T2	CLK low width	14		ns
T3	CLK high width	14		ns
T4	Signals setup to rising edge of data CLK	2.4		ns
T5	Signals hold to rising edge of data CLK	0		ns
T6	Signals delay from rising edge of data CLK		7	ns

Table 28. AC Timing Parameters for Parallel I/F (Modes 3 and 4)

	Description	Min	Max	Units
T1	Data CLK period	37		ns
T2	CLK low width	15		ns
T3	CLK high width	0		ns
T4	Signals setup to rising edge of data CLK	2.4		ns
T5	Signals hold to rising edge of data CLK	0		ns
T6	Signals delay from rising edge of data CLK	2.4	25	ns

Note: Measurements are based on a 20-pF loading.

1.11.8 Audio Interface on HSDI

1.11.8.1 HSDI0

On HSDI0, only DVD-Audio (MBLA) transmit and 60958 transmit are supported. DVD-Audio (MBLA) and 60958 data cannot be transmitted at the same time. Both interfaces share the same data buffer. The hardware selects the interface based on Iso*Cfg.DataType. For DVD-Audio transmit, the DVD-Audio signals are muxed onto the HSDI pins as follows:

Table 29. HSDI0 DVD Audio Signals

DVD-Audio Signal	Muxed HSDI Pin
BCLK	HSDI0_CLKz
LRCLK	HSDI0_ENz
D0	HSDI0_D0
D1	HSDI0_D1
D2	HSDI0_D2
Ancillary	HSDI0_D3

For 60958 data, the HSDI0_AMCLK_IN and HSDI0_60958_IN pins are used.

1.11.8.2 HSDI1

On HSDI1, 60958, SACD, and DVD-Audio (MBLA) are all supported for transmit or receive. The DVD-Audio (MBLA) has dedicated pins, which are not muxed with HSDI pins. However, the DVD-Audio (MBLA) pins and HSDI pins cannot be used at the same time. They access the same data buffer. The hardware selects the interface based on Iso*Cfg.DataType. DVD-Audio (MBLA) dedicated pins are also used for DVD-Audio (MBLA) flow control mode. HSDI1 signal descriptions are given in Table 30.

Table 30. HSDI1 DVD-Audio Signals

Audio Signal	Direction	Hardware Pin
SACD		
MCLK	Tx/Rx	HSDI1_CLKz
FRAME	Tx/Rx	HSDI1_SYNCz
D0	Tx/Rx	HSDI1_D0
D1	Tx/Rx	HSDI1_D1
D2	Tx/Rx	HSDI1_D2
D3	Tx/Rx	HSDI1_D3
D4	Tx/Rx	HSDI1_D4

Audio Signal	Direction	Hardware Pin
D5	Tx/Rx	HSDI1_D5
D6	Tx/Rx	HSDI1_D6
60958		
CLK	Tx	HSDI1_AMCLK_IN
DATA	Tx	HSDI1_60958_IN
CLK	Rx	HSDI1_AMCLK_OUT
DATA	Rx	HSDI1_60958_OUT
DVD-AUDIO (MBLA)		
BCLK	Tx/Rx	MLPCM_BCLK
LRCLK	Tx/Rx	MLPCM_LRCLK
D0	Tx/Rx	MLPCM_D0
D1	Tx/Rx	MLPCM_D1
D2	Tx/Rx	MLPCM_D2
Ancillary	Tx/Rx	MLPCM_A

1.11.8.3 IEC60958 I/F AC Timing Characteristic

1.11.8.3.1 AC Timing Characteristic on Receiving

The CeLynx_Micro must follow sections 5.3.4.2 and 5.3.4.3 of EIAJ (Electronic Industries Association of Japan) CP-1201 Digital Audio Interface standard.

Extracts from EIAJ CP-1201

[5.3.4.2 rise and fall time rates]

Rise and fall time rates are specified by the following equations.

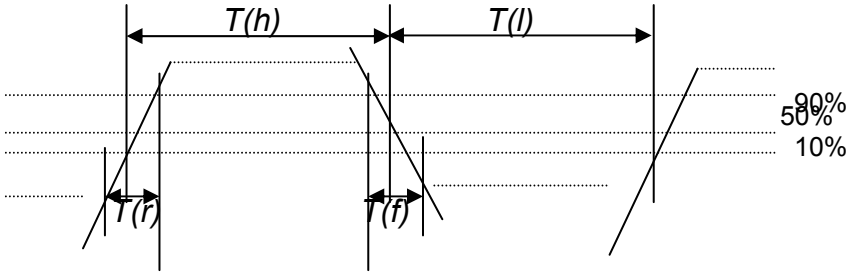
$$rise\_time\_rate = \frac{100 \times T(r)}{T(l) + T(h)} \quad (\%)$$

$$fall\_time\_rate = \frac{100 \times T(f)}{T(l) + T(h)} \quad (\%)$$

Rise and fall time rates must be less than the following ranges.

When the data bit is 1: 0% ~ 20%.

When the data bit is 0 continuously for two times: 0% ~ 10%



[5.3.4.3 duty cycle rate]

Duty cycle rate are specified by following equation.

$$duty\_cycle\_rate = \frac{100 \times T(h)}{T(l) + T(h)} \quad (\%)$$

Duty cycle rate must be less than following ranges.

When the data bit is logically 1: 40% ~ 60%

When the data bit is logically 0 continuously for 2 times: 45% ~ 55%

1.11.8.3.2 AC Timing Characteristic on Transmitting

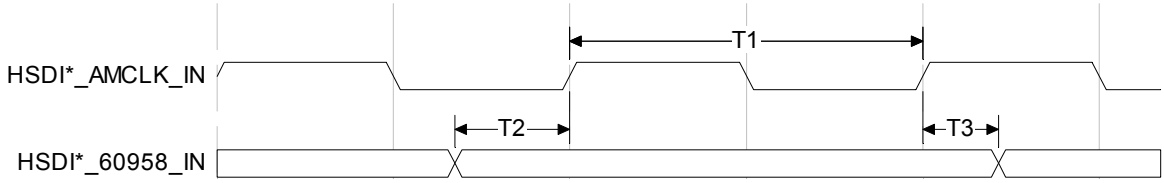


Figure 37. Example 1 Sampling Frequency (fs): 192 kHz, Master Clock Frequency: 256fs

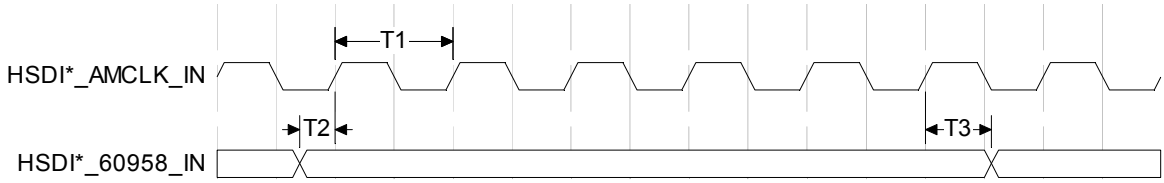
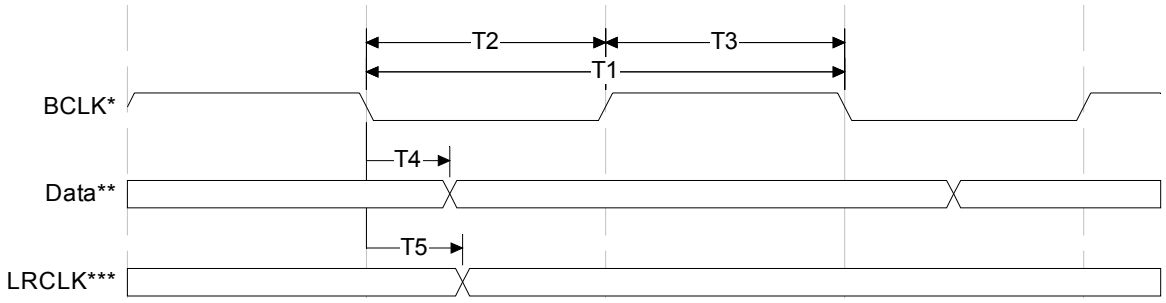


Figure 38. Example 2 Sample Frequency (fs): 48 kHz, Master Clock Frequency: 768fs

Table 31. AC Timing Parameters

Symbol	Description	Min	Max	Units
T1	Data CLK period	27		ns
T2	Signals setup to rising edge of data CLK	5		ns
T3	Signals hold to rising edge of data CLK	5		ns

1.11.8.3.3 MLPCM I/F AC Timing Characteristic



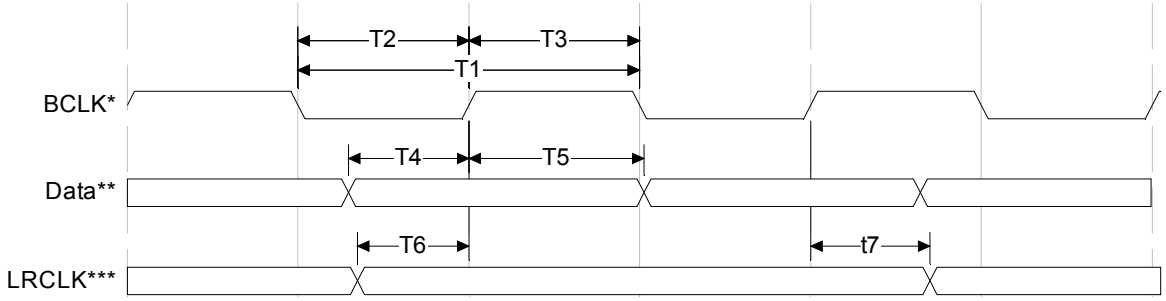
Notes:

- * BCLK includes the following: MLPCM_BCLK and FLWCTL_BCLK.
- ** Data includes the following: MLPCM_D[2:0], MLPCM_A, FLWCTL_D[2:0], and FLWCTL_A.
- *** LRCLK includes the following: MLPCM_LRCLK and FLWCTL_LRCLK.

Figure 39. AC Timing Characteristic on Receiving

Table 32. AC Timing Parameters

Description		Min	Max	Units
T1	Data CLK period	50		ns
T2	CLK low width	20		ns
T3	CLK high width	20		ns
T4	Signals delay to data CLK		10	ns
T5	Signals delay to data CLK		10	ns



Notes:

- * BCLK includes the following: HSDI0_MLPCM_BCLK and MLPCM_BCLK.
- ** Data includes the following: HSDI0_MLPCM_D[2:0], HSDI0_MLPCM_A, MLPCM_D[2:0], and MLPCM_A.
- *** LRCLK includes the following: HSDI0_MLPCM_LRCLK and MLPCM_LRCLK.

Figure 40. AC Timing Characteristic on Transmitting

Table 33. AC Timing Parameters

Description		Min	Max	Units
T1	Data CLK period	75		ns
T2	CLK low width	35		ns
T3	CLK high width	35		ns
T4	Signals setup to data CLK	8		ns
T5	Signals hold to data CLK	8		ns
T6r	Signals setup to data CLK	8		ns
T7	Signals hold to data CLK	8		ns

1.12 UART Interface

The iceLynx-Micro includes one UART port that is memory mapped and fully accessible from the internal CPU. The output of the UART requires level shifting for RS-232 compliance. This UART transmits/receives one start bit, 7 or 8 data bits, optional parity, and 1 or 2 stop bits.

The UART errors are indicated in the iceLynx-Micro interrupts shown in Table 34.

1.12.1 UART Registers

Software uses the iceLynx-Micro UART CFR (0x070) to access UART registers. The UART CFR contains address offset, data, and read/write control bits. The UART address offsets are described in Table 34.

Table 34. UART CFR Address Offsets

DLAB	A2	A1	A0	Name	Register
0	0	0	0	RBR/THR	Receiver buffer register (read) or transmitter holding register (write)
0	0	0	1	IER	Interrupt enable register
X	0	1	0	IIR	Interrupt ID register (read only)
X	0	1	0	FCR	FIFO control register (write)
X	0	1	1	LCR	Link control register
X	1	0	0	MCR	Modem control register
X	1	0	1	LSR	Link status register
X	1	1	0	MSR	Modem status register
X	1	1	1	SCR	Scratch register
1	0	0	0	DLL	Divisor latch (LSB)
1	0	0	1	DLH	Divisor latch (MSB)

Note: Only A2-A0 address bits are implemented in the UART register. The DLAB bit is set in the LCR register. If DLAB is set to 0, reads/writes to addresses 000b and 001b access the RBR/THR and IER registers. If DLAB is set to 1, reads/writes to addresses 000b and 001b access the DLL and DLH registers.

Table 35. UART Registers

Register	Address	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
RBR (RX only)	000 DLAB=0	Data bit 0	Data bit 1	Data bit 2	Data bit 3	Data bit 4	Data bit 5	Data bit 6	Data bit 7
THR (TX only)	000 DLAB=0	Data bit 0	Data bit 1	Data bit 2	Data bit 3	Data bit 4	Data bit 5	Data bit 6	Data bit 7
IER	001 DLAB=0	Enable receiver data available int	Enable transmitter holding register empty Int	Enable receiver line status Int	Enable Modem status Int	0	0	0	0
IIR (read only)	010	0 if int pending	Int ID bit 1	Int ID bit 2	Int ID bit 3	0	0	FIFOs enabled	FIFOs enabled
FCR (write only)	010	FIFO enable	RX FIFO reset	TX FIFO reset	DMA mode select	RSVD	RSVD	Receiver trigger (LSB)	Receiver trigger (MSB)
LCR	011	Word length select bit 0	Word length select bit 1	Number of stop bits	Parity enable	Even parity select	Stick parity	Break control	Divisor latch access bit (DLAB)
MCR	100	Data terminal ready	Request to send	OUT1	OUT2	Loop	Autoflow control enable	RSVD	RSVD
LSR	101	Data ready	Overrun error	Parity error	Framing error	Break int	Transmitter holding register	Transmitter empty	Error in RCVR FIFO
MSR	110	Data clear to send	Delta set ready	Trailing edge ring indicator	Delta carrier detect	Clear to send	Data set ready	Ring indicator	Carrier detect
SCR	111	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
DLL	000 DLAB=1	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
DLH	001 DLAB=1	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

1.12.2 UART Baud Rate

Example: To set the UART baud speed, Equation 1 must be used to determine the divisor value. The divisor value is written into the UART registers to set the baud rate.

$$\text{Baud rate} = 50\ \text{MHz} / (16 \times \text{divisor value}) \qquad \textbf{Equation 1}$$

Write 0x0000 43X1 to UART0 register. This tells the iceLynx-Micro to write a value of X1 to the UART address offset 3 (LCR register). The value X1 sets the DLAB bit to 1.

Write 0x0000 40XX to UART0 register. This tells the iceLynx-Micro to write a value of XX to the UART DLL register. This is the divisor latch LSB.

Write 0x0000 41XX to UART0 register. This tells the iceLynx-Micro to write a value of XX to the UART DLH register. This is the divisor latch MSB.

1.13 JTAG – Boundary Scan and ARM

The iceLynx-Micro implements IEEE 1149.1 JTAG for boundary scan (iceLynx-Micro and ARM core) and ARM debug. Control signals include:

- JTAG_TMS – Test mode select for JTAG boundary scan
- JTAG_TDI – Test data input for JTAG boundary scan
- JTAG_TDO - Test data output for JTAG boundary scan
- ARM_JTAG_TMS – Test mode select for ARM
- ARM_JTAG_TDI – Test data input for ARM
- ARM_JTAG_TDO – Test data output for ARM
- JTAG_TCK – Test clock - Common pin for boundary scan and ARM
- JTAG_TRSTn – Test reset (active low) common pin for boundary scan and ARM.

A JTAG boundary scan is always available.

To disable JTAG, the JTAG_TRSTn signal must be held high.

The JTAG_TCK can operate up to 10.358 MHz; the frequency used by the TI-ARM JTAG emulation tools.

The ARM JTAG can only be enabled by the ARM. A small program must be loaded into program memory that enables the ARM JTAG (InCPUCfg.DebugEn).

1.14 Integrated 3-Port PHY

1.14.1 3-Port PHY

The iceLynx-Micro contains an integrated 3-port PHY. The PHY operates at 100 Mbps, 200 Mbps, or 400 Mbps and meets the requirements as stated in the IEEE 1394-1995 and IEEE 1394a-2000 standards. For applications that only need two PHY ports, the TPB± signals are terminated to ground on the board, or the PHY port is disabled through a CFR. When this occurs, the PHY still reports itself as a 3-port node in self-ID packets.

The PHY core contains a CFR bit that controls the BIAS function. This bias function can either operate using the IEEE 1394-1995 method of bias or the IEEE 1394a-2000 method of bias. The IEEE 1394-1995 method always asserts a continuous bias. The IEEE 1394a-2000 method asserts bias for 980 ms.

The PHY can be set to operate at S100 and S200 nodes only. If the MSPCTL hardware pin is asserted to a high state, the maximum transaction speed is S200. Also PHY maximum node speed is recognized as S200. If MSPCTL is zero (i.e., pulled to ground), the PHY supports S100, S200, and S400.

The PHY registers are accessed through the PhyAccess configuration register as described in Table 36.

Table 36. PHY Access Register

31	30	29 28	27 24	23 16	15 12	11 8	7 0
RdReg	WrReg	RSVD	PhyRegAddr	PhyRegWrData	RSVD	PhyRegAddrRcvd	PhyRegDatRcvd

1.14.2 PHY Registers

In the iceLynx-Micro are 16 accessible internal PHY registers. They are accessed using the PHY access register. The address offset specifies the location. The configuration of the registers at addresses 0 through 7 (the base registers) is fixed, while the configuration of the registers at addresses 8 through Fh (the paged registers) is dependent upon which one of eight pages, numbered 0 through 7, is currently selected. The selected page is set in base register 7.

The configuration of the base registers is shown in Table 37 and the corresponding field descriptions are given in Table 38. The base register field definitions are unaffected by the selected page number.

A reserved register or register field (marked as Reserved or Rsvd in the register configuration tables below) is read as 0, but is subject to future usage. All registers in pages 2 through 6 are reserved.

Table 37. Base Register Configuration

Address	Bit Position							
	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (‘b111)			Rsvd	Num_Ports (‘b0011)			
0011	PHY_Speed (‘b010)			Rsvd	Delay (‘b0000)			
0100	LCtrl	C	Jitter (‘b000)			Pwr_Class		
0101	WDIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Reserved							
0111	Page_Select			Rsvd	Port_Select			

Table 38. Base Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Physical ID	6	Rd	This field contains the physical address ID of this node determined during self-ID. The physical-ID is invalid after a bus-reset until self-ID has completed as indicated by an unsolicited register-0 status transfer.
R	1	Rd	Root. This bit indicates that this node is the root node. The R bit is reset to 0 by bus-reset, and is set to 1 during tree-ID if this node becomes root.
CPS	1	Rd	Cable-power-status. This bit indicates the state of the CPS input pin. The CPS pin is normally pulled to serial bus cable power through a 400-kΩ resistor. A 0 in this bit indicates that the cable power voltage has dropped below its threshold for guaranteed reliable operation.
RHB	1	Rd/Wr	Root-holdoff bit. This bit instructs the PHY to attempt to become root after the next bus-reset. The RHB bit is reset to 0 by hardware reset and is unaffected by bus-reset.
IBR	1	Rd/Wr	Initiate bus-reset. This bit instructs the PHY to initiate a long (166 μs) bus reset at the next opportunity. Any receive or transmit operation in progress when this bit is set completes before the bus reset is initiated. The IBR bit is reset to 0 by hardware reset or bus reset.
Gap_Count	6	Rd/Wr	Arbitration gap count. This value sets the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count is set either by a write to this register or by reception or transmission of a PHY_CONFIG packet. The gap count is set to 3Fh by hardware reset or after two consecutive bus-resets without an intervening write to the gap count register (either by a write to the PHY register or by a PHY_CONFIG packet).
Extended	3	Rd	Extended register definition. For iceLynx-Micro this field is ‘b111, indicating that the extended register set is implemented.
Num_Ports	4	Rd	Number of ports. This field indicates the number of ports implemented in the PHY. For iceLynx-Micro this field is three.
PHY_Speed	3	Rd	PHY speed capability. For iceLynx-Micro PHY this field is ‘b010, indicating S400 speed capability. The setting of this field also depends on the MSPCTL setting.
Delay	4	Rd	PHY repeater data delay. This field indicates the worst-case repeater data delay of the PHY, expressed as 144+(delay*20) ns. This field is 0 (default.)

FIELD	SIZE	TYPE	DESCRIPTION
LCtrl	1	Rd/Wr	Link-active status control. This bit controls the active status of the LLC as indicated during self-ID. The logical AND of this bit and the LPS active status is replicated in the L field (bit 9) of the self-ID packet. The LLC is considered active only if both the LPS input is active and the LCtrl bit is set. The LCtrl bit provides software controllable means to indicate the LLC active status in lieu of using the LPS input. The LCtrl bit is set to 1 by hardware reset and is unaffected by bus reset. **Note:** The state of the PHY-LLC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit. If the PHY-LLC interface is operational as determined by the LPS input being active, then received packets and status information continues to be presented on the interface, and any requests indicated on the LREQ input is processed, even if the LCtrl bit is cleared to 0.
C	1	Rd/Wr	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the c field (bit 20) of the self-ID packet. This bit is set to the state specified by the C/LKON input pin upon hardware reset and is unaffected by bus reset.
Jitter	3	Rd	PHY repeater jitter. This field indicates the worst-case difference between the fastest and slowest repeater data delay, expressed as (JITTER+1)*20 ns. For iceLynx-Micro this field is 0.
Pwr_Class	3	Rd/Wr	Node power class. This field indicates this node's power consumption and source characteristics, and is replicated in the pwr field (bits 21–23) of the self-ID packet. This field is set to 000 default value at hardware reset and is unaffected by bus-reset. Software can program this field to change the power class. Software must perform a bus reset after setting this field.
WDIE	1	Rd/Wr	Watchdog interrupt enable. This bit, if set to 1, enables the port event interrupt (PEI) bit to be set whenever resume operations begin on any port. This bit also enables the C/LKON output signal to be activated whenever the LLC is inactive and any of the CTOI, CPSI, or STOI interrupt bits is set. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
ISBR	1	Rd/Wr	Initiate short arbitrated bus-reset. This bit, if set to 1, instructs the PHY to initiate a short (1.30 μs) arbitrated bus-reset at the next opportunity. This bit is reset to 0 by bus reset. **Note:** Legacy IEEE Std 1394-1995 compliant PHYs may not be capable of performing short bus-resets. Therefore, initiation of a short bus-reset in a network that contains such a legacy device results in a long bus reset being performed.
CTOI	1	Rd/Wr	Configuration time-out interrupt. This bit is set to 1 when the arbitration controller times out during tree-ID start, and indicates that the bus is configured in a loop. This bit is reset to 0 by hardware reset or by writing a 1 to this register bit. If the CTOI and RPIE bits are both set and the LLC is or becomes inactive, the PHY activates the C/LKON output to notify the LLC to service the interrupt. **Note:** If the network is configured in a loop, only those nodes that are part of the loop generate a configuration time-out interrupt. All other nodes instead, time-out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus reset.
CPSI	1	Rd/Wr	Cable power status interrupt. This bit is set to 1 whenever the CPS input transitions from high to low indicating that cable power is too low for reliable operation. This bit is reset to 1 by a hardware reset. It is cleared by writing a 1 to this register bit. If the CPSI and RPIE bits are both set and the LLC is or becomes inactive, the PHY activates the C/LKON output to notify the LLC to service the interrupt.
STOI	1	Rd/Wr	State time-out interrupt. This bit indicates that a state time-out has occurred (which also causes a bus reset to occur). This bit is reset to 0 by hardware reset or by writing a 1 to this register bit. If the STOI and RPIE bits are both set and the LLC is or becomes inactive, the PHY activates the C/LKON output to notify the LLC to service the interrupt.

FIELD	SIZE	TYPE	DESCRIPTION
PEI	1	Rd/Wr	Port event interrupt. This bit is set to 1 upon a change in the bias (unless disabled), connected, disabled, or fault bits for any port for which the port interrupt enable (PIE) bit is set. Additionally, if the resuming port interrupt enable (RPIE) bit is set, the PEI bit is set to 1 at the start of resume operations on any port. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit. If the PEI bit is set (regardless of the state of the RPEI bit) and the LLC is or becomes inactive, the PHY activates the C/LKON output to notify the LLC to service the interrupt.
EAA	1	Rd/Wr	Enable accelerated arbitration. This bit enables the PHY to perform the various arbitration acceleration enhancements defined in 1394a-2000 (ACK-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is reset to 0 by hardware reset and is unaffected by bus reset. **Note:** The EAA bit must be set only if the attached LLC is IEEE 1394a-2000 compliant. If the LLC is not IEEE 1394a-2000 compliant, use of the arbitration acceleration enhancements interferes with isochronous traffic by excessively delaying the transmission of cycle-start packets.
EMC	1	Rd/Wr	Enable multi-speed concatenated packets. This bit enables the PHY to transmit concatenated packets of differing speeds in accordance with the protocols defined in IEEE 1394a-2000. This bit is reset to 0 by a hardware reset and is unaffected by bus-reset. **Note:** The use of multi-speed concatenation is completely compatible with networks containing legacy IEEE Std 1394-1995 PHYs. However, use of multi-speed concatenation requires that the attached LLC be 1394a-2000 compliant.
Page_Select	3	Rd/Wr	Page-select. This field selects the register page to use when accessing register addresses 8 through 15. This field is reset to 0 by a hardware reset and is unaffected by bus-reset.
Port_Select	4	Rd/Wr	Port-select. This field selects the port when accessing per-port status or control (e.g., when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is reset to 0 by a hardware reset and is unaffected by bus-reset.

1.14.3 Port Status Page Register

The port status page provides access to configuration and status information for each of the ports. The port is selected by writing 0 to the Page_Select field and the desired port number to the Port_Select field in base register 7. The configuration of the port status page registers is shown in Table 39 and corresponding field descriptions given in Table 40. If the selected port is unimplemented, all registers in the Port Status page are read as 0.

Table 39. Page 0 (Port Status) Register Configuration

Address	Bit Position							
	0	1	2	3	4	5	6	7
1000	Astat		Bstat		Ch	Con	Bias	Dis
1001	Peer_Speed			PIE	Fault	Reserved		
1010	Reserved							
1011	Reserved							
1100	Reserved							
1101	Reserved							
1110	Reserved							
1111	Reserved							

Table 40. Page 0 (Port Status) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
AStat	2	Rd	TPA line state. This field indicates the TPA line state of the selected port, encoded as follows: Code – Line State 11 – Z 01 – 1 10 – 0 00 – invalid
Bstat	2	Rd	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the ASTAT field.
Ch	1	Rd	Child/parent status. A 1 indicates that the selected port is a child port. A 0 indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus reset until tree-ID has completed.
Con	1	Rd	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of approximately 341 ms for the Con bit to be set to 1. The Con bit is reset to 0 by hardware reset and is unaffected by bus reset. **Note:** The Con bit indicates that the port is physically connected to a peer PHY, but the port is not necessarily active.
Bias	1	Rd	Debounced incoming cable bias status. A 1 indicates that the selected port is detecting incoming cable bias. The incoming cable bias must be stable for the debounce time of 52 μs for the Bias bit to be set to 1.
Dis	1	Rd/Wr	Port disabled control. If 1, the selected port is disabled. The Dis bit is reset to 0 by hardware reset (all ports are enabled for normal operation following hardware reset). The Dis bit is not affected by bus reset.
Peer_Speed	3	Rd	Port peer speed. This field indicates the highest speed capability of the peer PHY connected to the selected port, encoded as follows: Code – Peer Speed 000 – S100 001 – S200 010 – S400 011–111 – invalid The Peer_Speed field is invalid after a bus-reset until self-ID has completed. **Note:** Peer speed codes higher than 'b010 (S400) are defined in 1394a-2000. However, iceLynx-Micro is only capable of detecting peer speeds up to S400.
PIE	1	Rd/Wr	Port event interrupt enable. When set to 1, a port event on the selected port sets the port event interrupt (PEI) bit and notify the link. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
Fault	1	Rd/Wr	Fault. This bit indicates that a resume-fault or suspend-fault has occurred on the selected port and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend-fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1 to this bit clears the Fault bit to 0. This bit is reset to 0 by hardware reset and is unaffected by bus reset.

1.14.4 Vendor Identification Page Register

The vendor identification page identifies the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page_Select field in base register 7. The configuration of the vendor identification page is shown in Table 41 and the corresponding field descriptions given in Table 42.

Table 41. Page 1 (Vendor ID) Register Configuration

	Bit Position							
Address	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
1000	Compliance							
1001	Reserved							
1010	Vendor_ID[0]							
1011	Vendor_ID[1]							
1100	Vendor_ID[2]							
1101	Product_ID[0]							
1110	Product_ID[1]							
1111	Product_ID[2]							

Table 42. Page 1 (Vendor ID) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	Rd	Compliance level. For iceLynx-Micro, this field is controlled by a link register bit.
Vendor_ID	24	Rd	Manufacturer's organizationally unique identifier (OUI). For iceLynx-Micro, this field is 08_00_28h (Texas Instruments) (the MSB is at register address 'b1010).
Product_ID	24	Rd	Product identifier. For iceLynx-Micro, this field is 41_44_99h (the MSB is at register address 'b1101).

1.14.5 PHY Application Information

The PHY pins must be connected as shown in the following figures. XI and XO pins must be connected to a crystal as described by Texas Instruments application note SLLA051.

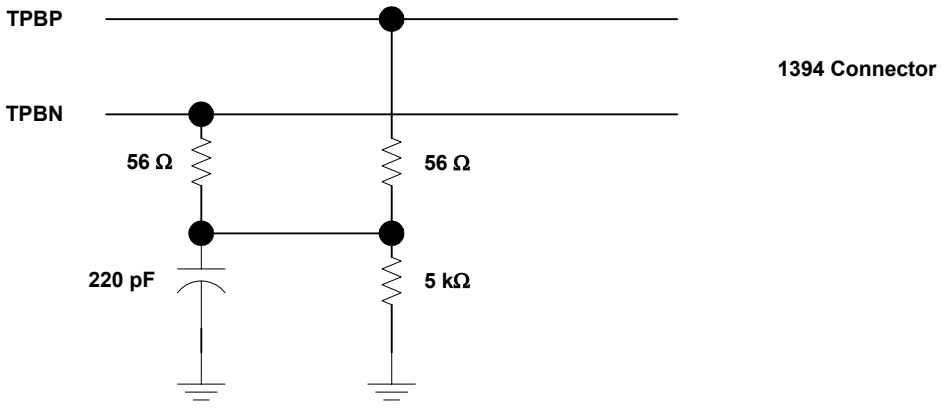


Figure 41. TPBP and TPBN Connection

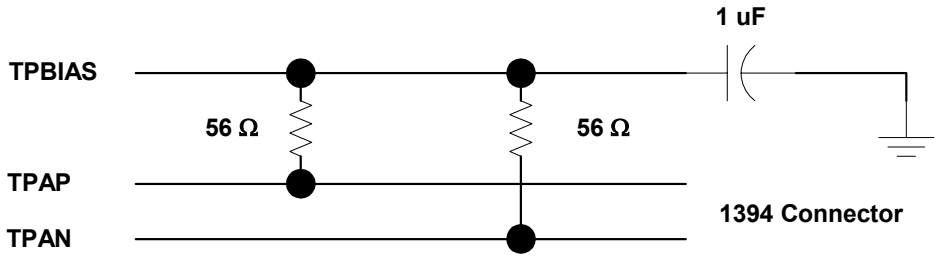


Figure 42. TPAP, TPAN, and TPBIAS Connection

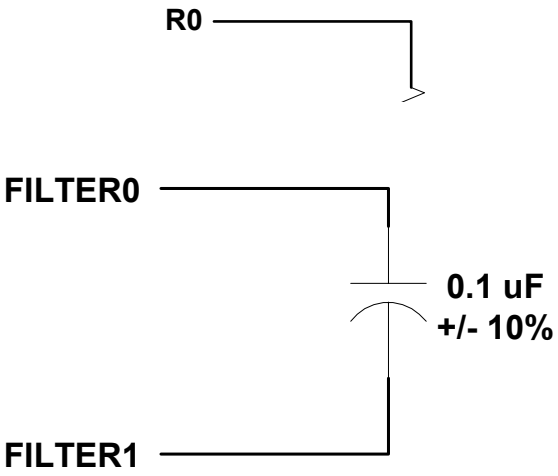


Figure 43. R0 and R1 Connection

Figure 44. FILTER0 and FILTER1 Connection

Figure 45. TPB, TPA, and TPBIAS Connection for Terminated Port (Port is not used)

1.14.6 PHY Reference Documents

Visit the Texas Instruments website to obtain the following reference documents:

Literature Number	Title
SLLA117	IEEE 1394 EMI Board Design and Layout Guidelines
SLLA051	Selection and Specification of Crystals for Texas Instruments IEEE 1394 Physical Layers

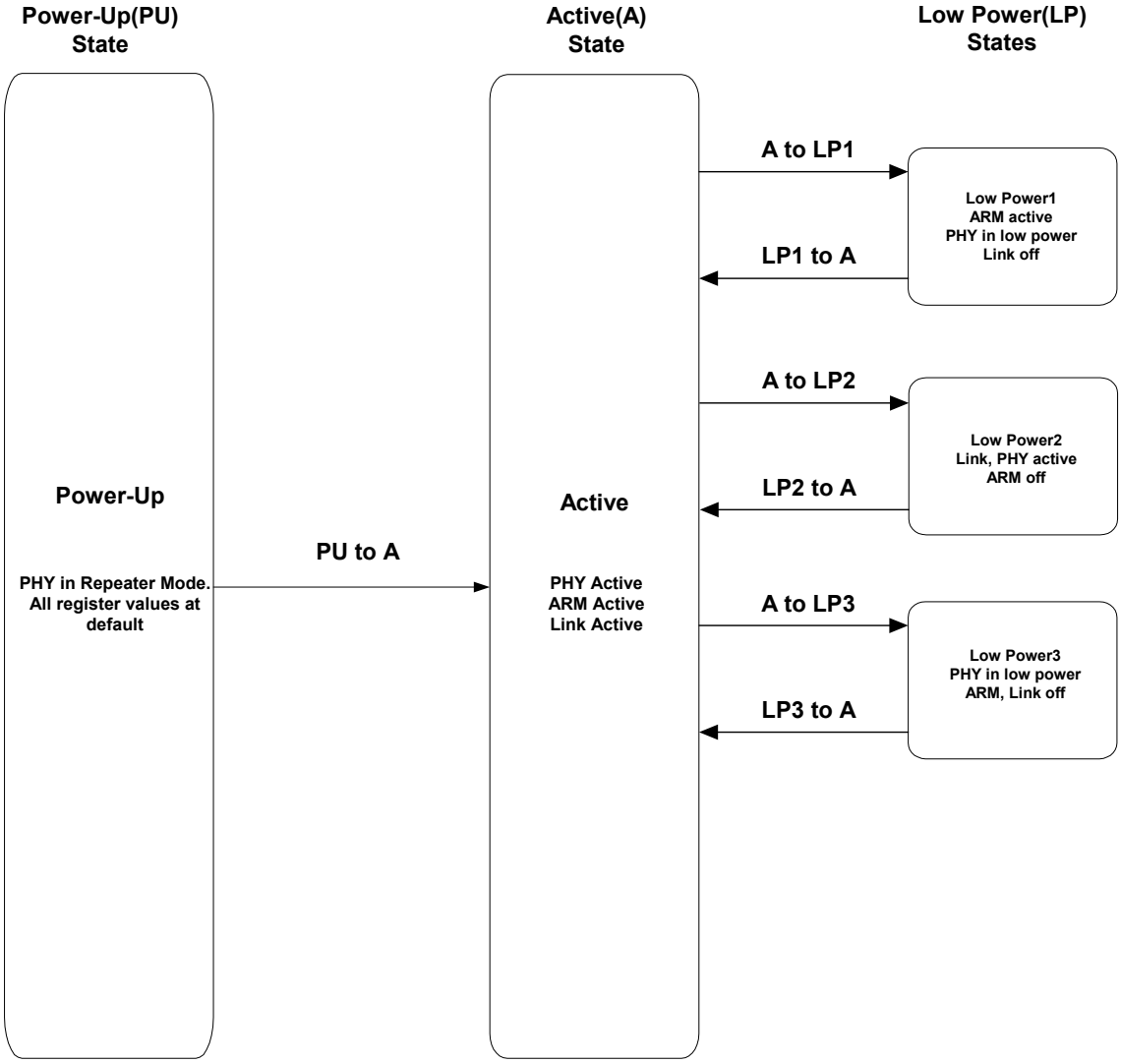
1.15 Power Management

The iceLynx-Micro operates from a single 3.3-V power supply. When REG_ENn is asserted, three internal regulators operate the 1.8-V core. When the internal regulator is not supplied, the application must externally supply the core voltage. The PHY also automatically conforms to IEEE1394a-2000 power states according to bus activity. Table 43 summarizes all the power modes that the iceLynx-Mirco supports.

Table 43. Power State Summary

Power State	InCPUCfg.Reset	PhyCfg.LPS	PHY Ports	Max Power w/Internal Regulator Enabled (mW)	Max Power w/External Regulator Enabled (mW)
Active - Full power Link, ARM, and PHY are active	0	1	Active	695	531
Low power 1 - ARM Active Link and PHY are low power	0	0	Disabled or suspended by software	473	223
Low power 2 - Link and PHY only ARM in low power	1	1	Active	125	102
Low power 3 - PHY only – PHY low power Link and ARM are low power	1	0	Disabled or suspended by software	31	4

Note: All other configurations are not valid for normal operation.



1.15.1 PU to A (Power-Up State to Active State)

At the power-up state, all registers are at the default value. Following are the power-up status of registers and signals related to power control.

Register/Pin Name	Power-up Status
InCPUCfg.Reset	0 (ARM is held in reset using RESET_ARMn pin)
InCPUCfg.ClkEn	1
InCPUCfg.PhyNoticeEn	0
PhyCfg.LPS	0 (PHY is in repeater mode)
WTCH_DG_TMRn	Low
HPS	High

1. The external system holds the ARM in reset using RESET_ARMn pin.
2. The external CPU loads the ARM program code. Once it has completed loading the code, it deasserts RESET_ARMn.
3. The ARM sets PhyCfg.LPS to 1. Now the PHY, link, and ARM are fully functional.

1.15.2 A to LP1 (Active State to Low Power 1 State)

In the active state, the link, ARM, and PHY are fully operational. In the low power state 1, the link is off. The PHY ports are suspended or disabled. The ARM may choose to put the iceLynx-Micro into a low power state based on the HPS pin. A falling edge of the HPS pin indicates the external system is ready for the iceLynx-Micro to go into low power mode.

The ARM sets the following bits to move to LP1 state.

1. Suspend or disable PHY ports. S/W can disable a PHY port by setting the Dis bit in PHY register b1000. S/W can suspend a PHY port by sending an IEEE 1394a-2000 remote command packet to its own node.
2. PhyCfg.LPS = 0 (PHY can go into low power mode according to IEEE 1394a-2000)

1.15.3 LP1 to A (Low Power 1 State to Active State)

1. On the detection of the following events, ARM must enable the link and PHY to the active state.
   - Rising edge of HPS input pin.
   - InCPUCfg.PhyNoticeEn = 1 and LinkOn or PHY_INT occurs.
2. ARM must set PhyCfg.LPS = 1. If any of the ports were disabled, software must reenable the PHY ports by setting the Dis bit in PHY register b1000 to make the PHY active. The software must issue a bus reset once PhyCfg.LPS is set to 1.

1.15.4 A to LP2 (Active State to Low Power 2 State)

In the active state, the Link, ARM, and PHY are fully operational. In the low power state 2, the ARM is off and the link and PHY are fully operational. The system may choose to put the iceLynx-Micro into the low power state 2 when the internal ARM is not used.

The ex-CPU sets the following bits to move to LP2 state:

1. Set InCPUCfg.Reset = 1 and InCPUCfg.ClkEn = 0 at the same time.

1.15.5 LP2 to A (Low Power 2 State to Active State)

1. The iceLynx-Micro hardware sets InCPUCfg.Reset = 0 and InCPUClkEn = 1 for either of the following conditions:
    - Rising edge of HPS input pin.
    - InCPUCfg.PhyNoticeEn=1 and LinkOn or PHY_INT occurs.

1.15.6 A to LP4 (Low Power 3 State to Active State)

In the active state, the link, ARM, and PHY are fully operational. In the low power state 4, the ARM and link are off. The PHY ports are suspended or disabled. The ARM may choose to put iceLynx-Micro into a low power state based on the HPS pin. A falling edge indicates the external system is ready for iceLynx-Micro to go into low power mode.

The ARM sets the following bits to move to LP4 state:

1. Suspend or disable PHY ports. S/W can disable a PHY port by setting the Dis bit in PHY register 0b1000. S/W can suspend a PHY port by sending an IEEE 1394a-2000 remote command packet to its own node.
2. PhyCfg.LPS = 0 {PHY can go into low power mode according to IEEE 1394a-2000}
3. Set InCPUCfg.Reset = 1 and InCPUClkEn = 0 at the same time.

1.15.7 LP4 to A (Low Power 3 State to Active State)

1. The iceLynx-Micro hardware sets InCPUCfg.Reset = 0 and InCPUClkEn = 1 for either of the following conditions:
    - Rising edge of HPS input pin
    - InCPUCfg.PhyNoticeEn=1 and LinkOn or PHY_INT occurs

Once the ARM and link are active, the ARM must set PhyCfg.LPS = 1. If any of the ports were disabled, software must reenable the PHY ports by setting the Dis bit in PHY register b1000 to make the PHY active. The software must issue a bus reset once PhyCfg.LPS is set to 1.

The input/output pins and CFRs that control each power management state are defined in Table 44.

Table 44. I/O Pin and CFR Descriptions for Controlling Power Management States

Signal Name	Location	Direction	Description
LOW_PWR_RDY InCPUCfg.LowPwrRdy	Pin and CFR	Output	This signal is output to the system to indicate iceLynx-Micro can go into a low power state. The ARM controls this output signal using CFR. The signal also depends on the watchdog timer output signal. If the watchdog timer is asserted, this signal is asserted.
WTCH_DG_TMRn	Pin	Output	Indicates watchdog timer status. Hardware asserts this when the ARM software is not functioning correctly.
HPS ExCPUCfg.HPS InCPUInt.HPSHi InCPUInt.HPSLo	Pin and CFR	Input	Host power status (ex-CPU power status). This signal indicates the ex-CPU's power status. A rising edge indicates the ex-CPU has been turned ON. The internal ARM must wake up. The internal ARM decides if it must wake up the rest of iceLynx-Micro. A falling edge indicates the ex-CPU has shut down. ARM can decide how to react. Interrupts are available for both the rising and falling edge of this signal.

Signal Name	Location	Direction	Description
PhyCfgLPS	CFR		This bit is set in CFR to indicate low power status to the PHY. The ARM must set this when it wants to put the link into lower power mode. The ARM must clear this bit to bring the link out of low power mode. **Note:** Software must wait at least 2 ms before setting PhyCtrl.LPS after iceLynx-Micro power up. This ensures the internal clocks are stable.
InCPUCfg.PhyNoticeEn	CFR		This bit enables PHY events. These PHY events signal a wake up event to the ARM while the ARM is powered down. The PHY events include LinkOn and PHY_INT.
RESET_ARMn InCPUCfg.Reset	Pin and CFR	Input	This pin and CFR bit put ARM into reset. ARM cannot be put into reset by setting InCPUCfg.Reset = 1 if InCPUCfg.ResetDis is set to 1. See the description for InCPUCfg.ResetDis. InCPUCfg.ResetDis bit must be cleared before the ARM is put into reset. The RESET_ARMn pin does not have these qualifying conditions. When RESET_ARMn = low, the ARM is put into reset regardless of InCPUCfg.ResetDis bit status.
LINKON PhyCfg.LinkOn	Pin and CFR	Output	This signal is asserted whenever LPS is low and a LinkOn packet is received. It is cleared whenever LPS is detected or the PHY register LCtrl bit is set to zero. PhyCfg.LinkOn gives the current status of the LINKON signal.
DISABLE_IFn	Pin	Input	Interface disable. When this pin is asserted by the system, all interfaces on iceLynx-Micro are in high-Z state. This includes Ex-CPU I/F, HSDI I/F, GPIO, and WTCH_DG_TMRn. This function does not include LOW_PWR_RDY. This function is active low. The interface is disabled if DISABLE_IFn=0.
InCPUCfg.ResetDis	CFR		This bit is set by hardware any time one of the following bits transitions from 0 to 1. PhyCfg.LinkOn LinkInt.PhyInt InCPUInt.HPSHi

Note: The WTCH_DG_TMRn is configured for output on the Timer2 interrupt.

1.16 16.5K Byte Memory - FIFO

1.16.1 Overview/Description

The iceLynx-Micro has 16.5K byte FIFO. The FIFO sizes are set and not programmable.

1.16.2 Isochronous FIFOs 0 and 1

These FIFOs are connected to the HSDI0 and HSDI1 ports, respectively. They are both 4K bytes in size. These FIFOs are designed to handle MPEG2, DSS, DV, or audio data. These data types cannot be interleaved. The buffer must be dedicated to one data type and a single direction. It can be reprogrammed to handle different data types. Both of these buffers can be configured for either transmit or receive. The buffer is only accessible using the HSDI. See Figure 46 for a block diagram of the isochronous FIFO architecture.

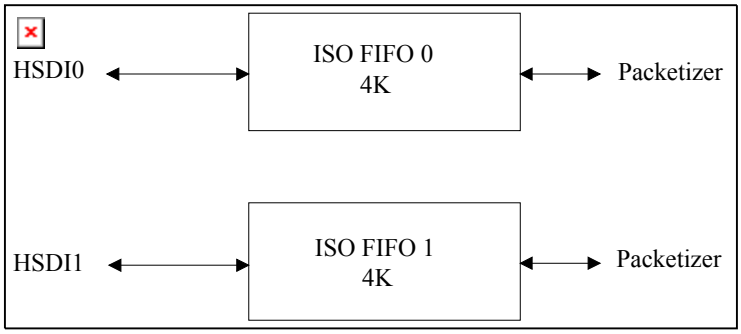


Figure 46. Isochronous FIFOs

1.16.3 Asynchronous/Asynchronous Stream FIFOs

These FIFOs are connected to the external and internal CPU interfaces. The transmit FIFOs are 2048 bytes each and the receive FIFOs are 2048 bytes each. Either FIFO can be configured for asynchronous stream or asynchronous packets. See Figure 47 for a block diagram of the asynchronous FIFO architecture.

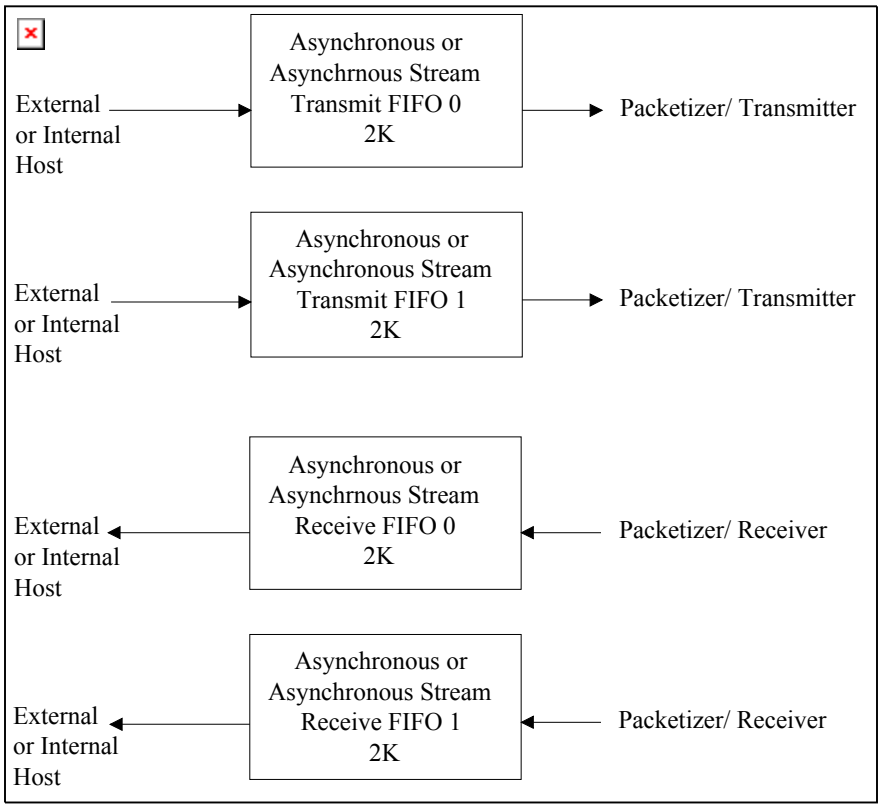


Figure 47. Asynchronous/ Asynchronous Stream FIFOs

Note: The iceLynx-Micro has the ability to insert headers for asynchronous stream transmit. This feature must be used for asynchronous stream TX only. For any type of packet other than asynchronous stream, do not enable this feature.

1.16.4 Broadcast Receive FIFO

This FIFO is designed to receive all broadcast packets, such as self-IDs, broadcast asynchronous packets, and PHY packets. The broadcast receive FIFO is 512 bytes in size to accommodate self-Ids for a 63-node network. This FIFO is accessed separately for software convenience. It is only accessible by the external or internal CPU. This FIFO is only for receive operations. All transmit operations must take place using an asynchronous transmit FIFO. See Figure 48 for a block diagram of the broadcast FIFO architecture.

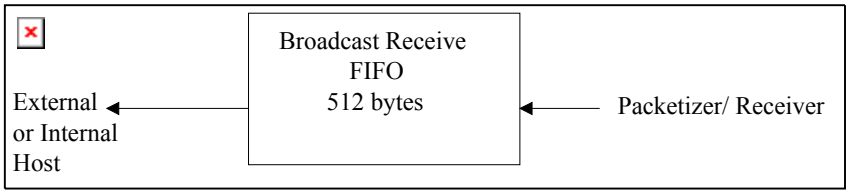


Figure 48. Broadcast Receive FIFO

1.16.5 FIFO Priority

For two FIFOs that are the same data type, the lower number FIFO always has priority. For example, if the iceLynx-Micro were configured for two asynchronous transmit FIFOs, FIFO 0 and 1, FIFO 0 would have priority over FIFO 1.

1.16.6 FIFO Monitoring

The FIFO size is monitored by several interrupts and status bits. An example of these monitoring bits is included in Table 45.

Table 45. FIFO Monitoring Bits

Name	Description
Watermark High (Iso*CPUInt.WtrMrk*, Iso*BufStat.WtrMrk*)	The watermark control (Iso*WtrMrk.Control*) needs to be set to 1. The watermark level is programmed at Iso*WtrMrk.Level*. When the level in the FIFO is above the programmed value at Iso*WtrMrk.Level*, the Watermark High is activated.
Watermark Low (Iso*CPUInt.WtrMrk*, Iso*BufStat.WtrMrk*)	The watermark control (Iso*WtrMrk.Control*) needs to be set to 0. The watermark level is programmed at Iso*WtrMrk.Level*. When the level in the FIFO is below the programmed value at Iso*WtrMrk.Level*, the watermark low is activated.
Cell Available (Iso*CPUInt.CellAvail, Iso*BufStat.CellAvail)	A full 1394 packet (or individual cell: 188 bytes for DVB, 480 bytes for DV, 130 or 140 bytes for DSS) is available in the FIFO. This is valid for transmit or receive.
Quadlets Available (Iso*BufStat.QuadAvail)	This value reflects the number of quadlets currently in FIFO. This is valid for transmit or receive.

Notes: The FIFO watermark levels are only checked on packet boundaries. If the buffer is not a multiple of (packet _length+ header length) and the watermark level is programmed between BUFFER SIZE and (BUFFER SIZE – 1 Packet Length – Header Length), watermark level indicators (Iso*CPUInt.WtrMrk*, Iso*BufStat.WtrMrk*) are not activated.

1.17 GPIO Configurations

GPIOs can be configured to achieve the following:

- DSS TX – DSS SCC (system clock count) input and DSS error flag
- Watermark level indicator in FIFOs
- Flow control
- GPIO interrupts. There are four possible GPIO interrupts. These are configured as ARM FIQ or IRQs.

Note: GPIO interrupts are synchronously detected. The interrupt must be held at the level for at least one 50-MHz clock cycle (for both level sensitive and edge sensitive interrupts).

Example:

The FIQ and IRQ GPIOs are programmed in CFR.

For example, the FIQ interrupt is input using GPIO9.

1. The GPIOCfg.GPIO9Sel is set to “general purpose input.”
2. The GPIOIntCfg.GPIOInt*Sel bits (or GPIOIntCfg.GPIOIntYSel bits) are set to reference GPIO 9.
3. The edge detection is set in GPIOIntCfg.GPIOInt*Det bit.
4. After this setup is complete, the InCPUInt.GPIO* (or InCPUInt.GPIOY) bit indicates when the programmed edge occurs on FIQ GPIO. This must be enabled in IntCPUHiIntEn.GPIO*. The GPIOData.GPIO9 indicates the GPIO9 status.

Table 46. Summary of GPIO Use

GPIO Function	Programmable GPIOs
DSS SCC input DSS error flag	GPIO 2, GPIO 3 for HSDI 0 GPIO 6, GPIO 7 for HSDI 1
Wather Marks for Iso FIFOs	GPIO 0, GPIO 1 for Iso data path 0 GPIO 4, GPIO 5 for Iso data path 1

Note: All GPIOs (i.e., GPIO 0 through GPIO 10) can be configured as general-purpose input/output.

1.17.1 GPIO Setup

The flow control writes to GPIOs through the software functions. The GPIO is set up as a general-purpose input or output. The values are read/written using the GPIOStat CFR for the appropriate GPIO.

The watermark GPIOs are linked to the watermark status bits.

1.18 IEEE 1394a-2000 Requirements

1.18.1 Features

The iceLynx-Micro is compliant to the IEEE 1394a-2000 standard. This requires the following features:

- Arbitrated (short) bus reset
- Ack-accelerated arbitration
- Fly-by concatenation
- Multi-speed packet concatenation
- PHY ping packets
- Priority arbitration
- Port disable, suspend, and resume

1.18.2 Cycle Master

The hardware automatically makes the node cycle master. This depends on the root status of the node. If LinkCfg.CycMasAuto = 1 and the node is root, the node becomes the cycle master after the next bus reset. The software must set LinkCfg.CycMasAuto = 1 at initialization phase immediately after device reset or power-up.

2 Appendix A: Configuration Registers

2.1 Configuration Registers

The configuration registers are maintained in a separate document.

2.2 Description Notes

- R – Bit location is read by software
- R0- Bit location is read by software and always returns 0 when read
- R1 - Bit location is read by software and always returns 1 when read
- R0W – Bit location is read by software and always returns 0 when read. Bit location can also be written by software.
- RCS – Bit location is read. Writing a 1 to the bit clears the field. The bit is synchronously updated.
- RS – Bit location is read by software and is synchronously updated
- RW – Bit location is read and written by software
- RWS - Bit location is read and written by software. Bit is synchronously updated.
- RM – Read, write to 1 modify. The result of the write depends on which CPU (internal or external) performed the write. This function is used for CPU communication interrupts. For the external CPU interrupts, a write from the internal CPU sets the bit. A write from the external CPU clears the bit. For the internal CPU interrupts, a write from the internal CPU clears the bit. A write from the external CPU sets the bit.

2.3 CFR Address Ranges (Offset from CFR Base Address)

The CFR Base Address is offset 10 0000 hex.

Table 47. CFR Address Ranges

Name	Starting Address Offset (hex)	Ending Address Offset (hex)
SYS	000	09F
LLC	0A0	0FF
IsoDP0	100	22F
IsoDP1	230	35F
Aud0	360	3DF
Aud1	3E0	45F
AsyTx0	460	4AF
AsyTx1	4B0	4FF
AsyRx0	500	54F
AsyRx1	550	59F
BrdCstRx	5A0	5DF
PLL	5E0	62F

2.4 Register Access

The IntCPUCfg.CFRLock bit is included to lock the ex-CPU from all DTCP related registers. When this bit is set to 1, the ex-CPU cannot access these registers.

All register accesses by the external CPU are 32 bits. During reads, a snap shot value is used for both the lower and upper 16-bit accesses. This snap shot value is created during the first access to the register. It expires after a short amount of time.

For the internal ARM, some registers have restricted accesses.

- 32-bit access only. These registers can only be accessed 32 bits at a time.
  - CycTmr
  - AsyTx*AckBuffer
  - Anc*Data
- 32-bit write access while the associated function is being used. 32-/16-/8-bit access during read accesses and when the associated function is not being used.
  - Iso*TmStmp
  - Iso*CIP1
  - Iso*FltrCIP1
  - Iso*MskCIP1
  - PLL*Cfg2
  - PLL*Cfg3
  - PLL*Cfg4
  - PLL*Cfg5
  - Aud*NoData
- 16-bit write access while the associated function is being used. 32-/16-/8-bit access during all read accesses and while the associated function is not being used
  - Timer0
  - Timer1
  - Timer2
  - BusRstDat (read only register)
  - Iso0BufStat
  - HSDI0Cfg
  - Iso*WtrMrk
  - Iso*Hdr
  - Iso*FltrIsoHdr
  - Iso*MskIsoHdr
  - Iso*DVTmgCtl
  - Iso*DVTmgCfg
  - Anc*Data
  - Anc*Def
  - Anc*Data1
  - Anc*Data2
  - Anc*NoData
  - AsyRx*WtrMrk
  - AsyTx*WtrMrk
  - AsyTx*StrmHdr

3 General Information

3.1 Package Size

The iceLynx-Micro includes two package pinout options: 176-pin MicroStar BGA and 176-pin QFP.

3.2 Operating Voltage

Min Voltage	Nominal Voltage	Max Voltage
3 V	3.3 V	3.6 V

Note: I/Os are not 5-V tolerant.

3.3 Operating Temperature

		MIN	NOM	MAX	Unit
Operating ambient temperature	Commercial	-20		70	°C
	Industrial	-40		85	°C

4 Absolute Maximum Ratings Over Operating Temperature Ranges†

Supply voltage range: ..... AV_{DD}	- 0.3 V to 4 V
V_{DD}	- 0.3 V to 4 V
PLL_V_{DD}	- 0.3 V to 4 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) (see Note 2)	± 20 mA
Electrostatic discharge (see Note 3)	HBM: 2 kV
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A (Commercial)	-20°C to 70°C
(Industrial)	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from cage for 10 seconds	260°C

† Stresses beyond those listed under the absolute maximum ratings causes' permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods affects device reliability.

NOTES: 1. Applies to external input and bidirectional buffers.
2. Applies to external output and bidirectional buffers.
3. HBM is human body model, MM is machine model.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
μ*BGA 176 #	1.1 W	13.8 mW/°C	0.5 W	0.3 W
μ*BGA 176 *	0.8 W	10.4 mW/°C	0.4 W	-
TQFP 176 #	1.8 W	22.6 mW/°C	0.8 W	-
TQFP 176 *	1.3 W	16.5 mW/°C	0.6 W	-

Notes: 1) *: Standard JEDEC Low-K board
2) #: Standard JEDEC High-K board

4.1 Recommended Operating Conditions (Analog IEEE 1394 I/F)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
Analog voltage, AV_{dd}			3	3.3	3.6	V
Supply voltage, V_{dd}			3	3.3	3.6	V
PLL supply voltage, PLL_V_{dd}			2.7	3	3.6	V
Output voltage, V_O	LVCMOS terminals		0		V_{DD}	V
High-level input voltage, V_{IH}†	LVCMOS terminals		2		V_{DD}	V
Low-level input voltage, V_{IL}†	LVCMOS terminals		0		0.8	V
Output current, I_O	TPBIAS outputs		-5.6		1.3	mA
Differential input voltage, V_{ID}	Cable inputs, during data reception		118		260	mV
	Cable inputs, during arbitration		168		265	
Common-mode input voltage, V_{IC}	TPB cable inputs, source power node		0.9706		2.515	V
	TPB cable inputs, nonsource power node		0.4706		2.015	
Maximum junction temperature, T_J	176-PQFP high-K JEDEC board $R\theta_{JA}$ =44.3°C /W, T_A = 70°C, P_D = 0.6 W			96.6		°C
	176-PQFP low-K JEDEC board $R\theta_{JA}$ = 60.8°C /W, T_A = 70°C, P_D = 0.6 W			107		
	176-u*BGA high-K JEDEC board $R\theta_{JA}$ = 72.5°C /W, T_A = 70°C, P_D = 0.6 W			113		
	176-u*BGA low-K JEDEC board $R\theta_{JA}$ = 96.7°C /W, T_A = 70°C, P_D = 0.6 W			128		
	176-u*BGA high-K JEDEC board $R\theta_{JA}$ =72.5°C /W, T_A = 85°C, P_D = 0.6 W			128		
Power-up reset time, t_{pu}	RESETn input		2			ms
Power-up reset time, t_{pu}	RESET_ARMn input					ms
Receive input jitter	TPA, TPB cable inputs, S100 operation				±1.08	ns
	TPA, TPB cable inputs, S200 operation				±0.5	ns
	TPA, TPB cable inputs, S400 operation				±0.315	ns
Receive input skew	Between TPA and TPB cable inputs, S100 operation				±0.8	ns
	Between TPA and TPB cable inputs, S200 operation				±0.55	ns
	Between TPA and TPB cable inputs, S400 operation				±0.5	ns

† Applies to external inputs and bidirectional buffers without hysteresis.
§ Applies to external output buffers.
¶ For a node that does not source power; see Section 4.2.2.2 in IEEE Std 1394a–2000.

4.2 Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER			OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage			I_{OH} = -2 mA	2.4		V
V_{OL}	Low-level output voltage			I_{OL} = 6 mA		0.5	V
I_{OZ}	3-state output high impedance	Output pins	3.6 V	V_O = V_{DD} or GND		±20	µA
I_{IL}	Low-level input current	Input pins	3.6 V	V_I = GND		±20	µA
		I/O pins†	3.6 V	V_I = GND	±20		
I_{IH}	High-level input current		3.6 V	V_I = V_{dd}	±20		µA

† For I/O terminals, input leakage (I_{IL} and I_{IH}) includes I_{OZ} of the disabled output.

4.3 Electrical Characteristics Over Recommended Ranges of Operating Conditions (Unless Otherwise Noted)

4.3.1 Device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{dd}	Supply current (internal voltage regulator enabled, REG_ENn = L)	See Note 4		180		mA
V_{TH}	Power status threshold, CPS input†	400-kΩ resistor†	4.7		7.5	V
V_O	TPBIAS output voltage	At rated I_O current	1.665		2.015	V
I_{IRST}	Pullup current (RESETn input)	V_I = 1.5 V	-90		-20	µA
		V_I = 0 V	-90		-20	

† Measured at cable power side of resistor.

NOTES: 4. Conditions:
VDD = 3.3 V
HSDI0: MPEG TS Tx (mode-7)
HSDI1: Audio Rx (IEC60958, 44.1 kHz)
Three Ports Connected
Cipher not enabled
ARM: Application PGM running

4.3.2 Driver

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OD}	Differential output voltage	56 Ω, see Figure 49	172	265	mV
I_{DIFF}	Driver difference current, TPA+, TPA-, TPB+, and TPB-	Drivers enabled, speed signaling off	-1.05‡	1.05‡	mA
I_{SP200}	Common-mode speed signaling current, TPB+, TPB-	S200 speed signaling enabled	-4.84§	-2.53§	mA
I_{SP400}	Common-mode speed signaling current, TPB+, TPB-	S400 speed signaling enabled	-12.4§	-8.10§	mA
V_{OFF}	Off-state differential voltage	Drivers disabled, see Figure 49		20	mV

‡ Limits defined as algebraic sum of TPA+ and TPA- driver currents. Limits also apply to TPB+ and TPB - algebraic sum of driver currents.

§ Limits defined as absolute limit of each of TPB+ and TPB - driver currents.

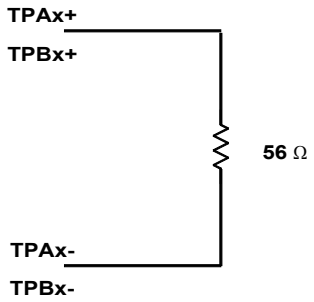


Figure 49. Test Load Diagram

4.3.3 Receiver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{ID}	Differential impedance	Drivers disabled	4	7	10	kΩ
					4	pF
Z_{IC}	Common-mode impedance	Drivers disabled	20			kΩ
					24	pF
V_{TH-R}	Receiver input threshold voltage	Drivers disabled	-30		30	mV
V_{TH-CB}	Cable bias detect threshold, TPBx cable inputs	Drivers disabled	0.6		1	V
V_{TH}+	Positive arbitration comparator threshold voltage	Drivers disabled	89		168	mV
V_{TH}-	Negative arbitration comparator threshold voltage	Drivers disabled	-168		-89	mV
$V_{TH-SP200}$	Speed signal threshold	TPBIAS-TPA common-mode voltage, drivers disabled	49		131	mV
$V_{TH-SP400}$	Speed signal threshold	TPBIAS-TPA common-mode voltage, drivers disabled	314		396	mV

4.4 Thermal Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
176-µBGA	$R\theta_{JA}$ high-K board	Board mounted, no air flow, JEDEC test board			63.93	°C/W
176-µBGA	$R\theta_{JA}$ low-K board	Board mounted, no air flow, JEDEC test board			82.1	°C/W
176-PQFP	$R\theta_{JA}$ high-K board	Board mounted, no air flow, JEDEC test board			44.3	°C/W
176-PQFP	$R\theta_{JA}$ low-K board	Board mounted, no air flow, JEDEC test board			60.8	°C/W

4.5 Switching Characteristics for PHY Port Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Jitter, transmit	Between TPA and TPB			±0.15	ns
	Skew, transmit	Between TPA and TPB			±0.1	ns
t_r	TP differential rise time, transmit	10% to 90%, at 1394 connector	0.5		1.2	ns
t_f	TP differential fall time, transmit	90% to 10%, at 1394 connector	0.5		1.2	ns

4.6 Operating, Timing, and Switching Characteristics of XI

PARAMETER		MIN	TYP	MAX	UNIT
V_{DD}	PLL_V_{DD}	3	3.3	3.6	V
V_{IH}	High-level input voltage		0.63 V_{DD}		V
V_{IL}	Low-level input voltage			0.33 V_{DD}	V
	Input clock frequency		24.576		MHz
	Input clock frequency tolerance			<100	ppm
	Input slew rate	0.2		4	V/ns
	Input clock duty cycle	40%		60%	

Note: When using an external clock, the input is supplied to XI, the XO terminal must be left unconnected, and the XI clock must be stable before the 2-ms device reset begins.

5 Reset Power States

Table 48. Pin State During Power On Reset, Just After Power On Reset and DISABLE_IFn=L

Pin Name	RESETn=L and DISABLE_IFn=L During Power On	RESETn=H and DISABLE_IFn=H Just After Power On	RESETn=H and DISABLE_IFn=L DISABLE_IFn=L
WTCH_DG_TMRn	High Z	0	High Z
LOW_PWR_RDY	0	0	0
MCIF_INTz	High Z	1	High Z
MCIF_CS_IOz=	High Z	High Z	High Z
MCIF_CS_MEMz	High Z	High Z	High Z
MCIF_ACKz	High Z	High Z	High Z
MCIF_WAITz	High Z	High Z	High Z
MCIF_DATA[15:0]	High Z	High Z	High Z
HSDI*_D[0]	High Z	High Z	High Z
HSDI*_D[7:1]	High Z	High Z	High Z
HSDI*_EN	High Z	High Z	High Z
HSDI*_SYNC	High Z	High Z	High Z
HSDI*_DVALID	High Z	High Z	High Z
HSDI*_AV	High Z	0	High Z
HSDI*_AMCLK_OUT	High Z	High Z	High Z
HSDI1_AUDIO_ERR	High Z	High Z	High Z
HSDI1_AUDIO_MUTE	High Z	High Z	High Z
MLPCM_LRCLK	High Z	High Z	High Z
MLPCM_BCLK	High Z	High Z	High Z
MLPCM_D{2:0]	High Z	High Z	High Z
MLPCM_A	High Z	High Z	High Z
HSDI*_60958_OUT	High Z	High Z	High Z

Note: All CFR values are the default value.

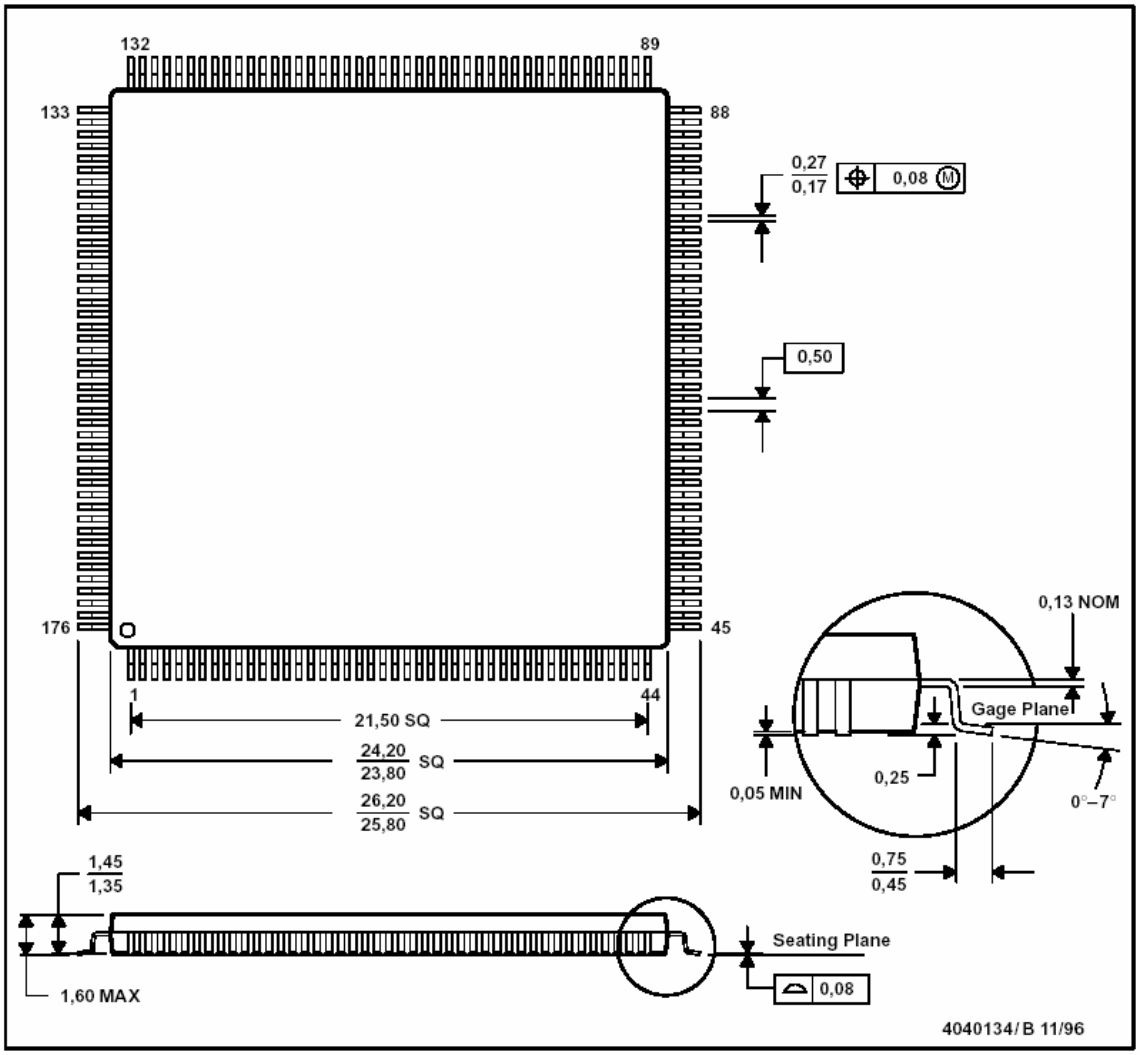
6 Configuration Register Map

See Appendix A for the configuration register map and descriptions.

7 Mechanical Data

7.1 PQFP Package Information

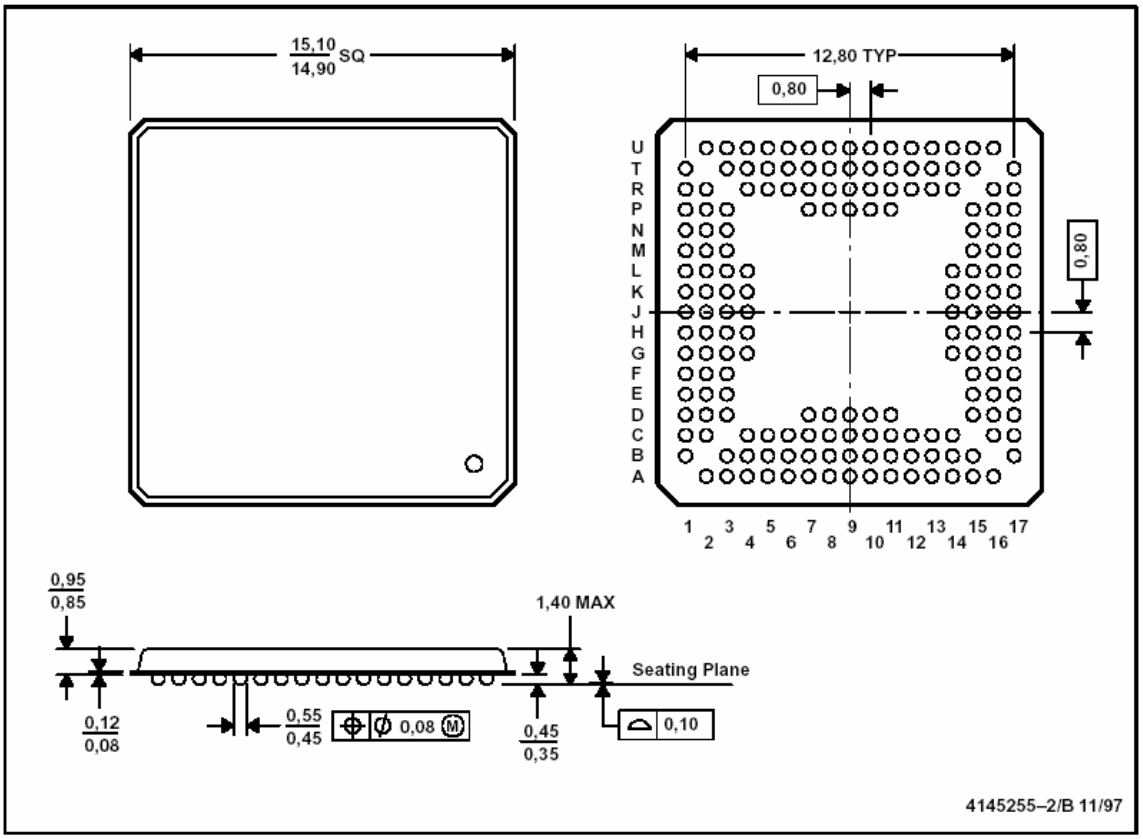
PGF (S-PQFP-G176) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

7.2 μ*BGA Package Dimensions

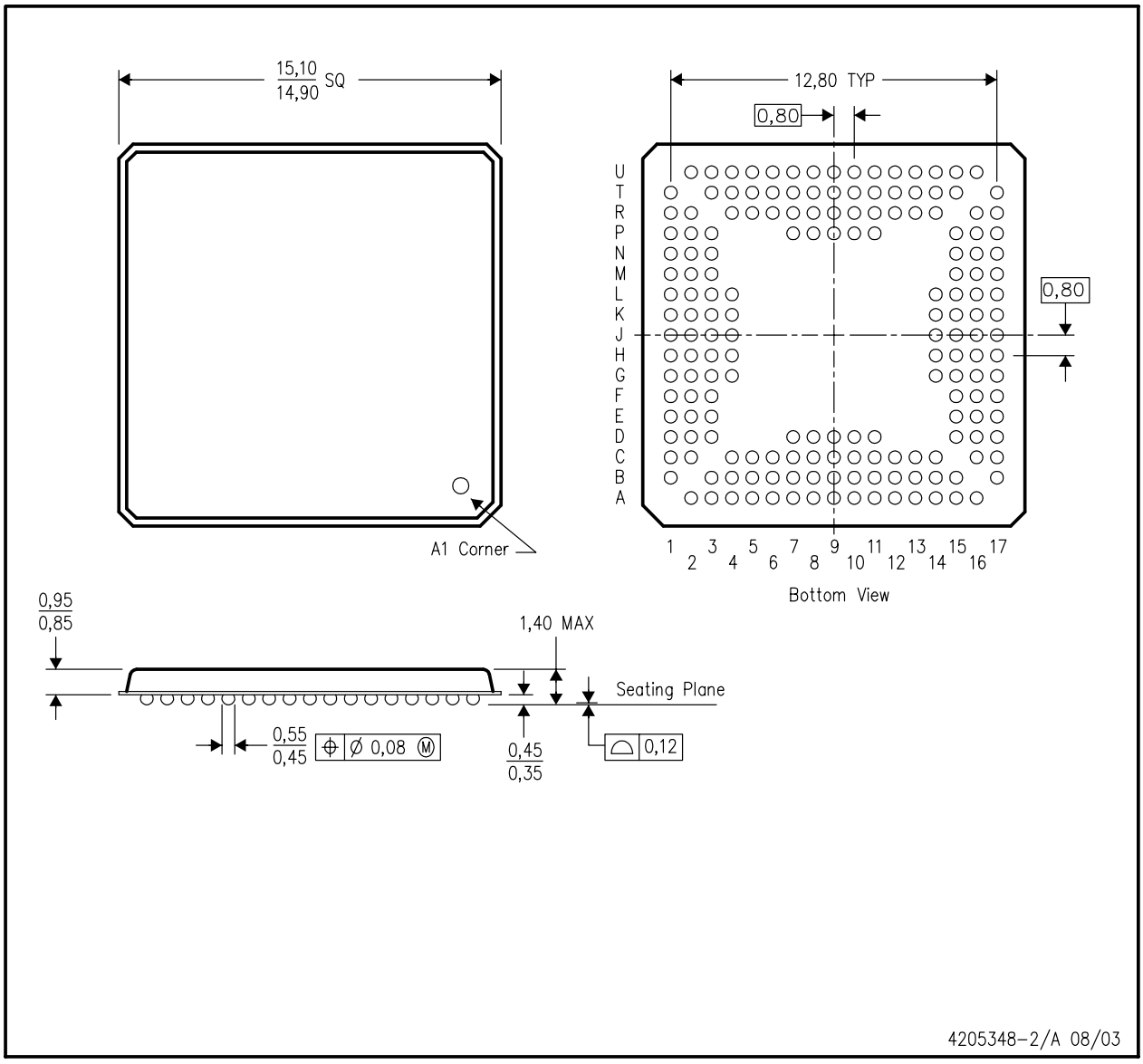
GGW (S-PBGA-N176) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

7.3 ZGW Package Dimensions

ZGW (S–PBGA–N176) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration
D. This package is lead–free.