

The RF Sub-Micron MOSFET Line **RF Power Field Effect Transistor** N-Channel Enhancement-Mode Lateral MOSFET

Designed for W-CDMA base station applications with frequencies from 1930 to 1990 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts, $I_{DQ} = 2 \times 800$ mA, $f_1 = 1955$ MHz, $f_2 = 1965$ MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @ $f_1 - 5$ MHz and $f_2 + 5$ MHz. Distortion Products Measured over a 3.84 MHz BW @ $f_1 - 10$ MHz and $f_2 + 10$ MHz, Each Carrier Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.

Output Power — 38 Watts Avg.

Power Gain — 14 dB

Efficiency — 26%

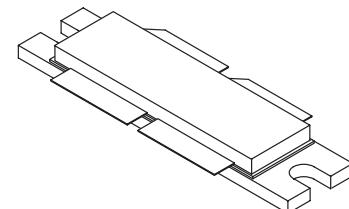
IM3 — -37.5 dBc

ACPR — -41 dBc

- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 1960 MHz, 120 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Qualified Up to a Maximum of 32 V_{DD} Operation
- In Tape and Reel. R6 Suffix = 150 Units per 56 mm, 13 inch Reel.

MRF5P20180R6

1990 MHz, 38 W AVG.,
 2 x W-CDMA, 28 V
**LATERAL N-CHANNEL
 RF POWER MOSFET**



CASE 375D-04, STYLE 1
 NI-1230

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	407 2.3	Watts $W/\text{^\circ C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$
CW Operation	CW	120	Watts

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 120 W CW Case Temperature 80°C, 38 W CW	$R_{\theta JC}$	0.43 0.43	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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ESD PROTECTION CHARACTERISTICS

Test Conditions		Class			
Human Body Model		2 (Minimum)			
Machine Model		M3 (Minimum)			
Charge Device Model		C7 (Minimum)			

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (1)

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65 \text{ Vdc}$, $V_{GS} = 0 \text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28 \text{ Vdc}$, $V_{GS} = 0$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5 \text{ Vdc}$, $V_{DS} = 0 \text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage ($V_{DS} = 10 \text{ Vdc}$, $I_D = 200 \mu\text{Adc}$)	$V_{GS(\text{th})}$	2.5	2.7	3.5	Vdc
Gate Quiescent Voltage ($V_{DS} = 28 \text{ Vdc}$, $I_D = 850 \text{ mA}$)	$V_{GS(Q)}$	—	3.6	—	Vdc
Drain-Source On-Voltage ($V_{GS} = 10 \text{ Vdc}$, $I_D = 2 \text{ Adc}$)	$V_{DS(\text{on})}$	—	0.26	0.3	Vdc
Forward Transconductance ($V_{DS} = 10 \text{ Vdc}$, $I_D = 2 \text{ Adc}$)	g_{fs}	—	5	—	S

DYNAMIC CHARACTERISTICS (1)

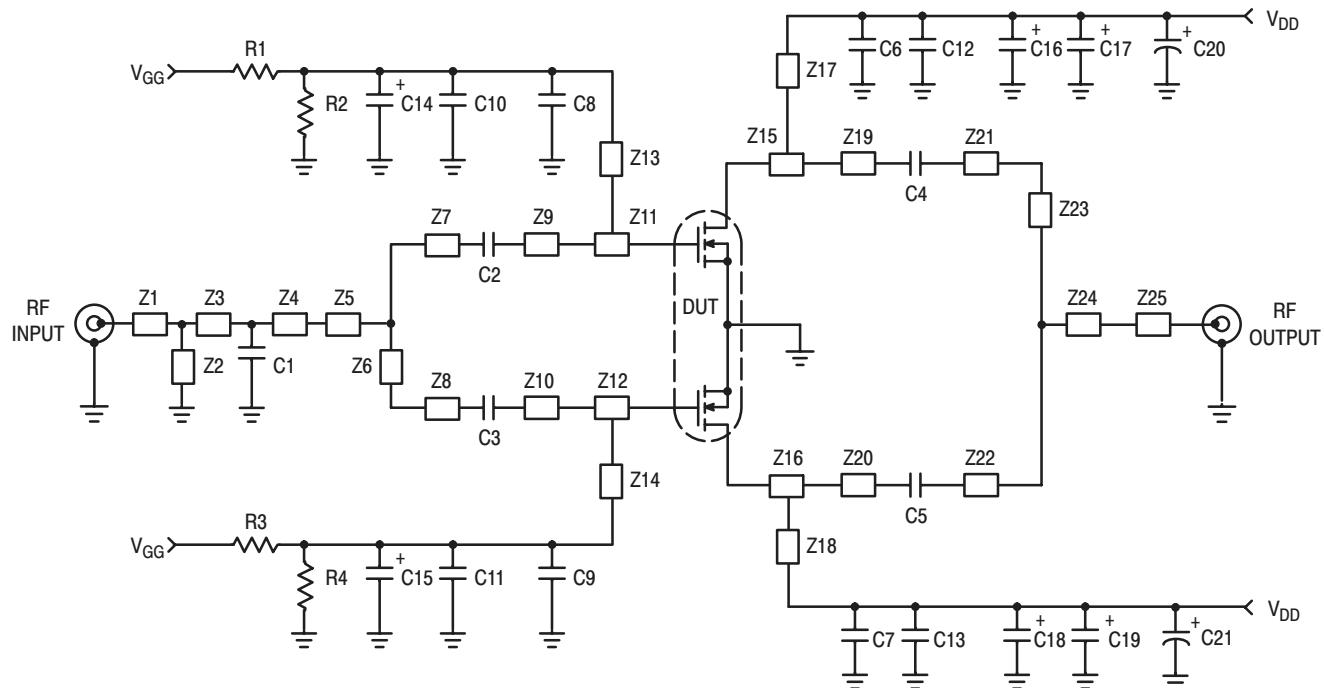
Reverse Transfer Capacitance ($V_{DS} = 28 \text{ Vdc} \pm 30 \text{ mV(rms)}$ ac @ 1 MHz, $V_{GS} = 0 \text{ Vdc}$)	C_{rss}	—	1.7	—	pF
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FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) 2-carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR and IM3 measured in 3.84 MHz Bandwidth. Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.

Common-Source Amplifier Power Gain ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 38 \text{ W Avg.}$, $I_{DQ} = 2 \times 800 \text{ mA}$, $f_1 = 1932.5 \text{ MHz}$, $f_2 = 1942.5 \text{ MHz}$ and $f_1 = 1977.5 \text{ MHz}$, $f_2 = 1987.5 \text{ MHz}$)	G_{ps}	12.5	14	—	dB
Drain Efficiency ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 38 \text{ W Avg.}$, $I_{DQ} = 2 \times 800 \text{ mA}$, $f_1 = 1932.5 \text{ MHz}$, $f_2 = 1942.5 \text{ MHz}$ and $f_1 = 1977.5 \text{ MHz}$, $f_2 = 1987.5 \text{ MHz}$)	η	23	26	—	%
Third Order Intermodulation Distortion ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 38 \text{ W Avg.}$, $I_{DQ} = 2 \times 800 \text{ mA}$, $f_1 = 1932.5 \text{ MHz}$, $f_2 = 1942.5 \text{ MHz}$ and $f_1 = 1977.5 \text{ MHz}$, $f_2 = 1987.5 \text{ MHz}$; IM3 measured over 3.84 MHz BW @ $f_1 - 10 \text{ MHz}$ and $f_2 + 10 \text{ MHz}$ referenced to carrier channel power.)	IM3	—	-37.5	-35	dBc
Adjacent Channel Power Ratio ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 38 \text{ W Avg.}$, $I_{DQ} = 2 \times 800 \text{ mA}$, $f_1 = 1932.5 \text{ MHz}$, $f_2 = 1942.5 \text{ MHz}$ and $f_1 = 1977.5 \text{ MHz}$, $f_2 = 1987.5 \text{ MHz}$; ACPR measured over 3.84 MHz BW @ $f_1 - 5 \text{ MHz}$ and $f_2 + 5 \text{ MHz}$.)	ACPR	—	-41	-38	dBc
Input Return Loss ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 38 \text{ W Avg.}$, $I_{DQ} = 2 \times 800 \text{ mA}$, $f_1 = 1932.5 \text{ MHz}$, $f_2 = 1942.5 \text{ MHz}$ and $f_1 = 1977.5 \text{ MHz}$, $f_2 = 1987.5 \text{ MHz}$)	IRL	—	-16	-9	dB

(1) Each side of device measured separately. Part is internally matched both on input and output.

(2) Measurements made with device in push-pull configuration.



Z1	0.081" x 1.126" Microstrip	Z11, Z12	0.341" x 0.945" Microstrip
Z2	0.079" x 0.138" Microstrip	Z13, Z14	0.035" x 0.913" Microstrip
Z3	0.081" x 0.091" Microstrip	Z15, Z16	0.581" x 0.823" Microstrip
Z4	0.081" x 0.117" Microstrip	Z17, Z18	0.059" x 1.057" Microstrip
Z5, Z24	0.134" x 0.874" Microstrip	Z19, Z20	0.081" x 0.046" Microstrip
Z6, Z23	0.081" x 2.269" Microstrip	Z21, Z22	0.081" x 0.126" Microstrip
Z7, Z8	0.081" x 0.118" Microstrip	Z25	0.081" x 0.793" Microstrip
Z9, Z10	0.081" x 0.079" Microstrip	PCB	Taconic TLX8-0300, 0.030", $\epsilon_r = 2.55$

Figure 1. MRF5P20180 Test Circuit Schematic

Table 1. MRF5P20180 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1	1.8 pF 100B Chip Capacitor	100B1R8BW	ATC
C2, C3, C4, C5, C6, C7	10 pF 100B Chip Capacitors	100B100GW	ATC
C8, C9	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C10, C11, C12, C13	10 nF 200B Chip Capacitors	200B103MW	ATC
C14, C15, C16, C17, C18, C19	22 μ F, 35 V Tantalum Capacitors	TAJE226M035	AVX
C20, C21	220 μ F, 63 V Electrolytic Capacitors	13668221	Philips
R1, R2, R3, R4	10 k Ω Chip Resistors (1206)		

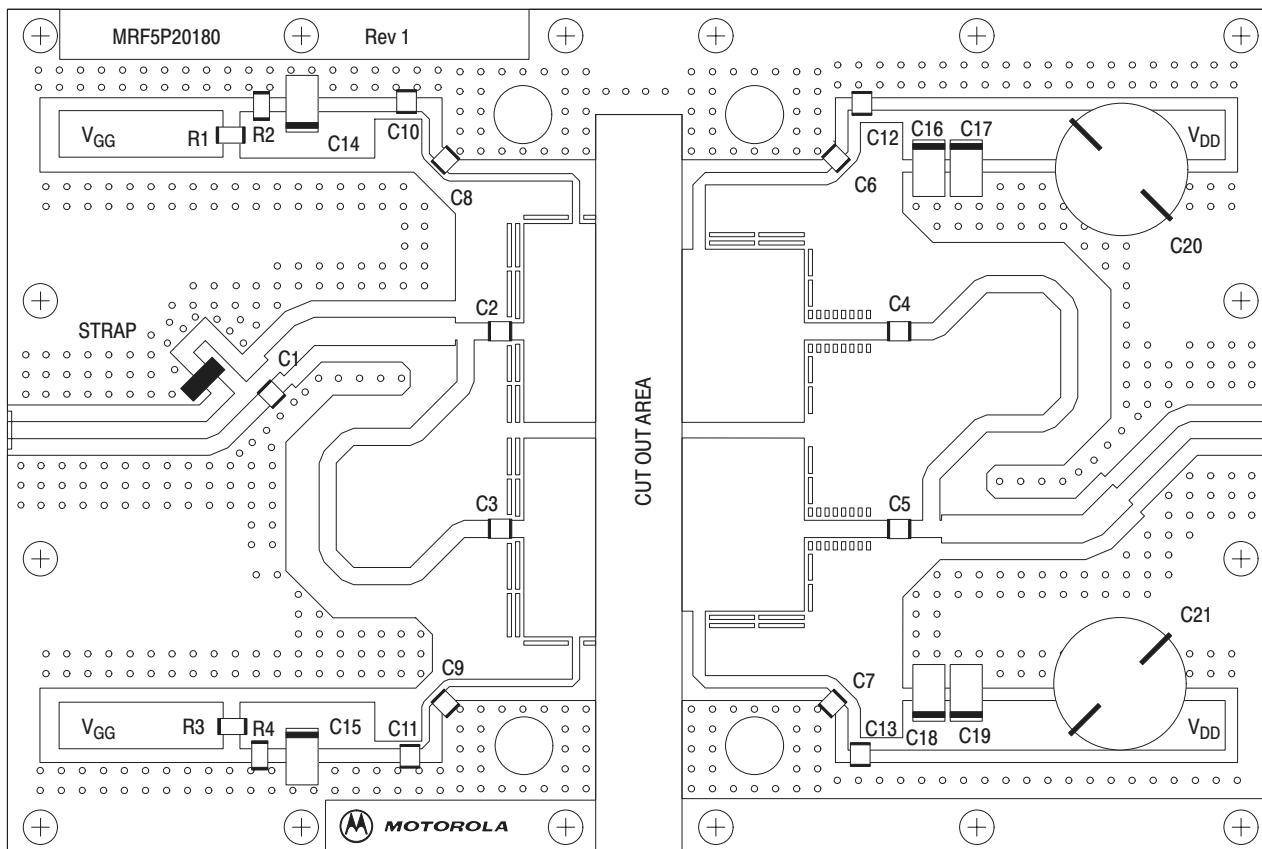


Figure 2. MRF5P20180 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

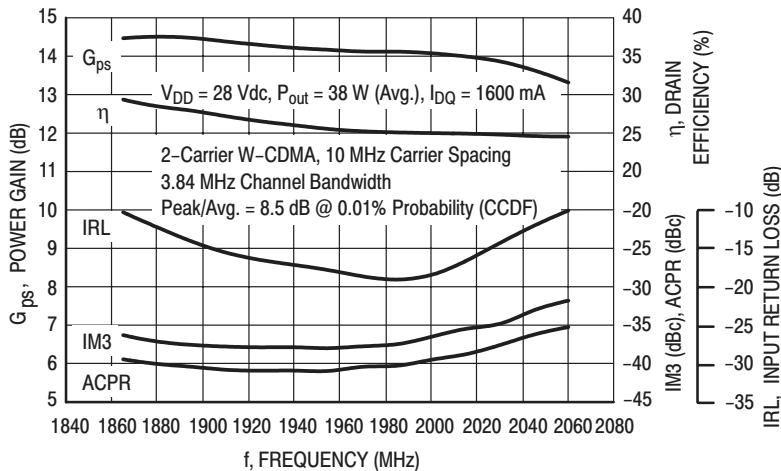


Figure 3. 2-Carrier W-CDMA Broadband Performance

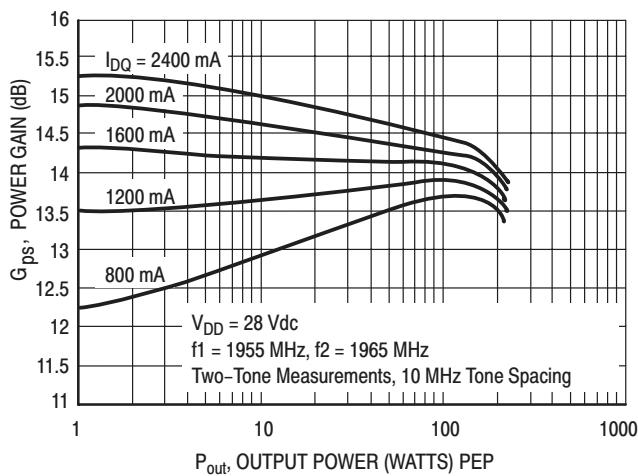


Figure 4. Two-Tone Power Gain versus Output Power

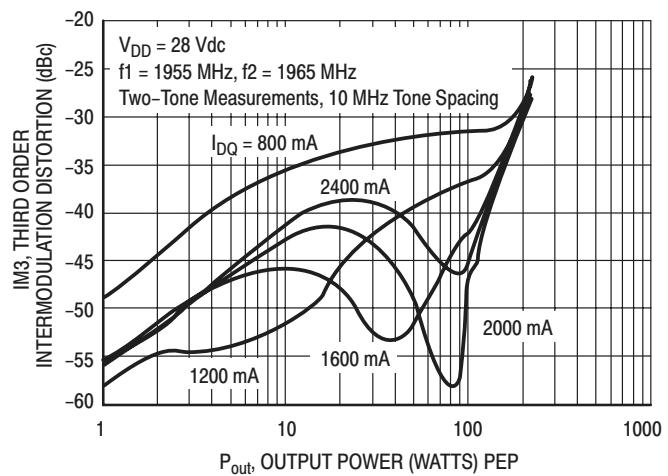


Figure 5. Third Order Intermodulation Distortion versus Output Power

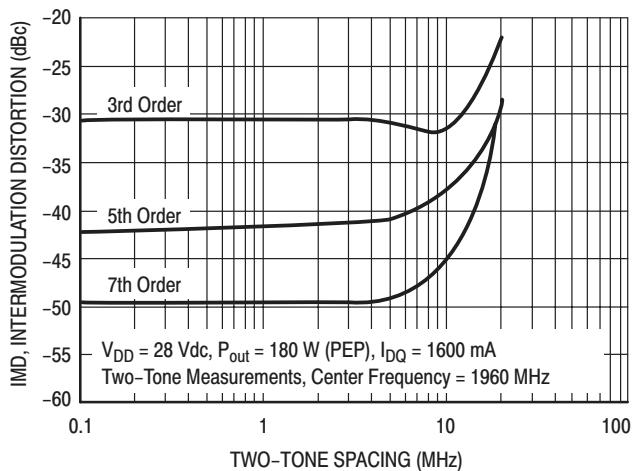


Figure 6. Intermodulation Distortion Products versus Tone Spacing

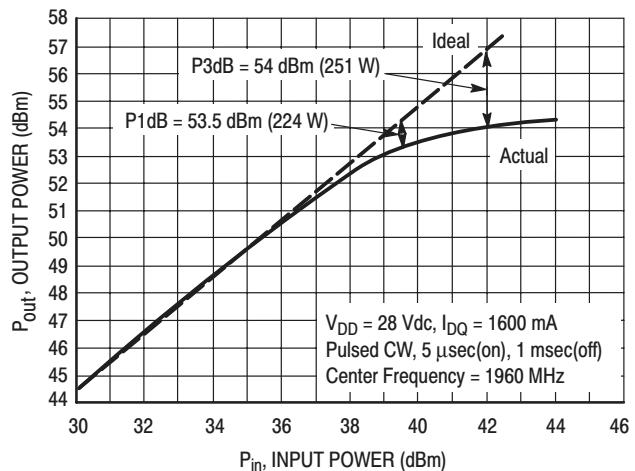


Figure 7. Pulse CW Output Power versus Input Power

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TYPICAL CHARACTERISTICS

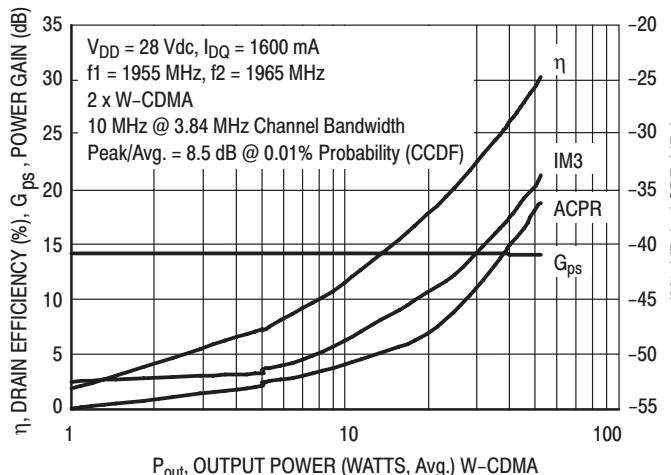


Figure 8. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

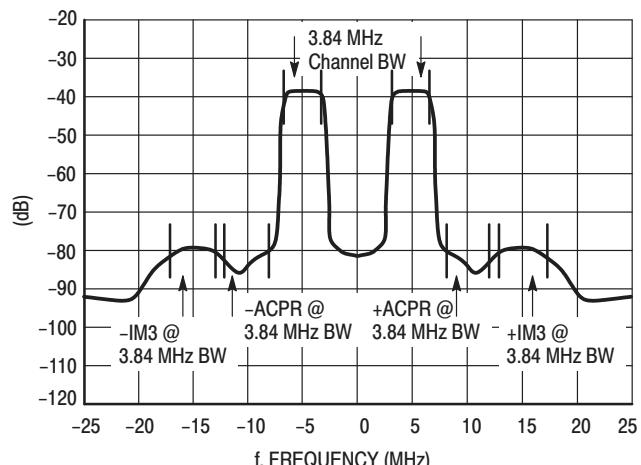


Figure 9. 2-Carrier W-CDMA Spectrum

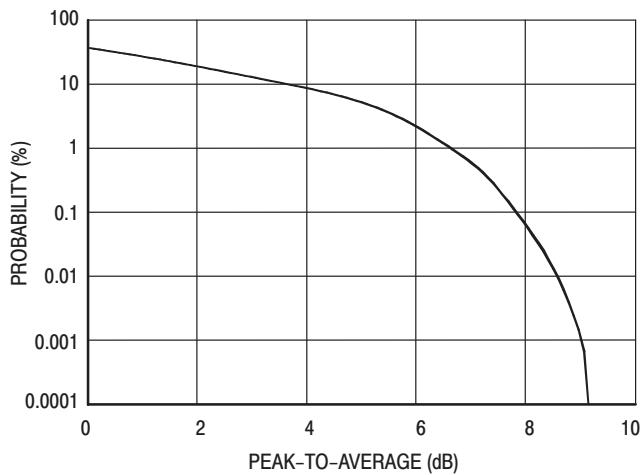
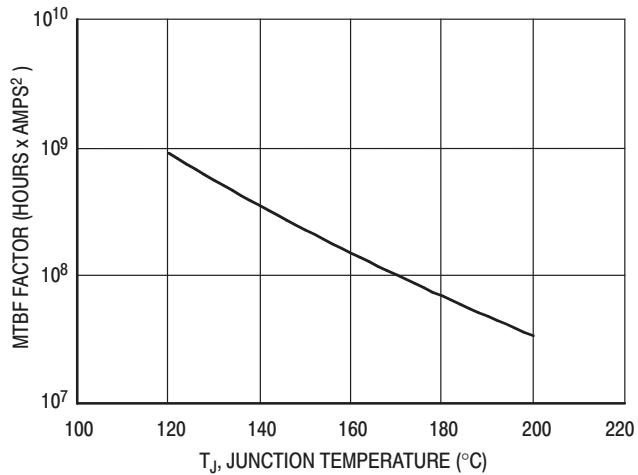
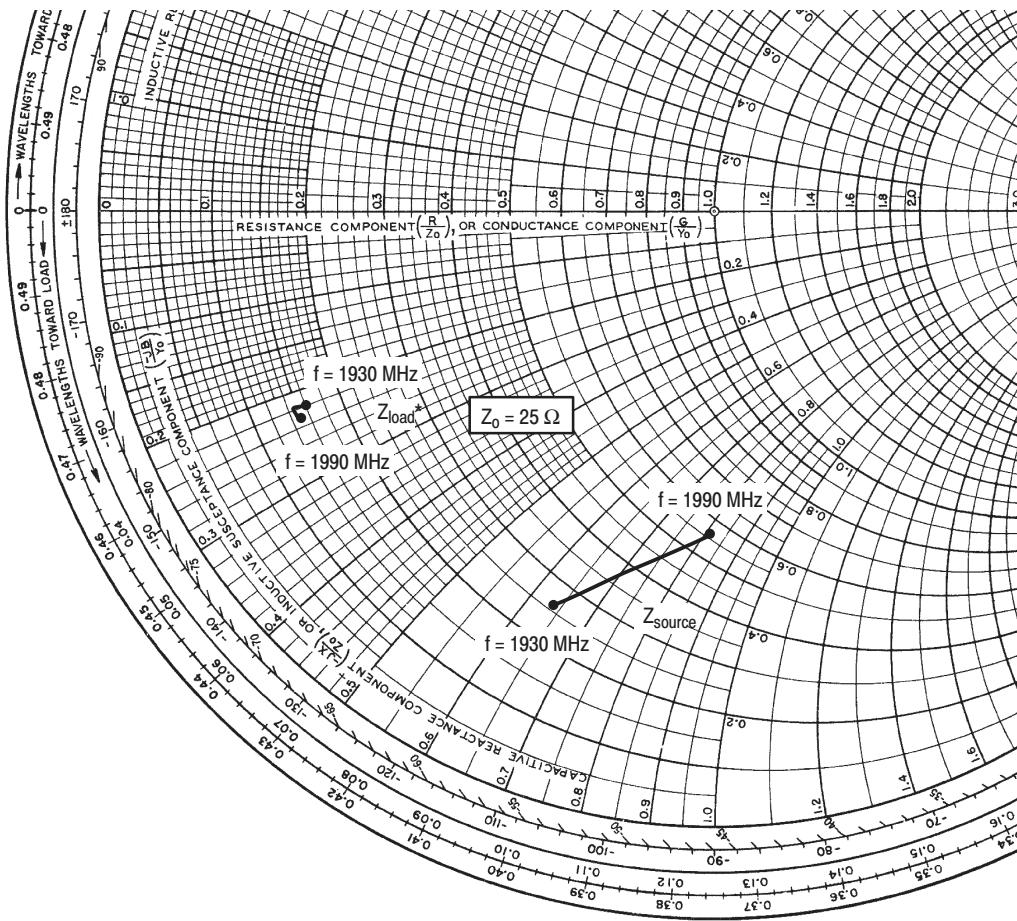


Figure 10. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCCH, 67% Clipping, Single Carrier Test Signal



This above graph displays calculated MTBF in hours \times ampere 2 drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 11. MTBF Factor versus Junction Temperature



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 2 \times 800 \text{ mA}$, $P_{out} = 38 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
1930	$6.54 - j16.04$	$4.06 - j5.56$
1960	$9.70 - j17.92$	$3.70 - j5.48$
1990	$13.88 - j20.46$	$3.64 - j5.76$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

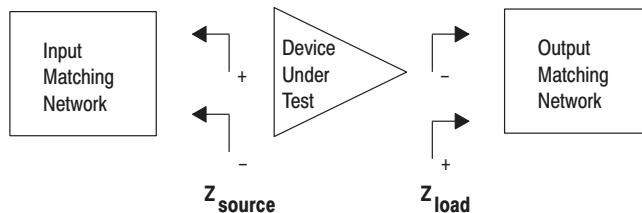
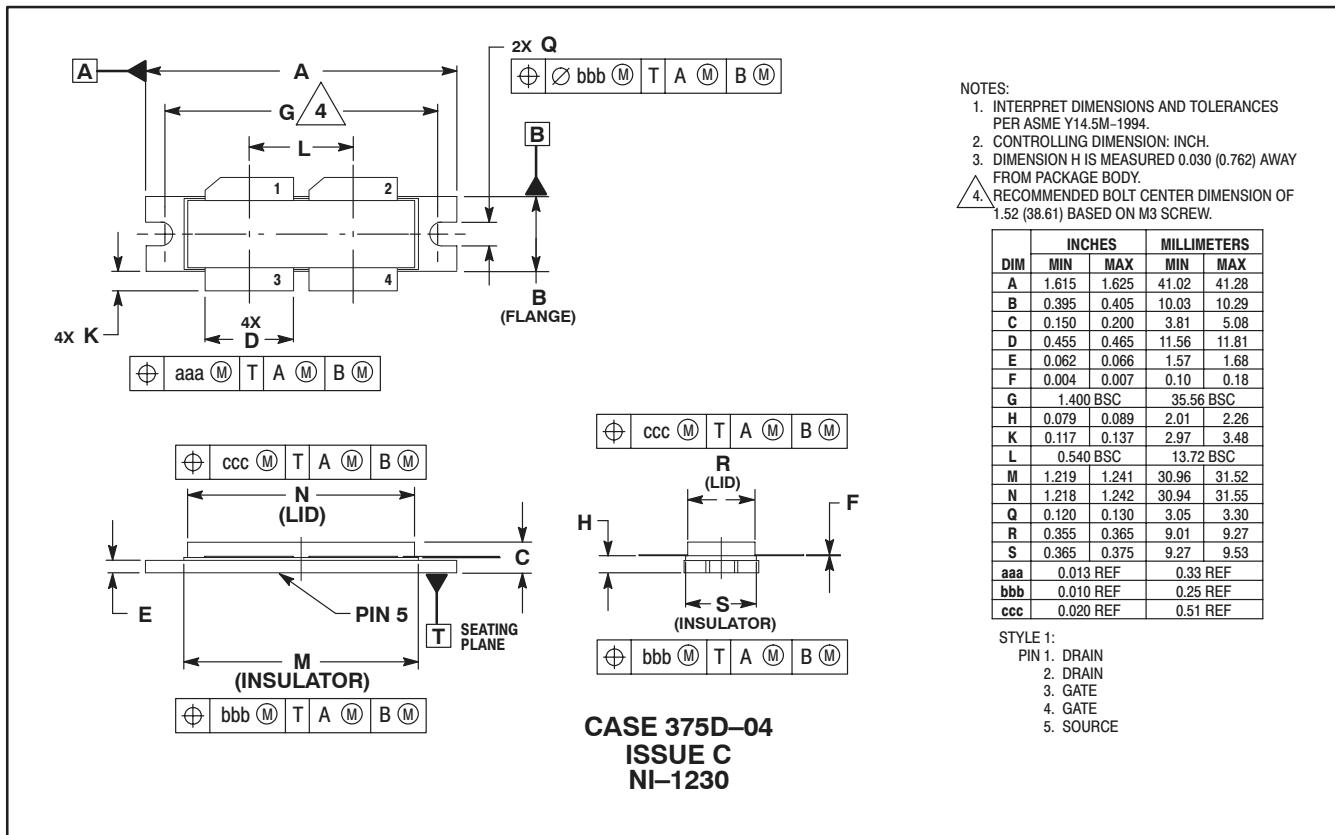


Figure 12. Series Equivalent Input and Output Impedance

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PACKAGE DIMENSIONS



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