

RTR025P02

- 1) Low On-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small and Surface Mount Package (TSMT3).

Power switching, DC / DC converter.

Silicon P-channel
MOS FET

Type	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	3000
RTR025P02		○

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	-20	V
Gate-source voltage		V_{GSS}	± 12	V
Drain current	Continuous	I_D	± 2.5	A
	Pulsed	I_{DP} ^{*1}	± 10	A
Source current (Body diode)	Continuous	I_S	-0.8	A
	Pulsed	I_{SP} ^{*1}	-3.2	A
Total power dissipation		P_D ^{*2}	1.0	W
Channel temperature		T_{ch}	150	°C
Range of Storage temperature		T_{stg}	-55 to +150	°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$
*2 Mounted on a ceramic board

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth (ch-A)	125	°C / W

Technical drawing of a TSMT3 package showing top and side views with dimensions.

Top View Dimensions:

- Overall width: 2.9 ± 0.1
- Lead width: 0.4 ± 0.1 (Note: Each lead has same dimensions)
- Lead pitch: 0.95
- Overall length: 1.9 ± 0.2
- Body width: 1.6 ± 0.1
- Lead thickness: 0.16 ± 0.06

Side View Dimensions:

- Maximum height: 1.0 MAX.
- Lead height: 0.85 ± 0.1
- Lead thickness: 0.7 ± 0.1
- Lead width: 0.3 ± 0.6
- Lead angle: $0-91^\circ$

Each lead has same dimensions

Abbreviated symbol : TY

(1) Gate
(2) Source
(3) Drain

*1 ESD PROTECTION DIODE
*2 BODY DIODE

Transistors

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	±10	μA	$V_{GS}=±12V$, $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	−20	—	—	V	$I_D = -1mA$, $V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	—	—	−1	μA	$V_{DS} = -20V$, $V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	−0.7	—	−2.0	V	$V_{DS} = -10V$, $I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	70	95	mΩ	$I_D = -2.5A$, $V_{GS} = -4.5V$
		—	75	105	mΩ	$I_D = -2.5A$, $V_{GS} = -4.0V$
		—	115	160	mΩ	$I_D = -1.25A$, $V_{GS} = -2.5V$
Forward transfer admittance	$ Y_{fs} $ *	2.3	—	—	S	$V_{DS} = -10V$, $I_D = -1.2A$
Input capacitance	C_{iss}	—	630	—	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	—	110	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	—	75	—	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	12	—	ns	$I_D = -1.25A$
Rise time	t_r *	—	18	—	ns	$V_{DD} = -15V$
Turn-off delay time	$t_{d(off)}$ *	—	50	—	ns	$V_{GS} = -4.5V$
Fall time	t_f *	—	20	—	ns	$R_L=12Ω$ $R_{GS}=10Ω$
Total gate charge	Q_g	—	7	—	nC	$V_{DD} = -15V$
Gate-source charge	Q_{gs}	—	1.5	—	nC	$V_{GS} = -4.5V$
Gate-drain charge	Q_{gd}	—	2.0	—	nC	$I_D = -2.5A$

*Pulsed

Body diode characteristics (source-drain characteristics)

Forward voltage	V_{SD}	—	—	−1.2	V	$I_S = -0.8A$, $V_{GS}=0V$
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Transistors

●Electrical characteristic curves

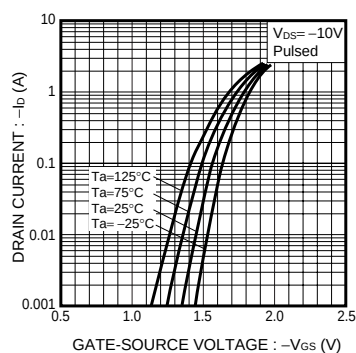


Fig.1 Typical Transfer Characteristics

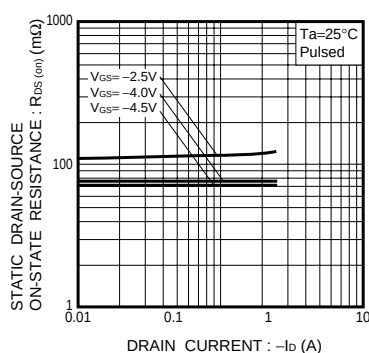


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

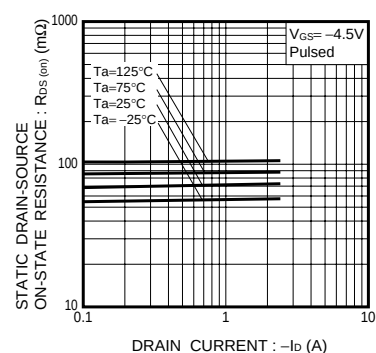


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

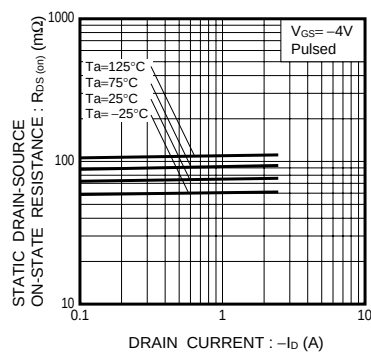


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

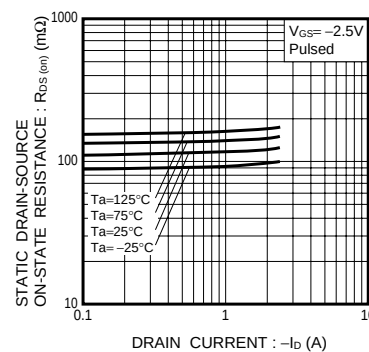


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

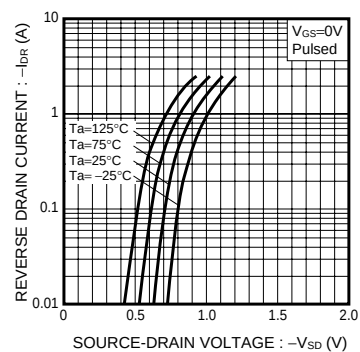


Fig.6 Reverse Drain Current vs. Source-Drain Voltage

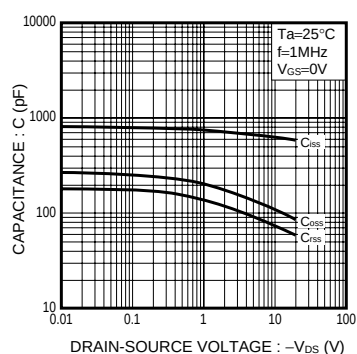


Fig.7 Typical Capacitance vs. Drain-Source Voltage

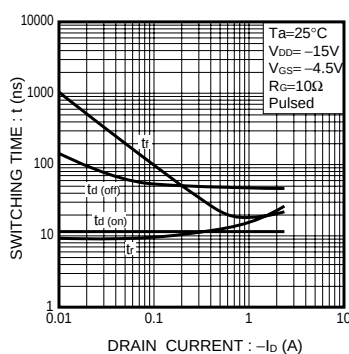


Fig.8 Switching Characteristics

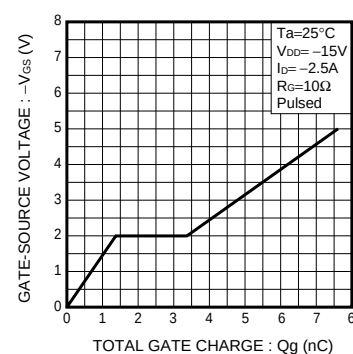


Fig.9 Dynamic Input Characteristics

Transistors

●Measurement circuits

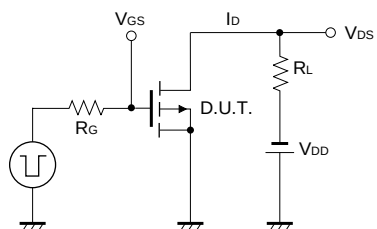


Fig.10 Switching Time Test Circuit

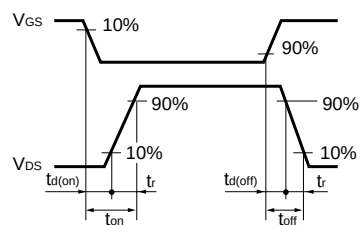


Fig.11 Switching Time Waveforms

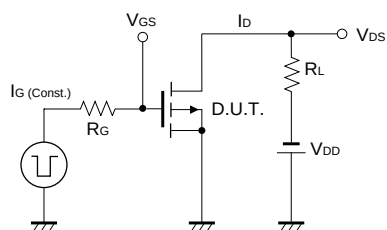


Fig.12 Gate Charge Test Circuit

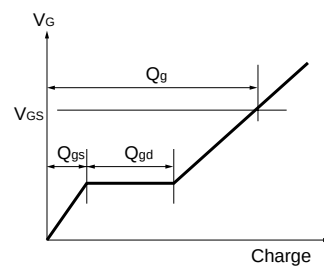


Fig.13 Gate Charge Waveform

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