

*ALC202*  
*AC'97 Audio CODEC*

**Draft Spec.**

*Preliminary*

*Version 0.62*

*September 26, 2001*



## 1. Features

- Single chip audio CODEC with high S/N ratio (>90 dB).
- 20-bit DAC, 18-bit ADC.
- Stereo full-duplex CODEC with independent and variable sampling rate.
- 4 analog line-level stereo input with 5-bit volume control : LINE\_IN, CD, VIDEO, AUX
- 2 analog line-level mono input : PC\_BEEP, PHONE\_IN.
- Mono output with 5-bit volume control.
- Stereo output with 6-bit volume control.
- 2 MIC inputs: Software selectable.
- Power management and enhanced power saving.
- 3D Stereo Enhancement
- External Amplifier power down capability.
- Multiple CODEC extension.
- Compliant with AC' 97 2.2 specification
- 50mW/8Ω amplifier at LINE/ Headphone output
- Jack-detect function to mute LINE/MONO/HP output, to control S/PDIF output.
- Supports S/PDIF out is compliant with AC' 97 rev2.2.
- 2 GPIO pins.
- 14.318MHz→24.576MHz digital PLL.
- Supports double sampling rate (96KHz) of DVD audio playback.
- +30dB boost preamplifier for MIC input.
- Power support: Digital: 3.3V Analog: 3.3V/5V
- Standard 48-Pin *LQFP* Package

## 2. Pin Description

### 2.1 Digital I/O pins: 11 pins

| Name          | Type | Pin No | Description                                                                                      | Characteristic Definition                                                                              |
|---------------|------|--------|--------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
| RESET#        | I    | 11     | AC'97 H/W reset                                                                                  | Schmitt trigger input                                                                                  |
| XTL-IN        | I    | 2      | Crystal input pad                                                                                | Crystal: <b>24.576M/14.318M</b> crystal input<br>External: <b>24.576M/14.318M</b> external clock input |
| XTL-OUT       | O    | 3      | Crystal output pad                                                                               | Crystal: <b>24.576M/14.318M</b> crystal output<br>External: <b>24.576M/14.318M</b> clock output        |
| SYNC          | I    | 10     | Sample Sync (48KHz)                                                                              | Schmitt trigger input                                                                                  |
| BIT-CLK       | IO   | 6      | Bit clock output (12.288Mhz)                                                                     | CMOS input/output $V_t=0.35V_{dd}$                                                                     |
| SDATA-OUT     | I    | 5      | Serial TDM AC97 output                                                                           | Schmitt trigger input                                                                                  |
| SDATA-IN      | O    | 8      | Serial TDM AC97 input                                                                            | CMOS output,                                                                                           |
| GPIO0         | I/O  | 43     | I: General purpose input pin-0. (Can be software volume up)<br>O: General purpose output pin-0.  | Internally pulled high by a 50K resistor.                                                              |
| GPIO1         | I/O  | 44     | I: General purpose input pin-1. (Can be software volume down)<br>O: General purpose output pin-1 | Internally pulled high by a 50K resistor.                                                              |
| ID0#          | I    | 45     | ID strap 0                                                                                       | CMOS input $V_t=0.35V_{dd}$                                                                            |
| EAPD / JD     | O    | 47     | External Amplifier power down control / Jack –Detect sense a low to high edge                    | CMOS output / input, JD should be internally pulled high by a 50K resistor                             |
| SPDIFO / TEST | O    | 48     | S/PDIF output / TEST output                                                                      | Digital output has <b>12 mA@75Ω</b> driving capability.                                                |

### 2.2 Analog I/O Pins: 18 pins

| Name    | Type | Pin No | Description               | Characteristic Definition |
|---------|------|--------|---------------------------|---------------------------|
| PC-BEEP | I    | 12     | PC speaker input          | Analog input (1Vrms)      |
| PHONE   | I    | 13     | Speakerphone input        | Analog input (1Vrms)      |
| AUX-L   | I    | 14     | AUX Left channel          | Analog input (1Vrms)      |
| AUX-R   | I    | 15     | AUX Right channel         | Analog input (1Vrms)      |
| VIDEO-L | I    | 16     | Video audio Left channel  | Analog input (1Vrms)      |
| VIDEO-R | I    | 17     | Video audio Right channel | Analog input (1Vrms)      |



|           |   |    |                                                                 |                                                                                                |
|-----------|---|----|-----------------------------------------------------------------|------------------------------------------------------------------------------------------------|
| CD-L      | I | 18 | CD audio Left channel                                           | Analog input (1Vrms)                                                                           |
| CD-GND    | I | 19 | CD audio analog GND                                             | Analog input (1Vrms)                                                                           |
| CD-R      | I | 20 | CD audio Right channel                                          | Analog input (1Vrms)                                                                           |
| MIC1      | I | 21 | First Mic input                                                 | Analog input (1Vrms)                                                                           |
| MIC2      | I | 22 | Second Mic input                                                | Analog input (1Vrms)                                                                           |
| LINE-L    | I | 23 | Line input Left channel                                         | Analog input (1Vrms)                                                                           |
| LINE-R    | I | 24 | Line input Right channel                                        | Analog input (1Vrms)                                                                           |
| LINE-OUTL | O | 35 | Line-Out Left channel                                           | ALC202: Analog output without op-amp (1.0Vrms)<br>ALC202A: Analog output with op-amp (1.4Vrms) |
| LINE-OUTR | O | 36 | Line-Out Right channel                                          | ALC202: Analog output without op-amp (1.0Vrms)<br>ALC202A: Analog output with op-amp (1.4Vrms) |
| HP-OUT-L  | O | 39 | Headphone Out – Left (ALC202)<br>True-LINE-Out-Left (ALC202A)   | ALC202: Analog output with op-amp<br>ALC202A: Analog output without op-amp                     |
| HP-OUT-R  | O | 41 | Headphone Out – Right (ALC202)<br>True-LINE-Out-Right (ALC202A) | ALC202: Analog output with op-amp<br>ALC202A: Analog output without op-amp                     |
| MONO-OUT  | O | 37 | Speaker Phone output                                            | Analog output (1Vrms)                                                                          |

### 2.3 Filter/References: 7 pins

| Name    | Type | Pin No | Description                        | Characteristic Definition          |
|---------|------|--------|------------------------------------|------------------------------------|
| VREF    |      | 27     | Reference voltage                  | 1uF capacitor to analog ground     |
| VREFOUT | O    | 28     | Ref. voltage out with 8mA drive    | Analog output (2.25V – 2.75V)      |
| AFILT1  |      | 29     | ADC anti-aliasing filter capacitor | 1000pF capacitor to analog ground. |
| AFILT2  |      | 30     | ADC anti-aliasing filter capacitor | 1000pF capacitor to analog ground. |
| VRAD    |      | 31     | ADC reference voltage capacitor    | 1uF capacitor to analog ground     |
| VRDA    |      | 32     | DAC reference voltage capacitor    | 1uF capacitor to analog ground     |

### 2.4 Power/Ground: 8 pins

| Name  | Type | Pin No | Description               | Characteristic Definition |
|-------|------|--------|---------------------------|---------------------------|
| AVDD1 | I    | 25     | Analog VDD (5.0V or 3.3V) |                           |
| AVDD2 | I    | 38     | Analog VDD (5.0V or 3.3V) |                           |
| AVSS1 | I    | 26     | Analog GND                |                           |
| AVSS2 | I    | 42     | Analog GND                |                           |
| DVDD1 | I    | 1      | Digital VDD (3.3V)        |                           |
| DVDD2 | I    | 9      | Digital VDD (3.3V)        |                           |
| DVSS1 | I    | 4      | Digital GND               |                           |
| DVSS2 | I    | 7      | Digital GND               |                           |

### 2.5 Others: 1 pin

| Name | Type | Pin No   | Description                    | Characteristic Definition      |
|------|------|----------|--------------------------------|--------------------------------|
| TEST | O    | 48       | Output DAC clock and ADC clock | Digital pin shared with SPDIFO |
| NC   |      | 33,40,34 | No Connection.                 |                                |

### 2.6 Crystal (Clock) Source Selection: 1 pin

| Name   | Type | Pin No | Description       | Characteristic Definition             |
|--------|------|--------|-------------------|---------------------------------------|
| XTLSEL | I    | 46a    | Crystal Selection | Internal pull high by a 50K resistor. |

#### XTLSEL:

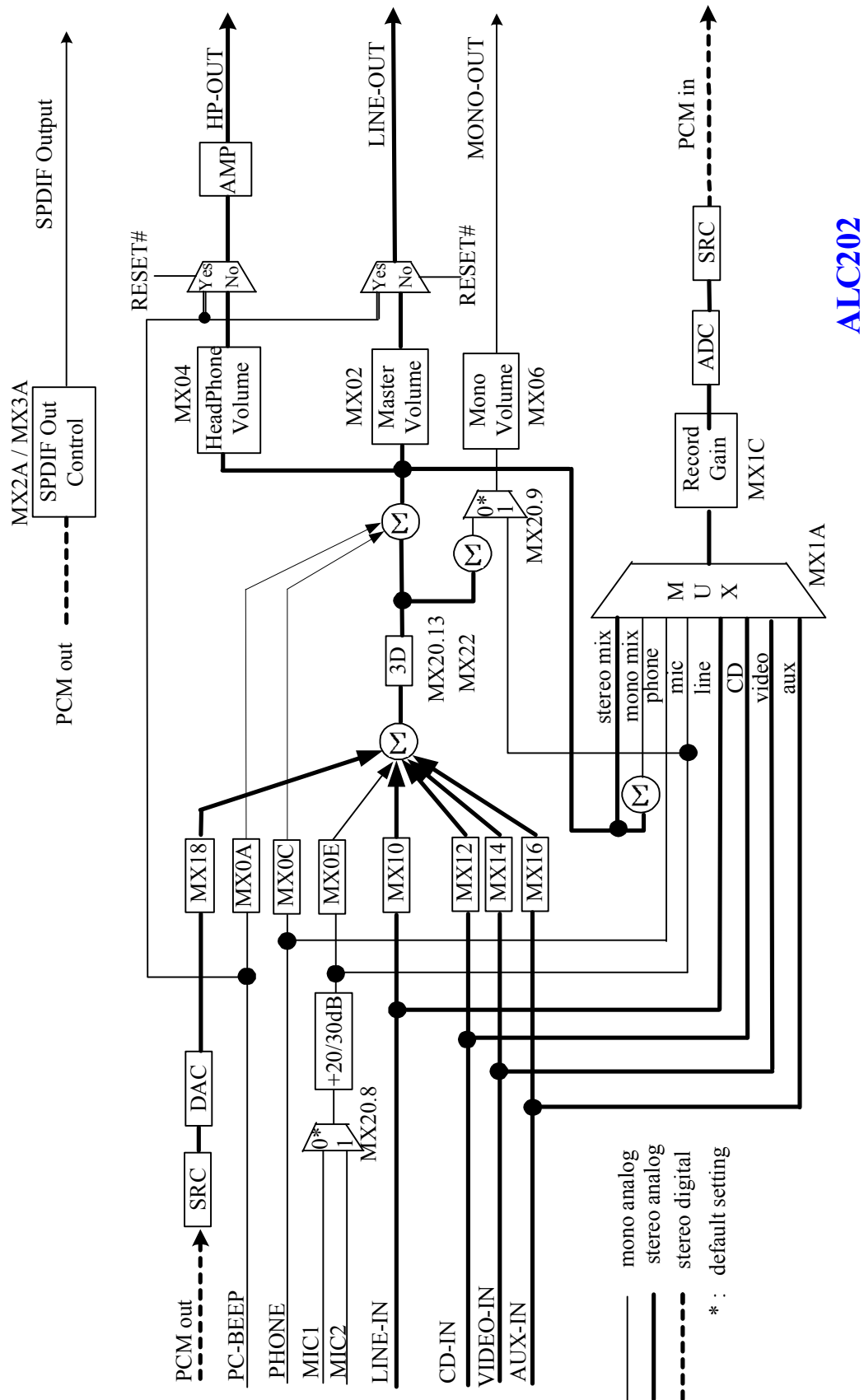
XTLSEL=floating, the clock source is 24.576MHz crystal or external clock. (Default)

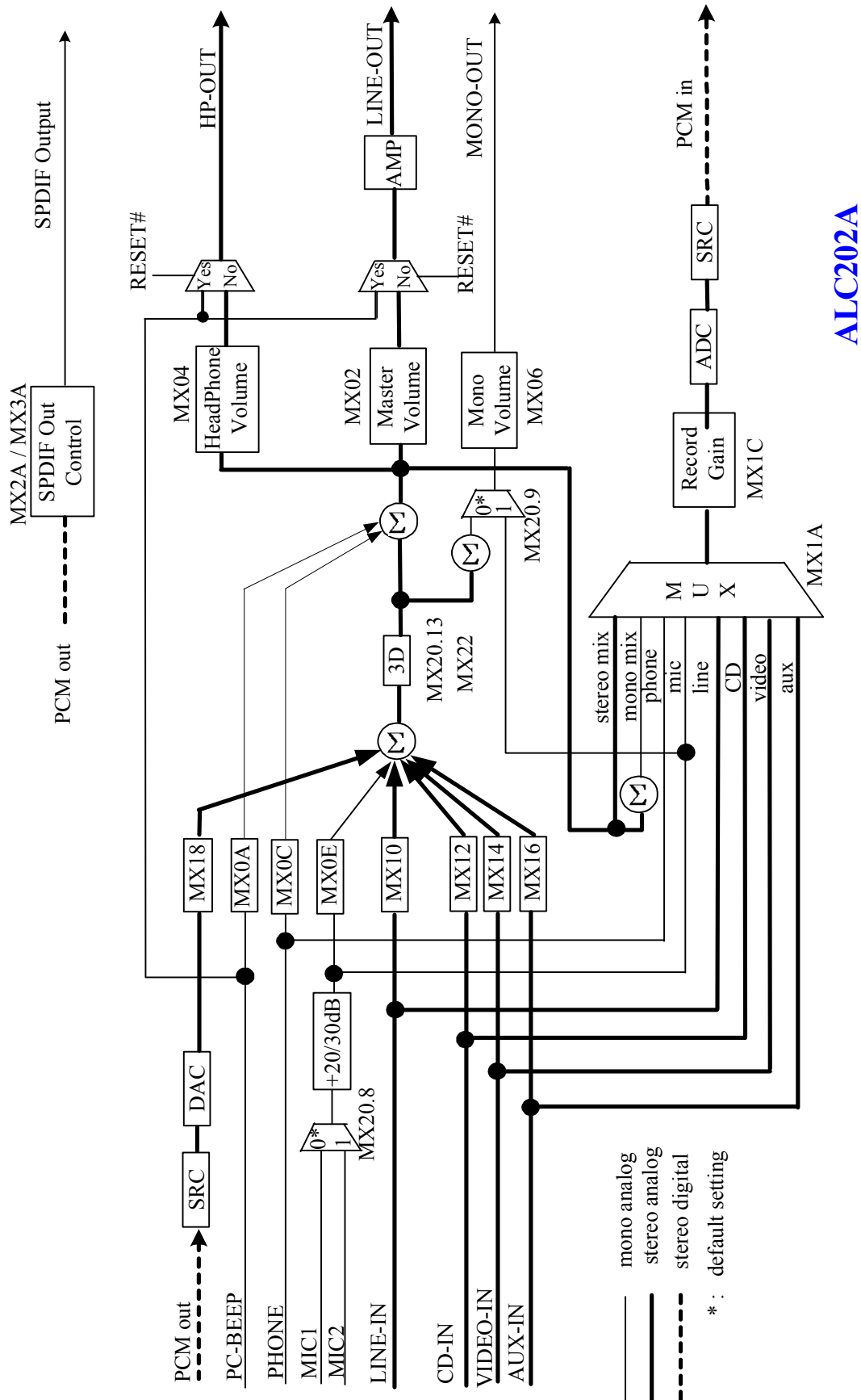
XTLSEL=pull low, select 14.318MHz→24.576MHz digital PLL

*The default state of MX7A.15 if power on latched inversely from XTLSEL.*



## 2.7 Mixer Block Diagram

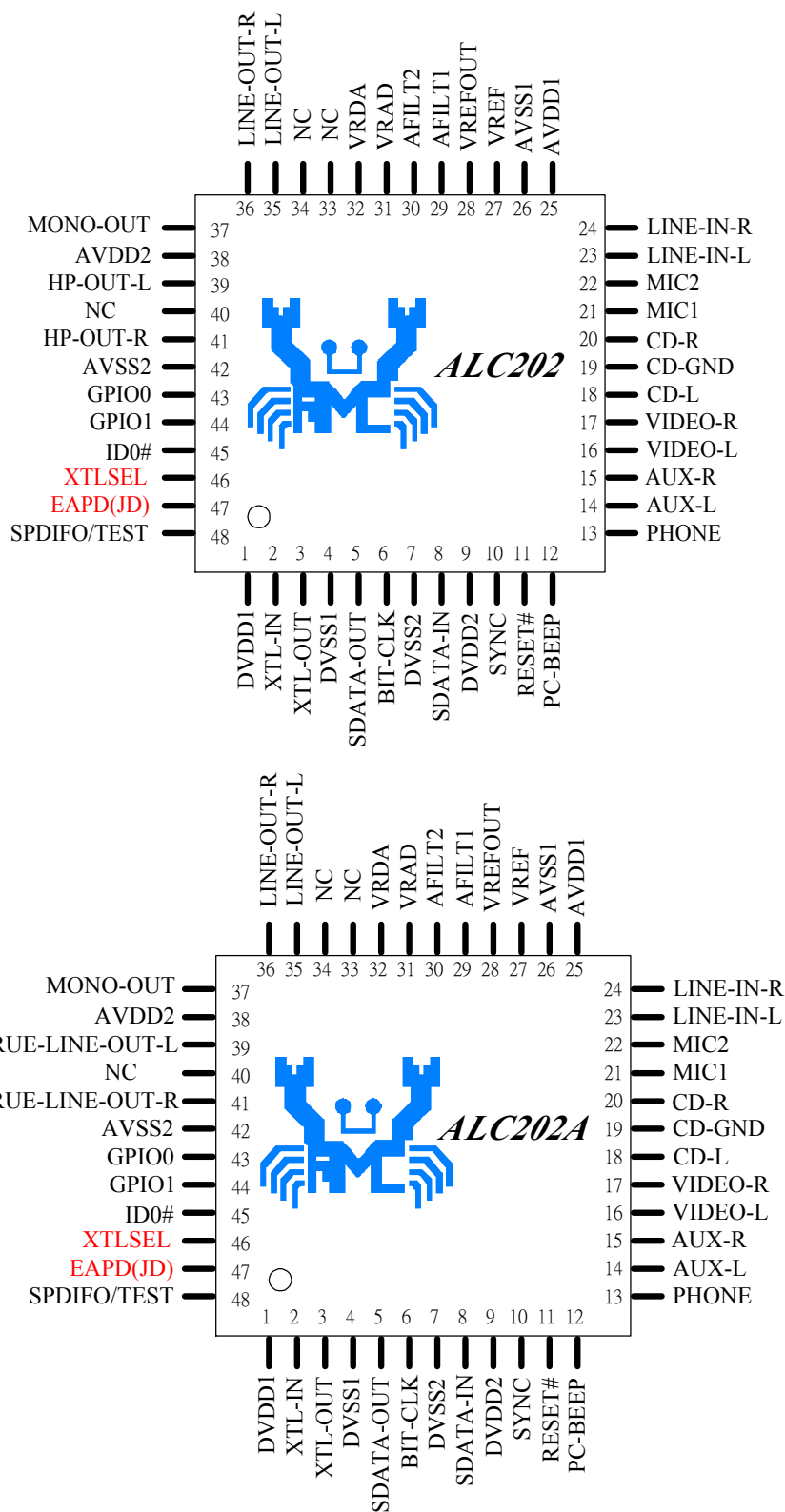




ALC202A

### 3. ALC202 Pin Assignment

#### 3.1 Pin-Out Diagram:





#### 4. Mixer Registers

*All mixer register access with odd-number will return with 0.*

*Reading unimplemented registers will return 0.*

| REG.<br>(HEX) | NAME                      | D15   | D14   | D13   | D12   | D11   | D10   | D9   | D8   | D7   | D6   | D5    | D4    | D3   | D2    | D1     | D0   | DEFAU<br>LT     |
|---------------|---------------------------|-------|-------|-------|-------|-------|-------|------|------|------|------|-------|-------|------|-------|--------|------|-----------------|
| 00h           | Reset                     | X     | SE4   | SE3   | SE2   | SE1   | SE0   | ID9  | ID8  | ID7  | ID6  | ID5   | ID4   | ID3  | ID2   | ID1    | ID0  | 5990h           |
| 02h           | Master Volume             | Mute  | X     | ML5   | ML4   | ML3   | ML2   | ML1  | ML0  | X    | X    | MR5   | MR4   | MR3  | MR2   | MR1    | MR0  | 8000h/<br>0000h |
| 04h           | Headphone volume          | Mute  | X     | HPL5  | HPL4  | HPL3  | HPL2  | HPL1 | HPL0 | X    | X    | HPR5  | HPR4  | HPR3 | HPR2  | HPR1   | HPR0 | 8000h/<br>0000h |
| 06h           | Mono-Out Volume           | Mute  | X     | X     | X     | X     | X     | X    | X    | X    | X    | X     | MM4   | MM3  | MM2   | MM1    | MM0  | 8000h/<br>0000h |
| 0Ah           | PC BEEP Volume            | Mute  | X     | X     | X     | X     | X     | X    | X    | X    | X    | X     | PB3   | PB2  | PB1   | PB0    | X    | 8000h           |
| 0Ch           | PHONE Volume              | Mute  | X     | X     | X     | X     | X     | X    | X    | X    | X    | X     | PH4   | PH3  | PH2   | PH1    | PH0  | 8008h           |
| 0Eh           | MIC Volume                | Mute  | X     | X     | X     | X     | X     | BGO1 | BGO0 | X    | BC   | X     | MI4   | MI3  | MI2   | MI1    | MI0  | 8008h           |
| 10h           | Line-In Volume            | Mute  | X     | X     | NL4   | NL3   | NL2   | NL1  | NL0  | X    | X    | X     | NR4   | NR3  | NR2   | NR1    | NR0  | 8808h           |
| 12h           | CD Volume                 | Mute  | X     | X     | CL4   | CL3   | CL2   | CL1  | CL0  | X    | X    | X     | CR4   | CR3  | CR2   | CR1    | CR0  | 8808h           |
| 14h           | Video Volume              | Mute  | X     | X     | VL4   | VL3   | VL2   | VL1  | VL0  | X    | X    | X     | VR4   | VR3  | VR2   | VR1    | VR0  | 8808h           |
| 16h           | Aux Volume                | Mute  | X     | X     | AL4   | AL3   | AL2   | AL1  | AL0  | X    | X    | X     | AR4   | AR3  | AR2   | AR1    | AR0  | 8808h           |
| 18h           | PCM Out Volume            | Mute  | X     | X     | PL4   | PL3   | PL2   | PL1  | PL0  | X    | X    | X     | PR4   | PR3  | PR2   | PR1    | PR0  | 8808h/<br>0808h |
| 1Ah           | Record Select             | X     | X     | X     | X     | X     | LRS2  | LRS1 | LRS0 | X    | X    | X     | X     | X    | RRS2  | RRS1   | RRS0 | 0000h           |
| 1Ch           | Record Gain               | Mute  | X     | X     | X     | LRG3  | LRG2  | LRG1 | LRG0 | X    | X    | X     | X     | RRG3 | RRG2  | RRG1   | RRG0 | 8000h           |
| 20h           | General Purpose           | POP   | X     | 3D    | X     | X     | X     | MIX  | MS   | LBK  | X    | X     | X     | X    | X     | X      | X    | 0000h           |
| 22h           | 3D Control                | X     | X     | X     | X     | X     | X     | X    | X    | X    | X    | X     | X     | X    | DP2   | DP1    | DP0  | 0000h           |
| 26h           | Power Down Ctrl/Status    | EAPD  | PR6   | PR5   | PR4   | PR3   | PR2   | PR1  | PR0  | X    | X    | X     | X     | REF  | ANL   | DAC    | ADC  | 000Fh           |
| 28h           | Extended Audio ID         | ID1   | ID0   | X     | X     | REV1  | REV0  | AMAP | X    | X    | X    | X     | X     | X    | SPDIF | X      | VRA  | 0605h           |
| 2Ah           | Extended Audio Status     | X     | X     | X     | X     | X     | SPCV  | X    | X    | X    | X    | SPSA1 | SPSA0 | X    | SPDIF | X      | VRA  | 0000h           |
| 2Ch           | PCM front Out Sample Rate | FSR15 | FSR14 | FSR13 | FSR12 | FSR11 | FSR10 | FSR9 | FSR8 | FSR7 | FSR6 | FSR5  | FSR4  | FSR3 | FSR2  | FSR1   | FSR0 | BB80h           |
| 32h           | PCM Input Sample Rate     | ISR15 | ISR14 | ISR13 | ISR12 | ISR11 | ISR10 | ISR9 | ISR8 | ISR7 | ISR6 | ISR5  | ISR4  | ISR3 | ISR2  | ISR1   | ISR0 | BB80h           |
| 3Ah           | S/PDIF Ctl                | V     | 0     | SPSR1 | SPSR0 | L     | CC6   | CC5  | CC4  | CC3  | CC2  | CC1   | CC0   | PRE  | COPY  | /AUDIO | PRO  | 2000h           |
| 76h           | GPIO Setup                | 0     | 0     | 0     | 0     | 0     | 0     | 0    | 0    | 0    | 0    | 0     | 0     | 0    | 0     | 0      | 0    | 0000h           |
| 78h           | GPIO Status               | 0     | 0     | 0     | 0     | 0     | 0     | 0    | 0    | 0    | 0    | 0     | 0     | 0    | 0     | 0      | 0    | 0000h           |
| 7Ch           | Vendor ID1                | 0     | 1     | 0     | 0     | 0     | 0     | 0    | 1    | 0    | 1    | 0     | 0     | 1    | 1     | 0      | 0    | 414Ch           |
| 7Eh           | Vendor ID2                | 0     | 1     | 0     | 0     | 0     | 1     | 1    | 1    | 0    | 0    | 0     | 1     | V3   | V2    | V1     | V0   | 4740h           |

X: reserved bit

**MX00 Reset Default: 5990H**

| Bit   | Type | Function                                                  |
|-------|------|-----------------------------------------------------------|
| 15    |      | Reserved                                                  |
| 14:10 | R    | return 10110b                                             |
| 9     | R    | Read as 0 (Not support 20-bit ADC)                        |
| 8     | R    | Read as 1 (Support 18-bit ADC)                            |
| 7     | R    | Read as 1 (Support 20-bit DAC)                            |
| 6     | R    | Read as 0 (Not support 18-bit DAC)                        |
| 5     | R    | Read as 0 (Not support for Loudness)                      |
| 4     | R    | Read as 1 (Headphone output support)                      |
| 3     | R    | Read as 0 (Not simulated stereo ,for analog 3D block use) |
| 2     | R    | Read as 0 (Not Bess & Treble Control)                     |
| 1     | R    | Reserved,Read as 0                                        |
| 0     | R    | Read as 0 (No Dedicated Mic PCM input)                    |

- ❶ Write to this register will reset all mixer register to their default value. The written data should be ignored.

**MX02 Master Volume Default: 8000H / 0000H**

| Bit  | Type | Function                                         |
|------|------|--------------------------------------------------|
| 15   | R/W  | Mute Control 0 : Normal 1 : Mute ( $-\infty$ dB) |
| 14   |      | Reserved                                         |
| 13:8 | R/W  | Master Left Volume (MLV[5..0]) in 1.5 dB step    |
| 7:6  |      | Reserved                                         |
| 5:0  | R/W  | Master Right Volume (MRV[5..0]) in 1.5 dB step   |

- ❶ For MRV/MLV, 00h 0 dB attenuation  
3Fh 94.5 dB attenuation  
❷ When ID=01,10,11, the default value is 0000H.

**MX04 Headphone Output Volume Default: 8000H / 0000H**

| Bit  | Type | Function                                                 |
|------|------|----------------------------------------------------------|
| 15   | R/W  | Mute Control 0 : Normal 1 : Mute ( $-\infty$ dB)         |
| 14   |      | Reserved                                                 |
| 13:8 | R/W  | Headphone Output Left Volume (HPL[5..0]) in 1.5 dB step  |
| 7:6  |      | Reserved                                                 |
| 5:0  | R/W  | Headphone Output Right Volume (HPR[5..0]) in 1.5 dB step |

- ❶ For HPR/HPL, 00h 0 dB attenuation  
3Fh 94.5 dB attenuation  
❷ When ID=01,10,11, the default value is 0000H.

**MX06 MONO OUT Volume Default: 8000H / 0000H**

| Bit  | Type | Function                                         |
|------|------|--------------------------------------------------|
| 15   | R/W  | Mute Control 0 : Normal 1 : Mute ( $-\infty$ dB) |
| 14:5 |      | Reserved                                         |
| 4:0  | R/W  | Mono Master Volume (MMV[4..0]) in 1.5 dB step    |

- ❶ For MMV, 00h 0 dB attenuation  
1Fh 46.5 dB attenuation  
❷ Implement 5-bit volume control only. Writing 1xxxxx will be interpreted as x11111 and response when read with x11111 too.  
❸ When ID=01,10,11, the default value is 0000H.

**MX0A PC BEEP Volume Default: 8000H**

| Bit  | Type | Function                                 |
|------|------|------------------------------------------|
| 15   | R/W  | Mute Control 0 : Normal 1 : Mute (-∞ dB) |
| 14:5 |      | Reserved                                 |
| 4:1  | R/W  | PC Beep Volume (PBV[3..0]) in 3 dB step  |
| 0    |      | Reserved                                 |

- ❶ For PBV,      00h      0 dB attenuation  
                      0Fh      45 dB attenuation

**MX0C PHONE Volume Default: 8008H**

| Bit  | Type | Function                                 |
|------|------|------------------------------------------|
| 15   | R/W  | Mute Control 0 : Normal 1 : Mute (-∞ dB) |
| 14:5 |      | Reserved                                 |
| 4:0  | R/W  | Phone Volume (PV[4..0]) in 1.5 dB step   |

- ❶ For PV,      00h      +12 dB Gain  
                      08h      0dB gain  
                      1Fh      -34.5dB Gain

**MX0E MIC Volume Default: 8008H**

| Bit   | Type | Function                                                                            |
|-------|------|-------------------------------------------------------------------------------------|
| 15    | R/W  | Mute Control 0: Normal 1 : Mute (-∞ dB)                                             |
| 14:10 |      | Reserved                                                                            |
| 9:8   | R/W  | Boost Gain Option (BGO)❷<br>00: 20 dB 01: 6 dB 10: 12 dB 11: 29.5 dB (V=30*Vmic-in) |
| 7     |      | Reserved                                                                            |
| 6     | R/W  | Boost Control (BC)<br>0: Disable 1: Enable Boost                                    |
| 5     |      | Reserved                                                                            |
| 4:0   | R/W  | Mic Volume (MV[4..0]) in 1.5 dB step                                                |

- ❶ For MV,      00h      +12 dB Gain  
                      08h      0dB gain  
                      1Fh      -34.5dB Gain

- ❷ If 29.5dB boost gain is selected, input resistor can be reduced to save area of feedback resistor.

**MX10 LINE IN Volume Default: 8808H**

| Bit   | Type | Function                                        |
|-------|------|-------------------------------------------------|
| 15    | R/W  | Mute Control 0 : Normal 1 : Mute (-∞ dB)        |
| 14:13 |      | Reserved                                        |
| 12:8  | R/W  | Line-In Left Volume (NLV[4..0]) in 1.5 dB step  |
| 7:5   |      | Reserved                                        |
| 4:0   | R/W  | Line-In Right Volume (NRV[4..0]) in 1.5 dB step |

- ❶ For NLV/NRV,      00h      +12 dB Gain  
                                  08h      0dB gain  
                                  1Fh      -34.5dB Gain

**MX12 CD Volume Default: 8808H**

| Bit | Type | Function                                 |
|-----|------|------------------------------------------|
| 15  | R/W  | Mute Control 0 : Normal 1 : Mute (-∞ dB) |



|       |     |                                            |
|-------|-----|--------------------------------------------|
| 14:13 |     | Reserved                                   |
| 12:8  | R/W | CD Left Volume (CLV[4..0]) in 1.5 dB step  |
| 7:5   |     | Reserved                                   |
| 4:0   | R/W | CD Right Volume (CRV[4..0]) in 1.5 dB step |

- ❶ For CLV/CRV,
- |     |              |
|-----|--------------|
| 00h | +12 dB Gain  |
| 08h | 0dB gain     |
| 1Fh | -34.5dB Gain |

#### MX14 VIDEO Volume Default: 8808H

| Bit   | Type | Function                                      |
|-------|------|-----------------------------------------------|
| 15    | R/W  | Mute Control 0 : Normal 1 : Mute (-∞ dB)      |
| 14:13 |      | Reserved                                      |
| 12:8  | R/W  | Video Left Volume (VLV[4..0]) in 1.5 dB step  |
| 7:5   |      | Reserved                                      |
| 4:0   | R/W  | Video Right Volume (VRV[4..0]) in 1.5 dB step |

- ❶ For VLV/VRV,
- |     |              |
|-----|--------------|
| 00h | +12 dB Gain  |
| 08h | 0dB gain     |
| 1Fh | -34.5dB Gain |

#### MX16 AUX Volume Default: 8808H

| Bit   | Type | Function                                    |
|-------|------|---------------------------------------------|
| 15    | R/W  | Mute Control 0 : Normal 1 : Mute (-∞ dB)    |
| 14:13 |      | Reserved                                    |
| 12:8  | R/W  | AUX Left Volume (ALV[4..0]) in 1.5 dB step  |
| 7:5   |      | Reserved                                    |
| 4:0   | R/W  | AUX Right Volume (ARV[4..0]) in 1.5 dB step |

- ❶ For ALV/ARV,
- |     |              |
|-----|--------------|
| 00h | +12 dB Gain  |
| 08h | 0dB gain     |
| 1Fh | -34.5dB Gain |

#### MX18 PCM OUT Volume Default: 8808H / 0808H

| Bit   | Type | Function                                    |
|-------|------|---------------------------------------------|
| 15    | R/W  | Mute Control 0 : Normal 1 : Mute (-∞ dB)    |
| 14:13 |      | Reserved                                    |
| 12:8  | R/W  | PCM Volume (PLV[4..0]) in 1.5 dB step       |
| 7:5   |      | Reserved                                    |
| 4:0   | R/W  | PCM Right Volume (PRV[4..0]) in 1.5 dB step |

- ❶ For PLV/PRV,
- |     |              |
|-----|--------------|
| 00h | +12 dB Gain  |
| 08h | 0dB gain     |
| 1Fh | -34.5dB Gain |

❷ When ID=01,10,11, the default value is 0808H.

#### MX1A Record Select Default: 0000H

| Bit   | Type | Function                               |
|-------|------|----------------------------------------|
| 15:11 |      | Reserved                               |
| 10:8  | R/W  | Left record source select (LRS[2..0])  |
| 7:3   |      | Reserved                               |
| 2:0   | R/W  | Right record source select (RRS[2..0]) |

- ❶ For LRS



|   |                          |
|---|--------------------------|
| 0 | MIC                      |
| 0 | CD LEFT                  |
| 0 | VIDEO LEFT               |
| 0 | AUX LEFT                 |
| 0 | LINE LEFT                |
| 0 | STEREO MIXER OUTPUT LEFT |
| 0 | MONO MIXER OUTPUT        |
| 7 | PHONE                    |

## ② For RRS

|   |                           |
|---|---------------------------|
| 0 | MIC                       |
| 0 | CD RIGHT                  |
| 0 | VIDEO RIGHT               |
| 0 | AUX RIGHT                 |
| 0 | LINE RIGHT                |
| 0 | STEREO MIXER OUTPUT RIGHT |
| 0 | MONO MIXER OUTPUT         |
| 0 | PHONE                     |

**MX1C Record Gain Default: 8000H**

| Bit   | Type | Function                                            |
|-------|------|-----------------------------------------------------|
| 15    | R/W  | Mute Control 0 : Normal 1 : Mute ( $-\infty$ dB)    |
| 14:12 |      | Reserved                                            |
| 11:8  | R/W  | Left Record Gain Select (LRG[3..0]) in 1.5 dB step  |
| 7:4   |      | Reserved                                            |
| 3:0   | R/W  | Right Record Gain Select (RRG[3..0]) in 1.5 dB step |

① For LRG/RRG, 0Fh +22.5dB  
00h 0 dB (No Gain)

**MX20 General Purpose Register Default : 0000H**

| Bit   | Type | Function                                          |
|-------|------|---------------------------------------------------|
| 15:14 |      | Reserved, Read as 0                               |
| 13    | R/W  | 3D Control 1: On 0: Off                           |
| 12:10 |      | Reserved, Read as 0                               |
| 9     | R/W  | Mono output select 0 : MIX 1 : MIC                |
| 8     | R/W  | Mic select 0 : Mic 1 1 : Mic 2                    |
| 7     | R/W  | AD to DA loop-back control 0 : Disable 1 : Enable |
| 6:0   |      | Reserved                                          |

**MX22 3D Control Default : 0000H**

| Bit  | Type | Function                 |
|------|------|--------------------------|
| 15:3 |      | Reserved ,Read as 0      |
| 2:0  | R/W  | Depth control (DP[2..0]) |

## ① 3D effect control

| DP[2:0] | Function | DP[2:0] | Function |
|---------|----------|---------|----------|
| 000     | 0%(off*) | 100     | 50%      |
| 001     | 12.5%    | 101     | 67.5%    |
| 010     | 25%      | 110     | 75%      |
| 011     | 37.5     | 111     | 100%     |

**MX26 Powerdown Control/Status Default: 000FH**

| Bit | Type | Function                                                         |
|-----|------|------------------------------------------------------------------|
| 15  | R/W  | PR7 External Amplifier Power Down (EAPD) 0: normal 1: Power down |
| 14  | R/W  | PR6 0: Normal 1: Power down Headphone Out (HP-OUT)               |
| 13  | R/W  | PR5 0: Normal 1: Disable internal clock                          |
| 12  | R/W  | PR4 0: Normal 1: Power down AC-Link                              |
| 11  | R/W  | PR3 0: Normal 1: Power down Mixer (Vref off)                     |
| 10  | R/W  | PR2 0: Normal 1: Power down Mixer (Vref still on)                |
| 9   | R/W  | PR1 0: Normal 1: Power down PCM DAC                              |
| 8   | R/W  | PR0 0: Normal 1: Power down PCM ADC and input MUX                |
| 7:4 |      | Reserved, Read as 0                                              |
| 3   | R    | Vref status 1: Vref is up to normal level 0: Not yet             |
| 2   | R    | Analog Mixer status 1: Ready 0: Not yet                          |
| 1   | R    | DAC status 1: Ready 0: Not yet                                   |
| 0   | R    | ADC status 1: Ready 0: Not yet                                   |

**MX28 Extended Audio ID Default: 060Fh**

| Bit   | Type | Function                                                                                                                              |
|-------|------|---------------------------------------------------------------------------------------------------------------------------------------|
| 15    | R    | ID1 ❶                                                                                                                                 |
| 14    | R    | ID0                                                                                                                                   |
| 13:12 |      | Reserved, Read as 0                                                                                                                   |
| 11:10 | R    | REV[1:0]=01 to indicates ALC202 is AC' 97 rev2.2 compliant.                                                                           |
| 9     | R    | AMAP read as 1 (DAC mapping based on ID)                                                                                              |
| 8:6   |      | Reserved, Read as 0                                                                                                                   |
| 5:4   | R/W  | DSA[1:0], DAC Slot Assignment❷ (Default value depends on ID[1:0])<br>DSA[1:0] control DAC slot assignment described in AC' 97 rev2.2. |
| 3     |      | Reserved, Read as 0                                                                                                                   |
| 2     | R    | SPDIF read as 1 (S/PDIF is supported)                                                                                                 |
| 1     | R    | DRA read as 1                                                                                                                         |
| 0     | R    | VRA read as 1 (Variable Rate Audio is supported)                                                                                      |

❶ID1 is latched inversely from pin 46 when system reset. ID0 is latched inversely from pin 45 when system reset.

❷ALC202 maps DAC slot according to the following table: (default maps to AC' 97 spec. rev2.2)

| DSA[1:0] | Left DAC slot # | Right DAC slot # | Comment                    |
|----------|-----------------|------------------|----------------------------|
| 0,0      | 3               | 4                | Default when ID[1:0]=00    |
| 0,1      | 7               | 8                | Default when ID[1:0]=01,10 |
| 1,0      | 6               | 9                | Default when ID[1:0]=11    |
| 1,1      | 10              | 11               |                            |

**MX2A Extended Audio Status and control register Default: 0000H**

| Bit   | Type | Function                                                                                                                                                                                                |
|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 |      | Reserved                                                                                                                                                                                                |
| 10    | R    | SPCV (S/PDIF Configuration Valid)<br>0: current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is not valid.<br>1: current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is valid.                     |
| 9:6   |      | Reserved                                                                                                                                                                                                |
| 5:4   | R/W  | SPSA[1:0] (S/PDIF Slot Assignment)<br>00: S/PDIF source data assigned to AC-LINK slot3/4.<br>01: S/PDIF source data assigned to AC-LINK slot7/8.<br>10: S/PDIF source data assigned to AC-LINK slot6/9. |



|   |     |                                                          |
|---|-----|----------------------------------------------------------|
|   |     | 11: S/PDIF source data assigned to AC-LINK slot10/11.    |
| 3 |     | Reserved                                                 |
| 2 | R/W | SPDIF 1: enable 0: disable (SPDIFO is in high impedance) |
| 1 | R/W | DRA 1: enable 0: disable                                 |
| 0 | R/W | VRA. 1: enable 0: disable①                               |

① If VRA = 0, ALC202 ADC/DAC operate at fixed 48KHz sampling rate. Otherwise, it operates with variable sampling rate defined in MX2C and MX32. VRA also control write operation of MX2C and MX32.

#### MX2C PCM DAC Rate Default: BB80H

| Bit  | Type | Function                         |
|------|------|----------------------------------|
| 15:0 | R/W  | FOSR[15:0] Output sampling rate. |

① ALC202 support the following sampling rate required in PC99/PC2001 design guide.

| Sampling rate | FOSR[15:0] |
|---------------|------------|
| 8000          | 1F40h      |
| 11025         | 2B11h      |
| 12000         | 2EE0       |
| 16000         | 3E80h      |
| 22050         | 5622h      |
| 24000         | 5DC0       |
| 32000         | 7D00h      |
| 44100         | AC44h      |
| 48000         | BB80h      |

Note that If the value written is not support, the closest value is returned .

② When MX2A.0=0 (VRA is disable), this register will return BB80h when read.

#### MX32 PCM ADC Rate Default: BB80H

| Bit  | Type | Function                         |
|------|------|----------------------------------|
| 15:0 | R/W  | FISR[15:0] Output sampling rate. |

① ALC202 support the following sampling rate required in PC99/PC2001 design guide.

| Sampling rate | FISR[15:0] |
|---------------|------------|
| 8000          | 1F40h      |
| 11025         | 2B11h      |
| 12000         | 2EE0       |
| 16000         | 3E80h      |
| 22050         | 5622h      |
| 24000         | 5DC0       |
| 32000         | 7D00h      |
| 44100         | AC44h      |
| 48000         | BB80h      |

Note that If the value written is not support, the closest value is returned .

② When MX2A.0=0 (VRA is disable), this register will return BB80h when read.

#### MX3A S/PDIF Channel Status and Control Default: 2000H

| Bit | Type | Function                                                                                                                                                                                                                                                                |
|-----|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | R/W  | <b>Validity Control</b> (control V bit in Sub-Frame)<br>0: the V bit (valid flag) in sub-frame depends on whether the S/PDIF data is under-run or over-run.<br>1: the V bit in sub-frame is always send as 1 to indicate the invalid data is not suitable for receiver. |



|       |     |                                                                                                                                                                                                          |
|-------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14    | R   | DRS (Double Rate S/PDIF)<br>ALC202 doesn't support double rate S/PDIF, this bit is always 0.                                                                                                             |
| 13:12 | R/W | SPSR[1:0] (S/PDIF Sample Rate)<br>00: sample rate set to 44.1KHz, Fs[0:3]=0000<br>01: reserved<br>10: sample rate set to 48.0KHz, Fs[0:3]=0100 (default)<br>11: sample rate set to 32.0KHz, Fs[0:3]=1100 |
| 11    | R/W | LEVEL (Generation Level)                                                                                                                                                                                 |
| 10:4  | R/W | CC[6:0] (Category Code)                                                                                                                                                                                  |
| 3     | R/W | PRE (Preemphasis)<br>0: None                      1: filter preemphasis is 50/15 usec                                                                                                                    |
| 2     | R/W | COPY (Copyright)<br>0: Not asserted            1: Asserted                                                                                                                                               |
| 1     | R/W | /AUDIO (Non-Audio Data type)<br>0: PCM data            1: AC3 or other digital non-audio data                                                                                                            |
| 0     | R   | PRO (Professional or Consumer format)<br>0: consumer format    1: professional format<br>ALC202 supports consumer channel status format, this bit is always 0.                                           |

❶ The consumer channel status block (bit0~bit31):

|       |        |      |     |     |     |     |       |
|-------|--------|------|-----|-----|-----|-----|-------|
| 0     | 1      | 2    | 3   | 4   | 5   | 6   | 7     |
| PRO=0 | /AUDIO | COPY | PRE | 0   | 0   | 0   | 0     |
| 8     | 9      | 10   | 11  | 12  | 13  | 14  | 15    |
| CC0   | CC1    | CC2  | CC3 | CC4 | CC5 | CC6 | LEVEL |
| 16    | 17     | 18   | 19  | 20  | 21  | 22  | 23    |
| 0     | 0      | 0    | 0   | 0   | 0   | 0   | 0     |
| 24    | 25     | 26   | 27  | 28  | 29  | 30  | 31    |
| Fs0   | Fs1    | Fs2  | Fs3 | 0   | 0   | 0   | 0     |

### Vendor Define Registers:

| MX6A  |      | Miscellaneous Control                                                                                                                             | Default: 0000h |
|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| Bit   | Type | Function                                                                                                                                          |                |
| 15:14 |      | <b>Reserved.</b>                                                                                                                                  |                |
| 13    | R/W  | DAC PCM(n+1) Slot# Select (When DRA=1)<br>0: PCM(n+1) captured from Slot-10/11. (Default in AC' 97 rev2.2)<br>1: PCM(n+1) captured from Slot-7/8. |                |
| 12    | R/W  | <b>S/PDIF Source❶</b><br>0: S/PDIF data is from controller (default)<br>1: S/PDIF data is from ADC                                                |                |
| 11:4  |      | Reserved                                                                                                                                          |                |
| 3     | R/W  | SPDIF Out Volume Control – Mute Bit<br>0: Normal            1: Clamp SPDIF output data to 0. (Mute)                                               |                |
| 2:0   | R/W  | SPDIF Out Volume Control – in 6 dB Step Attenuation ❷<br>000: 0dB<br>001: - 6dB<br>010: -12dB<br>...<br>111: -42dB                                |                |

❶ The default source of S/PDIF output is data sent by controller. When this bit is set, S/PDIF data comes from ALC202's ADC. To keep data concurrence, **software must guarantee the sample rates in MX32 and MX3A[13:12] are the same**. SPCV is no more a validity for S/PDIF configuration. If

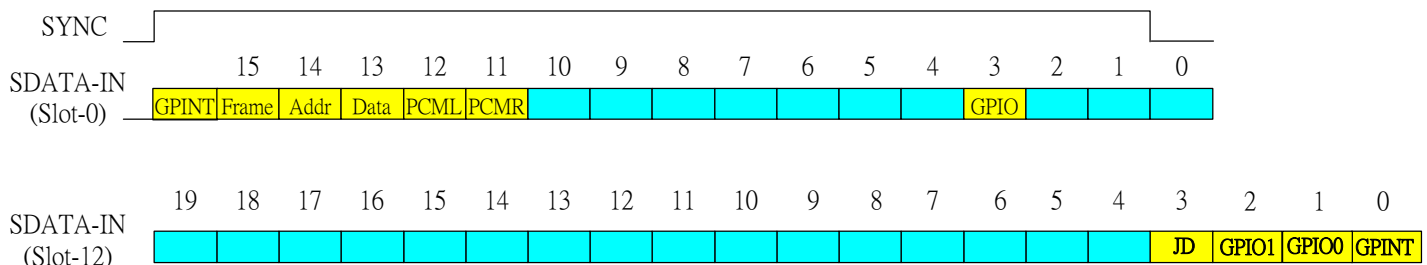
software doesn't keep the same sample rates, the S/PDIF output will be auto forbidden by hardware, and undefined consequence may be occurred.

***Extension Registers:***

| MX76 | GPIO Setup | Default: 0000h                                                                                                                                                                                        |
|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit  | Type       | Function                                                                                                                                                                                              |
| 15   | R/W        | GPIO Statue Indication in SDATA_IN<br>0: The status of GPIO0/GPIO1/JD and its valid tag are not indicated in SDATA_IN.<br>1: The status of GPIO0/GPIO1/JD and its valid tag are indicated in SDATA_IN |
| 14:6 |            | Reserved                                                                                                                                                                                              |
| 6    | R/W        | JD (Jack-Detect) interrupt Enable (when pin-47 is used as Jack-Detect)<br>0: Disable    1: Enable.<br>A low to high transaction will trigger the JD interrupt in bit0 of SDATA_IN's slot-12. ❶        |
| 5    | R/W        | GPIO1 interrupt Enable (when GPIO1 is used as input)<br>0: Disable    1: Enable.<br>A low to high transaction will trigger the GPIO interrupt in bit0 of SDATA_IN's slot-12.                          |
| 4    | R/W        | GPIO0 interrupt Enable (when GPIO0 is used as input)<br>0: Disable    1: Enable.<br>A low to high transaction will trigger the GPIO interrupt in bit0 of SDATA_IN's slot-12.                          |
| 3:2  |            | Reserved                                                                                                                                                                                              |
| 1    | R/W        | GPIO1Primitiveness Control<br>0: Set GPIO1 as input pin.<br>1: Set GPIO1 as output pin.                                                                                                               |
| 0    | R/W        | GPIO0 Primitiveness Control<br>0: Set GPIO0 as input pin.<br>1: Set GPIO0 as output pin.                                                                                                              |

❶ Software programmer can enable JD interrupt to know the “Jack Detection” event occurs.

## ②The Bit-Allocation of GPIO/JD status in AC-LINK:



**\*GPINT = (MX78.6 | MX78.5 | MX78.4)**

| MX78 |       | GPIO Status |  | Default: 0000h |
|------|-------|-------------|--|----------------|
| Bit  | Type  | Function    |  |                |
| 7    | Input | GPIO Pin 7  |  |                |
| 6    | Input | GPIO Pin 6  |  |                |
| 5    | Input | GPIO Pin 5  |  |                |
| 4    | Input | GPIO Pin 4  |  |                |
| 3    | Input | GPIO Pin 3  |  |                |
| 2    | Input | GPIO Pin 2  |  |                |
| 1    | Input | GPIO Pin 1  |  |                |
| 0    | Input | GPIO Pin 0  |  |                |



|       |     |                                                                                                                                                                                                                                |
|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 |     | Reserved                                                                                                                                                                                                                       |
| 9     | R/W | GPIO1 Output Control<br>0: Drive GPIO1 low.<br>1: Drive GPIO1 high.                                                                                                                                                            |
| 8     | R/W | GPIO0 Output Control<br>0: Drive GPIO0 as low.<br>1: Drive GPIO0 as high.                                                                                                                                                      |
| 7     | NA  | Reserved                                                                                                                                                                                                                       |
| 6     | R/W | JD Interrupt Status (JD_IS)❶<br>0: Not JD interrupt.<br>1: JD interrupt.<br>JD_IS= (MX78.2==1)&(MX76.6==1) & (JD low-to-high transition).<br>Write 1 to clear this status bit.                                                 |
| 5     | R/W | GPIO1 Interrupt Status (GPIO1_IS). (When GPIO1 is used as input)❶<br>0: No GPIO1 interrupt.<br>1: GPIO1 interrupt.<br>GPIO1_IS= (MX76.1==0)&(MX76.5==1) & (GPIO1 low-to-high transition).<br>Write 1 to clear this status bit. |
| 4     | R/W | GPIO0 Interrupt Status (GPIO0_IS). (When GPIO0 is used as input)❶<br>0: No GPIO0 interrupt.<br>1: GPIO0 interrupt.<br>GPIO0_IS= (MX76.0==0)&(MX76.4==1) & (GPIO0 low-to-high transition)<br>Write 1 to clear this status bit.  |
| 3     | NA  | Reserved                                                                                                                                                                                                                       |
| 2     | R   | Jack-Detect Event (JDEVT)<br>0: No Jack-Detect event occurs.<br>1: Jack-Detect event occurs.<br><b>JDEVT = MX7A.0 &amp; MX7A.1</b>                                                                                             |
| 1     | R   | GPIO1 Input Status ❷<br>0: GPIO1 is driven low by external device (input).<br>1: GPIO1 is driven high by external device (input).                                                                                              |
| 0     | R   | GPIO0 Input Status ❷<br>0: GPIO0 is driven low by external device (input).<br>1: GPIO0 is driven high by external device (input).                                                                                              |

❶GPIO interrupt (GPINT) in bit0 of SDATA\_IN's slot-12 = (MX78.4 | MX78.5 | MX78.6).

❷When GPIO1/0 is used as input pin, its status will be also reflected in bit2/1 of SDIN's slot-12. Once GPIO1/0 is used as output pin, the bit2/1 of SDATA\_IN's slot-12 is always 0.  
The GPIOx is internally pulled high by a weak resistor.

**MX7A****Default: 57C0H**

| Bit  | Type | Function                                                                                                                                                                                                       |
|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | R    | Clock Source Selection (XTLSEL)<br>0: 24.576MHz crystal is used. DPLL is bypass. (XTLSEL is floating or open)<br>1: 14.318MHz crystal is used. 14.318M→24.576M digital PLL is enabled.<br>(XTLSEL is pull low) |
| 14   | R/W  | ENHPF, Digital high-pass filter to eliminate variation in DC offset.<br>0: Disable 1: Enable (default)                                                                                                         |
| 13:8 | NA   | Reserved                                                                                                                                                                                                       |
| 7    | R/W  | Pin-48 Function Selection<br>0: S/PDIF output (default) 1: TEST                                                                                                                                                |
| 6    | R/W  | Output value of TEST (when bit-7 is set)<br>0: ADC CLK 1: DAC CLK                                                                                                                                              |
| 5    | R/W  | Pin-47 Function Selection<br>0: EAPD output (default) 1: Jack-Detect input                                                                                                                                     |



|   |     |                                                                                                                                                       |
|---|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4 | R/W | HP-OUT Control<br>0: Normal<br>1: HP-OUT is auto muted by H/W when JDS=1                                                                              |
| 3 | R/W | MONO-OUT Control<br>0: Normal<br>1: MONO-OUT is auto muted by H/W when JDS=1                                                                          |
| 2 | R/W | SPDIF Output Gating<br>0: SPDIF output is not gated with JDS.<br>1: SPDIF output is gated with JDS.                                                   |
| 1 | R   | Jack-Detect status (JDS)<br>0: JD is pull low<br>1: JD is floating or pull high<br><i>This bit always indicates the JD pin status after power on.</i> |
| 0 | R/W | LINE-OUT Control<br>0: Normal<br>1: LINE-OUT is auto muted by H/W when JDS=1                                                                          |

**MX7C                      VENDOR ID1                      Default : 414CH**

| Bit  | Type | Function       |
|------|------|----------------|
| 15:0 | R    | Vendor ID "AL" |

**MX7E                      VENDOR ID2                      Default : 4740H**

| Bit  | Type | Function                                                                            |
|------|------|-------------------------------------------------------------------------------------|
| 15:8 | R    | Vendor ID "G"                                                                       |
| 7:4  | R    | Chip ID 0100 (ALC202)                                                               |
| 3:0  | R    | Version number    00: version A.<br>For WHQL issue, The version number is always 0. |

## 5. Design Suggestion

### 5.1 Clocking

The clock source of different configuration is listed below:

| CODEC ID[1..0] | BIT-CLK (12.288MHz) | Clock source                                                         |
|----------------|---------------------|----------------------------------------------------------------------|
| 00             | Output              | 24.576M/14.318M crystal or external clock source input from XTAL-IN* |
| 01             | Input               | 12.288MHz clock input from BIT-CLK                                   |
| 10             | Input               | 12.288MHz clock input from BIT-CLK                                   |
| 11             | Input               | 12.288MHz clock input from BIT-CLK                                   |

\*The default clock source should be decided by XTLSEL, once 14.318MHz clock is selected, internal digital PLL transfers it into 24.576MHz clock.

### 5.2 AC-Link

When ALC202 take serial data from AC97 controller, it sample **SDATA\_OUT** on the falling edge of **BIT\_CLK**. When ALC202 send serial data to AC97 controller, it start to drive **SDATA\_IN** on the rising edge of **BIT\_CLK**.

ALC202 will return any uninstalled bits or registers with 0 for read operation.. ALC202 also stuff the unimplemented slot or bit with 0 in **SDATA-IN**. Note that AC-LINK is MSB-justified.

Refer to “Audio CODEC ’97 Component Specification Revision 2.1/2.2” for detail.

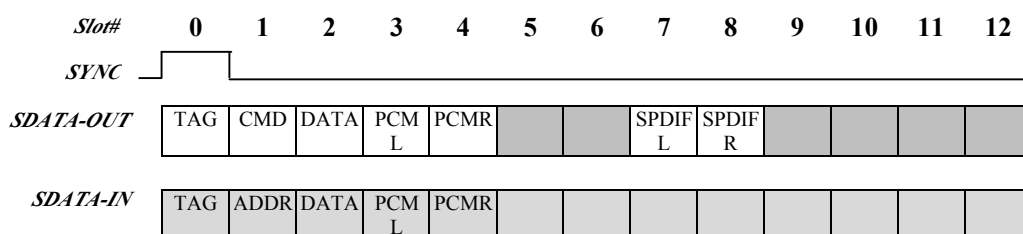


Fig5.2-1 Default ALC202 slot arrangement – CODEC ID = 00

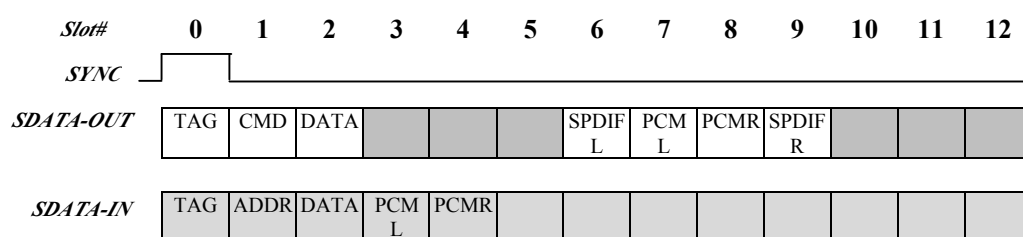


Fig5.2-2 Default ALC202 slot arrangement – CODEC ID = 01, 10

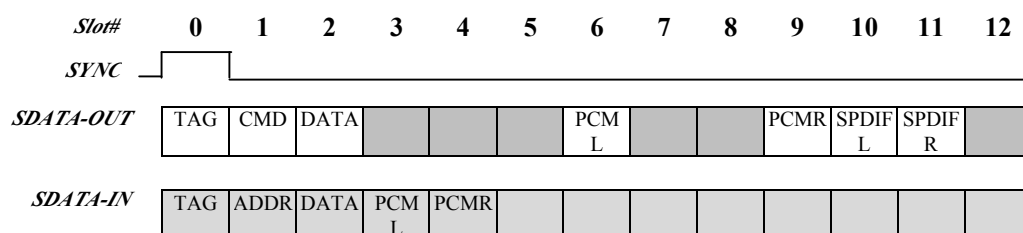




Fig5.2-3 Default ALC202 slot arrangement – CODEC ID = 11

### 5.3 Reset

There are 3 kinds of reset operation. *Cold*, *Warm* and *Register* reset which listed below:

| Reset Type      | Trigger condition                                     | CODEC response                                                   |
|-----------------|-------------------------------------------------------|------------------------------------------------------------------|
| <b>Cold</b>     | Assert RESET# for a specified period                  | Reset all hardware logic and all registers to its default value. |
| <b>Register</b> | Write register indexed 00h                            | Reset all registers to its default value.                        |
| <b>Warm</b>     | Driven SYNC high for specified period without BIT_CLK | Reactivates AC-LINK, no change to register values.               |

The AC97 controller should drive SYNC and SDATA-OUT low during the period of RESET# assertion to guarantee ALC202 reset successfully.

### 5.4 CD Input

Pay attention to differential CD input. Below is an example of differential CD input.

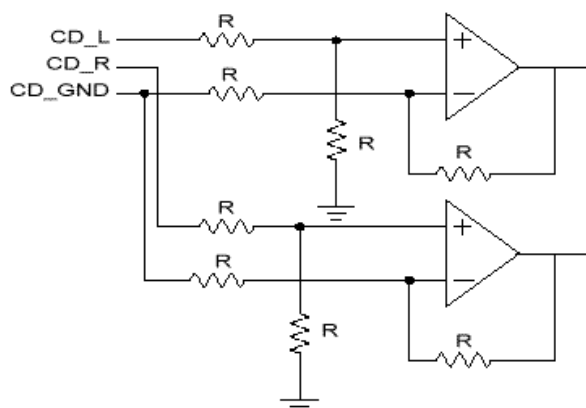


Fig 5.4-1 Example of differential CD input

### 5.5 Odd Addressed Register Access

ALC202 will return “0000h” when those odd-addressed registers and unimplemented registers are read.

### 5.6 Power-down Mode

Pay special attention to power down control register (index 26h), especially PR4 (powerdown AC-link).

### 5.7 Test Mode

#### 5.7.1 ATE In Circuit Test Mode:

SDATA\_OUT is sampled high at the trailing edge of RESET#. At this mode ALC202 will drive BIT\_CLK, SDATA\_IN, EAPD and SPDIFO to high impedance.

#### 5.7.2 Vendor Specific Test Mode:

SYNC is sampled high at the trailing edge of RESET#. At this mode ALC202 will drive BIT\_CLK, SDATA\_IN, EAPD and SPDIFO to high impedance.

**Note:** To make the most compatibility with AC' 97 rev2.2, ALC202 will float its digital output pins in both ATE and Vendor-Specific test mode. Please refer to AC' 97 rev2.2 section 9.2 for detail description about test mode.



### 5.8 Jack-Detect Function

JD (Jack-Detect) is an **internal pull high** input pin used to decide whether LINE-OUT should be auto muted or not. If JDE (Jack Detect Enable) is set and ALC202 detects the JD is floating or pull high (JDS=1), ALC202 will disable the analog output of LINE-OUT even the MX02 is not muted.

Fig5.8-1 shows the jack detect example to implement this function. If no audio plug is inserted in HP-OUT jack, JD is detected as low, LINE output normally. If audio plug is inserted, ALC202 **disable LINE output, still output to HP-OUT and MONO-OUT**. It's useful to some PC application especially in notebook environment.

If headphone output jack is not implemented and HP-OUT kept as floating, once JDE is enable, LINE output will be muted unless JD is pull low by a 10K ohm resistor (Fig5.8-2). To conquer this disadvantage, *the Jack-Detect mute LINE-OUT function is disable after power up (default JDE is 0)*, that make ALC202 compatible with others AC' 97. So *it is software's responsibility to enable this function if headphone jack detection is implemented*.

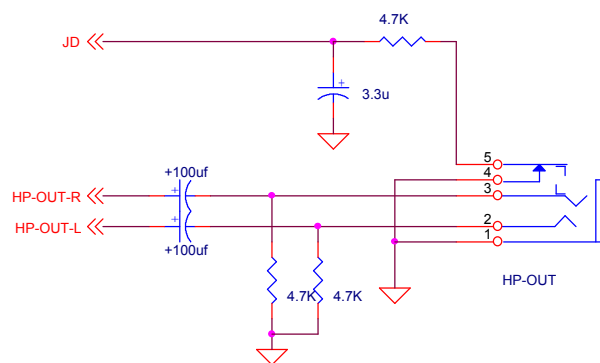


Fig5.8-1 Jack detect connection example

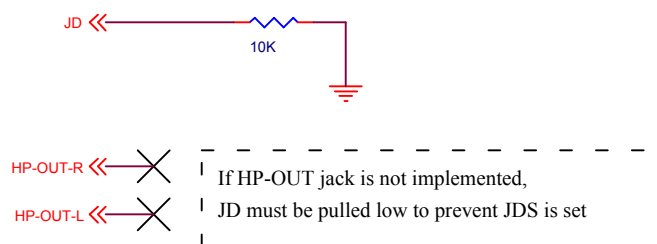


Fig5.8-2 JD is pull low by a 10K ohm resistor



Figure 5.8-3 shows another simple way to implement jack detect function without using ALC202's JD pin. It is especially easy for motherboard maker. No extra components needed, just layout issue. Once the HP-OUT jack is plugged in, output signals to LINE-OUT will be isolated, no signals output at LINE-OUT jack. The only drawback to this plan is software will not sense the HP-OUT jack is plugged in. It may be not convenient for software to pay attention to special application.

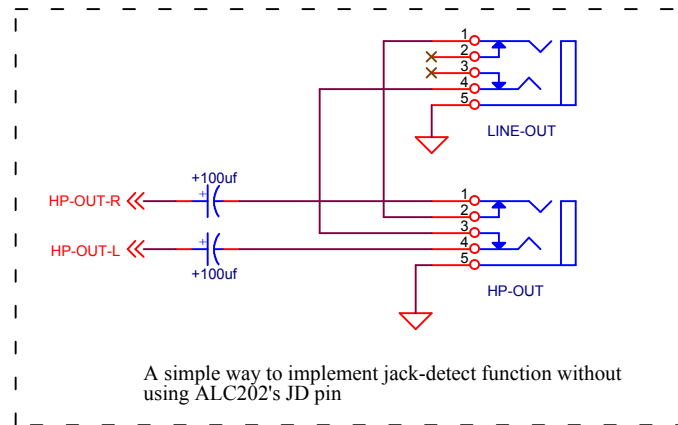


Fig5.9-3 Implement Jack-Detect function without using ALC202's pin



## 6. Electrical Characteristics

### 6.1 DC Characteristics

#### 6.1.0 Absolute Maximum Ratings:

| Parameter                            | Symbol                 | Min | Typ | Max  | Units |
|--------------------------------------|------------------------|-----|-----|------|-------|
| Power Supplies                       |                        |     |     |      |       |
| Digital                              | DVdd                   | 3.0 | 3.3 | 3.6  | V     |
| Analog                               | AVdd                   | 4.5 | 5.0 | 5.5  | V     |
| Operating Ambient Temperature        | Ta                     | 0   | -   | +70  | °C    |
| Storage Temperature                  | Ts                     |     |     | +125 | °C    |
| <b>ESD (Electrostatic Discharge)</b> |                        |     |     |      |       |
|                                      | Susceptibility Voltage |     |     |      |       |
| Others                               | Over 5000V             |     |     |      |       |

#### 6.1.1 Threshold Hold Voltage:

Dvdd= 3.3V±5%, T<sub>ambient</sub>=25°C, with 50pF external load.

| Parameter                                        | Symbol          | Min     | Typ  | Max       | Units |
|--------------------------------------------------|-----------------|---------|------|-----------|-------|
| Input voltage range                              | V <sub>in</sub> | -0.30   | -    | Dvdd+0.30 | V     |
| Low level input voltage (SYNC,SDATA_OUT,RESET#)  | V <sub>IL</sub> | -       | 0.7  | 0.35Dvdd  | V     |
| Low level input voltage (XTAL_IN,BIT_CLK)        | V <sub>IL</sub> | -       | 1.0  | 0.35Dvdd  | V     |
| Low level input voltage (ID1#,ID0#)              | V <sub>IL</sub> | -       | 1.2  | 0.35Dvdd  | V     |
| High level input voltage (SYNC,SDATA_OUT,RESET#) | V <sub>IH</sub> | 0.4DVdd | 1.7  | -         | V     |
| High level input voltage (XTAL_IN,BIT_CLK)       | V <sub>IH</sub> | 0.4DVdd | 2.2  | -         | V     |
| High level input voltage (ID1#,ID0#)             | V <sub>IH</sub> | 0.4DVdd | 1.7  | -         | V     |
| High level output voltage                        | V <sub>OH</sub> | 0.9DVdd |      | -         | V     |
| Low level output voltage                         | V <sub>OL</sub> | -       | -    | 0.1DVdd   | V     |
| Input leakage current                            | -               | -10     | -    | 10        | uA    |
| Output leakage current (Hi-Z)                    | -               | -10     | -    | 10        | uA    |
| Output buffer drive current                      | -               | -       | 5    | -         | mA    |
| Internal pull up resistance                      | -               | 50k     | 100k | 200k      | Ω     |

#### 6.1.2 Digital Filter Characteristics:

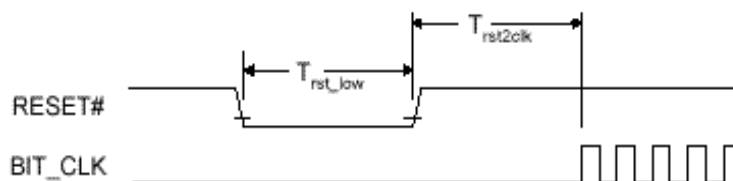
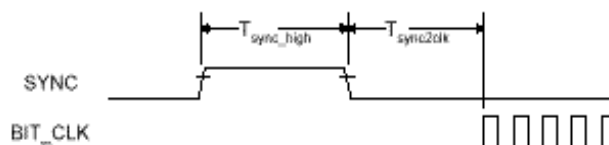
| Filter             | Symbol                      | Min  | Typ      | Max  | Units |
|--------------------|-----------------------------|------|----------|------|-------|
| ADC Lowpass Filter | Passband                    | 0    | -        | 19.2 | KHz   |
|                    | Stopband                    | 28.8 |          |      | KHz   |
|                    | Stopband Rejection          |      | -76.0    |      | dB    |
|                    | Passband Frequency Response |      | +/- 0.15 |      | dB    |
| DAC Lowpass Filter | Passband                    | 0    | -        | 19.2 | KHz   |
|                    | Stopband                    | 28.8 |          |      | KHz   |
|                    | Stopband Rejection          |      | -78.5    |      | dB    |
|                    | Passband Frequency Response |      | +/- 0.15 |      | dB    |

**6.1.3 S/PDIF Output Characteristics:**Dvdd= 3.3V, T<sub>ambient</sub>=25<sup>0</sup>C, with 75 ohm external load.

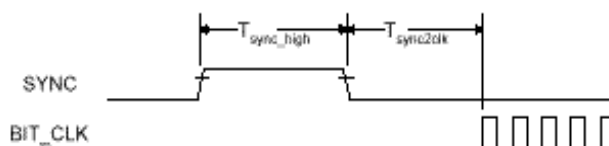
| Parameter                 | Symbol          | Min | Typ | Max | Units |
|---------------------------|-----------------|-----|-----|-----|-------|
| High level output voltage | V <sub>OH</sub> | 3.0 | 3.3 |     | V     |
| Low level output voltage  | V <sub>OL</sub> | -   | 0   | 0.5 | V     |

**6.2 AC Timing Characteristics****6.2.1 Cold Reset:**

| Parameter                                | Symbol               | Min   | Typ | Max | Units |
|------------------------------------------|----------------------|-------|-----|-----|-------|
| RESET# active low pulse width            | T <sub>rst_low</sub> | 1.0   | -   | -   | us    |
| RESET# inactive to BIT_CLK Startup delay | T <sub>rst2clk</sub> | 162.8 | -   | -   | ns    |

**Fig 6.2.1-1 Cold reset timing diagram****6.2.2 Warm Reset:****Fig 6.2.2-1 Cold reset timing diagram**

| Parameter                              | Symbol                 | Min   | Typ | Max | Units |
|----------------------------------------|------------------------|-------|-----|-----|-------|
| SYNC active high pulse width           | T <sub>sync_high</sub> | 1.0   | -   | -   | us    |
| SYNC inactive to BIT_CLK Startup delay | T <sub>sync2clk</sub>  | 162.8 | -   | -   | ns    |

**6.2.3 AC-Link Clocks:****Fig 6.2.3-1 BIT\_CLK and SYNC timing diagram**

| Parameter                         | Symbol                  | Min | Typ    | Max | Units |
|-----------------------------------|-------------------------|-----|--------|-----|-------|
| BIT_CLK frequency                 |                         | -   | 12.288 | -   | MHz   |
| BIT_CLK period                    | T <sub>clk_period</sub> | -   | 81.4   | -   | ns    |
| BIT_CLK output jitter             |                         | -   | -      | 750 | ps    |
| BIT_CLK high pulse width (note 2) | T <sub>clk_high</sub>   | 36  | 40.7   | 45  | ns    |
| BIT_CLK low pulse width (note 2)  | T <sub>clk_low</sub>    | 36  | 40.7   | 45  | ns    |
| SYNC frequency                    |                         | -   | 48.0   | -   | KHz   |



|                       |                          |   |      |   |    |
|-----------------------|--------------------------|---|------|---|----|
| SYNC period           | $T_{\text{sync period}}$ | - | 20.8 | - | us |
| SYNC high pulse width | $T_{\text{sync high}}$   | - | 1.3  | - | us |
| SYNC low pulse width  | $T_{\text{sync low}}$    | - | 19.5 | - | us |

Note 1: Worse case duty cycle restricted to 45/55.

#### 6.2.4 Data Output and Input Times:

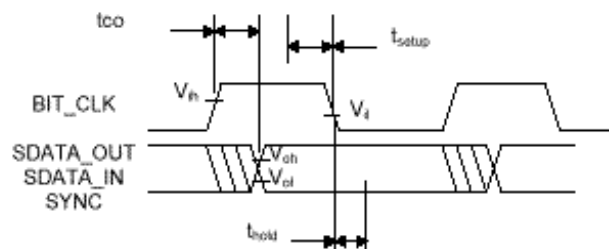


Fig 6.2.4-1 Data Output and Input timing diagram

| Parameter                                      | Symbol   | Min | Typ | Max | Units |
|------------------------------------------------|----------|-----|-----|-----|-------|
| Output Valid Delay from rising edge of BIT_CLK | $t_{co}$ | -   | -   | 15  | ns    |

Note 1 : Timing is for SDATA and SYNC outputs with respect to BIT\_CLK *at the device driving the output.*  
Note 2 : 50pF external load

| Parameter                               | Symbol             | Min | Typ | Max | Units |
|-----------------------------------------|--------------------|-----|-----|-----|-------|
| Input Setup to falling edge of BIT_CLK  | $t_{\text{setup}}$ | 10  | -   | -   | ns    |
| Input Hold from falling edge of BIT_CLK | $t_{\text{hold}}$  | 10  | -   | -   | ns    |

Note : Timing is for SDATA and SYNC outputs with respect to BIT\_CLK *at the device driving the output.*

| Parameter                                      | Symbol | Min | Typ | Max | Units |
|------------------------------------------------|--------|-----|-----|-----|-------|
| BIT_CLK combined rise or fall plus flight time |        | -   | -   | 7   | ns    |
| SDATA combined rise or fall plus flight time   |        | -   | -   | 7   | ns    |

Note : Combined rise or fall plus flight times are provided for worst case scenario modeling purpose.

#### 6.2.5 Signal Rise and Fall Times:

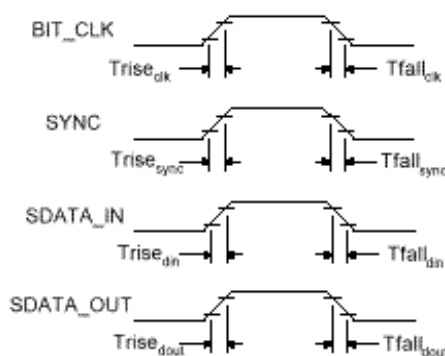


Fig 6.2.5-1 Signal Rise and Fall timing diagram



| Parameter                                                                                | Symbol            | Min | Typ | Max | Units |
|------------------------------------------------------------------------------------------|-------------------|-----|-----|-----|-------|
| BIT_CLK rise time                                                                        | $T_{rise_{clk}}$  | -   | -   | 6   | ns    |
| BIT_CLK fall time                                                                        | $T_{fall_{clk}}$  | -   | -   | 6   | ns    |
| SYNC rise time                                                                           | $T_{rise_{sync}}$ | -   | -   | 6   | ns    |
| SYNC fall time                                                                           | $T_{fall_{sync}}$ | -   | -   | 6   | ns    |
| SDATA_IN rise time                                                                       | $T_{rise_{din}}$  | -   | -   | 6   | ns    |
| SDATA_IN fall time                                                                       | $T_{fall_{din}}$  | -   | -   | 6   | ns    |
| SDATA_OUT rise time                                                                      | $T_{rise_{dout}}$ | -   | -   | 6   | ns    |
| SDATA_OUT fall time                                                                      | $T_{fall_{dout}}$ | -   | -   | 6   | ns    |
| Note 1: 75pF external load (50 pF in AC'97 rev2.1)                                       |                   |     |     |     |       |
| Note 2: rise is from 10% to 90% of V <sub>dd</sub> (V <sub>ol</sub> to V <sub>oh</sub> ) |                   |     |     |     |       |
| Note 3: fall is from 90% to 10% of V <sub>dd</sub> (V <sub>oh</sub> to V <sub>ol</sub> ) |                   |     |     |     |       |

### 6.2.6 AC-Link Low Power Mode Timing:



Fig 6.2.6-1 AC-Link low power mode timing diagram

| Parameter                              | Symbol          | Min | Typ | Max | Units |
|----------------------------------------|-----------------|-----|-----|-----|-------|
| End of slot 2 to BIT_CLK, SDATA_IN low | $T_{s2\_pdown}$ | -   | -   | 1.0 | us    |

### 6.2.7 ATE Test Mode:

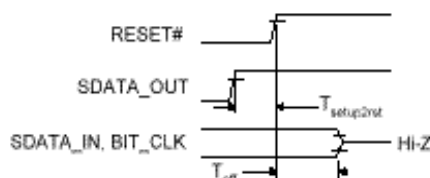


Fig 6.2.6-1 ATE test mode timing diagram

\*To meet AC'97 rev2.2, there are EAPD, SPDIFO, BIT\_CLK and SDATA\_IN should be floating in test mode.

| Parameter                                               | Symbol          | Min  | Typ | Max  | Units |
|---------------------------------------------------------|-----------------|------|-----|------|-------|
| Setup to trailing edge of RESET# (also applies to SYNC) | $T_{setup2rst}$ | 15.0 | -   | -    | ns    |
| Rising edge of RESET# to Hi-Z delay                     | $T_{off}$       | -    | -   | 25.0 | ns    |

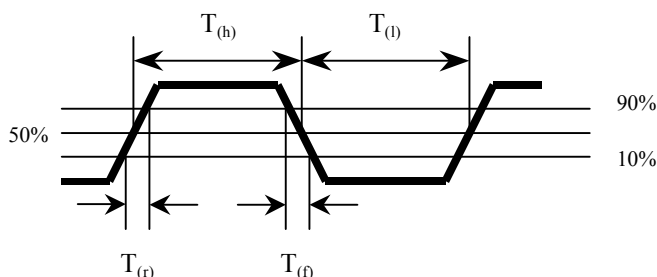
**6.2.8 AC-Link IO Pin Capacitance and Loading:**

| Output Pin                        | 1 Codec | 2 Codec | 3 Codec | 4 Codec |
|-----------------------------------|---------|---------|---------|---------|
| BIT_CLK (must support ≥ 2 Codecs) | 55pF    | 62.5pF  | 75pF    | 85pF    |
| SDATA_IN                          | 47.5pF  | 55pF    | 60pF    | 62.5pF  |

**6.2.9 SPDIF output:**

| SPDIF OUT           | Min | Typ | Max | Unit |
|---------------------|-----|-----|-----|------|
| Rise time/fall time | 0   |     | 10  | %    |
| Duty cycle          | 45  |     | 55  | %    |

Note :



$$\text{Rise time} = 100 * T(r) / (T(l) + T(h)) \%$$

$$\text{Fall time} = 100 * T(f) / (T(l) + T(h)) \%$$

$$\text{Duty cycle} = 100 * T(h) / (T(l) + T(h)) \%$$

**6.2.10 BIT-CLK and SDATA-IN state when RESET# is active:**

When RESET# is active the BIT-CLK and SDATA-IN must be floating by internal pull low 100K resistors. So the ac-link signals are driven by another AC' 97 on CNR board. This requirement is not mentioned in AC' 97 specification rev2.1, please refer CNR (Communication Network Riser) specification rev1.0 page23~25 to get detail information.

**7. Analog Performance Characteristics**

Standard test conditions:  $T_{\text{ambient}} = 25^{\circ}\text{C}$ ,  $Dvdd = 3.3\text{V} \pm 5\%$ ,  $Avdd = 5.0\text{V} \pm 5\%$

1KHz input sine wave; Sampling frequency=48KHz; 0dB=1Vrms

**10KΩ/50pF load**; Test bench Characterization BW: 10Hz~22KHz

0dB attenuation; tone and 3D disabled

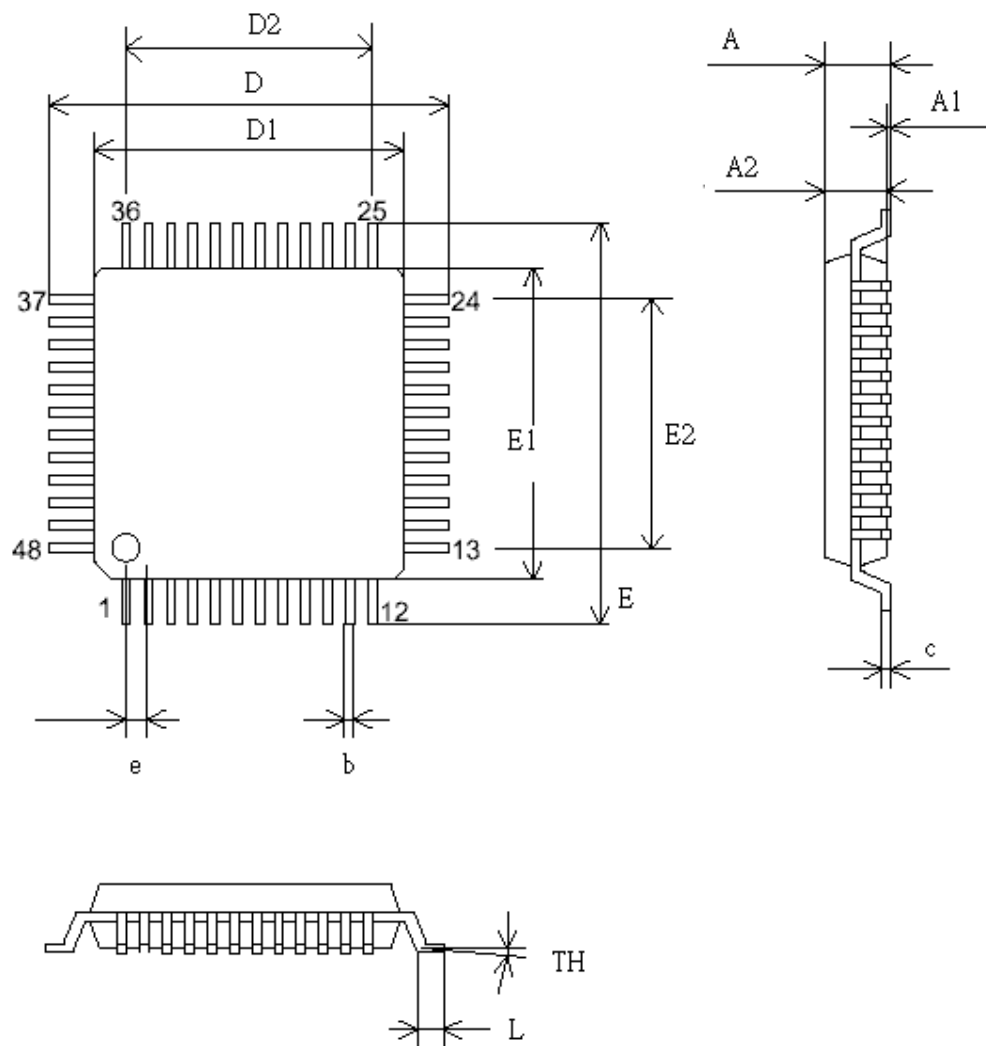
| Parameter                 | Min | Typ  | Max  | Units |
|---------------------------|-----|------|------|-------|
| Full scale input voltage  |     |      |      |       |
| Line inputs (Mixers)      | -   | 1.6  | -    | Vrms  |
| Line inputs (A/D)         | -   | 1.2  | -    |       |
| Mic input (0 dB)          | -   | 1.6  | -    |       |
| Mic input (20 dB boost)   | -   | 0.16 | -    |       |
| Full scale output voltage |     |      |      |       |
| LINE-OUT                  | -   | 1.0  | 1.50 | Vrms  |
| HEADPHONE-OUT             | -   | 1.7  | -    | Vrms  |



|                                           |        |      |          |            |
|-------------------------------------------|--------|------|----------|------------|
| Analog to Analog S/N                      | -      | 95   | -        | dB         |
| CD to LINE-OUT                            | -      | 95   | -        |            |
| Other to LINE-OUT                         | -      | 95   | -        |            |
| Analog frequency response                 | 16     | -    | 22,000   | Hz         |
| S/N (A-weighted)                          |        |      |          |            |
| D/A                                       | -      | 90   | -        | dB         |
| A/D                                       | -      | 90   | -        |            |
| Total Harmonic Distortion (A-weighted)    |        |      |          |            |
| D/A                                       | -      | -85  | -        | dB         |
| A/D                                       | -      | -85  | -        |            |
| D/A & A/D frequency response              | 20     | -    | 19,200   | Hz         |
| Transition Band                           | 19,200 | -    | 28,800   | Hz         |
| Stop Band                                 | 28,800 | -    | $\infty$ | Hz         |
| Stop Band Rejection                       | -75    | -    | -        | dB         |
| Out-of-Band Rejection                     | -      | -65  | -        | dB         |
| Group delay                               | -      | -    | 1        | ms         |
| Power Supply Rejection                    | -      | -65  | -        | dB         |
| MIC Amplifier 20dB Gain                   | 18     | 20   | 22       | dB         |
| Master Volume (Mono,Stereo) : 32 step     |        |      |          |            |
| Step Size                                 | -      | 1.5  | -        | dB         |
| Attenuation Control Range                 | 0      | -    | 46.5     | dB         |
| PC Beep Volume : 16 step                  |        |      |          |            |
| Step Size                                 | -      | 3.0  | -        | dB         |
| Attenuation Control Range                 | 0      | -    | 45       | dB         |
| Analog Mixer Volume : 32 step             |        |      |          |            |
| Step Size                                 | -      | 1.5  | -        | dB         |
| Gain Control Range                        | -34.5  | -    | +12      | dB         |
| Record Gain : 16 step                     |        |      |          |            |
| Step Size                                 | -      | 1.5  | -        | dB         |
| Gain Control Range                        | 0      | -    | +22.5    | dB         |
| Input impedance (gain = 0dB, mixer = off) |        |      |          |            |
| LINE-IN                                   |        | 64   |          | K $\Omega$ |
| CD-IN, AUX-IN, VIDEO-IN, MIC-IN           |        | 32   |          | K $\Omega$ |
| PCBEEP, PHONE                             |        | 16   |          | K $\Omega$ |
| Analog Output Impedance (LINE-OUT)        |        | 10   |          | $\Omega$   |
| Analog Output Impedance (HP-OUT)          |        | 10   |          | $\Omega$   |
| Power Supply Current                      |        |      |          |            |
| VA=5.0v,                                  |        | 60   | 70       | mA         |
| VD=3.3v                                   |        | 10   |          | mA         |
| Power Down Current                        |        |      |          |            |
| VA=5.0v                                   |        | -    | 500      | $\mu$ A    |
| VD=3.3v                                   |        |      | 1000     | $\mu$ A    |
| V <sub>refout</sub>                       | -      | 2.50 | -        | V          |
| V <sub>refout</sub> Drive Current         |        | 8    |          | mA         |



## 8. Package:



| SYMBOL | MILLIMETER |      |      | INCH      |       |       |
|--------|------------|------|------|-----------|-------|-------|
|        | MIN.       | TYP. | MAX. | MIN.      | TYP.  | MAX.  |
| A      |            |      | 1.60 |           |       | 0.063 |
| A1     | 0.05       |      | 0.15 | 0.002     |       | 0.006 |
| A2     | 1.35       | 1.40 | 1.45 | 0.053     | 0.055 | 0.057 |
| c      | 0.09       |      | 0.20 | 0.004     |       | 0.008 |
| D      | 9.00 BSC   |      |      | 0.354 BSC |       |       |
| D1     | 7.00 BSC   |      |      | 0.276 BSC |       |       |
| D2     | 5.50       |      |      | 0.217     |       |       |
| E      | 9.00 BSC   |      |      | 0.354 BSC |       |       |
| E1     | 7.00BSC    |      |      | 0.276 BSC |       |       |
| E2     | 5.50       |      |      | 0.217     |       |       |
| b      | 0.17       | 0.20 | 0.27 | 0.007     | 0.008 | 0.011 |
| e      | 0.50 BSC   |      |      | 0.016 BSC |       |       |
| TH     | 0°         | 3.5° | 7°   | 0°        | 3.5°  | 7°    |
| L      | 0.45       | 0.60 | 0.75 | 0.018     | 0.024 | 0.030 |

