

Audio sound controller

BD3861FS

The BD3861FS is an audio sound controller IC for micro-component stereo systems. Tone and volume can be controlled easily by two-line serial control from micro-controller.

●Applications

Micro-component stereo systems, radio cassette players and mini-component stereo systems

●Features

- 1) Built-in volume, tone (bass, middle and treble), input gain amplifier and input selector.
- 2) The volume control of resistance ladder type allows the low distortion and low noise in Bi-CMOS process.
- 3) Two-line serial interface.
- 4) The built-in input gain amplifier reduces the needs of external input, and this IC is suitable for space-saving design.
- 5) Residual noise can be reduced by separating the front stage volume control from the rear stage volume control.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{CC}	10	V
Power dissipation	P _d	800*	mW
Operating temperature	T _{opr}	–25 to +75	°C
Storage temperature	T _{stg}	–55 to +150	°C

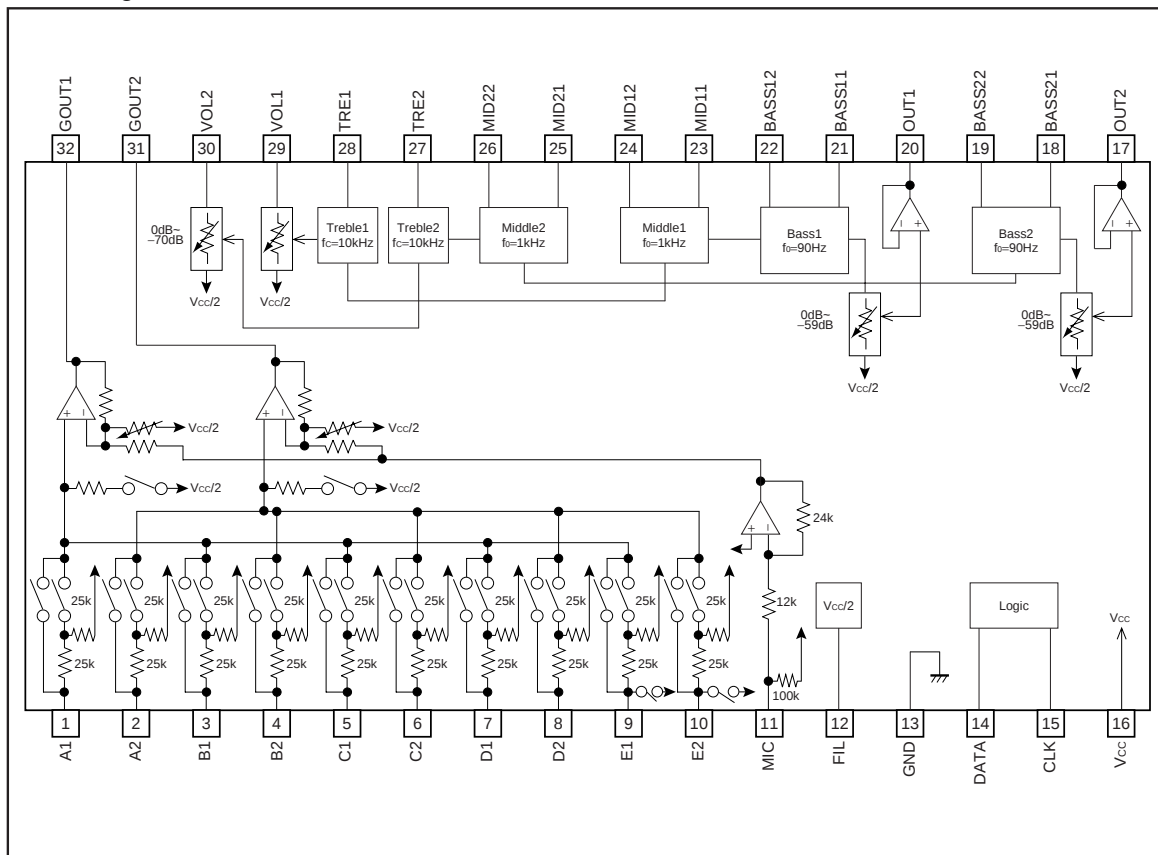
*Reduced by 6.4mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V _{CC}	6.5	–	9.5	V

Audio ICs

●Block diagram



Audio ICs

●Pin equivalent circuit and description

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
1 2 3 4 5 6 7 8	A1 A2 B1 B2 C1 C2 D1 D2	$V_{CC}/2$		A pin for inputting a sound signal. It is suitable for input of CD, MD, tuner and tape. Connect this pin to a front stage circuit through a coupling capacitor.
9 10	E1 E2	$V_{CC}/2$		A pin for inputting a sound signal. It is suitable for input from outside of the pin.
11	MIC	$V_{CC}/2$		A pin for microphone input.
12	FIL	$V_{CC}/2$		$V_{CC}/2$ Voltage for power supply of signal system.

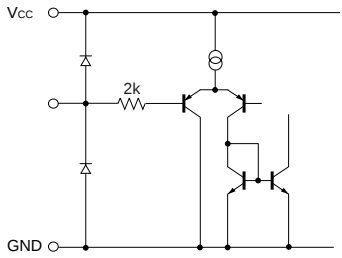
Audio ICs

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
17 20	OUT2 OUT1	$V_{CC}/2$		A pin for outputting a sound signal. Connect this pin to a rear stage circuit through a coupling capacitor.
18 21	BASS21 BASS11	$V_{CC}/2$		A pin for setting central frequency (f_0) of bass and for setting gain.
19 22	BASS22 BASS12	$V_{CC}/2$		A pin for setting central frequency (f_0) of bass and for setting gain.
23 25	MID11 MID21	$V_{CC}/2$		A pin for setting central frequency (f_0) of middle and for setting gain.

Audio ICs

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
24 26	MID12 MID22	$V_{CC}/2$		A pin for setting central frequency (f_0) of middle and for setting gain.
27 28	TRE2 TRE1	$V_{CC}/2$		A pin for setting cut-off frequency (f_c) of treble and for setting gain.
29 30	VOL1 VOL2	$V_{CC}/2$		A pin for inputting sound signal into input volume control. The input impedance is 36k Ω (upon Typ.).
31 32	GOUT2 GOUT1	$V_{CC}/2$		A pin for outputting input gain.

Audio ICs

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
14	DATA	—		A pin for inputting a serial control data.
15	CLK			
16	Vcc	Vcc	—	Power supply pin.
13	GND	0V	—	A ground pin.

Audio ICs

● **Electrical characteristics** (Unless specified particularly, $V_{CC}=9V$, $f=1kHz$, $V_{IN}=1V_{rms}$, $R_g=600\Omega$, $R_L=10k\Omega$, $T_a=25^\circ C$, INPUT Gain=0dB, VOL=0dB, Bass, Middle, Treble=0dB) Measurement circuit is Fig.1.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	SW No.								Select address/Serial data (HEX notation)								Measurement point
							1/4	2/5	3/8	7	8	9/10	11/12	1	2	3	4-1	4-2	5-1	5-2			
<TOTAL>																							
Circuit current	I _Q	—	13.0	26.0	mA	Without signal	1	1	—	2	1	1	2	00	02	01	05	0D	03	0B		I	
Output voltage gain	GV	-1.5	0.0	1.5	dB	G _V =20log(O1/V _{IN})	1	2	2	2	2	1	2	00	02	01	05	0D	03	0B		O1	
						G _V =20log(O2/V _{IN})																O2	
Total harmonic distortion	THD	—	0.02	0.08	%	V _{IN} =2V _{rms} 400-30kHz BPF	1	2	2	2	2	1	2	00	02	01	05	0D	03	0B		O1	
Maximum output voltage	V _{OM}	2.0	2.5	—	V _{rms}	THD=1%	1	2	2	2	2	1	2	00	02	01	05	0D	03	0B		O1	
																						O2	
Maximum noise voltage	V _{NO}	—	8.0	15.0	μV _{rms}	R _g =0kΩ, IHF-A	1	1	—	2	2	1	2	00	02	01	05	0D	03	0B		O1	
																						O2	
Cross-talk between channels	CT	—	-80	-70	dB	R _g =0kΩ, IHF-A	1	2/1	2/-	2	2	1	2	00	02	01	05	0D	03	0B		O2	
						CT=20log(O1/O2)																O1	
<INPUT>																							
6dBSW gain	G _{V6}	5	6	7	dB	V _{IN} =200mV _{rms}	G _V =20log(G1/V _{IN})	1	2	2	2	2	1	1	00	02	11	05	0D	03	0B		G1
							G _V =20log(G2/V _{IN})																G2
Input voltage gain1	* G _{Vmax1}	-1	*1	+1	dB	V _{IN} =200mV _{rms} From 0 to 10dB	G _{Vmax1} =20log(G1/V _{IN})	1	2	2	2	2	1	1	00	02	01	*3 A5	0D	03	0B		G1
							G _{Vmax1} =20log(G2/V _{IN})															G2	
Input voltage gain2	* G _{Vmax12}	-1.5	*2	+1.5	dB	V _{IN} =200mV _{rms} From 12 to 20dB	G _{Vmax1} =20log(G1/V _{IN})	1	2	2	2	2	1	1	00	02	01	*4 F5	0D	03	0B		G1
							G _{Vmax1} =20log(G2/V _{IN})															G2	
Input gain switch step	G _{Vmax1st}	—	2	—	dB	From 0 to 20dB		1	2	2	2	2	1	1	00	02	01	—	0D	03	0B		G1
																						G2	
INPUT total harmonic distortion	THD _I	—	0.02	0.08	%	V _{IN} =2V _{rms} 400-30kHz BPF	1	2	2	2	2	1	1	00	02	01	05	0D	03	0B		G1	
INPUT maximum output voltage	V _{OMI}	2.0	2.5	—	dB	THD=1%	1	2	2	2	2	1	1	00	02	01	05	0D	03	0B		G1	
																						G2	
Cross-talk between selectors	CS	—	-80.0	-70.0	dB	R _g =0kΩ, IHF-A	CS=20log(G1/V _{IN})	1	2	2	2	2	1	1	00	02	81	05	0D	03	0B		G1
							CS=20log(G2/V _{IN})																G2
Input resistance	R _I	35.0	50.0	65.0	kΩ	R _I =51k×V _{R2} / (V _{IN} -V _{R1})	1	2	1	2	2	1	1	00	02	01	05	0D	03	0B		V _{R1}	
						R _I =51k×V _{R2} / (V _{IN} -V _{R2})																V _{R2}	
"E" input SW attenuation	G _{RE}	—	-20.0	-15.0	dB	G _{RE} =20log(G1/V _{IN})	5	2	2	2	2	1	1	00	02	29	05	0D	03	0B		G1	
						G _{RE} =20log(G2/V _{IN})																G2	
<INPUT Volume>																							
Input Volume Gain1	* G _{IV1}	-2	*5	+2	dB	From 0 to -50dB	G _{IV1} =20log(O1/V _{IN})	1	1	—	2	2	2	1	00	*7 1A	01	05	0D	03	0B		O1
							G _{IV1} =20log(O2/V _{IN})															O2	
Input Volume Gain2	* G _{IV2}	-3	*6	+3	dB	From -54 to -70dB	G _{IV2} =20log(O1/V _{IN})	1	1	—	2	2	2	1	00	*8 7A	01	05	0D	03	0B		O1
							G _{IV2} =20log(O2/V _{IN})															O2	
Volume switch step1	G _{IVst1}	—	2	—	dB	From 0 to -50dB		1	1	—	2	2	2	1	00	—	01	05	0D	03	0B		O1
																						O2	
Volume switch step2	G _{IVst2}	—	4	—	dB	From -54 to -70dB		1	1	—	2	2	2	1	00	—	01	05	0D	03	0B		O1
																						O2	
MUTE level	G _{minI}	—	—	-90.0	dB	IHF-A	G _{minI} =20log(O1/V _{IN})	1	1	—	2	2	2	1	00	FA	01	05	0D	03	0B		O1
							G _{minI} =20log(O2/V _{IN})															O2	
<OUTPUT Volume>																							
Output Volume Gain	* G _{OV}	-1	*9	+1	dB	From 0 to -59dB	G _{OV} =20log(O1/V _{IN})	1	1	—	2	2	2	1	*10 DC	02	01	05	0D	03	0B		O1
							G _{OV} =20log(O2/V _{IN})															O2	
OUTPUT switch step	G _{OVst}	—	1	—	dB	From 0 to -59dB		1	1	—	2	2	2	1	—	02	01	05	0D	03	0B		O1
																						O2	
MUTE level	G _{minO}	—	—	-90.0	dB	IHF-A	G _{minO} =20log(O1/V _{IN})	1	1	—	2	2	2	1	FC	02	01	05	0D	03	0B		O1
							G _{minO} =20log(O2/V _{IN})															O2	

* It shows a specified value at the deviation from the setting value.

*1 0.2, 4, 6, 8, 10dB
 *2 12, 14, 16, 18, 20dB
 *3 Setting 10dB
 *4 Setting 20dB
 *5 From 0 to -50dB -2dB/STEP
 *6 From -54 to -70dB -4dB/STEP
 *7 Setting -50dB
 *8 Setting -70dB
 *9 From 0 to -59dB -1dB/STEP
 *10 Setting -59dB

Audio ICs

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	SW No.						Select address/Serial data (HEX notation)								Measurement point	
							1/4	2/5	3/8	7	8	9/10	11/12	1	2	3	4-1	4-2	5-1	5-2		
<BASS>																						
Maximum Bass boost gain	G _{BB}	12	14	16	dB	V _N =200mVrms, f=90Hz	G _{BB} =20log(O1/V _N)	1	2	2	2	1	2	00	02	01	05	ED	03	0B	O1	
						G _{BB} =20log(O2/V _N)	O2															
Maximum Bass cut gain	G _{BC}	-16	-14	-12	dB	V _N =200mVrms, f=90Hz	G _{BC} =20log(O1/V _N)	1	2	2	2	2	1	2	00	02	01	05	FD	03	0B	O1
						G _{BC} =20log(O2/V _N)	O2															
Bass switch step	G _{BST}	-	2	-	dB	V _N =200mVrms, f=90Hz		1	2	2	2	2	1	2	00	02	01	05	-	03	0B	O1
																						O2
<MIDDLE>																						
Maximum Middle boost gain	G _{MB}	10	12	14	dB	V _N =200mVrms	G _{MB} =20log(O1/V _N)	1	2	2	2	2	1	2	00	02	01	05	0D	E3	0B	O1
						G _{MB} =20log(O2/V _N)	O2															
Maximum Middle cut gain	G _{MC}	-14	-12	-10	dB	V _N =200mVrms	G _{MC} =20log(O1/V _N)	1	2	2	2	2	1	2	00	02	01	05	0D	F3	0B	O1
						G _{MC} =20log(O2/V _N)	O2															
Middle switch step	G _{MST}	-	2	-	dB	V _N =200mVrms		1	2	2	2	2	1	2	00	02	01	05	0D	-	0B	O1
																						O2
<TREBLE>																						
Maximum Treble boost gain	G _{TB}	10	12	14	dB	V _N =200mVrms, f=10kHz	G _{TB} =20log(O1/V _N)	1	2	2	2	2	1	2	00	02	01	05	0D	03	EB	O1
						G _{TB} =20log(O2/V _N)	O2															
Maximum Treble cut gain	G _{TC}	-14	-12	-10	dB	V _N =200mVrms, f=10kHz	G _{TC} =20log(O1/V _N)	1	2	2	2	2	1	2	00	02	01	05	0D	03	FB	O1
						G _{TC} =20log(O2/V _N)	O2															
Treble switch step	G _{TST}	-	2	-	dB	V _N =200mVrms, f=10kHz		1	2	2	2	2	1	2	00	02	01	05	0D	03	-	O1
																						O2
<Microphone amplifier>																						
Microphone voltage gain	G _{MIC}	4.5	6.0	7.5	dB	V _N =200mVrms	G _{MIC} =20log(O1/V _N)	1	1	-	1	2	1	2	00	02	01	05	0D	03	0B	O1
						G _{MIC} =20log(O2/V _N)	O2															

* It shows a specified value at the deviation from the setting value.

Audio ICs

●Measurement circuit

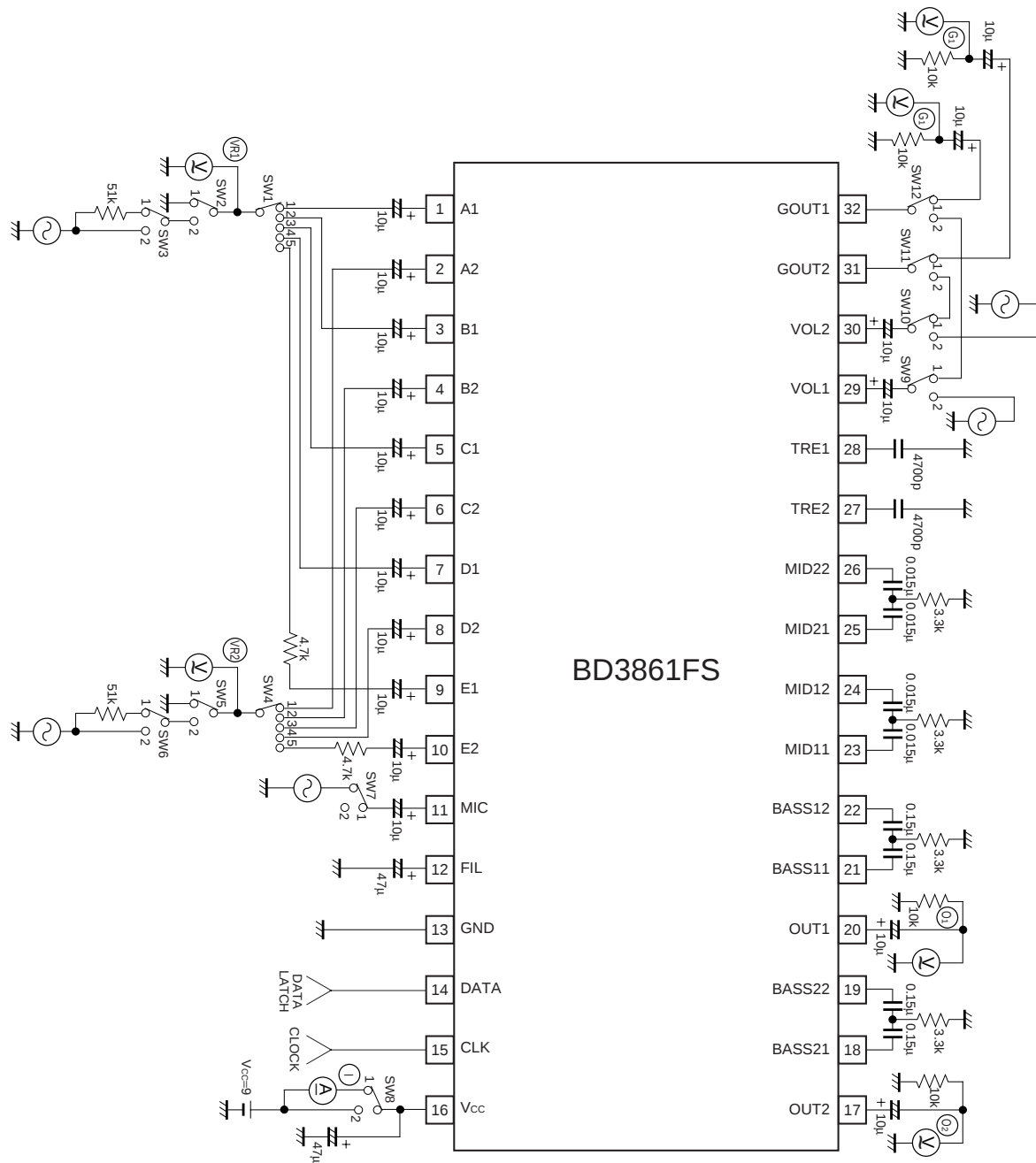


Fig.1

Audio ICs

●Attached components

External Parts of measurement circuit.

(1) Element marked with *

- Carbon-film resistor: $\pm 1\%$
- Film capacitor: $\pm 1\%$
- Ceramic capacitor: $\pm 1\%$

(2) Unless specified particularly, use the following external parts:

- Carbon-film resistor: $\pm 5\%$
- Film capacitor: $\pm 20\%$
- Electrolytic capacitor: $\pm 20\%$

Notes on wiring

- (1) GND shall be wired solidly.
- (2) Wiring pattern of CLK and DATA shall be away from that of analog unit and cross talk shall not be acceptable.
- (3) Wiring pattern of CLK and DATA shall not be parallel if possible. They shall be shielded, if they are adjacent to each other.

●Circuit operations

Specifications for control signal

(1) Timing of control signal

- Data is read at a leading edge of clock.
- Latch is read at a trailing edge of clock.
- Be sure to set DATA to LOW after latching.

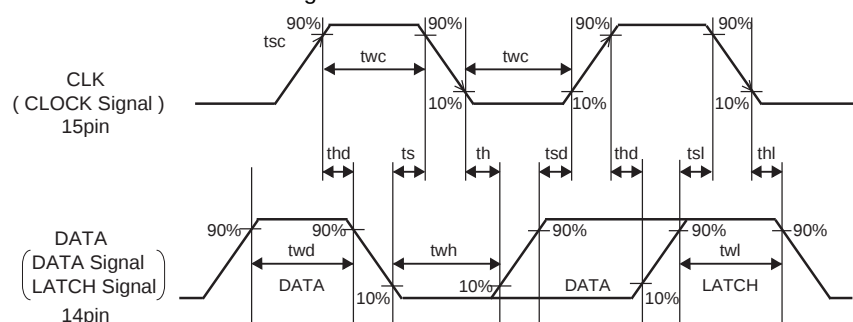


Fig.2

Constant of timing chart (Ta=25°C, Vcc=9V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
"High" input voltage	V _{IH}	2.6	—	5.5	V
"Low" input voltage	V _{IL}	0	—	1.1	V
Clock width	twc	2.0	—	—	μs
Data width	twd	2.0	—	—	μs
Latch width	twl	2.0	—	—	μs
"Low" hold width	twh	2.0	—	—	μs
Setup time (DATA→CLK)	tsd	1.0	—	—	μs
Hold time (CLK→DATA)	thd	1.0	—	—	μs
Setup time (CLK→LATCH)	tsl	1.0	—	—	μs
Hold time (DATA→LATCH)	thl	1.0	—	—	μs
"Low" setup time	ts	1.0	—	—	μs
"Low" hold time	th	1.0	—	—	μs

●Application example

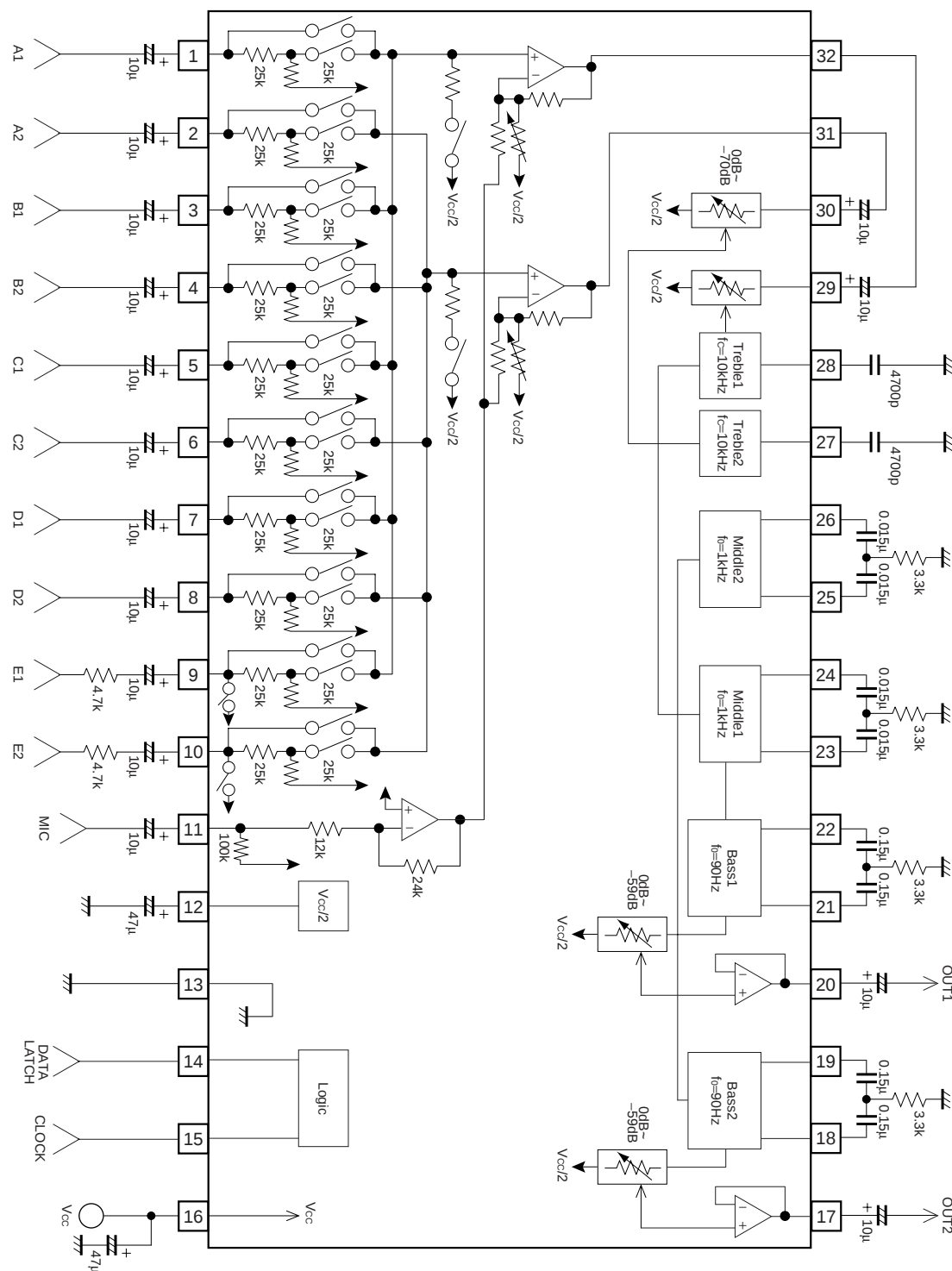


Fig.3

Audio ICs

●Operation notes

1. About operation voltage supply range

Within operation voltage supply range, basic circuit function operation is guaranteed within operation ambient temperature. But please confirm set up of constant and element, voltage set up and temperature set up on use.

2. About operation temperature range

If it within recommended operation voltage range, circuit function operation is guaranteed within operation temperature. It correlated to conditions of power dissipation to temperature.

Please watch out except condition stipulated by electrical characteristics within the range, It cannot guarantee standard value of electrical characteristics. But it retains original function.

3. About Application circuit

Example of application circuit drawing is convinced as recommendable, but please confirm characteristic including above-mentioned notes. At use with modification of external constant, please decide with enough margin considering distribution of this IC, external parts including quiescence characteristics and excessive characteristics. Please note that we have not yet confirmed any concerned patent rights completely.

4. Power-on reset

Any circuit to perform initialization in the IC upon power on is not contained. Therefore, be sure to send initial data to all the addresses upon power on. Moreover, be sure to mute the set side until the initial data has been sent. For data setting at the second time or later, necessary address only can be modified.

5. Schmidt circuit

This IC has the Schmidt circuit as preventive measures against logic signal input into the DATA (14pin) and CLK (15pin) terminals. Therefore, this IC is not affected so much by noise to a logic signal line. For the "High" voltage for logic control, voltage in a range from 2.6 to 5.5V is available.

6. Setting of input gain

Because of the S/N characteristics, it is recommendable to turn ON 6dBSW in input gain in a range between 6 and 20dB (in 2dB increment).

7. Input pin E1 (9pin) and E2 (10pin)

Input pin E1 (9pin) and E2 (10pin) has a built-in mute circuit. It is the optimal for the auxiliary input.

8. Microphone terminal

If the microphone terminal (11pin) is not used, use this IC in "open" because of the S/N characteristics.

9. Serial control

Wire the CLK terminal and DATA terminal taking care not to interfere with an analog signal line.

Audio ICs

●Electrical characteristic curves

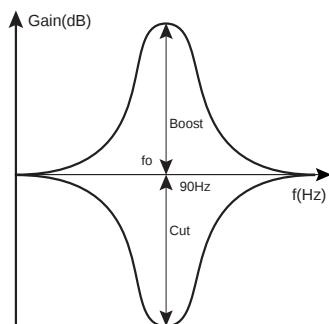


Fig.4 Tone control (Bass)

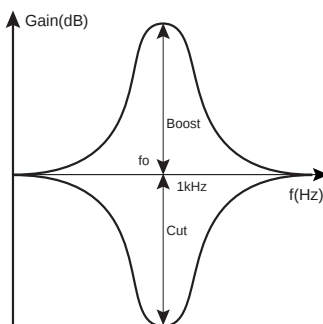


Fig.5 Tone control (Middle)

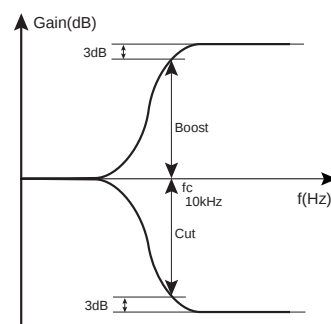
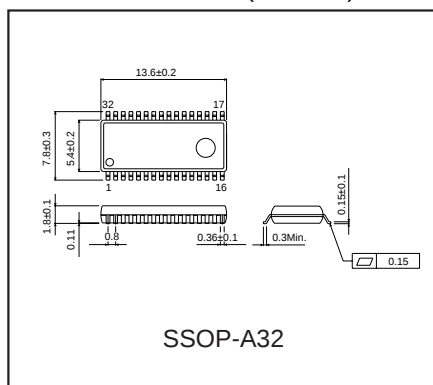


Fig.6 Tone control (Treble)

●External dimensions (Unit : mm)



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