

BB404M

Build in Biasing Circuit MOS FET IC
UHF/VHF RF Amplifier

HITACHI

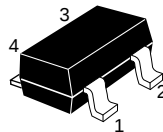
ADE-208-717A (Z)
2nd. Edition
Dec. 1998

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- High gain;
(PG = 29 dB typ. at $f = 200$ MHz)
- Low noise characteristics;
(NF = 1.2 dB typ. at $f = 200$ MHz)
- Wide supply voltage range;
Applicable with 5V to 9V supply voltage.
- Withstanding to ESD;
Build in ESD absorbing diode. Withstand up to 200V at $C=200\text{pF}$, $R_s=0$ conditions.
- Provide mini mold packages; MPAK-4R(SOT-143 var.)

Outline

MPAK-4R



1. Source
2. Drain
3. Gate2
4. Gate1

Notes: 1. Marking is "DX-".

2. BB404M is individual type number of HITACHI BBFET.

Absolute Maximum Ratings (Ta = 25°C)

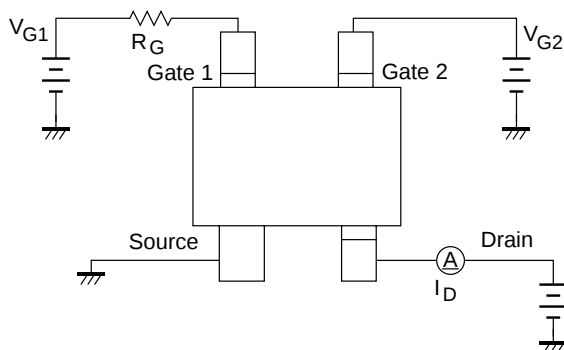
Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DS}	12	V
Gate1 to source voltage	V _{G1S}	±10 – 0	V
Gate2 to source voltage	V _{G2S}	±10	V
Drain current	I _D	25	mA
Channel power dissipation	P _{ch}	150	mW
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	–55 to +150	°C

Electrical Characteristics (Ta = 25°C)

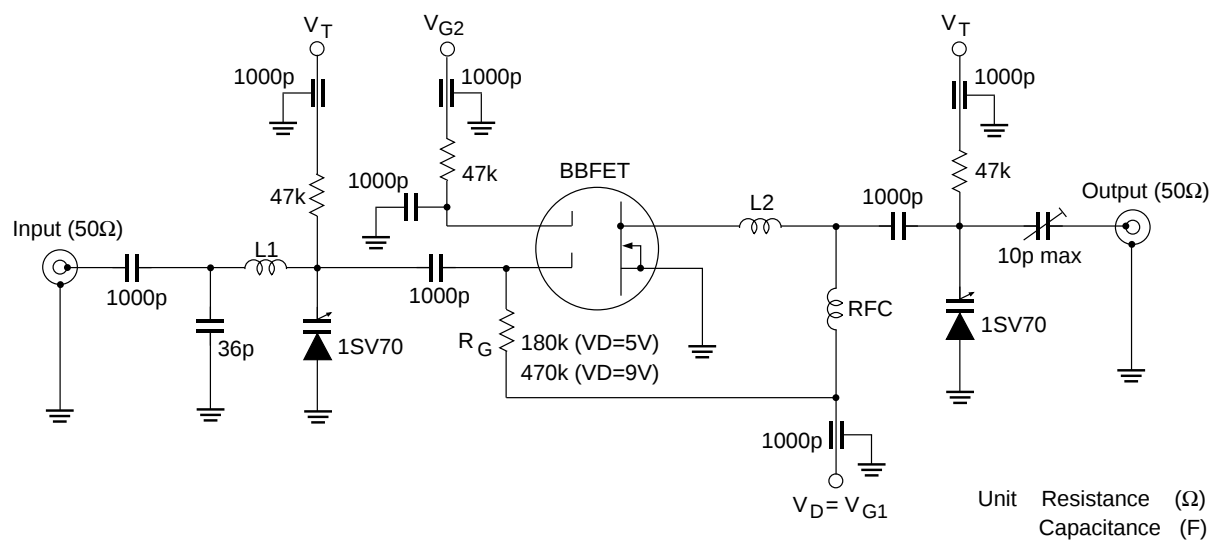
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	12	—	—	V	I _D = 200μA, V _{G1S} = V _{G2S} = 0
Gate1 to source breakdown voltage	V _{(BR)G1SS}	+10	—	—	V	I _{G1} = +10μA, V _{G2S} = V _{DS} = 0
Gate2 to source breakdown voltage	V _{(BR)G2SS}	±10	—	—	V	I _{G2} = ±10μA, V _{G1S} = V _{DS} = 0
Gate1 to source cutoff current	I _{G1SS}	—	—	+100	nA	V _{G1S} = +9V, V _{G2S} = V _{DS} = 0
Gate2 to source cutoff current	I _{G2SS}	—	—	±100	nA	V _{G2S} = ±9V, V _{G1S} = V _{DS} = 0
Gate1 to source cutoff voltage	V _{G1S(off)}	0.4	0.7	1.0	V	V _{DS} = 5V, V _{G2S} = 4V, I _D = 100μA
Gate2 to source cutoff voltage	V _{G2S(off)}	0.5	0.7	1.0	V	V _{DS} = 5V, V _{G1S} = 5V, I _D = 100μA
Input capacitance	C _{iss}	2.3	2.8	3.6	pF	V _{DS} = 5V, V _{G1} = 5V V _{G2S} = 4V, R _G = 180kΩ f = 1MHz
Output capacitance	C _{oss}	0.9	1.3	2.0	pF	
Reverse transfer capacitance	C _{rss}	0.003	0.02	0.05	pF	
Drain current	I _{D(op) 1}	9	15	19	mA	V _{DS} = 5V, V _{G1} = 5V V _{G2S} = 4V, R _G = 180kΩ
	I _{D(op) 2}	—	13	—	mA	V _{DS} = 9V, V _{G1} = 9V V _{G2S} = 6V, R _G = 470kΩ
Forward transfer admittance	y _{fs} 1	22	27	34	mS	V _{DS} = 5V, V _{G1} = 5V, V _{G2S} = 4V R _G = 180kΩ, f = 1kHz
	y _{fs} 2	—	27	—	mS	V _{DS} = 9V, V _{G1} = 9V, V _{G2S} = 6V R _G = 470kΩ, f = 1kHz
Power gain	PG1	24	29	32	dB	V _{DS} = 5V, V _{G1} = 5V, V _{G2S} = 4V R _G = 180kΩ, f = 200MHz
	PG2	—	29	—	dB	V _{DS} = 9V, V _{G1} = 9V, V _{G2S} = 6V R _G = 470kΩ, f = 200MHz
Noise figure	NF1	—	1.2	1.9	dB	V _{DS} = 5V, V _{G1} = 5V, V _{G2S} = 4V R _G = 180kΩ, f = 200MHz
	NF2	—	1.2	—	dB	V _{DS} = 9V, V _{G1} = 9V, V _{G2S} = 6V R _G = 470kΩ, f = 200MHz

Main Characteristics

Test Circuit for Operating Items ($I_{D(op)}$, $|y_{fs}|$, C_{iss} , C_{oss} , C_{rss} , NF , PG)

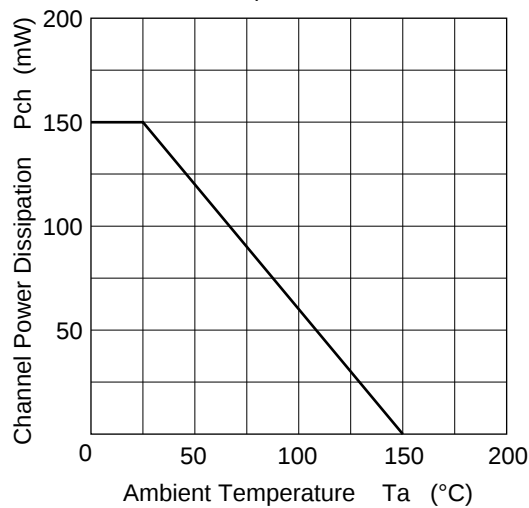


Power Gain, Noise Figure Test Circuit

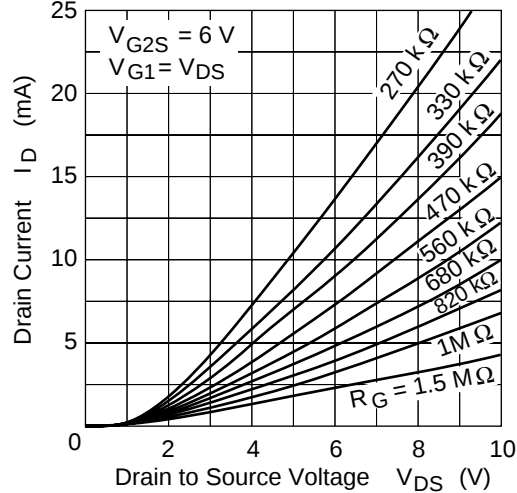


L1 : ϕ 1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
L2 : ϕ 1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
RFC : ϕ 1mm Enameled Copper Wire,Inside dia 5mm, 2Turns

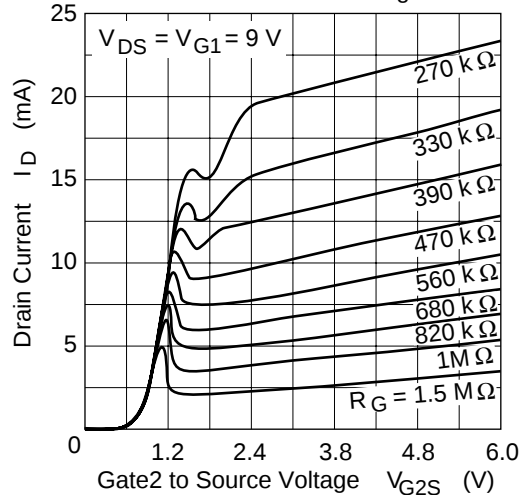
Maximum Channel Power
Dissipation Curve



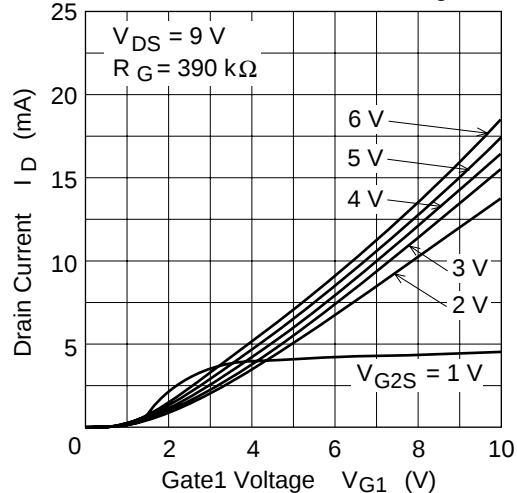
Typical Output Characteristics

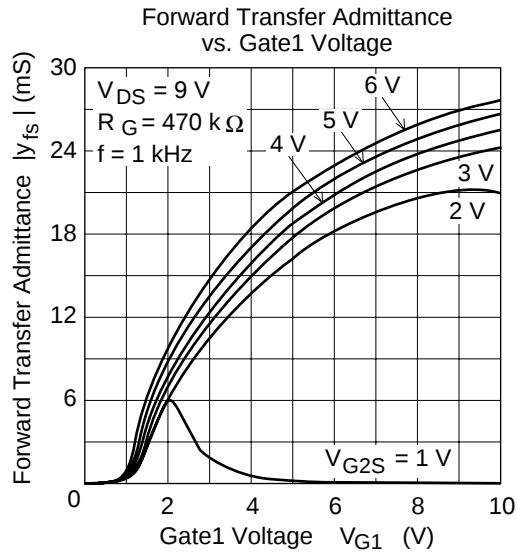
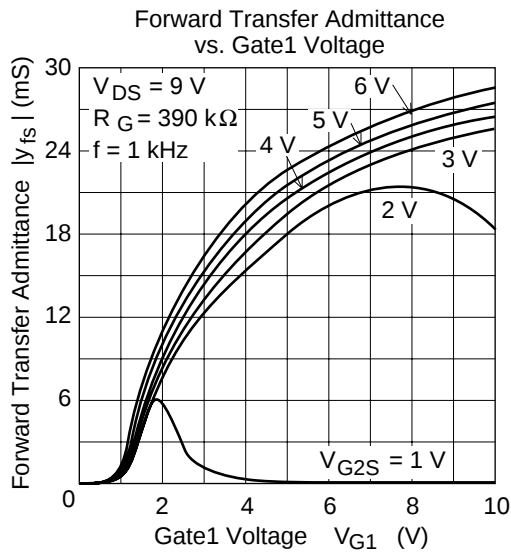
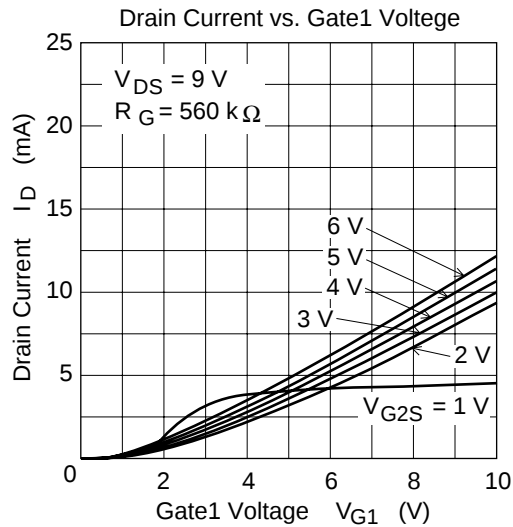
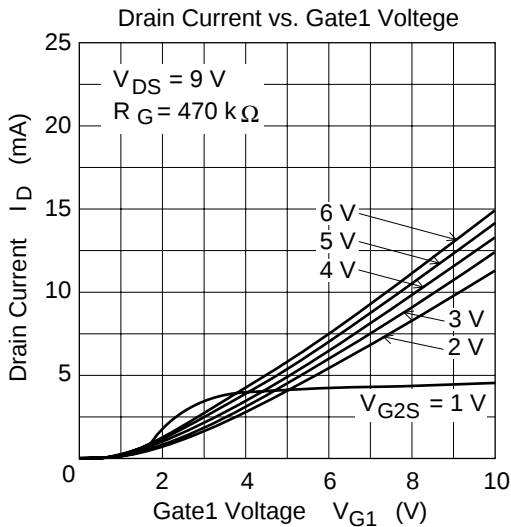


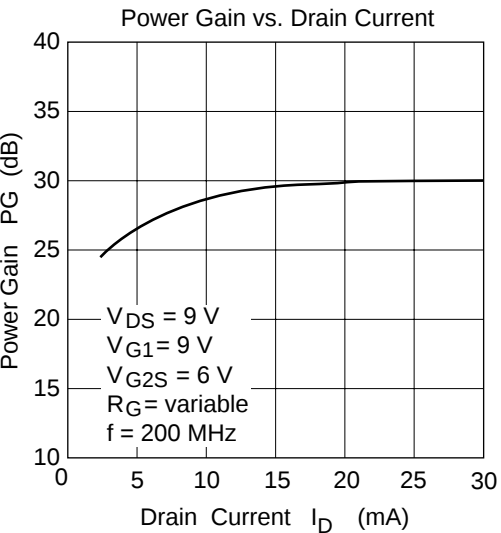
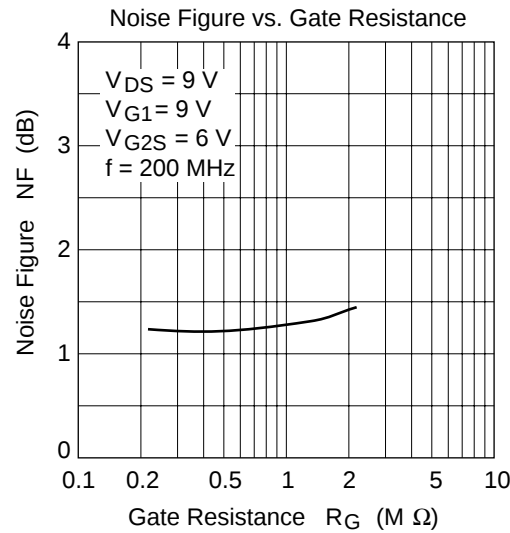
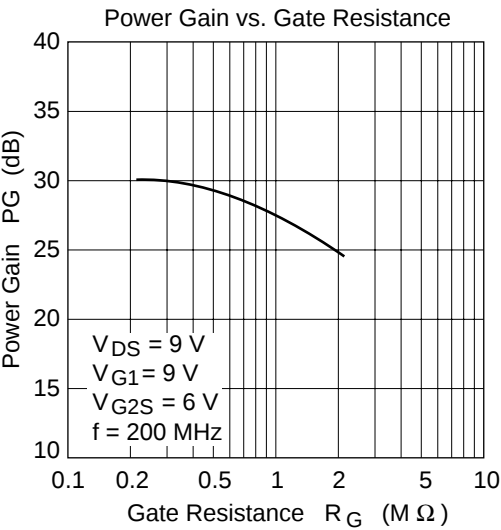
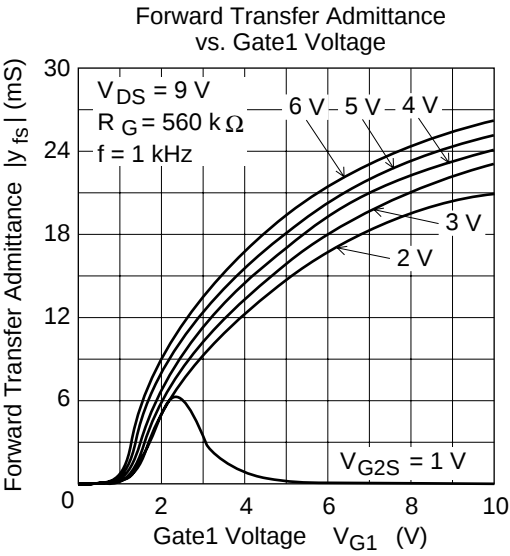
Drain Current vs.
Gate2 to Source Voltage

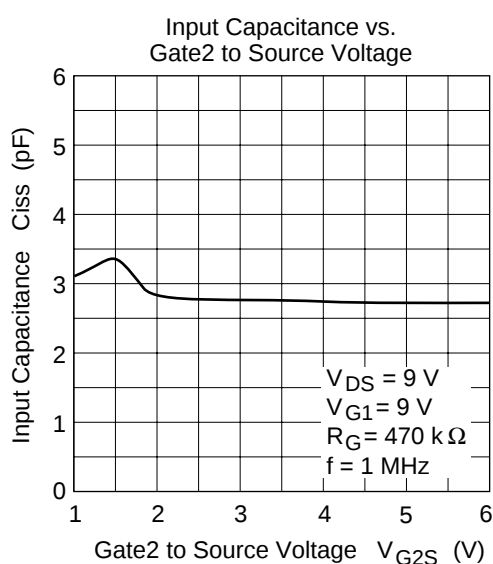
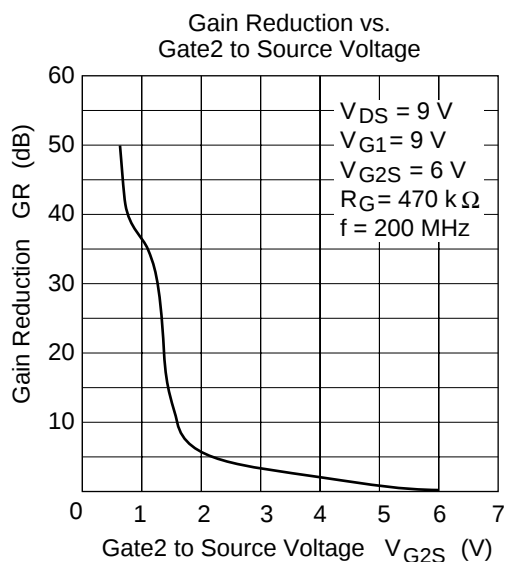
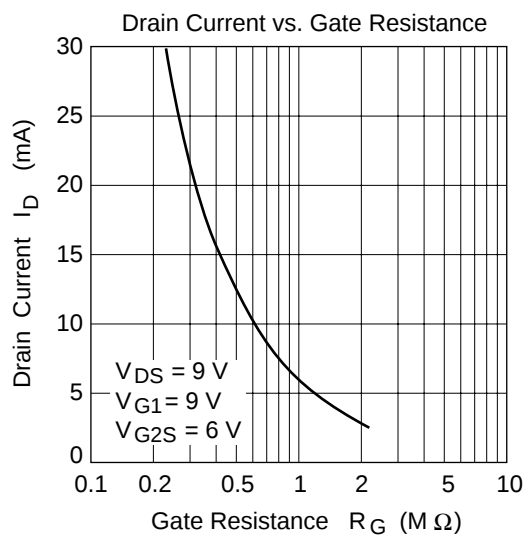
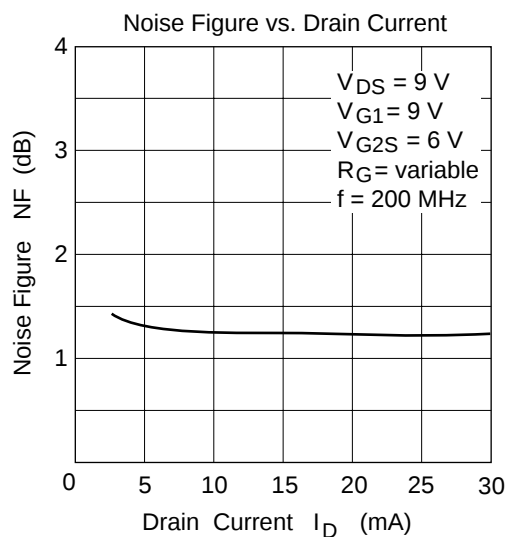


Drain Current vs. Gate1 Voltage

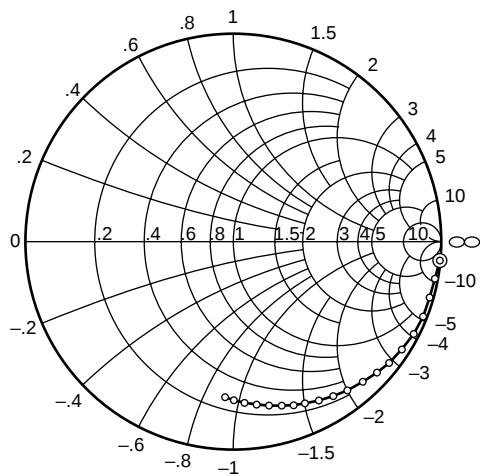






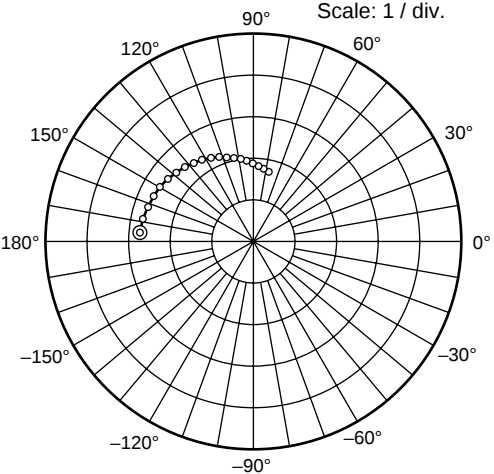


S11 Parameter vs. Frequency



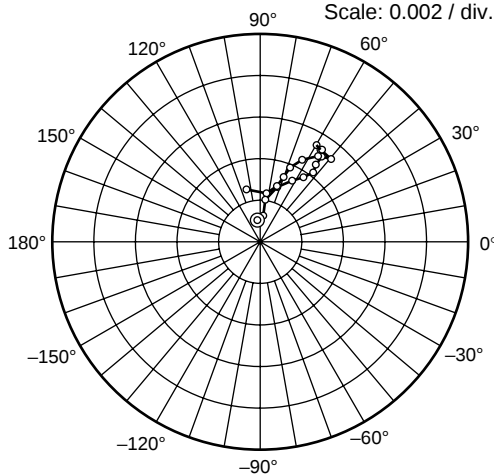
Test Condition : $V_{DS} = 9\text{ V}$, $V_{G1} = 9\text{ V}$
 $V_{G2S} = 6\text{ V}$, $R_G = 470\text{ k}\Omega$
50—1000 MHz (50 MHz step)

S21 Parameter vs. Frequency



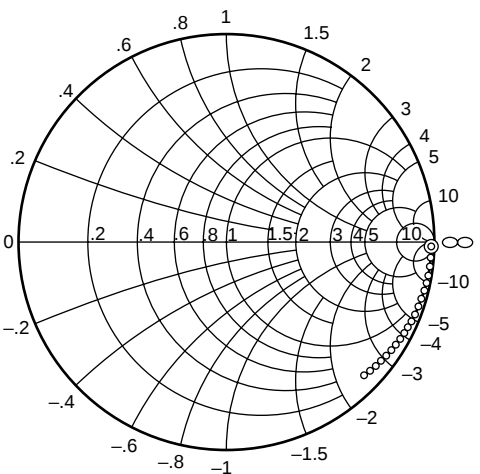
Test Condition : $V_{DS} = 9\text{ V}$, $V_{G1} = 9\text{ V}$
 $V_{G2S} = 6\text{ V}$, $R_G = 470\text{ k}\Omega$
50—1000 MHz (50 MHz step)

S12 Parameter vs. Frequency



Test Condition : $V_{DS} = 9\text{ V}$, $V_{G1} = 9\text{ V}$
 $V_{G2S} = 6\text{ V}$, $R_G = 470\text{ k}\Omega$
50—1000 MHz (50 MHz step)

S22 Parameter vs. Frequency



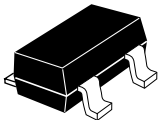
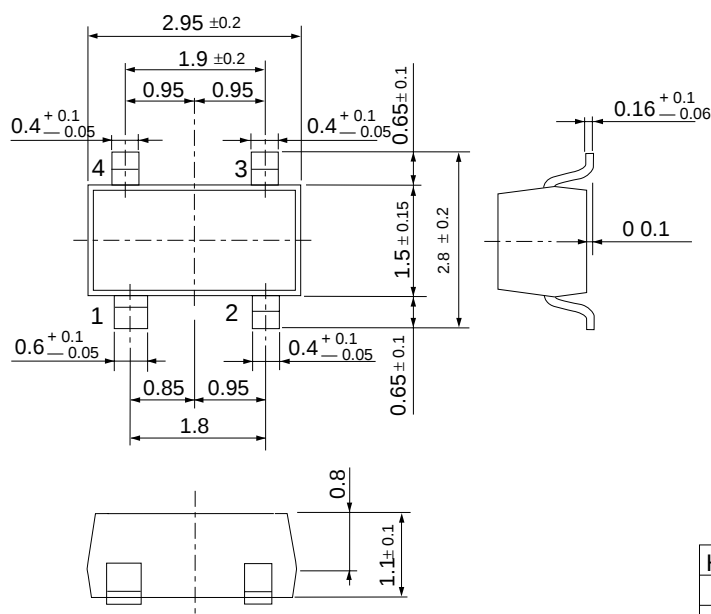
Test Condition : $V_{DS} = 9\text{ V}$, $V_{G1} = 9\text{ V}$
 $V_{G2S} = 6\text{ V}$, $R_G = 470\text{ k}\Omega$
50—1000 MHz (50 MHz step)

Sparameter ($V_{DS} = V_{G1} = 9V$, $V_{G2S} = 6V$, $R_G = 470k\Omega$, $Z_0 = 50\Omega$)

f (MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.996	-5.3	2.74	174.0	0.00096	98.6	0.985	-1.9
100	0.993	-10.9	2.73	168.0	0.00130	84.4	0.991	-4.5
150	0.987	-16.6	2.68	162.3	0.00203	83.6	0.990	-6.5
200	0.978	-21.9	2.66	156.3	0.00285	72.3	0.988	-9.4
250	0.972	-27.4	2.63	150.4	0.00335	69.7	0.985	-11.6
300	0.954	-33.2	2.57	144.3	0.00385	68.3	0.982	-14.0
350	0.943	-38.2	2.50	138.7	0.00455	63.2	0.979	-16.2
400	0.925	-43.2	2.43	133.3	0.00488	55.4	0.975	-18.4
450	0.910	-48.0	2.37	128.0	0.00526	59.8	0.971	-21.0
500	0.893	-52.5	2.30	122.6	0.00522	56.1	0.967	-23.0
550	0.880	-57.4	2.24	117.5	0.00498	53.2	0.962	-25.2
600	0.861	-62.1	2.17	112.7	0.00512	49.1	0.957	-27.3
650	0.847	-66.1	2.10	108.1	0.00497	53.4	0.952	-29.4
700	0.829	-69.9	2.02	103.6	0.00455	53.6	0.947	-31.6
750	0.816	-74.1	1.96	99.1	0.00418	51.6	0.943	-33.7
800	0.804	-78.2	1.91	94.8	0.00372	55.7	0.937	-35.8
850	0.791	-82.4	1.85	80.4	0.00329	62.4	0.933	-38.0
900	0.779	-86.1	1.79	86.3	0.00275	73.0	0.928	-40.0
950	0.764	-89.5	1.73	82.2	0.00233	82.4	0.921	-42.1
1000	0.753	-92.4	1.68	78.3	0.00258	105.1	0.918	-44.2

Package Dimensions

Unit: mm



Hitachi Code	MPAK—4R
EIAJ	
JEDEC	

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