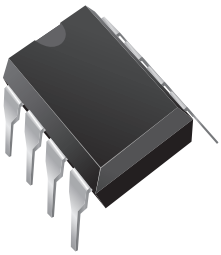
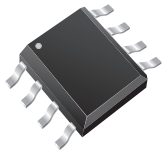
Switched-Capacitor Voltage Converter



8 Pin Dip



SO-8

Features

- Low output impedance (typical 35Ω at V_{IN} = 5V)
- Low quiescent current (typical 36µA at V_{IN} = 5V)
- High power conversion efficiency (typical 98%)
- Simple and accurate voltage conversion from positive to negative polarities
- Improved latch-up protection
- No external diodes required

Applications

- – 5V supply from + 5V logic supply
- EIA/TIA – 232E and EIA/TIA – 562 power supplies
- Portable telephones
- Data acquisition systems
- Personal communications equipment
- Panel meters
- Handheld instruments

Description

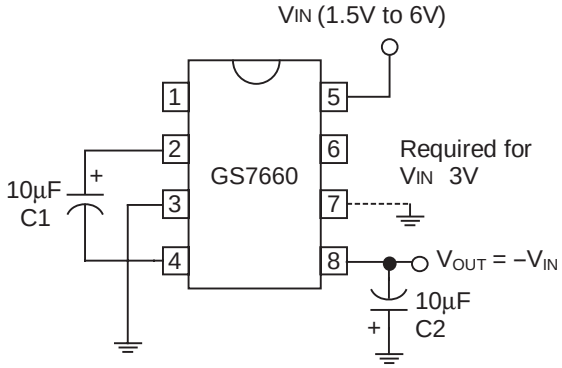
The GS7660 is a monolithic CMOS switched capacitor voltage converter, designed to be an improved direct replacement of the popular ICL7660, MAX1044 and LTC1044. They perform supply voltage conversions from positive to negative for an input voltage range of +1.5V to +6.0V to their negative complements of –1.5V to –6.0V. The input voltage can also be doubled (V_{OUT} = 2V_{IN}), halved (V_{OUT} = V_{IN}/2), or multiplied (V_{OUT} = ± n.V_{IN}).

Contained on the chip are a series Power Supply regulator, Oscillator, control Circuitry and four Power MOS Switches. The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz, with an Input voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the “Osc” terminal or overdriven by an external frequency source.

An Oscillator “boost” function is available to increase the oscillator frequency which will optimize performance of certain parameters. The Lv input can be connected to ground to improve low voltage operation (V_{IN} ≤ 3V), or left open for input voltages greater than 3V to reduce power dissipation.

The GS7660 provides superior performance over earlier designs by combining low output impedance and low quiescent current with high efficiency and by eliminating diode voltage drop losses. The only external components required are two low cost electrolytic capacitors.

Typical Application Circuit



Negative Voltage Converter

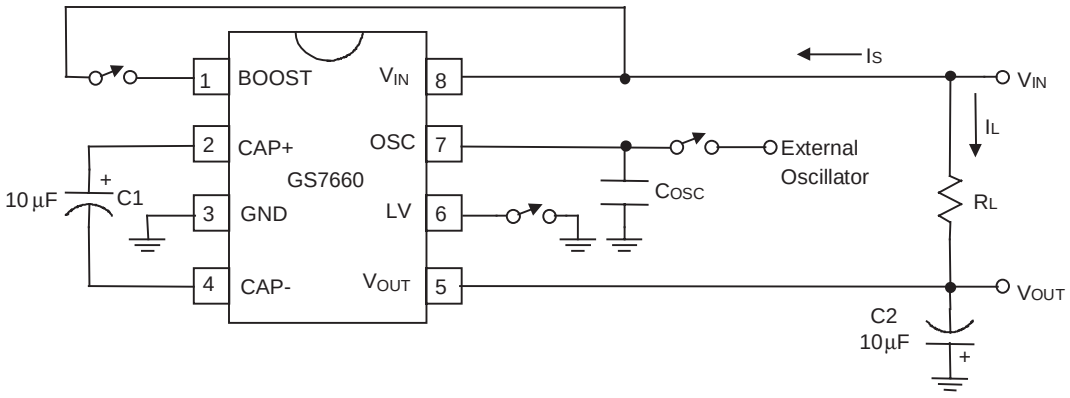
Ordering Information

Order Number	Pin Configuration
GS7660IS (Plastic SO-8)	Top View Boost 1 — 8 V_{IN} Cap+ 2 — 7 OSC GND 3 — 6 LV Cap– 4 — 5 V_{OUT}
GS7660IP (8-Pin Plastic Dip)	Top View Boost 1 — 8 V_{IN} Cap+ 2 — 7 OSC GND 3 — 6 LV Cap– 4 — 5 V_{OUT}

GS7660x x

- Package Outline
  - P: Plastic Dip
  - S: SO-8
- Operating Junction Temperature Range
  - I: –40°C to +125°C

Test Circuit



Maximum Ratings

Ratings at 25°C ambient temperature unless otherwise specified.

Parameter	Symbol	Value	Unit
Supply Voltage (V_{IN} to GND)	V_{IN}	6.0	V
Input Voltage (Pin 1, 6 and 7)	V_{IN}	$-0.3V \le V_{IN} \le (V_{IN}, +0.3V)$	V
L_V Input Current	L_V1	20	µA
Output Short Circuit Duration		Continuous	
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_S	–65 to +150	°C
Continuous Power Dissipation Plastic Dip (Derate 7.9mW/°C above 70°C) SO-8 (Derate 6mW/°C above 70°C)	P_D	 630 480	mW

Note: (1) Stresses beyond those listed above may cause permanent damage to the device. Operating at the levels stated above may affect device reliablity.

Electrical Characteristics

V_{IN} = 5.0V LVPin = open, Oscillator free running, I load = 0mA, T_A = –40°C to +125°C unless otherwise noted.

Parameter	Conditions		Min	Typ	Max	Unit
Supply Current	L_V = Open	T_A = 25°C	–	36	70	µA
			–	–	100	
	Pin 1,7, V_{IN} = 3V		–	20	–	
Supply Voltage(1)	R_L = 10KΩ, L_V Open R_L = 10KΩ, L_V Gnd		3.0 1.5	– –	6.0 6.0	V
Output Resistance	I_L = 20mA, F_{OSC} = 10kHz L_V = Open	T_A = 25°C	–	35	70	Ω
			–	–	110	
	I_L = 3mA, F_{OSC} = 1kHz V_{IN} = 2V, L_V to Gnd	T_A = 25°C	–	–	250	
			–	–	370	
Oscillator Frequency	C_{OSC} = 0pF, L_V to Gnd Pin 1 Open	V_{IN} = 5.0V	–	5.0	–	kHz
		V_{IN} = 2.0V	2.0	–	–	
Power Efficiency	R_L = 5K, F_{OSC} =10kHz, L_V = Open		96	98	–	%
Voltage Conversion Efficiency	L_V = Open	T_A = 25°C	98	99.9	–	%
Oscillator Sink or Source Current	V_{OSC} = 0V or V_{IN} L_V = Open	Pin 1 = 0V	–	–	3.0	µA
		Pin 1 = V_{IN}	–	–	20	
Oscillator Impedance	T_A = 25°C	V_{IN} = 2.0V	–	1.0	–	mΩ
		V_{IN} = 5.0V	–	100	–	kΩ

Note: (1) The GS7660 can operate with or without an external output diode over the full temperature and voltage range. Eliminating the diode reduces voltage drop losses.

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 1 – Supply Current vs. Supply Voltage

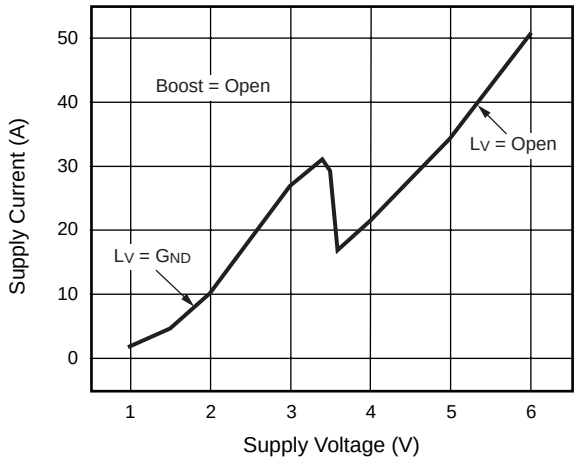


Fig. 2 – Power Efficiency vs. Load Current (V_{IN} = 5V)

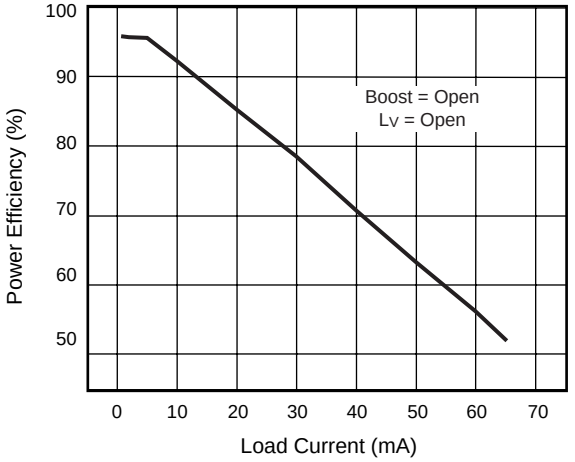


Fig. 3 – Output Voltage vs. Load Current (V_{IN} = 5V)

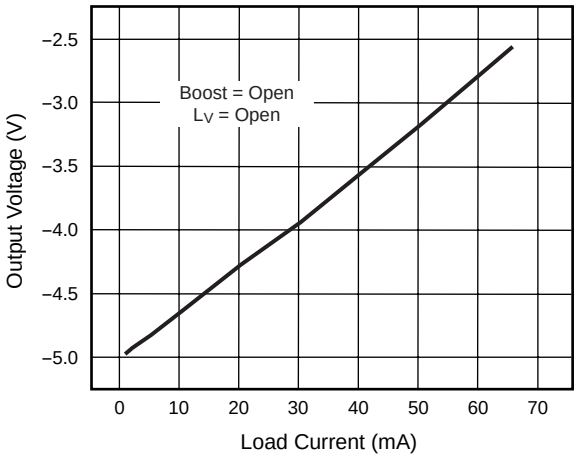


Fig. 4 – Output Voltage vs. Load Current (V_{IN} = 2V)

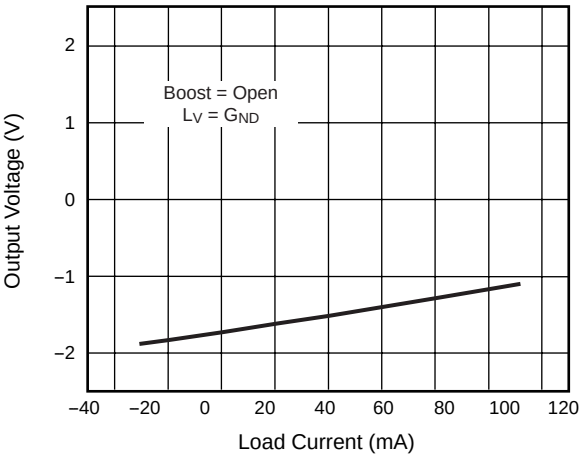


Fig. 5 – Oscillator Frequency vs. Supply Voltage

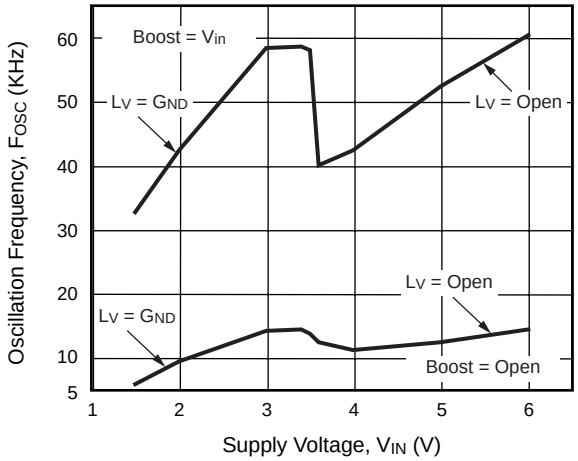
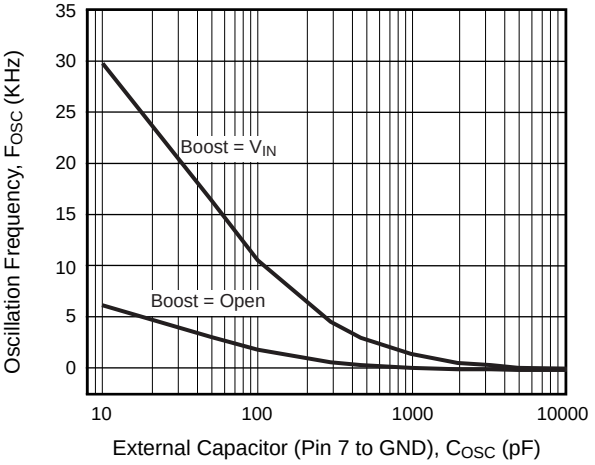


Fig. 6 – Oscillator Frequency vs. Value of C_{OSC}



Pin Description

Pin	Name	Function
1	BOOST	Frequency Boost. Connecting BOOST to V_{IN} increases the oscillator frequency by a factor of five. When the oscillator is driven externally, BOOST has no effect and should be left open.
	N.C.	No Connection
2	CAP+	Connection to positive terminal of Charge-Pump Capacitor
3	GND	Ground. For most applications, the positive terminal of the reservoir capacitor is connected to this pin.
4	CAP–	Connection to negative terminal of Charge-Pump Capacitor
5	V_{OUT}	Negative Voltage Output. For most applications, the negative terminal of the reservoir capacitor is connected to this pin.
6	LV	Low-Voltage Operation. Connect to ground for supply voltages below 3.5V.
7	OSC	Oscillator Control Input. Connecting an external capacitor reduces the oscillator frequency.
8	V_{IN}	Power Supply Positive Voltage Input. (1.5V to 6V). V_{IN} is also the substrate connection.

Detailed Description

The GS7660 is a charge-pump voltage converter. The basic operations is as follows: Switch pairs S1, S2 and S3, S4 (Fig.7) are alternately closed and opened at the rate of the oscillator frequency divided by two.

During the first half of the cycle, when S1 and S2 are closed and S3 and S4 are open, bucket capacitor C1 is charged by input voltage. During the second half of the cycle, when the switches assume the opposite state, capacitor C1 is connected in parallel with output capacitor C2 and any voltage differential causes a transfer of charge from C1 to C2. This process will continue until the voltage across C2 equals the $–V_{IN}$ voltage.

In normal operation, the output voltage will be less than $–V_{IN}$, since the switches have internal resistance and C2 is being discharged by the load.

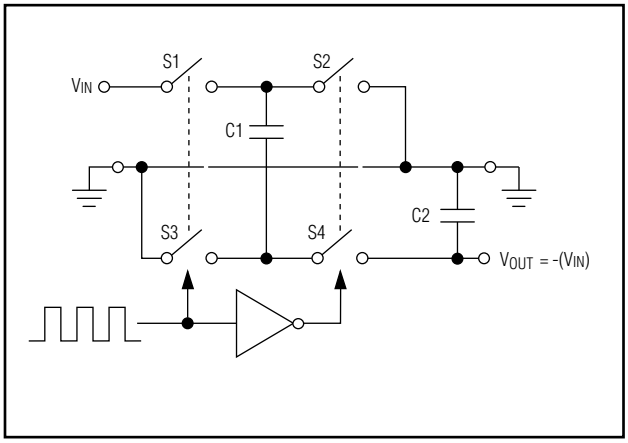


Fig. 7 – Ideal Voltage Inverter

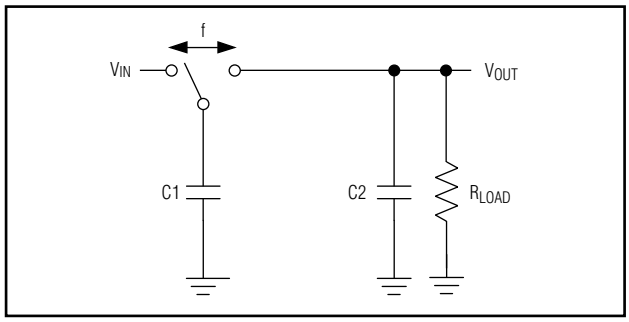


Fig. 8 – Switched Capacitor Model

To better understand the theory of operation, a review of the basic switched capacitor building block is helpful (see Fig. 8). Referring to Fig. 8 and looking at one full cycle of operation, the charge being drained by the load is Qavg or IL x T (T being the time period of one full cycle).

All the charge (Δq) flowing into the output is being delivered by the input to C1 during only half the cycle. Under steady-state condition, C1 will charge to the level of the input voltage (V_{IN}) and discharge to the peak level of the output voltage (V_{OUT}). Therefor the voltage change on C1 is $V_{IN} – V_{OUT}$.

$$Q_{avg} = \Delta q = C1(V_{in} - V_{out})$$

$$I_L \times T = C1(V_{in} - V_{out}) \text{ or } I_L = f \times C1(V_{in} - V_{out}) \quad f = 1/T$$

$$I_L = \frac{(V_{in} - V_{out})}{\frac{1}{f \times C1}} \text{ and } R_{EQUIV} = \frac{1}{f \times C1} \text{ (See fig. 9)}$$

Where f is one-half the oscillator frequency. This resistance is a major component of the output resistance of switched capacitor circuits.

With C1 = C2 = 10µF and Fosc = 10kHz, this resistance represents 20Ω.

Under the same conditions, the typical value in the “Electrical Characteristics” section of the GS7660 is 35Ω.

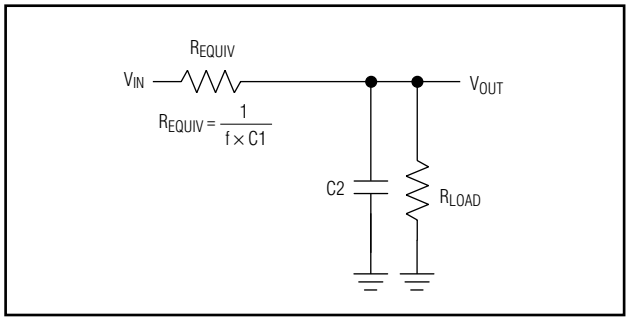


Fig. 9 – Equivalent Impedance

Design Information

Low Voltage (L_V) Pin

Fig. 10 (below) shows a simplified circuit diagram of the GS7660.

It shows a voltage regulator between the V_{IN} and Gnd, in series with the Oscillator.

Grounding the LV pin removes the regulator from this series path and improves low voltage performance down to 1.5V. For supply voltages less than 3.0V, the LV pin should be connected to ground and left open for voltages above 3.0V.

The LV pin can be left grounded over the total range of Input Voltages. This will improve low voltage operation and increase oscillator frequency. The disadvantage is increased quiescent current and reduced efficiency at higher voltages.

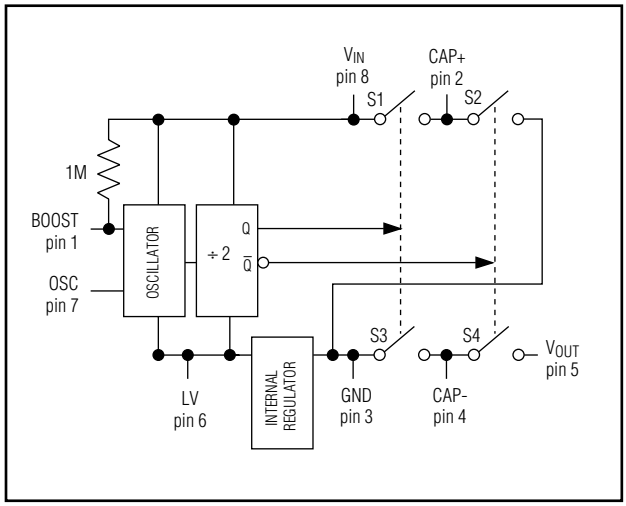


Fig. 10 – Functional Diagram

Oscillator Frequency Control

For normal operation, the Boost, and Oscillator Pins should be left open. Connecting the Boost pin to the V_{IN} supply will increase oscillator frequency by a factor of 5, resulting in lower Output Impedance, less ripple, smaller required capacitor values and moves the switching noise out of the audio band. Lower oscillator frequency reduces quiescent current.

The oscillator frequency can be further controlled by driving the oscillator input from an external frequency source or lowered , by connecting an external capacitor to the oscillator input.

Efficiency, Output Impedance and Output Ripple

The power efficiency of a switched capacitor voltage converter is dependent on the internal losses.
The total power loss is:

$$\sum P\ loss = \frac{P\ outp.}{Res.} + \frac{P\ switch}{Res.} + \frac{P\ cap.}{Res.} + P\ conversion$$

$$\frac{P\ outp.}{Res.} = \frac{I_L^2}{f.C1} \qquad f = f\ osc/2$$

$$\frac{P\ switch}{Res.} + \frac{P\ cap.}{Res.} = I_L^2 \left(8\ R_{SW} + 4\ Esr_{C1} + Esr_{C2}\right)$$

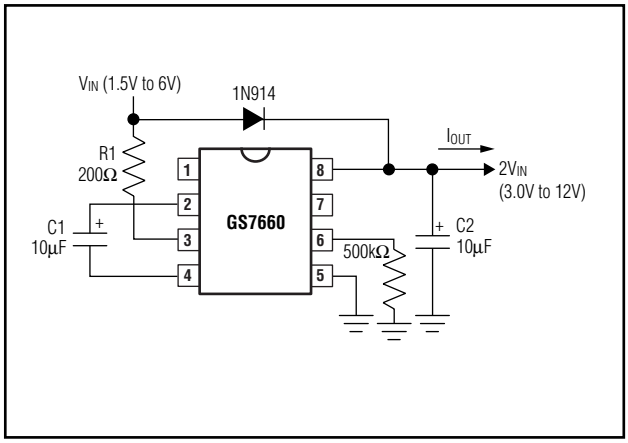
$$P\ conversion =$$

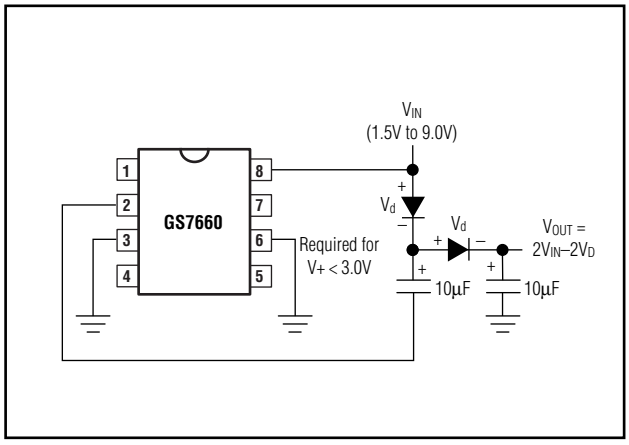
$$f\left[\frac{1}{2} C1\left(V_{in}^2 - V_{out}^2\right) + \frac{1}{2} C2\left(V\ ripple^2 - 2\ Vout.\ V\ ripple\right)\right]$$

$$f = f\ osc/2$$

Vripple

$$V\ ripple = I_L \left(\frac{1}{2.\ C2\ .f} + 2\ Esr_{C2}\right) \qquad f = f\ osc/2$$





Figs. 11a and 11b – Voltage Doubler

Voltage Doubling

Figure 11 shows two methods of voltage doubling. In Fig. 11a , R1 is added to ensure that doubling is not inhibited by a non-destructive latch-up at start-up. This condition can occur, since the ground pin (pin 3) is raised above the V_{IN} pin (pin 8) during start-up.

R1 increases output impedance and in higher current applications where the voltage drop across R1 exceeds a two diode drop, the doubling circuit of Fig 11b is recommended.

The voltage doubler of Fig. 11a is more accurate at low load currents since the voltage drop across the diode is not reflected at the output.

Ultra Precision Voltage Divider

An ultra precision voltage divider is shown below in Fig. 12. To achieve the 0.002% accuracy, the load current has to be kept below 100nA. However with a slight loss in accuracy, the load current can be increased.

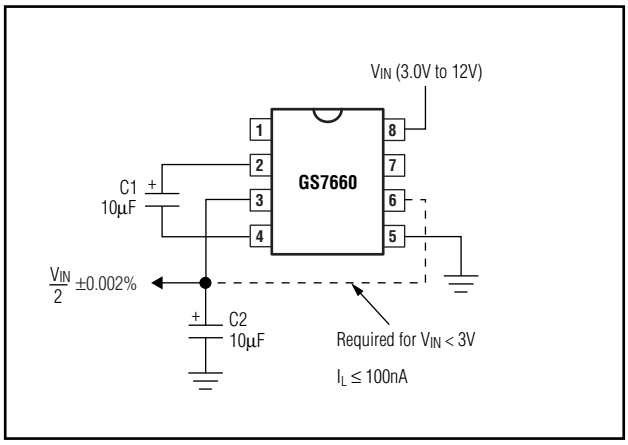


Fig. 12 – Ultra Precision Voltage Divider

Battery Splitter

Fig. 13 shows a simple solution to obtain complementary + and – supplies from a single power supply. The output voltages are + and – half the supply voltage. Good accuracy requires low load currents.

A disadvantage is the requirement of a floating input supply, which in the case of a battery is not an issue.

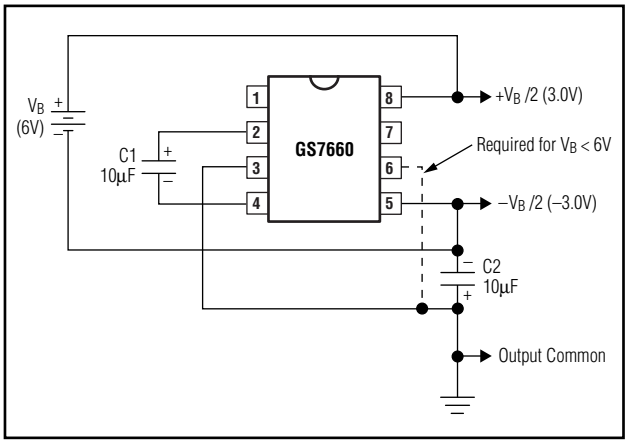


Fig. 13 – Battery Splitter

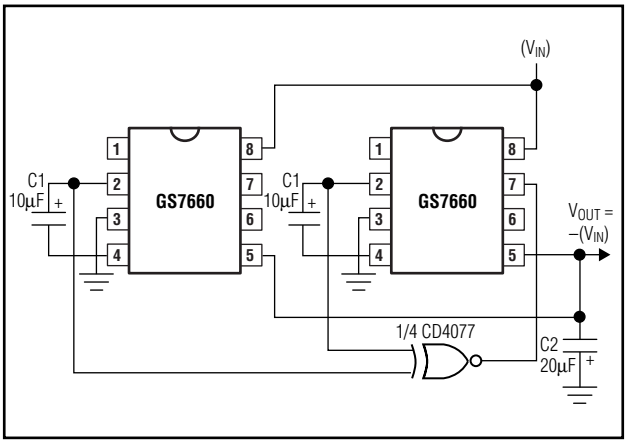
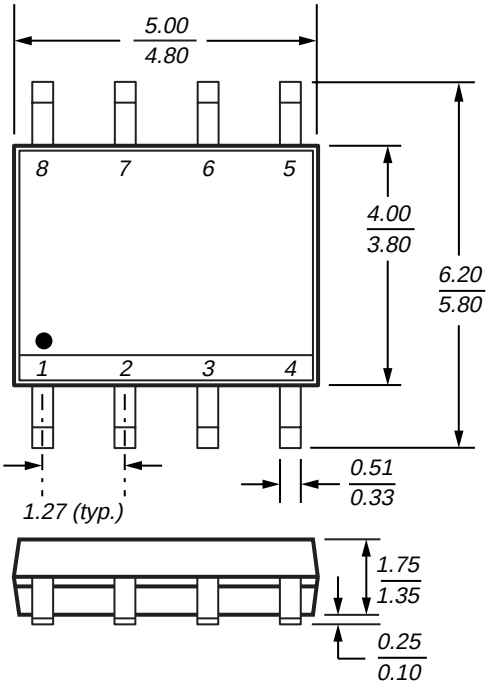


Fig. 14 – Paralleling for Lower Output Resistance

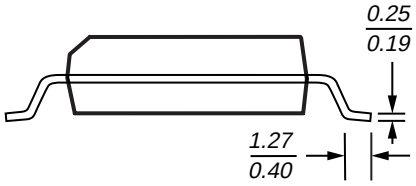
Paralleling For Lower Output Impedance

Fig. 14 above shows two GS7660s connected in parallel to achieve a lower output resistance. If the output resistance is dominated by 1/ f C1, which is normally the case with the GS7660, increasing C1 offers a greater advantage than the paralleling of circuits.

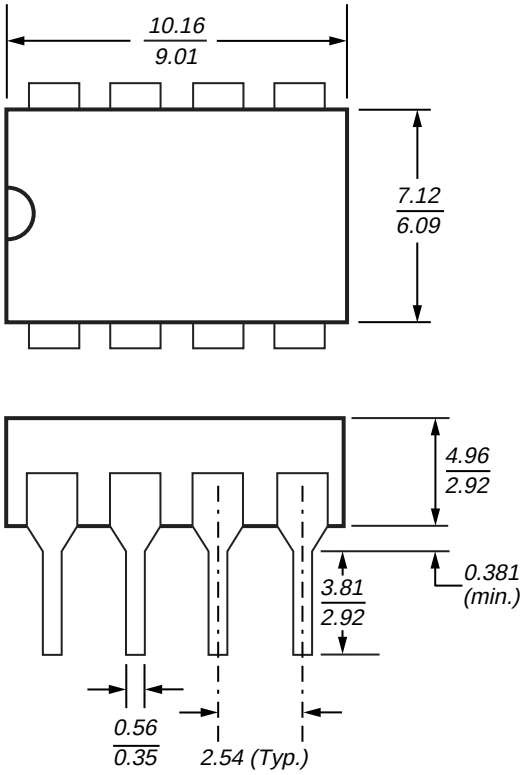
SO-8 Case Outline



Dimensions in millimeters



8-Pin Dip Case Outline



Dimensions in millimeters