

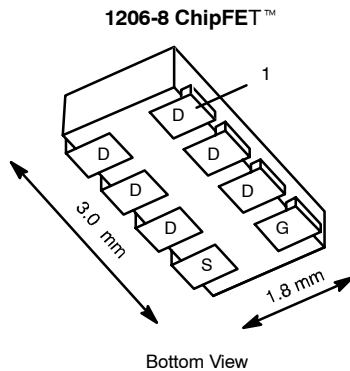


P-Channel 2.5-V (G-S) MOSFET

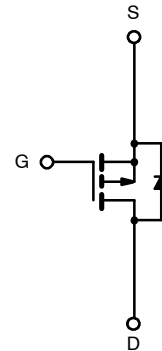
PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.065 @ $V_{GS} = -4.5$ V	± 4.9
	0.074 @ $V_{GS} = -3.6$ V	± 4.6
	0.110 @ $V_{GS} = -2.5$ V	± 3.8

TrenchFET®
Power MOSFETs
2.5-V Rated



Marking Code
BB XX
Lot Traceability
and Date Code
Part # Code



P-Channel MOSFET

Ordering Information: Si5443DC-T1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	-20		V
Gate-Source Voltage		V _{GS}	± 12		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	± 4.9	± 3.6	A
	T _A = 85°C		± 3.5	± 2.6	
Pulsed Drain Current		I _{DM}	± 15		
Continuous Source Current ^a		I _{AS}	-2.1	-1.1	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.5	1.3	W
	T _A = 85°C		1.3	0.7	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{thJA}	40	50	$^\circ\text{C/W}$
	Steady State		80	95	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	15	20	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

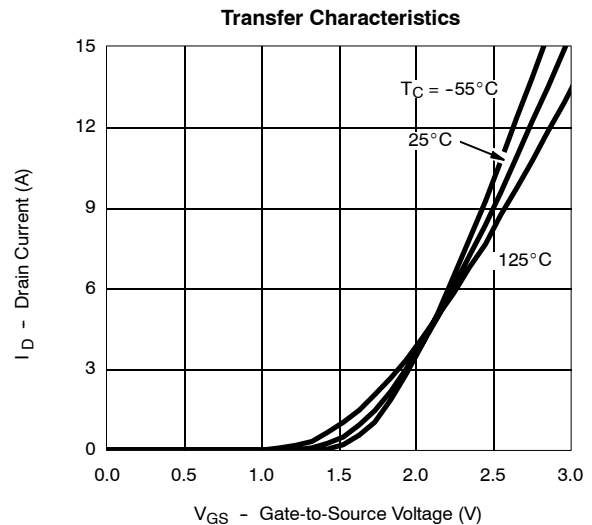
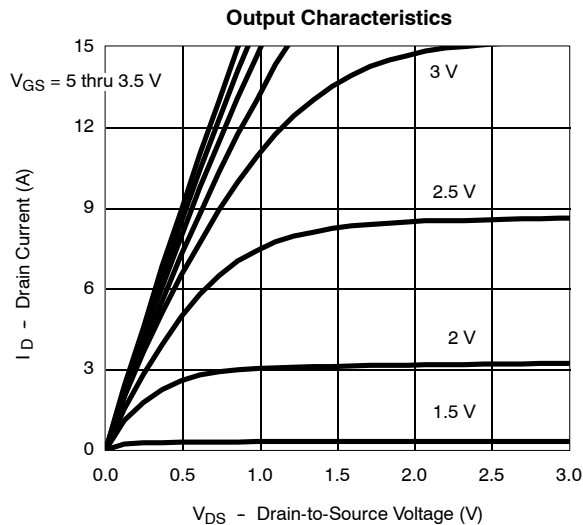
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -16\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 85^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}$, $V_{GS} = -4.5\ \text{V}$	-15			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}$, $I_D = -3.6\ \text{A}$		0.056	0.065	Ω
		$V_{GS} = -3.6\ \text{V}$, $I_D = -3.3\ \text{A}$		0.065	0.074	
		$V_{GS} = -2.5\ \text{V}$, $I_D = -2.7\ \text{A}$		0.095	0.110	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\ \text{V}$, $I_D = -3.6\ \text{A}$		10		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.1\ \text{A}$, $V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}$, $V_{GS} = -4.5\ \text{V}$, $I_D = -3.6\ \text{A}$		9	14	nC
Gate-Source Charge	Q_{gs}			2.2		
Gate-Drain Charge	Q_{gd}			2.2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}$, $V_{GEN} = -4.5\ \text{V}$, $R_G = 6\ \Omega$		15	25	μs
Rise Time	t_r			30	45	
Turn-Off Delay Time	$t_{d(off)}$			50	75	
Fall Time	t_f			35	50	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.1\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		30	60	ns

Notes

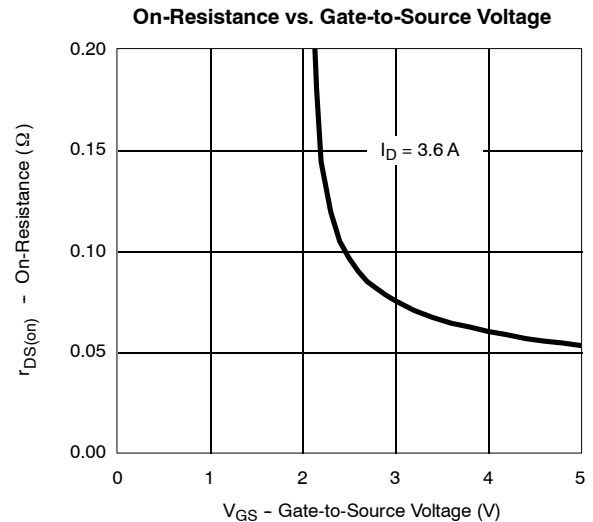
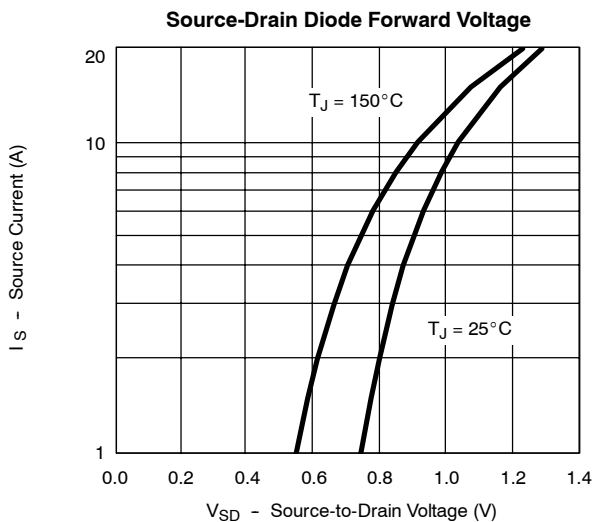
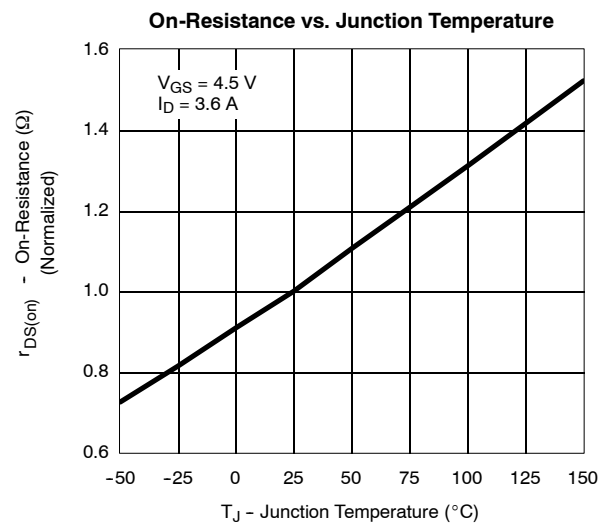
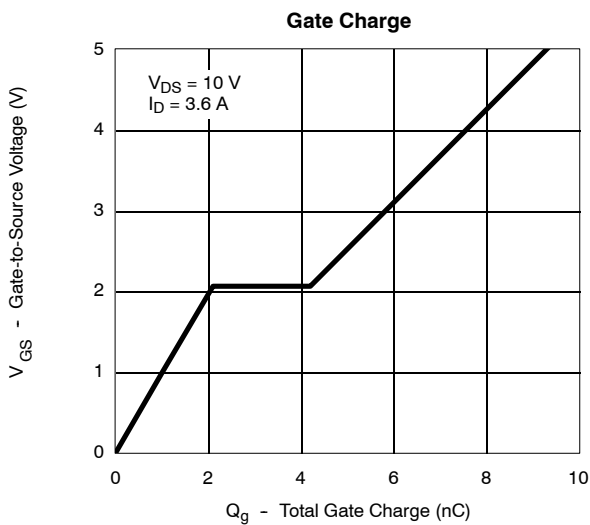
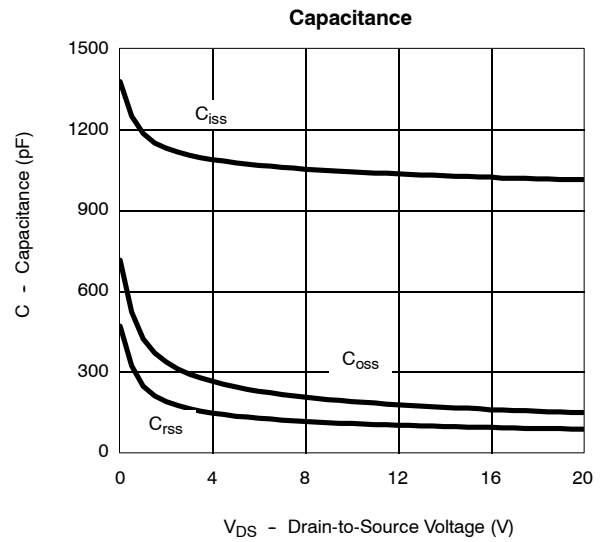
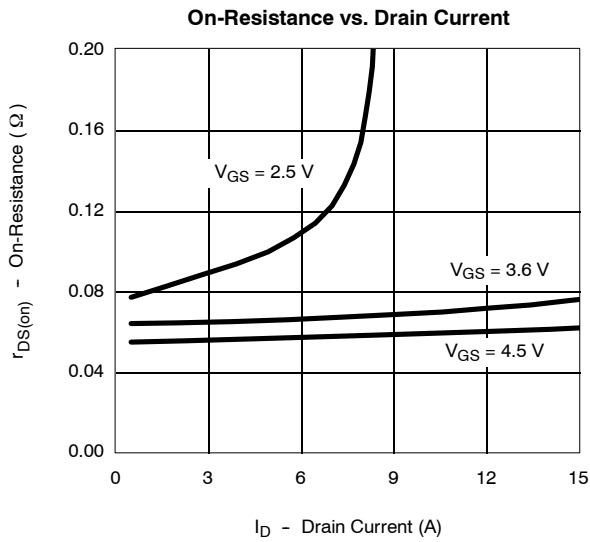
a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)
