Burr-Brown Products
from Texas Instruments

PCM2901
PCM2903

SLES034B − MARCH 2002 − REVISED JUNE 2004

STEREO AUDIO CODEC WITH USB INTERFACE, SINGLE-ENDED ANALOG INPUT/OUTPUT AND S/PDIF

FEATURES

- **PCM2901: Without S/PDIF**
- **PCM2903: With S/PDIF**
- **On-Chip USB Interface:**
  - **With Full-Speed Transceivers**
  - **Fully Compliant With USB 1.1 Specification**
  - **Certified by USB-IF**
  - **Partially Programmable Descriptors(1)**
  - **USB Adaptive Mode for Playback**
  - **USB Asynchronous Mode for Record**
  - **Self-Powered**
- **16-Bit Delta Sigma ADC and DAC**
- **Sampling Rate:**
  - **DAC: 32, 44.1, 48 kHz**
  - **ADC: 8, 11.025, 16, 22.05, 32, 44.1, 48 kHz**
- **On-Chip Clock Generator:**
  - **With Single 12-MHz Clock Source**
- **Single Power Supply: 3.3 V TYP**
- **Stereo ADC**
  - **Analog Performance at $V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = V_{DD} = 3.3$ V**
    - **THD+N = 0.01%**
    - **SNR = 89 dB**
    - **Dynamic Range = 89 dB**
  - **Decimation Digital Filter**
    - **Pass-Band Ripple = ±0.05 dB**
    - **Stop-Band Attenuation = –65 dB**
  - **Single-Ended Voltage Input**
  - **Antialiasing Filter Included**
  - **Digital LCF Included**
- **Stereo DAC**
  - **Analog Performance at $V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = V_{DD} = 3.3$ V**
    - **THD+N = 0.005%**
    - **SNR = 96 dB**
    - **Dynamic Range = 93 dB**
  - **Oversampling Digital Filter**
    - **Pass-Band Ripple = ±0.1 dB**
    - **Stop-Band Attenuation = –43 dB**
  - **Single-Ended Voltage Output**
  - **Analog LPF Included**
- **Multifunctions:**
  - **Human Interface Device (HID) Volume ± Control and Mute Control**
  - **Suspend Flag**
- **Package: 28-Pin SSOP**

APPLICATIONS

- **USB Audio Speaker**
- **USB Headset**
- **USB Monitor**
- **USB Audio Interface Box**

DESCRIPTION

The PCM2901/2903 is TI's single-chip USB stereo audio codec with USB-compliant full-speed protocol controller and S/PDIF (only PCM2903). The USB protocol controller works with no software code, but the USB descriptors can be modified in some areas (for example, vendor ID/product ID). The PCM2901/2903 employs SpAct™ architecture, TI's unique system that recovers the audio clock from USB packet data. On-chip analog PLLs with SpAct enable playback and record with low clock jitter and with independent playback and record sampling rates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

---

(1)The descriptor can be modified by changing a mask.

SpAct is a trademark of Texas Instruments, Incorporated.
Other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS
www.ti.com

Copyright © 2004, Texas Instruments Incorporated

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING ORDERING INFORMATION

PCM2901						
PRODUCT	**PACKAGE−LEAD**	**PACKAGE DESIGNATOR**	**SPECIFIED TEMPERATURE RANGE**	**PACKAGE MARKING**	**ORDERING NUMBER(1)**	**TRANSPORT MEDIA**
PCM2901E	SSOP-28	28DB	−25°C to 85°C	PCM2901E	PCM2901E	Rails
					PCM2901E/2K	Tape and reel

(1) Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of PCM2901E/2K gets a single 2000-piece tape and reel.

PCM2903						
PRODUCT	**PACKAGE−LEAD**	**PACKAGE DESIGNATOR**	**SPECIFIED TEMPERATURE RANGE**	**PACKAGE MARKING**	**ORDERING NUMBER(2)**	**TRANSPORT MEDIA**
PCM2903E	SSOP-28	28DB	−25°C to 85°C	PCM2903E	PCM2903E	Rails
					PCM2903E/2K	Tape and reel

(2) Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of PCM2903E/2K gets a single 2000-piece tape and reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		PCM2901/PCM2903	**UNIT**
Supply voltage, V_{CCC}, V_{CCP1}, V_{CCP2}, V_{CCX}, V_{DD}		–0.3 to 4	V
Supply voltage differences, V_{CCC}, V_{CCP1}, V_{CCP2}, V_{CCX}, V_{DD}		±0.1	V
Ground voltage differences, AGNDC, AGNDP, AGNDX, DGND, DGNDU		±0.1	V
Digital input voltage	SEL0, SEL1, TEST0 (DIN)(2)	−0.3 to 6.5	V
	D+, D–, HID0, HID1, HID2, XTI, XTO, TEST1 (DOUT)(2), $\overline{SSPND}$	−0.3 to (V_{DD} + 0.3) < 4	V
Analog input voltage	$V_{IN}L$, $V_{IN}R$, V_{COM}, $V_{OUT}R$, $V_{OUT}L$	−0.3 to (V_{CCC} + 0.3) < 4	V
Input current (any pins except supplies)		±10	mA
Ambient temperature under bias		−40 to 125	°C
Storage temperature, T_{stg}		−55 to 150	°C
Junction temperature T_J		150	°C
Lead temperature (soldering)		260	°C, 5 s
Package temperature (IR reflow, peak)		250	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) ( ): PCM2903

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, $V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = V_{DD}$ = 3.3 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

PARAMETER			TEST CONDITIONS	PCM2901E, PCM2903E			UNIT
				MIN	TYP	MAX	UNIT
Digital Input/Output							
	Host interface		Apply USB Revision 1.1, full speed				
	Audio data format		USB isochronous data format				
Input Logic							
V_{IH}	High-level input voltage	D+, D−		2		V_{DD}	VDC
		XTI, HID0, HID1, and HID2		$0.7V_{DD}$		V_{DD}	
		SEL0, SEL1		2		5.25	
		DIN, PCM2903		$0.7V_{DD}$		5.25	
V_{IL}	Low-level input voltage	D+, D−		V_{DD}		0.8	VDC
		XTI, HID0, HID1, and HID2				$0.3V_{DD}$	
		SEL0, SEL1				0.8	
		DIN, PCM2903				$0.3V_{DD}$	
I_{IH}	High-level input current	D+, D−, XTI, SEL0, SEL1	V_{IN} = 3.3 V			±10	μA
		HID0, HID1, and HID2	V_{IN} = 3.3 V		50	80	
		DIN, PCM2903	V_{IN} = 3.3 V		65	100	
I_{IL}	Low-level input current	D+, D−, XTI, SEL0, SEL1	V_{IN} = 0 V			±10	μA
		HID0, HID1, and HID2	V_{IN} = 0 V			±10	
		DIN, PCM2903	V_{IN} = 0 V			±10	
Output Logic							
V_{OH}	High-level output voltage	D+, D−		2.8			VDC
		DOUT, PCM2903	I_{OH} = –4 mA	2.8			
		$\overline{\text{SSPND}}$	I_{OH} = –2 mA	2.8			
V_{OL}	Low-level output voltage	D+, D−				0.3	VDC
		DOUT, PCM2903	I_{OL} = 4 mA			0.5	
		$\overline{\text{SSPND}}$	I_{OL} = 2 mA			0.5	
Clock Frequency							
	Input clock frequency, XTI			11.994	12	12.006	MHz
ADC Characteristics							
	Resolution				8, 16		bits
	Audio data channel				1, 2		channel

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, $V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = V_{DD}$ = 3.3 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	PCM2901E, PCM2903E			UNIT
			MIN	TYP	MAX	UNIT
Clock Frequency						
f_S	Sampling frequency		8, 11.025, 16, 22.05, 32, 44.1, 48			kHz
DC Accuracy						
	Gain mismatch channel-to-channel			±1	±5	% of FSR
	Gain error			±2	±10	% of FSR
	Bipolar zero error			±0		% of FSR
Dynamic Performance(1)						
THD+N	Total harmonic distortion plus noise	V_{IN} = –0.5 dB		0.01%	0.02%	
		V_{IN} = –60 dB		5%		
	Dynamic range	A-Weighted	81	89		dB
SNR	Signal-to-noise ratio	A-Weighted	81	89		dB
	Channel separation		80	85		dB
Analog Input						
	Input voltage			0.6 V_{CCC}		Vp−p
	Center voltage			0.5 V_{CCC}		V
	Input impedance			30		kΩ
	Antialiasing filter frequency response	–3 dB		150		kHz
		f_{IN} = 20 kHz		–0.08		dB
Digital Filter Performance						
	Pass band				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Pass-band ripple				±0.05	dB
	Stop-band attenuation		–65			dB
t_d	Delay time			17.4/f_S		s
	LCF frequency response	–3 dB		0.078 f_S		MHz
DAC Characteristics						
	Resolution			8, 16		bits
	Audio data channel			1, 2		channel
Clock Frequency						
f_S	Sampling frequency		32, 44.1, 48			kHz

(1) f_{IN} = 1 kHz, using Audio Precision System II, RMS mode with 20-kHz LPF, 400-Hz HPF in calculation.

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, $V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = V_{DD}$ = 3.3 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

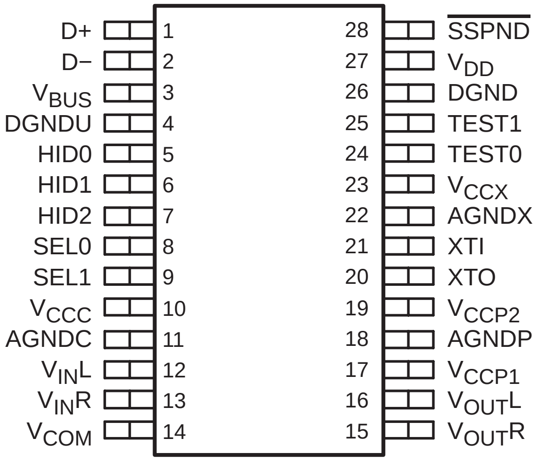
PARAMETER		TEST CONDITIONS	PCM2901E, PCM2903E			UNIT
			MIN	TYP	MAX	UNIT
DC Accuracy						
	Gain mismatch channel-to-channel			±1	±5	% of FSR
	Gain error			±2	±10	% of FSR
	Bipolar zero error			±2		% of FSR
Dynamic Performance(1)						
THD+N	Total harmonic distortion plus noise	V_{OUT} = 0 dB		0.005%	0.016%	
		V_{OUT} = –60 dB		3%		
	Dynamic range	EIAJ, A-weighted	87	93		dB
SNR	Signal-to-noise ratio	EIAJ, A-weighted	90	96		dB
	Channel separation		86	92		dB
Analog Output						
V_O	Output voltage			0.6 V_{CCC}		Vp−p
	Center voltage			0.5 V_{CCC}		V
	Load impedance	AC coupling	10			kΩ
	LPF frequency response	–3 dB		250		kHz
		f = 20 kHz		–0.03		dB
	Digital filter performance					
	Pass band				0.445 f_S	Hz
	Stop band		0.555 f_S			Hz
	Pass-band ripple				±0.1	dB
	Stop-band attenuation		–43			dB
t_d	Delay time			14.3 f_S		s
Power Supply Requirements						
	Voltage range (V_{DD}, V_{CCC}, V_{CCP1}, V_{CCP2}, V_{CCX})		3	3.3	3.6	VDC
	Supply current	ADC, DAC operation		54	70	mA
		Suspend mode(2)		210		µA
P_D	Power dissipation	ADC, DAC operation		178	252	mW
		Suspend mode(2)		0.69		mW
Temperature Range						
	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance	28-pin SSOP		100		°C/W

(1) f_{OUT} = 1 kHz, using Audio Precision System II, RMS mode with 20-kHz LPF, 400-Hz HPF.

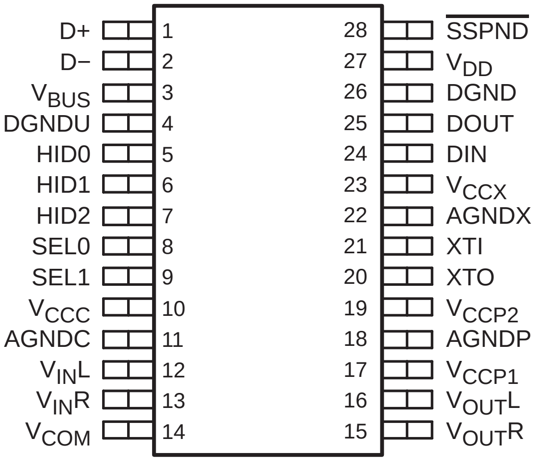
(2) Under USB suspend state

PIN ASSIGNMENTS

PCM2901
(TOP VIEW)


D+ 1
D− 2
V_{BUS} 3
DGNDU 4
HID0 5
HID1 6
HID2 7
SEL0 8
SEL1 9
V_{CCC} 10
AGNDC 11
$V_{IN}L$ 12
$V_{IN}R$ 13
V_{COM} 14
28 $\overline{\text{SSPND}}$
27 V_{DD}
26 DGND
25 TEST1
24 TEST0
23 V_{CCX}
22 AGNDX
21 XTI
20 XTO
19 V_{CCP2}
18 AGNDP
17 V_{CCP1}
16 $V_{OUT}L$
15 $V_{OUT}R$

PCM2903
(TOP VIEW)


D+ 1
D− 2
V_{BUS} 3
DGNDU 4
HID0 5
HID1 6
HID2 7
SEL0 8
SEL1 9
V_{CCC} 10
AGNDC 11
$V_{IN}L$ 12
$V_{IN}R$ 13
V_{COM} 14
28 $\overline{\text{SSPND}}$
27 V_{DD}
26 DGND
25 DOUT
24 DIN
23 V_{CCX}
22 AGNDX
21 XTI
20 XTO
19 V_{CCP2}
18 AGNDP
17 V_{CCP1}
16 $V_{OUT}L$
15 $V_{OUT}R$

PCM2901 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGNDC	11	−	Analog ground for codec
AGNDP	18	−	Analog ground for PLL
AGNDX	22	−	Analog ground for oscillator
D–	2	I/O	USB differential input/output minus(1)
D+	1	I/O	USB differential input/output plus(1)
DGND	26	−	Digital ground
DGNDU	4	−	Digital ground for USB transceiver
HID0	5	I	HID key state input (mute), active high(3)
HID1	6	I	HID key state input (volume up), active high(3)
HID2	7	I	HID key state input (volume down), active high(3)
SEL0	8	I	Must be set to high(5)
SEL1	9	I	Connected to the USB port of V_{BUS}(5)
$\overline{\text{SSPND}}$	28	O	Suspend flag, active low (Low: suspend, High: operational)
TEST0	24	I	Test pin, must be connected to GND
TEST1	25	O	Test pin, must be left open
V_{BUS}	3	−	Must be connected to V_{DD}
V_{CCC}	10	−	Analog power supply for codec(4)
V_{CCP1}	17	−	Analog power supply for PLL(4)
V_{CCP2}	19	−	Analog power supply for PLL(4)
V_{CCX}	23	−	Analog power supply for oscillator(4)
V_{COM}	14	−	Common for ADC/DAC (V_{CCC}/2) (4)
V_{DD}	27	−	Digital power supply(4)
$V_{IN}L$	12	I	ADC analog input for L-channel
$V_{IN}R$	13	I	ADC analog input for R-channel
$V_{OUT}L$	16	O	DAC analog output for L-channel
$V_{OUT}R$	15	O	DAC analog output for R-channel
XTI	21	I	Crystal oscillator input(2)
XTO	20	O	Crystal oscillator output

(1) LV-TTL level

(2) 3.3-V CMOS level input

(3) 3.3-V CMOS level input with internal pulldown. This pin informs the PC of serviceable control signals such as mute, volume up, or volume down, which has no connection with the internal DAC or ADC directly. See the *Interface #3* and *End-Points* sections.

(4) Connect a decouple capacitor to GND

(5) TTL Schmitt trigger, 5 V tolerant

PCM2903 Terminal Functions

TERMINAL NAME	PIN	I/O	DESCRIPTIONS
AGNDC	11	−	Analog ground for codec
AGNDP	18	−	Analog ground for PLL
AGNDX	22	−	Analog ground for oscillator
D–	2	I/O	USB differential input/output minus(1)
D+	1	I/O	USB differential input/output plus(1)
DGND	26	−	Digital ground
DGNDU	4	−	Digital ground for USB transceiver
DIN	24	I	S/PDIF input(5)
DOUT	25	O	S/PDIF output
HID0	5	I	HID key state input (mute), active high(3)
HID1	6	I	HID key state input (volume up), active high(3)
HID2	7	I	HID key state input (volume down), active high(3)
SEL0	8	I	Must be set to high(6)
SEL1	9	I	Connected to the USB port of V_{BUS}(6)
$\overline{SSPND}$	28	O	Suspend flag, active low (Low: suspend, High: operational)
V_{BUS}	3	−	Must be connected to V_{DD}
V_{CCC}	10	−	Analog power supply for codec(4)
V_{CCP1}	17	−	Analog power supply for PLL(4)
V_{CCP2}	19	−	Analog power supply for PLL(4)
V_{CCX}	23	−	Analog power supply for oscillator(4)
V_{COM}	14	−	Common for ADC/DAC (V_{CCC}/2) (4)
V_{DD}	27	−	Digital power supply(4)
$V_{IN}L$	12	I	ADC analog input for L-channel
$V_{IN}R$	13	I	ADC analog input for R-channel
$V_{OUT}L$	16	O	DAC analog output for L-channel
$V_{OUT}R$	15	O	DAC analog output for R-channel
XTI	21	I	Crystal oscillator input(2)
XTO	20	O	Crystal oscillator output

(1) LV-TTL level

(2) 3.3-V CMOS level input

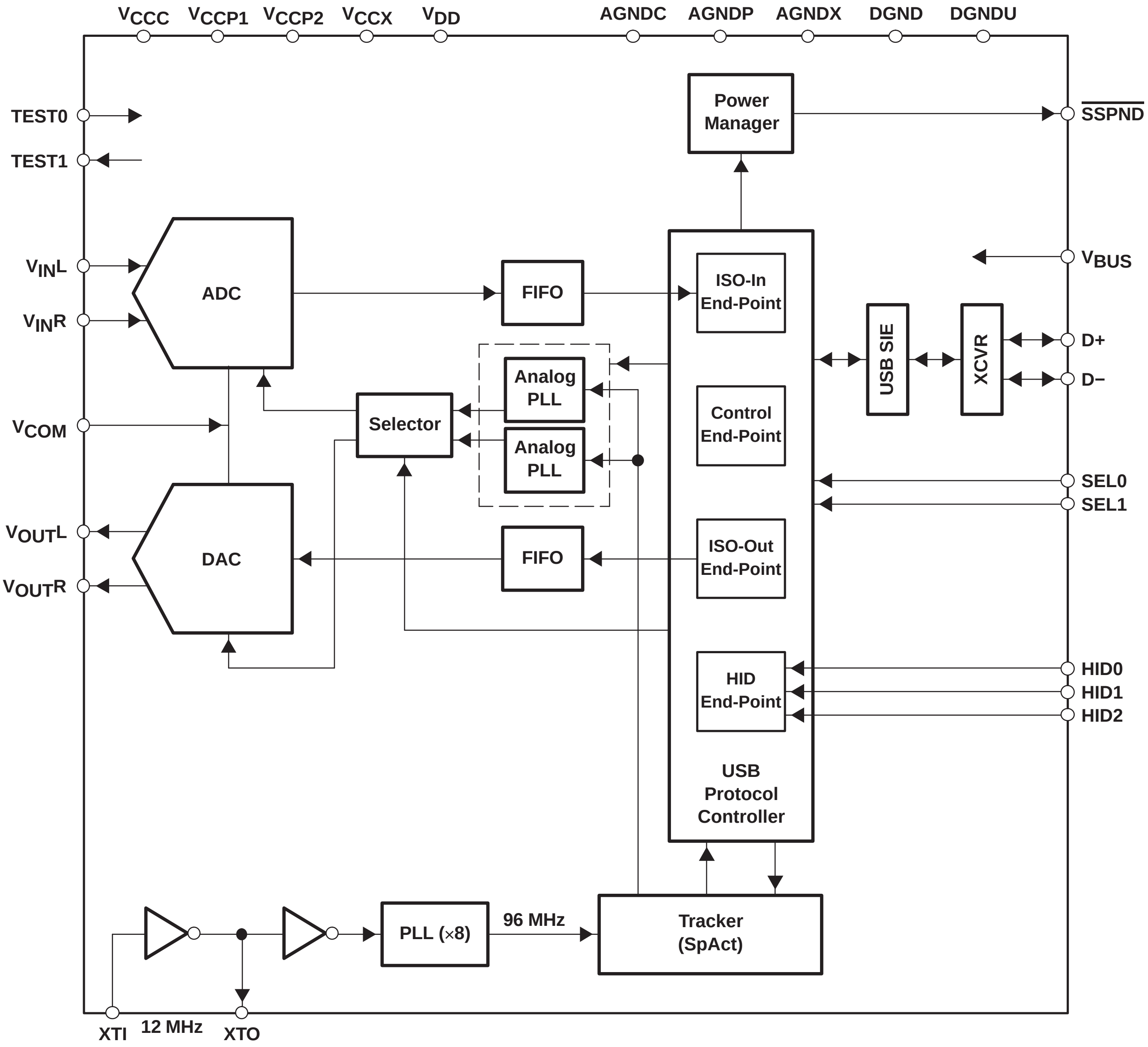
(3) 3.3-V CMOS level input with internal pulldown. This pin informs the PC of serviceable control signals such as mute, volume up, or volume down, which has no connection with the internal DAC or ADC directly. See the *Interface #3* and *End-Points* sections.

(4) Connect a decouple capacitor to GND

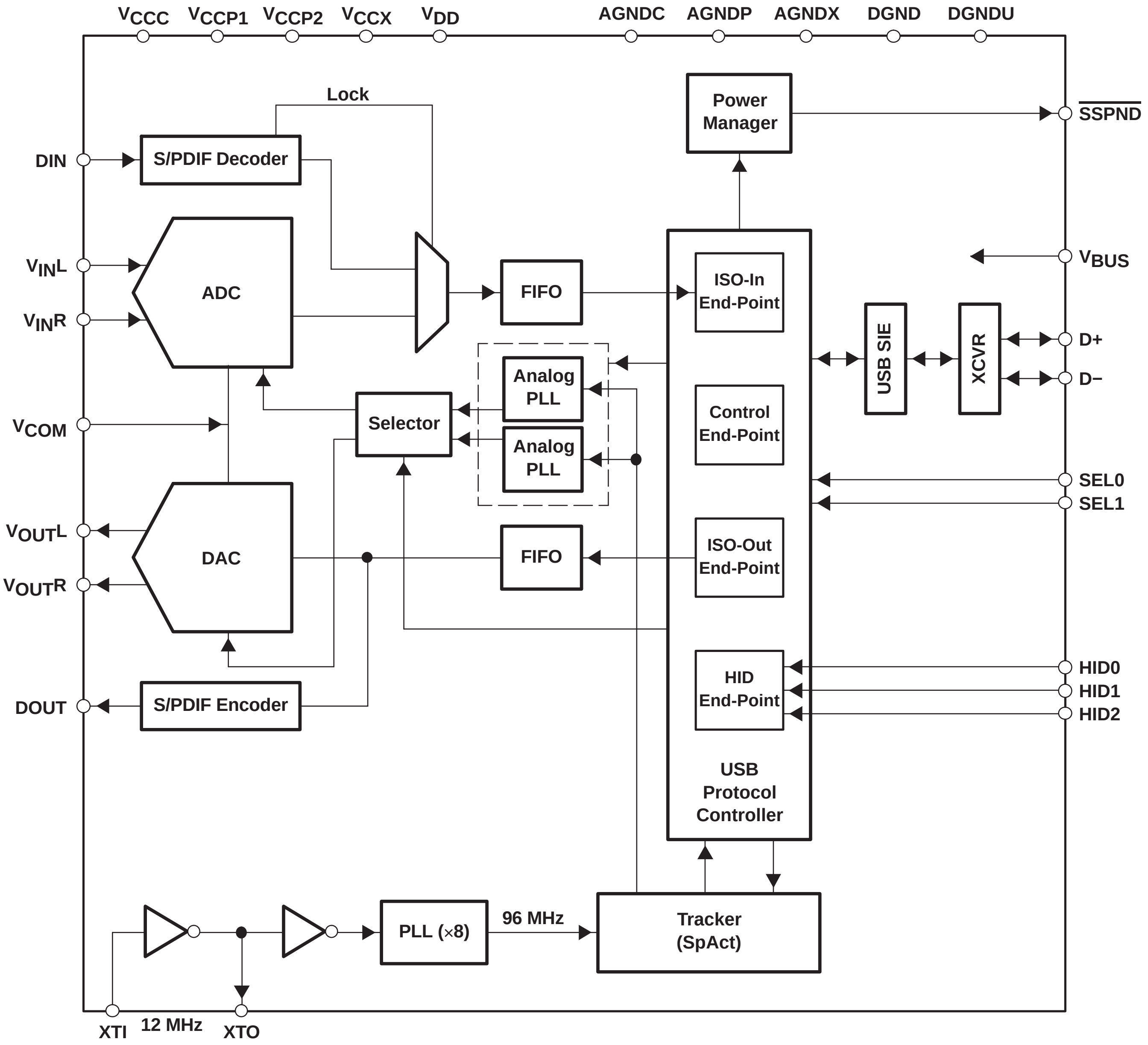
(5) 3.3-V CMOS level input with internal pulldown, 5 V tolerant

(6) TTL Schmitt trigger, 5 V tolerant

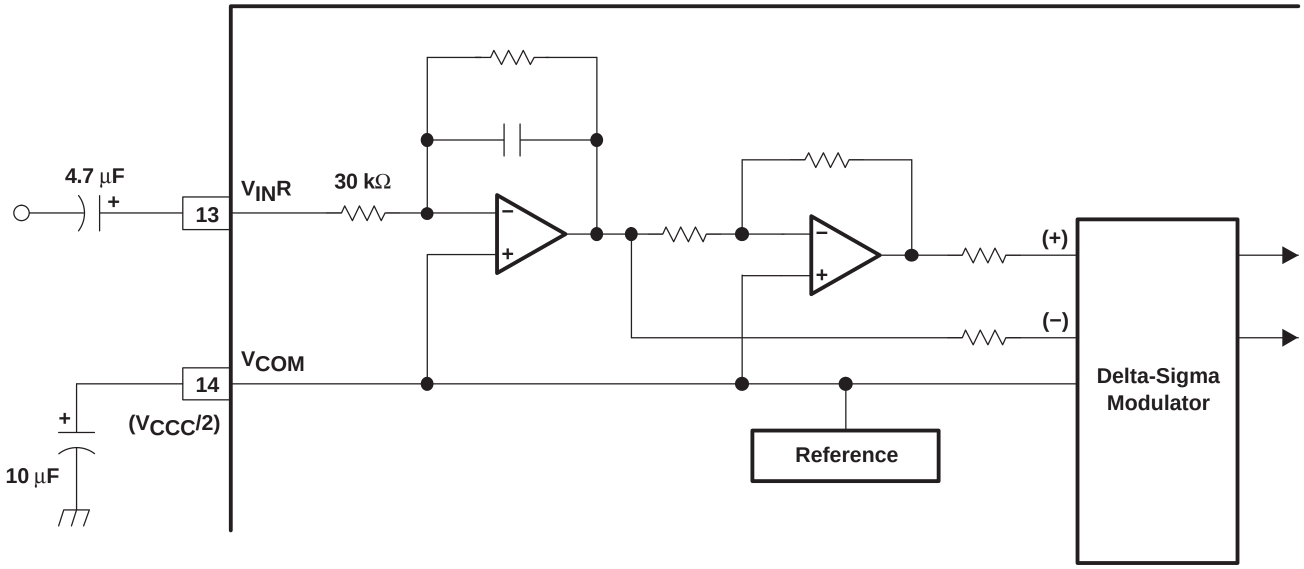
PCM2901 FUNCTIONAL BLOCK DIAGRAM


VCCC
VCCP1
VCCP2
VCCX
VDD
AGNDC
AGNDP
AGNDX
DGND
DGNDU
TEST0
TEST1
Power Manager
SSPND
VINL
VINR
ADC
FIFO
ISO-In End-Point
VBUS
USB SIE
XCVR
D+
D−
Analog PLL
Analog PLL
Selector
VCOM
Control End-Point
SEL0
SEL1
VOUTL
VOUTR
DAC
FIFO
ISO-Out End-Point
HID End-Point
HID0
HID1
HID2
USB Protocol Controller
PLL (×8)
96 MHz
Tracker (SpAct)
XTI
12 MHz
XTO

PCM2903 FUNCTIONAL BLOCK DIAGRAM


VCCC
VCCP1
VCCP2
VCCX
VDD
AGNDC
AGNDP
AGNDX
DGND
DGNDU
Lock
Power Manager
SSPND
DIN
S/PDIF Decoder
VINL
VINR
ADC
FIFO
ISO-In End-Point
VBUS
USB SIE
XCVR
D+
D−
Analog PLL
Analog PLL
Selector
VCOM
Control End-Point
SEL0
SEL1
VOUTL
VOUTR
DAC
FIFO
ISO-Out End-Point
HID End-Point
HID0
HID1
HID2
DOUT
S/PDIF Encoder
USB Protocol Controller
PLL (×8)
96 MHz
Tracker (SpAct)
XTI
12 MHz
XTO

PCM2901/2903 BLOCK DIAGRAM OF ANALOG FRONT-END (RIGHT CHANNEL)


4.7 µF
+
13
$V_{IN}R$
30 kΩ
−
+
−
+
(+)
(−)
V_{COM}
14
$(V_{CCC}/2)$
+
10 µF
Reference
Delta-Sigma
Modulator

TYPICAL CHARACTERISTICS

ADC

**TOTAL HARMONIC DISTORTION + NOISE at −0.5 dB
vs
FREE-AIR TEMPERATURE**

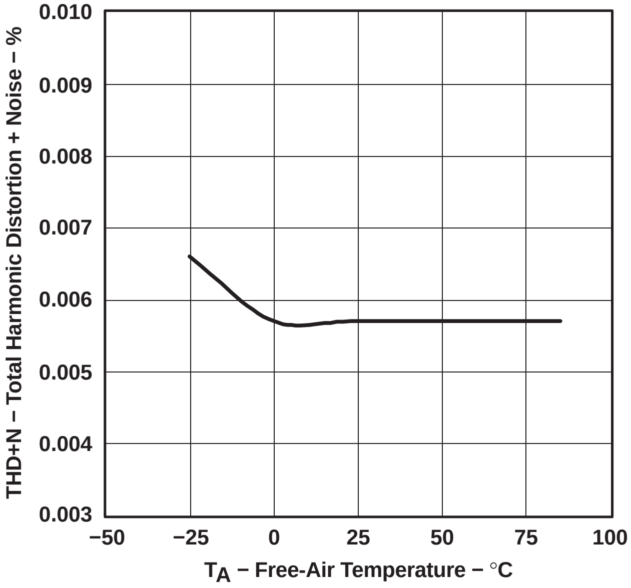


Figure 1

**DYNAMIC RANGE and SNR
vs
FREE-AIR TEMPERATURE**

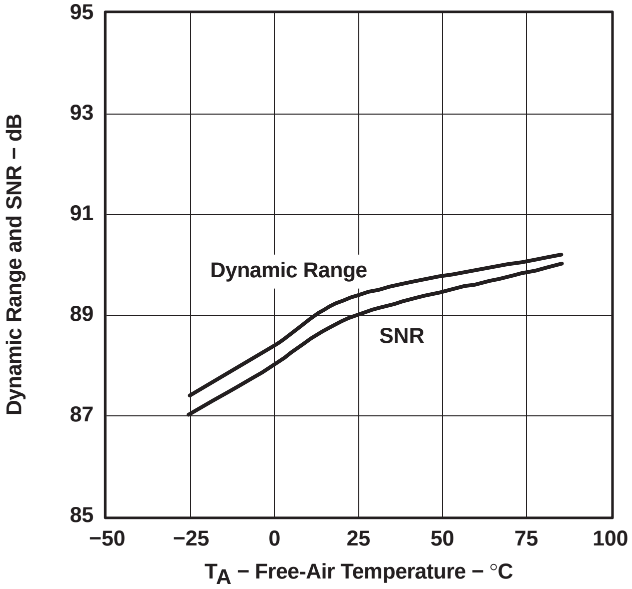


Figure 2

**TOTAL HARMONIC DISTORTION + NOISE at −0.5 dB
vs
SUPPLY VOLTAGE**

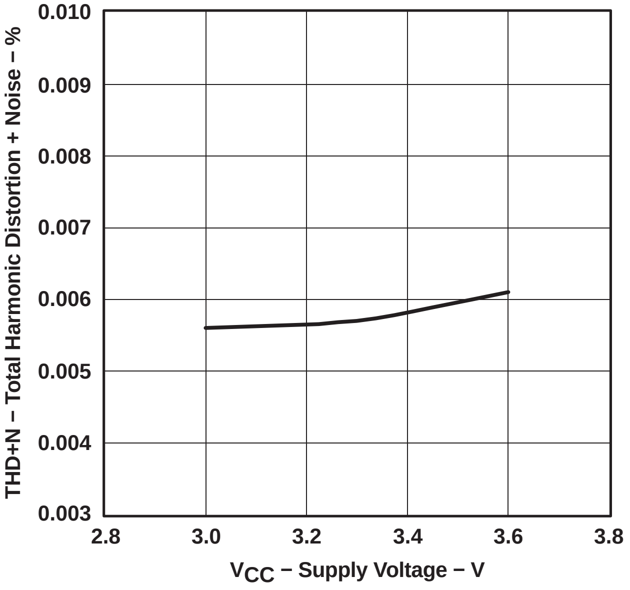


Figure 3

**DYNAMIC RANGE and SNR
vs
SUPPLY VOLTAGE**

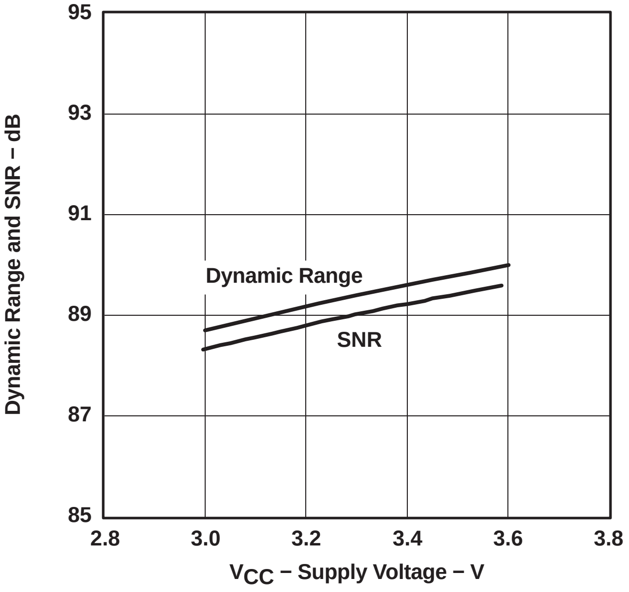


Figure 4

All specifications at T_A = 25°C, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX}$ = 3.3 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

ADC (CONTINUED)

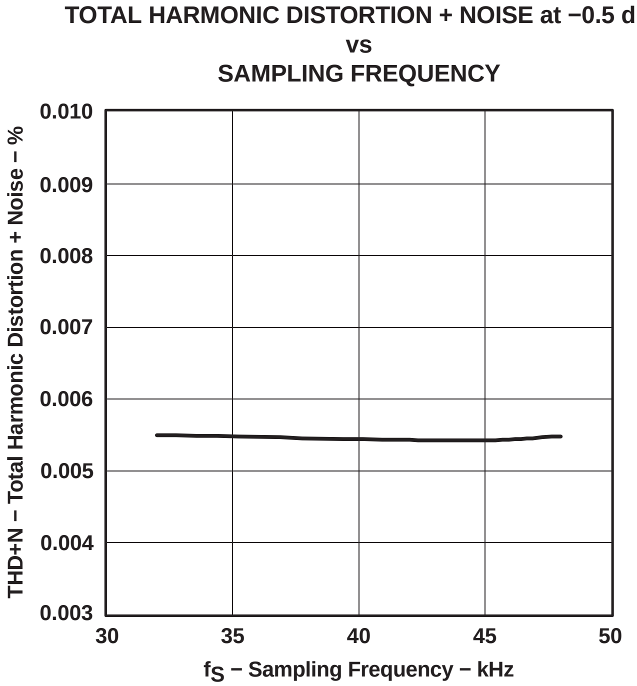


Figure 5

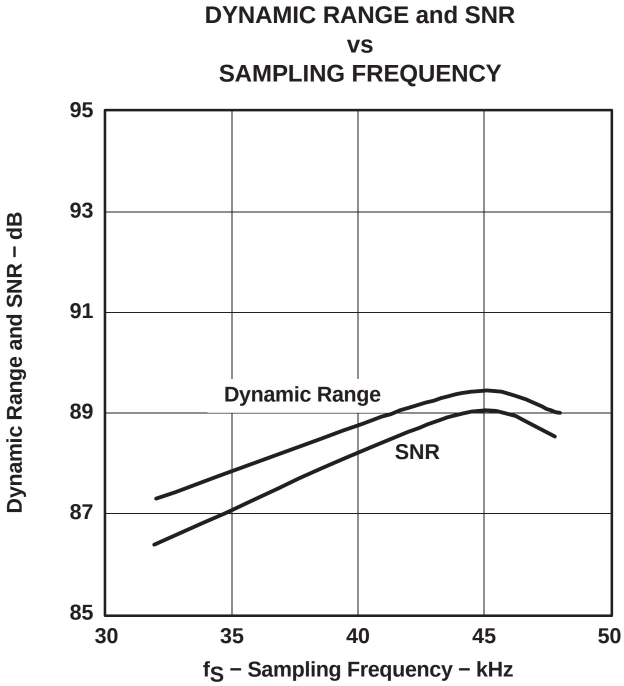


Figure 6

DAC

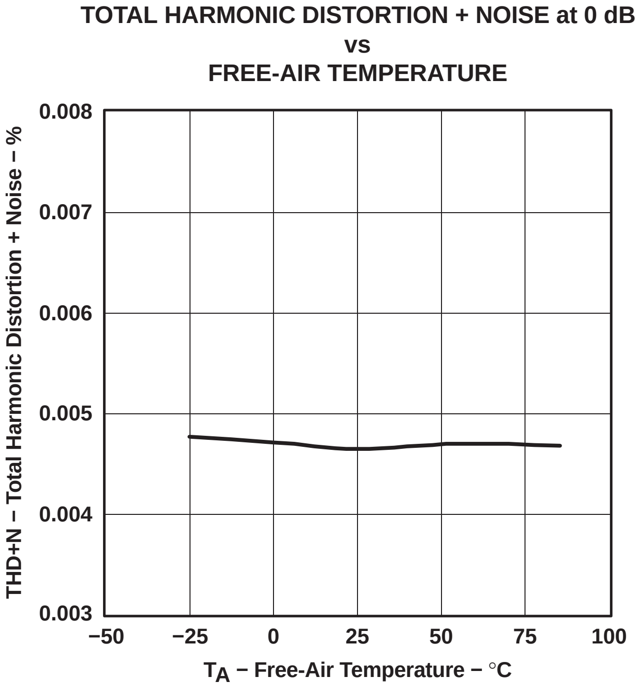


Figure 7

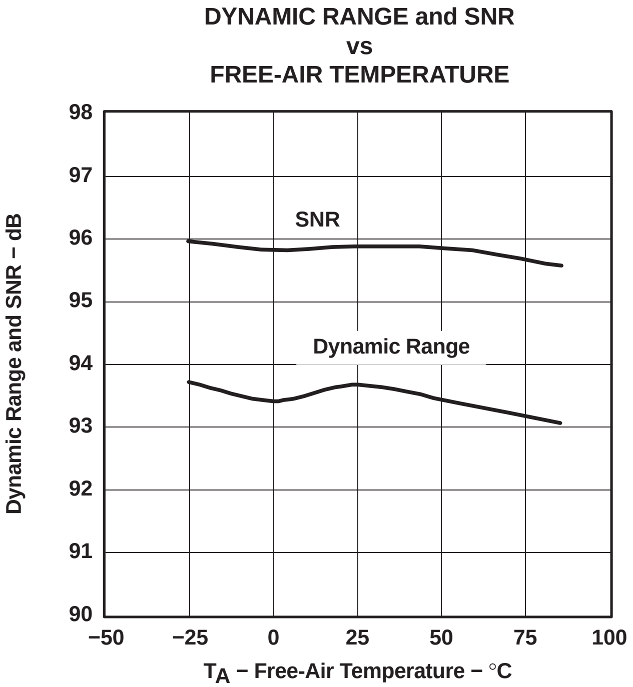


Figure 8

All specifications at T_A = 25°C, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX}$ = 3.3 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

DAC (CONTINUED)

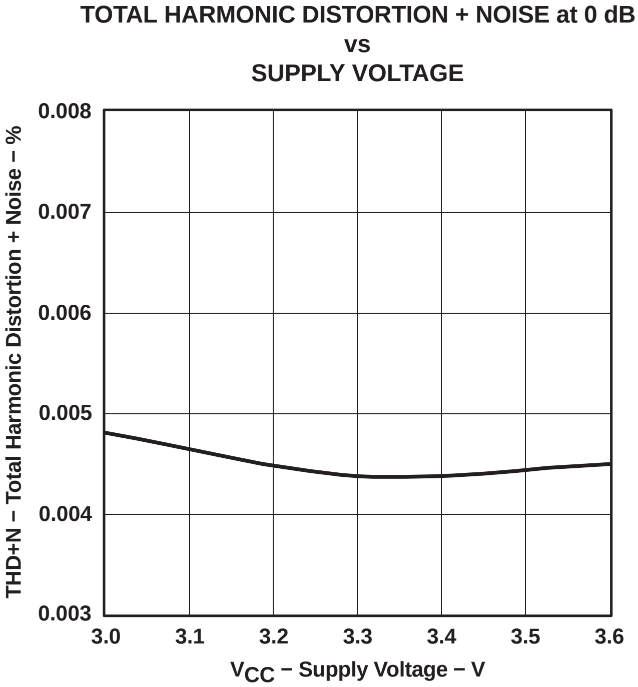


Figure 9

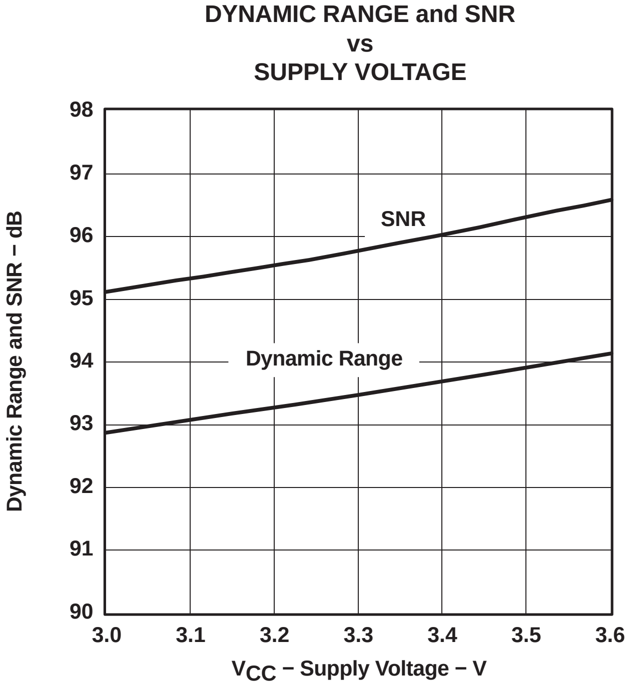


Figure 10

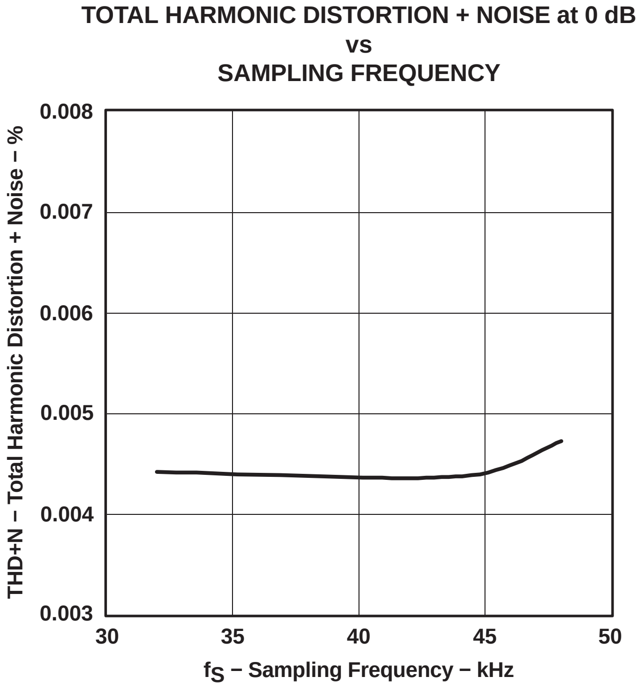


Figure 11

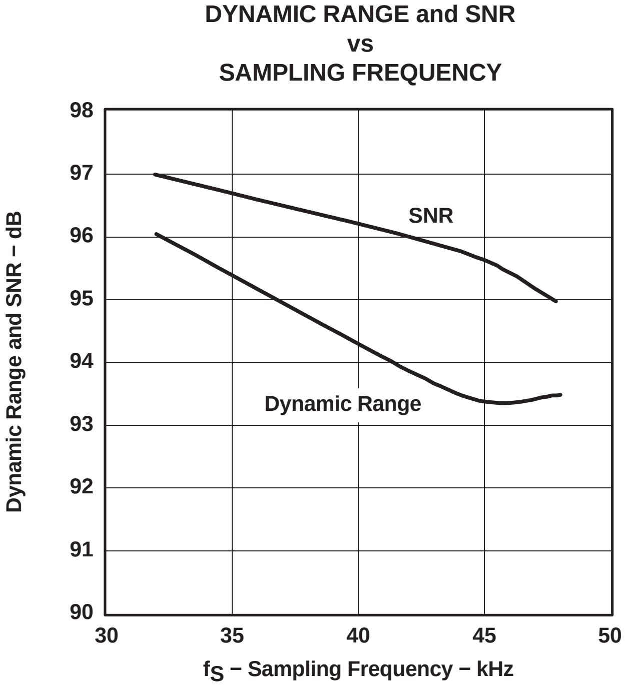


Figure 12

All specifications at T_A = 25°C, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCx}$ = 3.3 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

ADC OUTPUT SPECTRUM

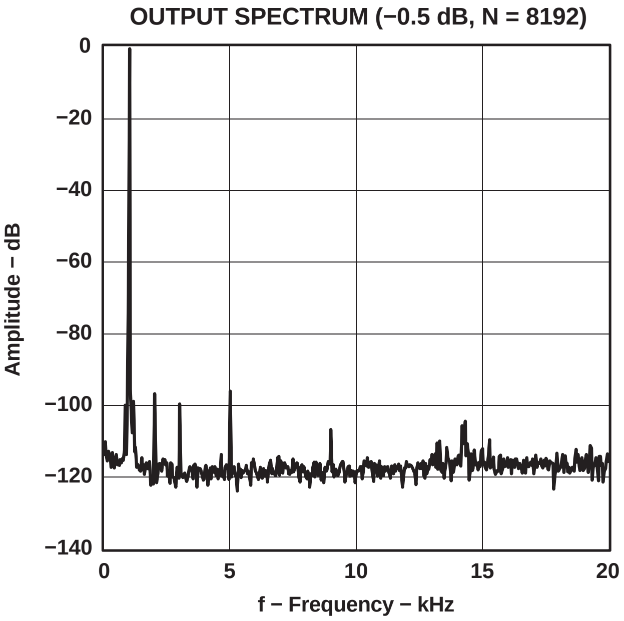


Figure 13

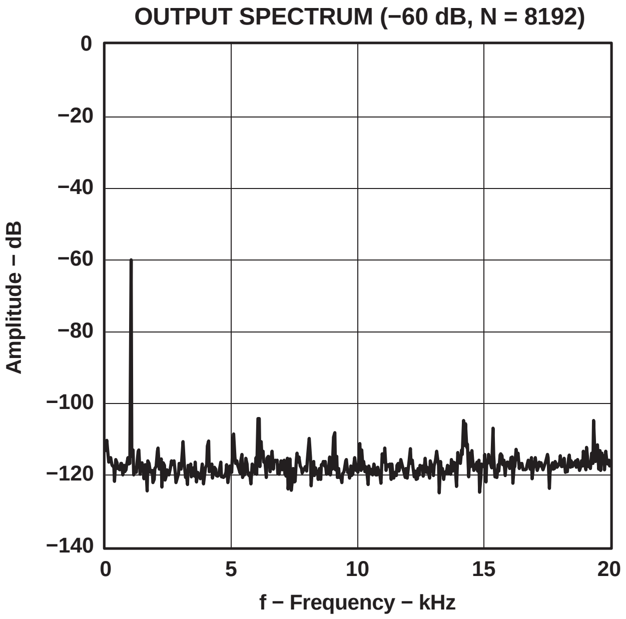


Figure 14

DAC OUTPUT SPECTRUM

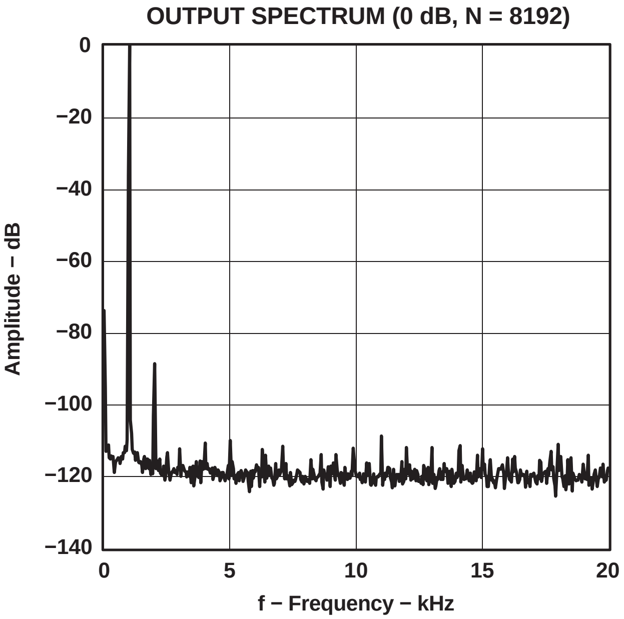


Figure 15

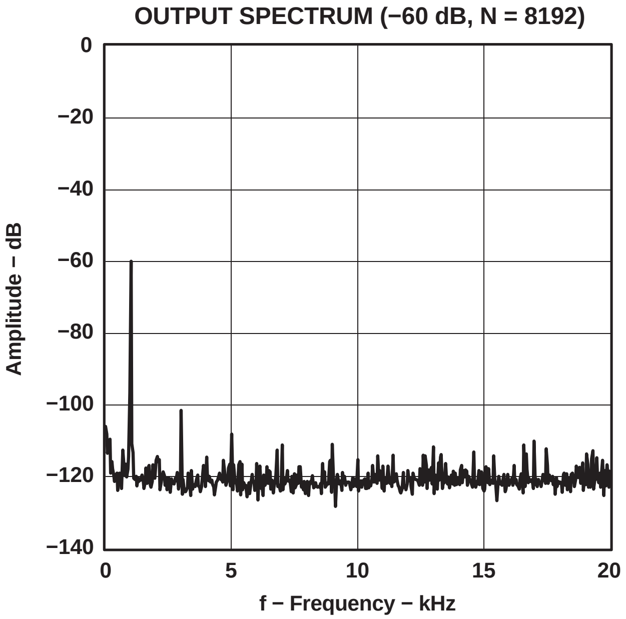


Figure 16

SUPPLY CURRENT

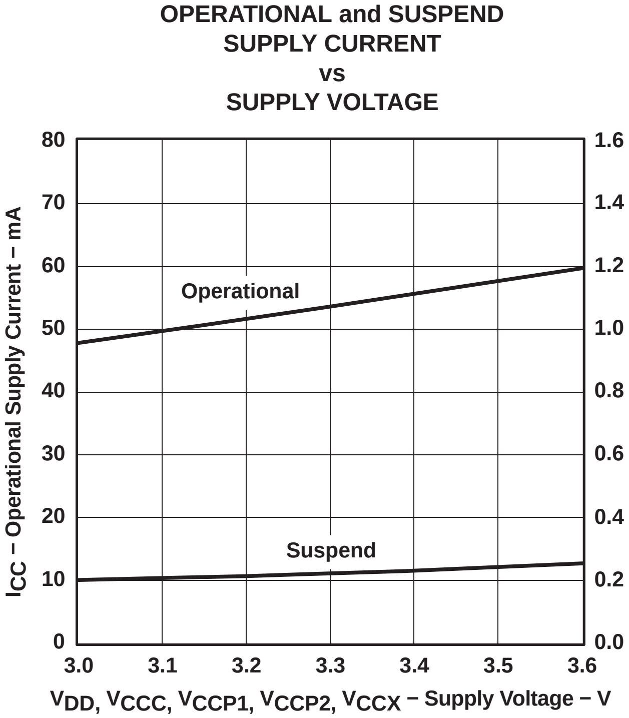


Figure 17

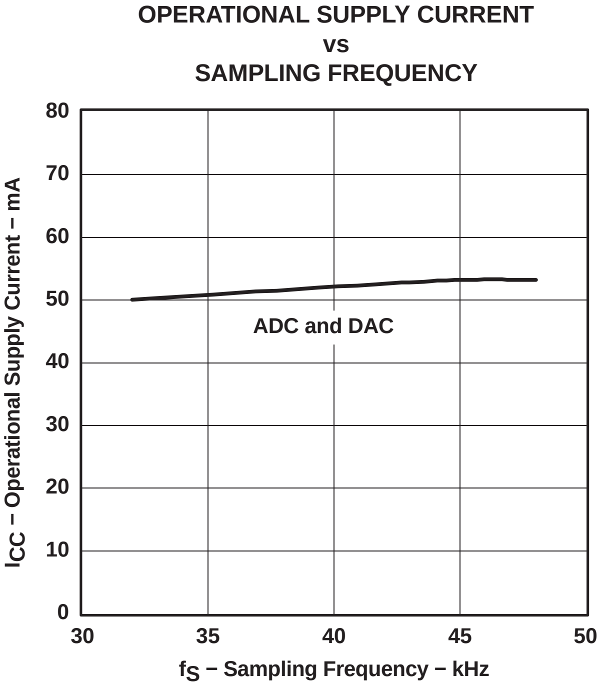


Figure 18

All specifications at T_A = 25°C, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX}$ = 3.3 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

ADC DIGITAL DECIMATION FILTER FREQUENCY RESPONSE

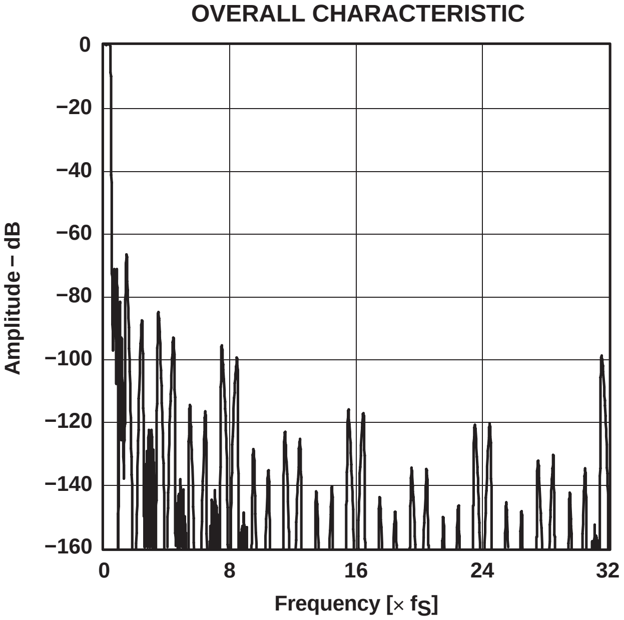


Figure 19

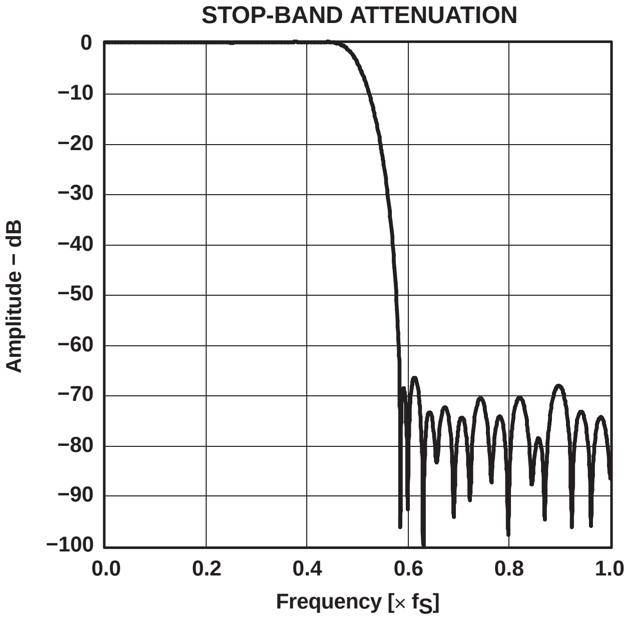


Figure 20

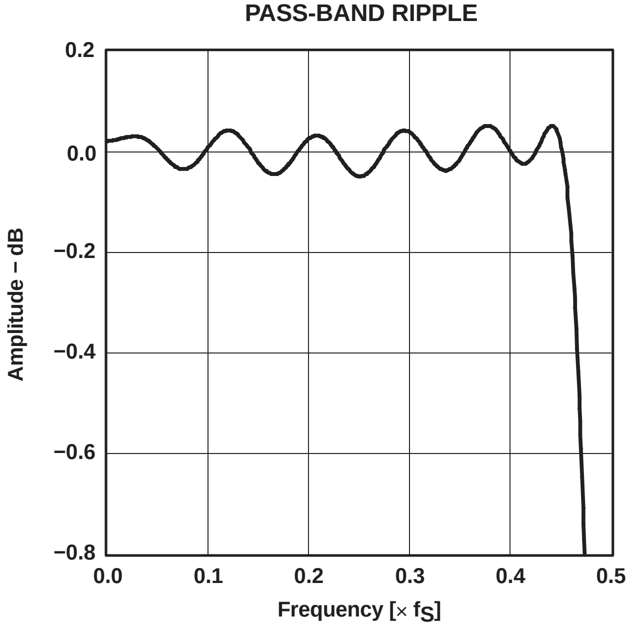


Figure 21

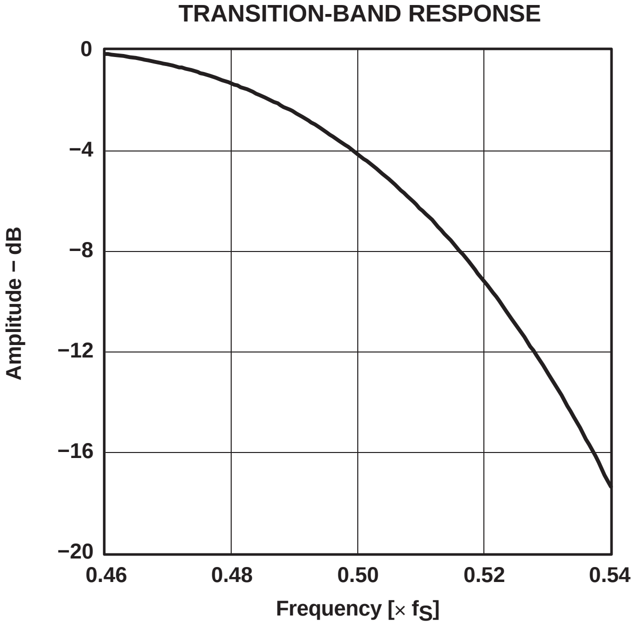


Figure 22

ADC DIGITAL HIGH-PASS FILTER FREQUENCY RESPONSE

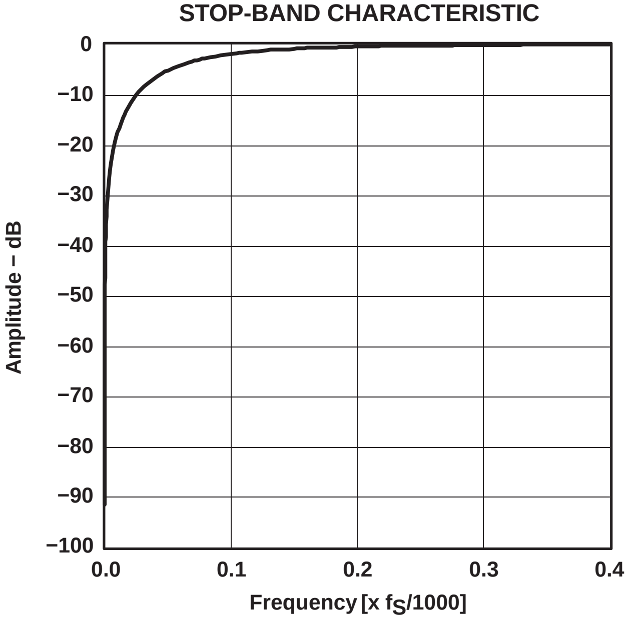


Figure 23

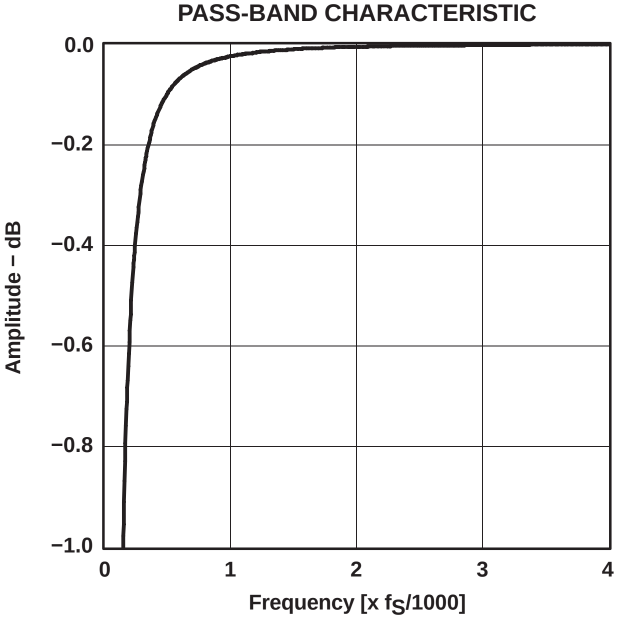


Figure 24

ADC ANALOG ANTIALIASING FILTER FREQUENCY RESPONSE

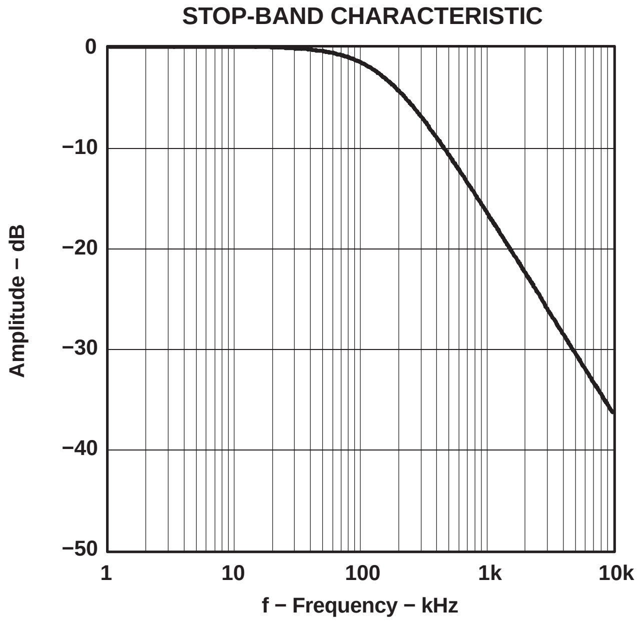


Figure 25

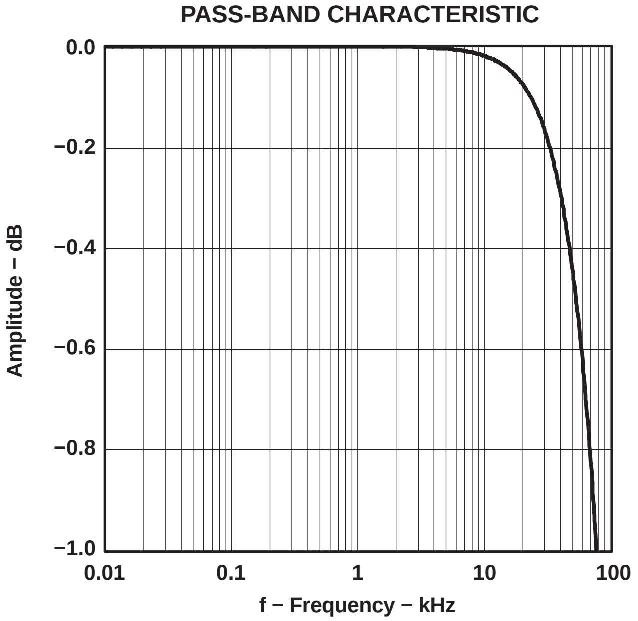


Figure 26

All specifications at T_A = 25°C, V_{DD} = V_{CCC} = V_{CCP1}= V_{CCP2} = V_{CCx} = 3.3 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

DAC DIGITAL INTERPOLATION FILTER FREQUENCY RESPONSE

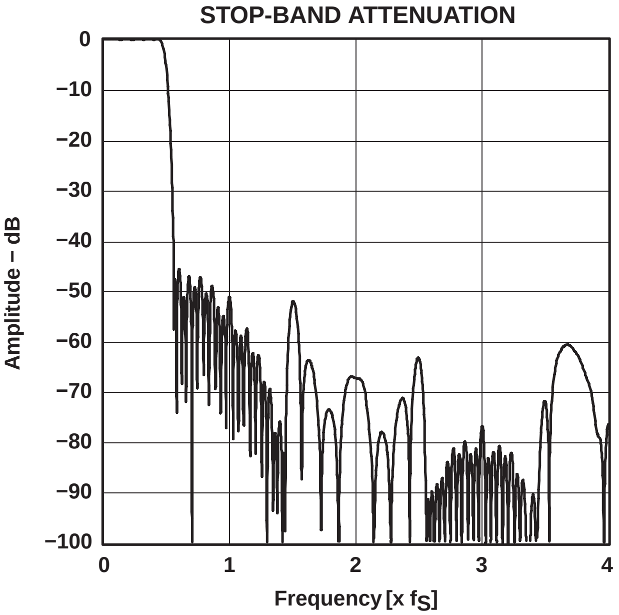


Figure 27

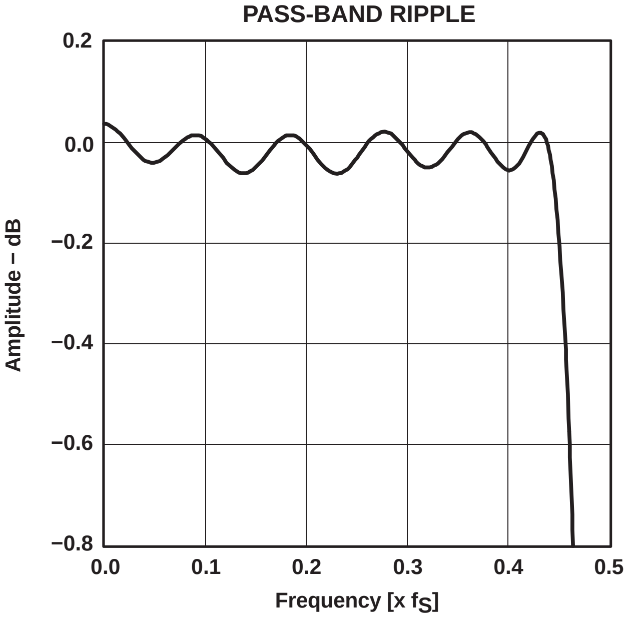


Figure 28

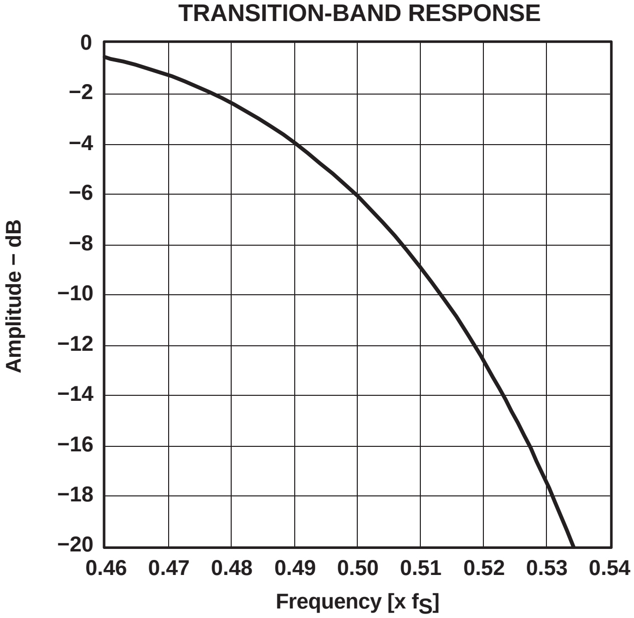


Figure 29

All specifications at T_A = 25°C, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX}$ = 3.3 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

DAC ANALOG FIR FILTER FREQUENCY RESPONSE

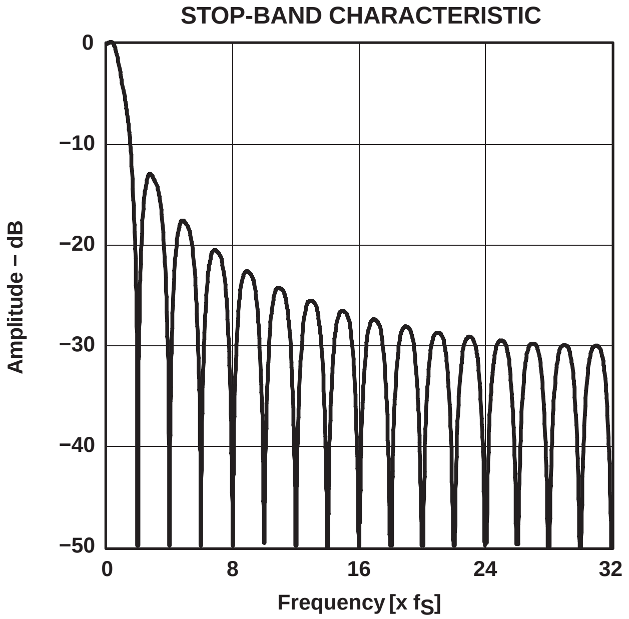


Figure 30

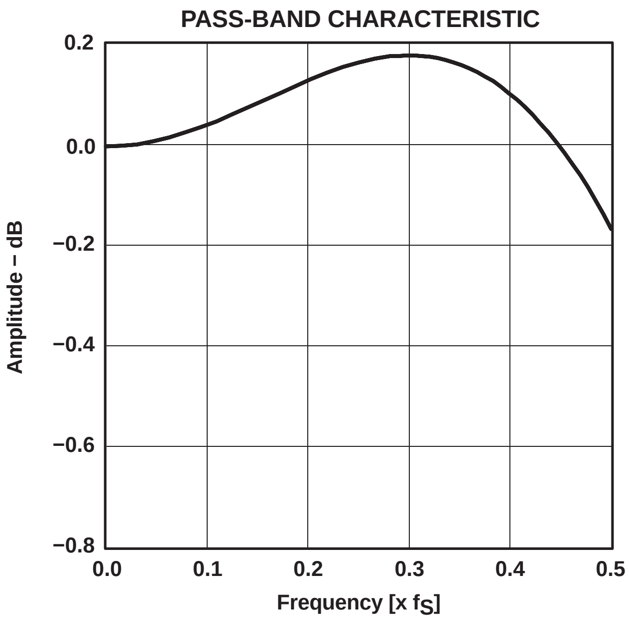


Figure 31

DAC ANALOG LOW-PASS FILTER FREQUENCY RESPONSE

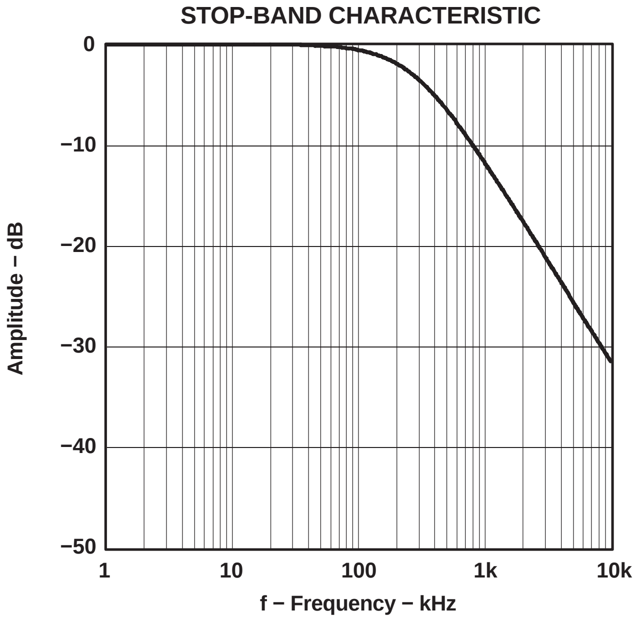


Figure 32

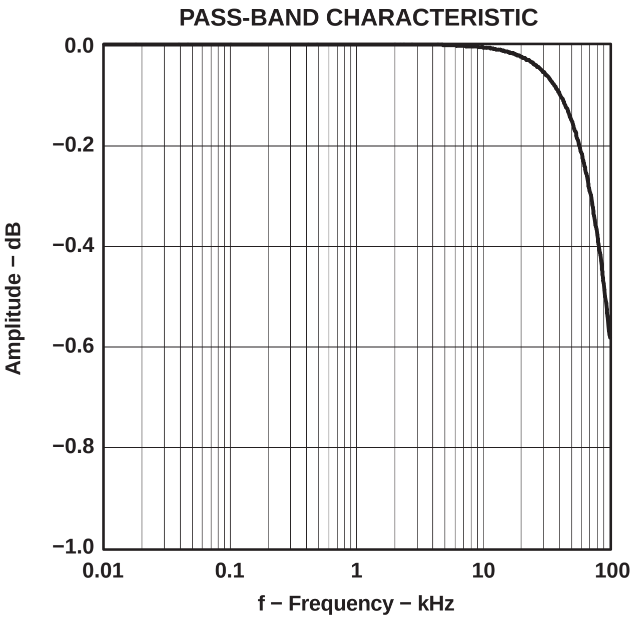


Figure 33

All specifications at T_A = 25°C, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX}$ = 3.3 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

USB INTERFACE

Control data and audio data are transferred to the PCM2901/2903 via D+ (pin 1) and D– (pin 2). All data to/from the PCM2901/2903 is transferred at full speed. The device descriprtor contains the information described in Table 1. The device descriptor can be modified on request; contact a Texas Instruments representative for details.

Table 1. Device Descriptor

USB revision	1.1 compliant
Device class	0x00 (device defined interface level)
Device sub class	0x00 (not specified)
Device protocol	0x00 (not specified)
Max packet size for end-point 0	8 byte
Vendor ID	0x08BB (default value, can be modified)
Product ID	0x2901 / 0x2903 (default value, can be modified)
Device release number	1.0 (0x0100)
Number of configurations	1
Vendor strings	String #1 (see Table 3)
Product strings	String #2 (see Table 3)
Serial number	Not supported

The configuration descriptor contains the information described in Table 2. The configuration descriptor can be modified on request; contact a Texas Instruments representative for details.

Table 2. Configuration Descriptor

Interface	Four interfaces
Power attribute	0xC0 (Self-powered, no remote wakeup)
Maximum power	0x00 (0 mA. Default value, can be modified)

The string descriptor contains the information described in Table 3. The string descriptor can be modified on request; contact a Texas Instruments representative for details.

Table 3. String Descriptor

#0	0x0409
#1	Burr-Brown from TI (default value, can be modified)
#2	USB audio codec (default value, can be modified)

DEVICE CONFIGURATION

Figure 34 illustrates the USB audio function topology. The PCM2901/2903 has four interfaces. Each interface is constructed by alternative settings.

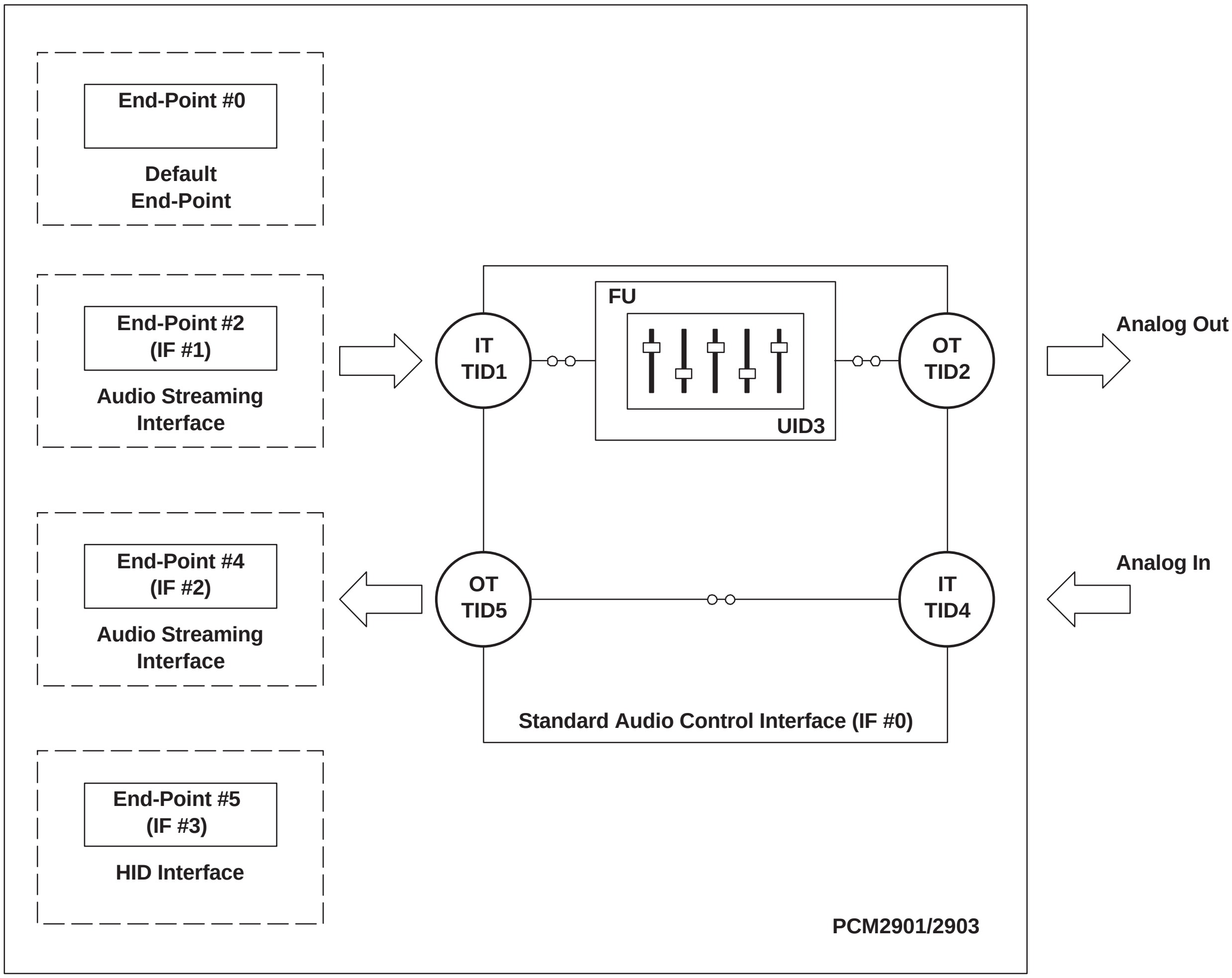

End-Point #0
Default
End-Point
End-Point #2
(IF #1)
Audio Streaming
Interface
End-Point #4
(IF #2)
Audio Streaming
Interface
End-Point #5
(IF #3)
HID Interface
FU
IT
TID1
OT
TID2
UID3
Analog Out
OT
TID5
IT
TID4
Analog In
Standard Audio Control Interface (IF #0)
PCM2901/2903

Figure 34. USB Audio Function Topology

Interface #0

Interface #0 is defined as the control interface. Alternative setting #0 is the only possible setting for interface #0. Alternative setting #0 describes the standard audio control interface. A terminal constructs the audio control interface. The PCM2901/2903 has the following five terminals.

- Input terminal (IT #1) for isochronous-out stream
- Output terminal (OT #2) for audio analog output
- Feature unit (FU #3) for DAC digital attenuator
- Input terminal (IT #4) for audio analog input
- Output terminal (OT #5) for isochronous-in stream

Input terminal #1 is defined as USB stream (terminal type 0x0101). Input terminal #1 can accept 2-channel audio streams constructed by left and right channels. Output terminal #2 is defined as a speaker (terminal type 0x0301). Input terminal #4 is defined as microphone (terminal type 0x0201). Output terminal #5 is defined as a USB stream (terminal type 0x0101). Output terminal #5 can generate 2-channel audio streams constructed by left and right channels. Feature unit #3 supports the following sound control features.

- Volume control
- Mute control

The built-in digital volume controller can be manipulated by an audio class specific request from 0 dB to –64 dB in 1-dB steps. Changes are made by incrementing or decrementing by one step (1 dB) for every 1/f_S time interval until the volume level has reached the requested value. Each channel can be set for different values. The master volume control is not supported. A request to the master volume is stalled and ignored. The built-in digital mute controller can be manipulated by audio class specific request. A master mute control request is acceptable. A request to an individual channel is stalled and ignored.

Interface #1

Interface #1 is defined as the audio streaming data-out interface. Interface #1 has the following seven alternative settings. Alternative setting #0 is the zero bandwidth setting.

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero bandwidth				
01	16 bit	Stereo	2s complement (PCM)	Adaptive	32, 44.1, 48
02	16 bit	Mono	2s complement (PCM)	Adaptive	32, 44.1, 48
03	8 bit	Stereo	2s complement (PCM)	Adaptive	32, 44.1, 48
04	8 bit	Mono	2s complement (PCM)	Adaptive	32, 44.1, 48
05	8 bit	Stereo	Offset binary (PCM8)	Adaptive	32, 44.1, 48
06	8 bit	Mono	Offset binary (PCM8)	Adaptive	32, 44.1, 48

Interface #2

Interface #2 is defined as the audio streaming data-in interface. Interface #2 has the following 19 alternative settings. Alternative setting #0 is the zero bandwidth setting. All other alternative settings are operational settings.

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero Bandwidth				
01	16 bit	Stereo	2s complement (PCM)	Asynchronous	48
02	16 bit	Mono	2s complement (PCM)	Asynchronous	48
03	16 bit	Stereo	2s complement (PCM)	Asynchronous	44.1
04	16 bit	Mono	2s complement (PCM)	Asynchronous	44.1
05	16 bit	Stereo	2s complement (PCM)	Asynchronous	32
06	16 bit	Mono	2s complement (PCM)	Asynchronous	32
07	16 bit	Stereo	2s complement (PCM)	Asynchronous	22.05
08	16 bit	Mono	2s complement (PCM)	Asynchronous	22.05
09	16 bit	Stereo	2s complement (PCM)	Asynchronous	16
0A	16 bit	Mono	2s complement (PCM)	Asynchronous	16
0B	8 bit	Stereo	2s complement (PCM)	Asynchronous	16
0C	8 bit	Mono	2s complement (PCM)	Asynchronous	16
0D	8 bit	Stereo	2s complement (PCM)	Asynchronous	8
0E	8 bit	Mono	2s complement (PCM)	Asynchronous	8
0F	16 bit	Stereo	2s complement (PCM)	Synchronous	11.025
10	16 bit	Mono	2s complement (PCM)	Synchronous	11.025
11	8 bit	Stereo	2s complement (PCM)	Synchronous	11.025
12	8 bit	Mono	2s complement (PCM)	Synchronous	11.025

Interface #3

Interface #3 is defined as the interrupt data-in interface. Alternative setting #0 is the only possible setting for interface #3. Interface #3 constructs the HID consumer control device. Interface #3 reports the following three key statuses.

- Mute (0xE209)
- Volume up (0xE909)
- Volume down (0xEA09)

End-Points

The PCM2901/2903 has the following four end-points.

- Control end-point (EP #0)
- Isochronous-out audio data stream end-point (EP #2)
- Isochronous-in audio data stream end-point (EP #4)
- HID end-point (EP #5)

The control end-point is a default end-point. The control end-point is used to control all functions of the PCM2901/2903 by the standard USB request and USB audio class specific request from the host. The isochronous-out audio data stream end-point is an audio sink end-point, which receives the PCM audio data. The isochronous-out audio data stream end-point accepts the adaptive transfer mode. The isochronous-in audio data stream end-point is an audio source end-point, which transmits the PCM audio data. The isochronous-in audio data stream end-point uses asynchronous transfer mode. The HID end-point is an interrupt-in end-point. HID end-point reports HID0, HID1, and HID2 pin status every 32 ms.

The human interface device (HID) pins are defined as consumer control devices. The HID function is designed as an independent end-point from both isochronous-in and -out end-points. This means that the result of affection for the HID operation depends on the host software. Typically, the HID function is affected for the primary audio-out device.

Clock and Reset

The PCM2901/2903 requires a 12-MHz (±500 ppm) clock for the USB and audio function, which can be generated by a built-in crystal oscillator with a 12-MHz crystal resonator or supplied by an external clock. The 12-MHz crystal resonator must be connected to XTI (pin 21) and XTO (pin 20) with one high (1-MΩ) resistor and two small capacitors, the capacitance of which depends on the load capacitance of the crystal resonator. If the external clock is used, the clock must be supplied to XTI, and XTO must be open.

The PCM2901/2903 has an internal power-on reset circuit, which works automatically when V_{DD} (pin 27) exceeds 2.5 V typical (2.7 V to 2.2 V) and about 700 µs is required until internal reset release.

Digital Audio Interface (PCM2903)

The PCM2903 employs both S/PDIF input and output. Isochronous-out data from the host is encoded to the S/PDIF output and the DAC analog output. Input data is selected as either S/PDIF or ADC analog input. When the device detects an S/PDIF input and successfully locks on the received data, the isochronous-in transfer data source is automatically selected from S/PDIF itself; otherwise, the data source is selected to ADC analog input.

Supported Input Data (PCM2903)

The following data formats are accepted by the S/PDIF input and output. All other data formats are unable to use S/PDIF.

- 48-kHz 16-bit stereo
- 44.1-kHz 16-bit stereo
- 32-kHz 16-bit stereo

Mismatch between input data format and host command may cause unexpected results except in the following conditions.

- Record monaural format from stereo data input at the same data rate
- Record 8-bit format from 16-bit data input at the same data rate

A combination between the above conditions is not accepted.

For the playback, all possible data rate source is converted to 16-bit stereo format at the same source data rate.

Channel Status Information (PCM2903)

The channel status information is fixed as consumer application, PCM mode, copyright, and digital/digital converter. All other bits are fixed as 0s except for the sample frequency, which is set automatically according to the data received through the USB.

Copyright Management (PCM2903)

Isochronous-in data is affected by the serial copy management system (SCMS). Where receiving digital audio data that is indicated as original data in the control bit, input digital audio data transfers to the host. If the data is indicated as first generation or higher, transferred data is selected to analog input.

Digital audio data output is always encoded as original with SCMS control.

The implementation of this feature is an option for the customer. Note that it is the user’s responsibility whether they implement this feature in their product or not.

INTERFACE SEQUENCE

Power On, Attach, and Playback Sequence

The PCM2901/2903 is ready for setup when the reset sequence has finished and the USB bus is attached. In order to perform certain reset sequences defined in the USB specification, V_{DD}, V_{CCC}, V_{CCP1}, V_{CCP2}, and V_{CCX} must rise up with 10 ms / 3.3 V. After connection has been established by setup, the PCM2901/2903 is ready to accept USB audio data. While waiting, the audio data (idle state) and analog output are set to bipolar zero (BPZ).

When receiving the audio data, the PCM2901/2903 stores the first audio packet, which contained 1-ms audio data, into the internal storage buffer. The PCM2901/2903 starts playing the audio data when detecting the following start of frame (SOF) packet.

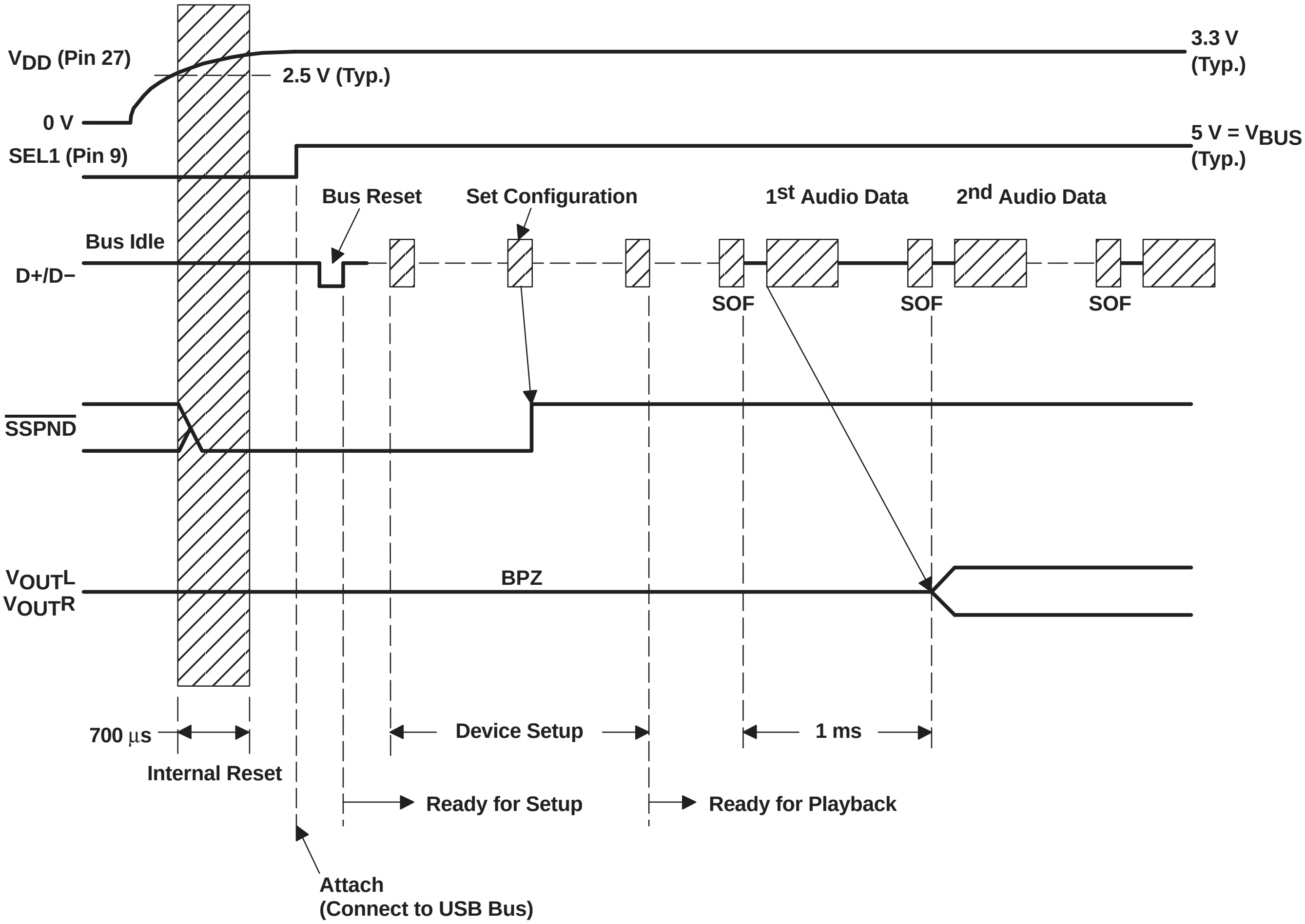

VDD (Pin 27)
0 V
2.5 V (Typ.)
3.3 V (Typ.)
SEL1 (Pin 9)
5 V = VBUS (Typ.)
Bus Reset
Set Configuration
1st Audio Data
2nd Audio Data
Bus Idle
D+/D−
SOF
SOF
SOF
SSPND
VOUTL
VOUTR
BPZ
700 µs
Internal Reset
Device Setup
1 ms
Ready for Setup
Ready for Playback
Attach (Connect to USB Bus)

Figure 35. Attach After Power-On

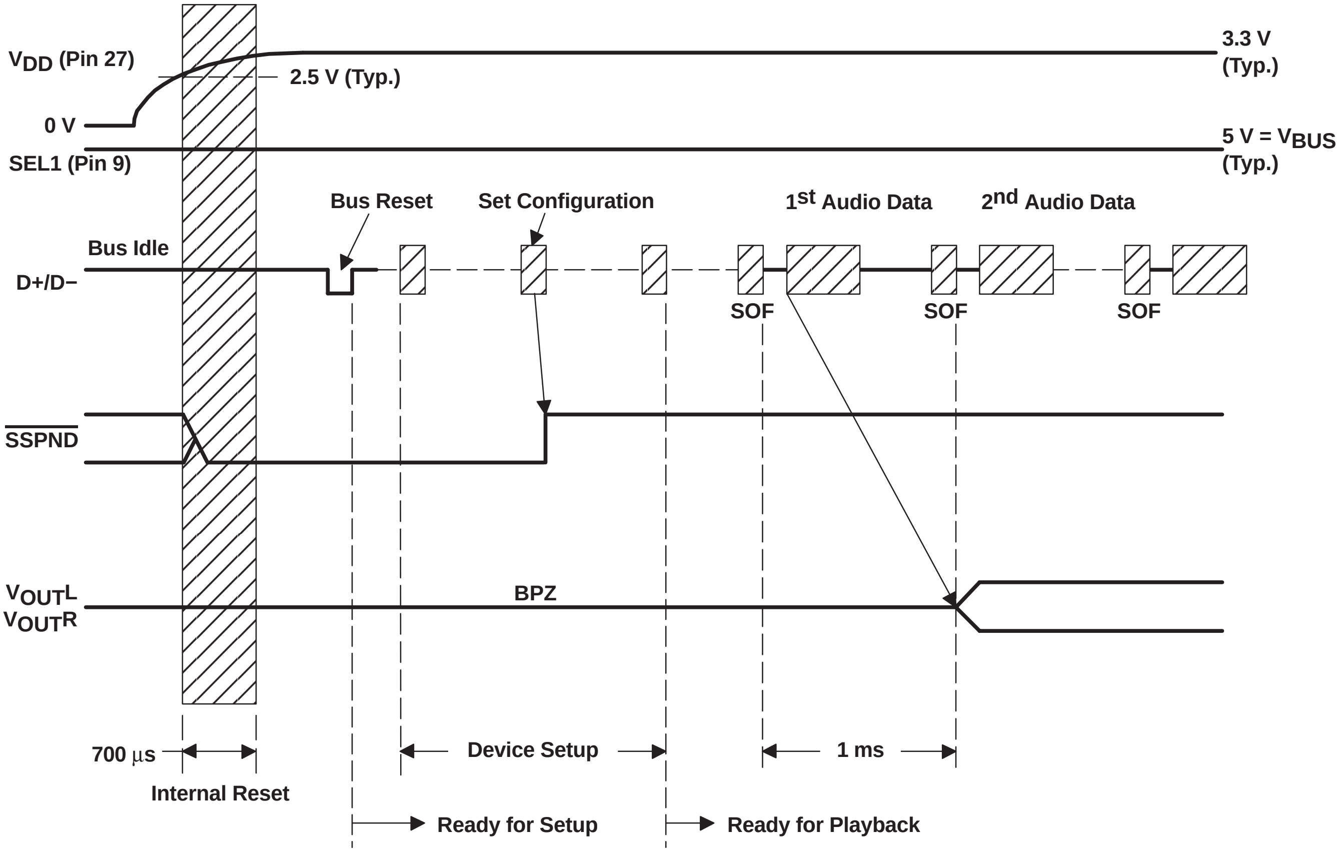

VDD (Pin 27)
0 V
2.5 V (Typ.)
3.3 V (Typ.)
SEL1 (Pin 9)
5 V = VBUS (Typ.)
Bus Reset
Set Configuration
1st Audio Data
2nd Audio Data
Bus Idle
D+/D−
SOF
SOF
SOF
SSPND
VOUTL
VOUTR
BPZ
700 µs
Internal Reset
Device Setup
1 ms
Ready for Setup
Ready for Playback

Figure 36. Power-On Under Attach

Play, Stop, and Detach Sequence

When the host finishes or aborts the playback, the PCM2901/2903 stops playing after the last audio data has played.

Record Sequence

The PCM2901/2903 starts the audio capture into the internal memory after receiving the SET_INTERFACE command.

Suspend and Resume Sequence

The PCM2901/2903 enters the suspend state after it sees a constant idle state on the USB bus, approximately 5 ms. While the PCM2901/2903 enters the suspend state, the $\overline{\text{SSPND}}$ flag (pin 28) is asserted. The PCM2901/2903 wakes up immediately after detecting a non-idle state on the USB bus.

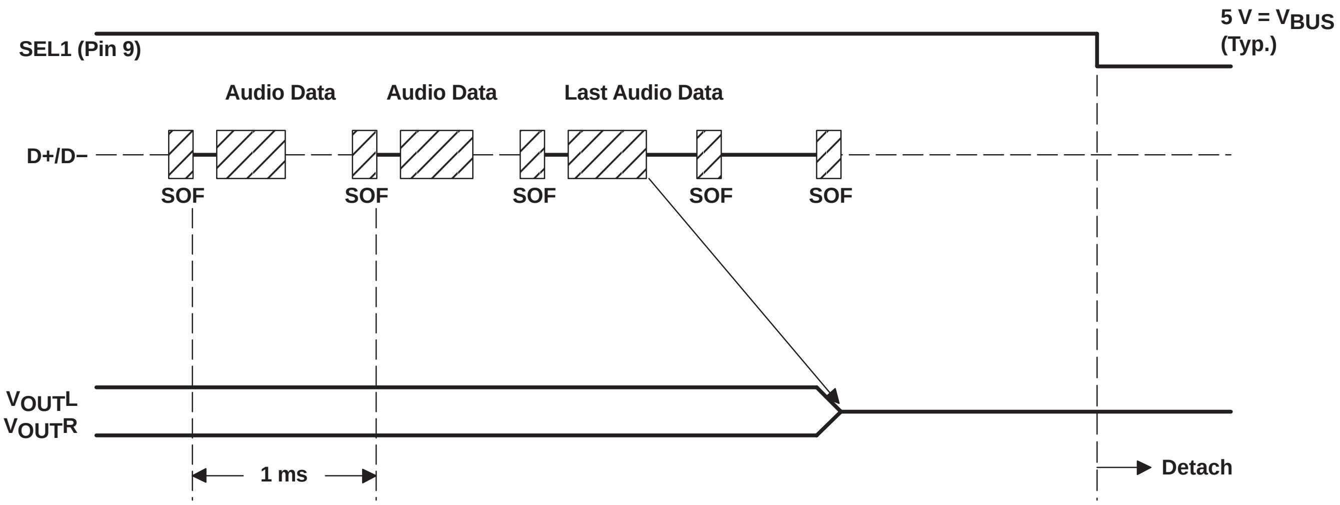

SEL1 (Pin 9)
5 V = VBUS
(Typ.)
Audio Data
Audio Data
Last Audio Data
D+/D−
SOF
SOF
SOF
SOF
SOF
VOUTL
VOUTR
1 ms
Detach

Figure 37. Play, Stop, and Detach

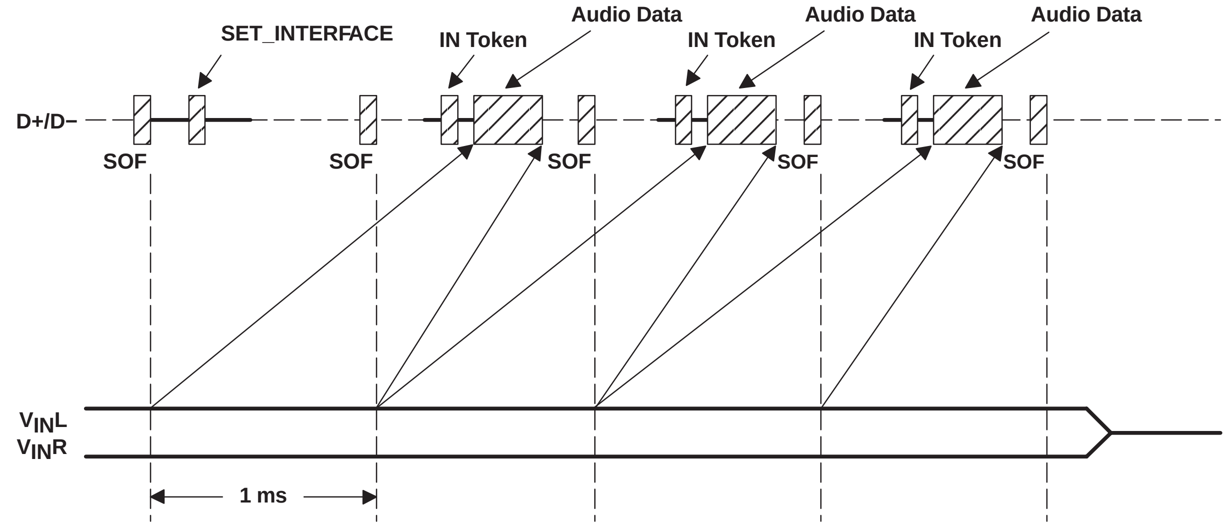

SET_INTERFACE
IN Token
Audio Data
IN Token
Audio Data
IN Token
Audio Data
D+/D−
SOF
SOF
SOF
SOF
SOF
VINL
VINR
1 ms

Figure 38. Record Sequence

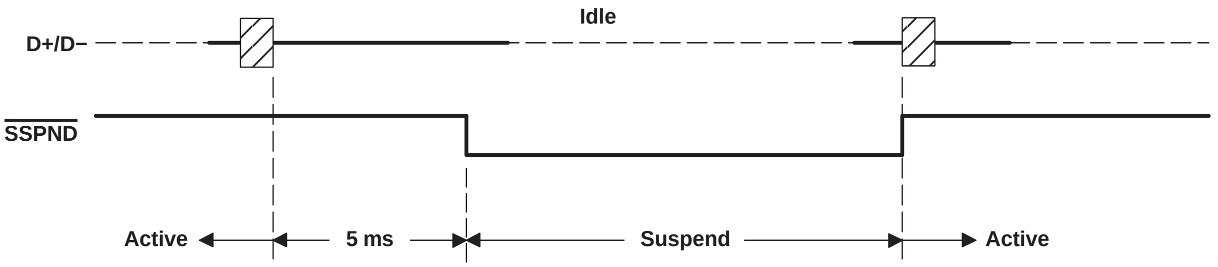
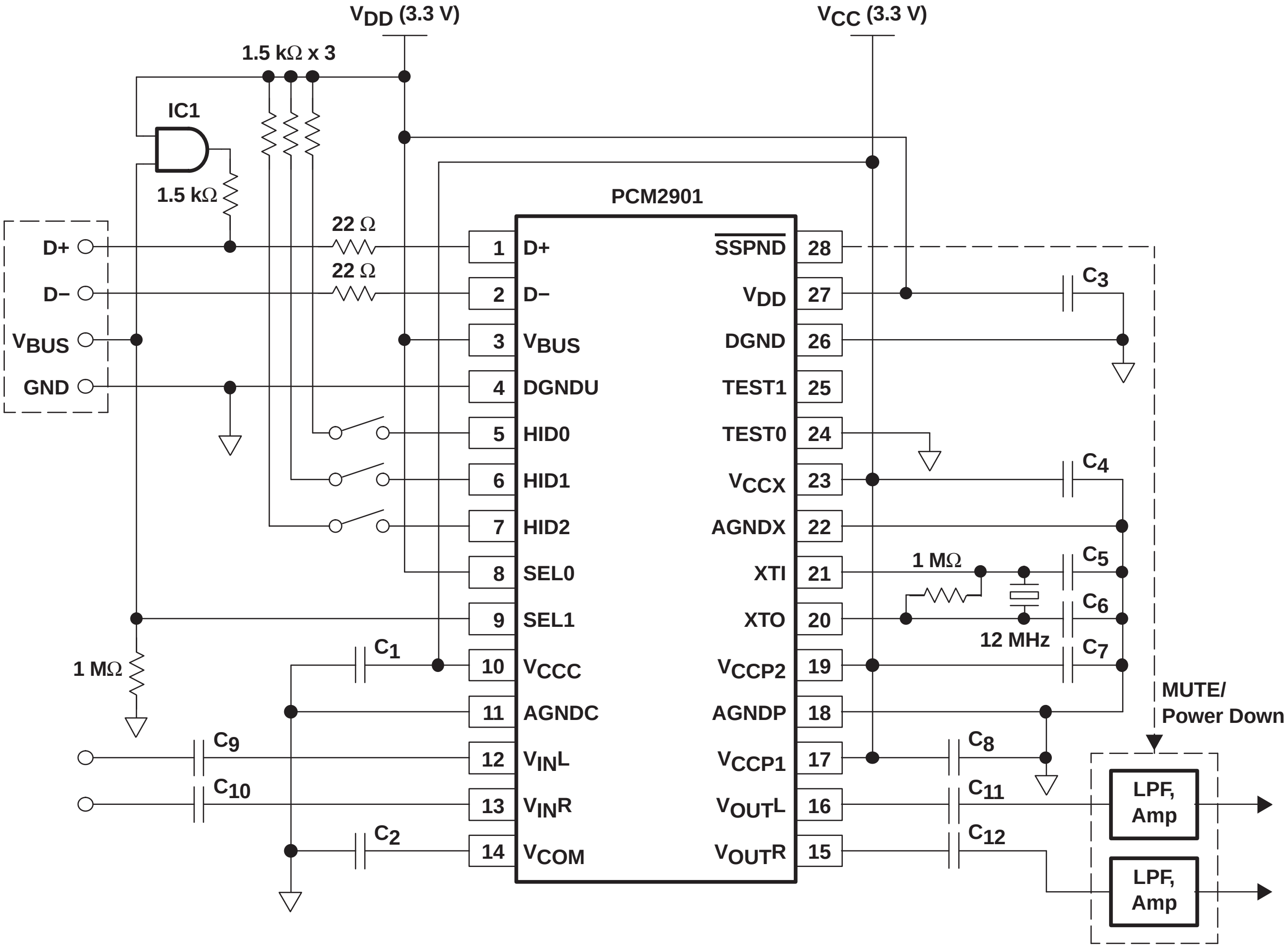

Idle
D+/D−
SSPND
Active
5 ms
Suspend
Active

Figure 39. Suspend and Resume

PCM2901 TYPICAL CIRCUIT CONNECTION

Figure 40 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.


V_{DD} (3.3 V)
V_{CC} (3.3 V)
1.5 kΩ x 3
IC1
1.5 kΩ
PCM2901
22 Ω
22 Ω
D+
D−
V_{BUS}
GND
1 D+
2 D−
3 V_{BUS}
4 DGNDU
5 HID0
6 HID1
7 HID2
8 SEL0
9 SEL1
10 V_{CCC}
11 AGNDC
12 $V_{IN}L$
13 $V_{IN}R$
14 V_{COM}
28 $\overline{SSPND}$
27 V_{DD}
26 DGND
25 TEST1
24 TEST0
23 V_{CCX}
22 AGNDX
21 XTI
20 XTO
19 V_{CCP2}
18 AGNDP
17 V_{CCP1}
16 $V_{OUT}L$
15 $V_{OUT}R$
C_3
C_4
C_5
C_6
C_7
C_8
C_1
C_2
C_9
C_{10}
C_{11}
C_{12}
1 MΩ
1 MΩ
12 MHz
MUTE/ Power Down
LPF, Amp
LPF, Amp

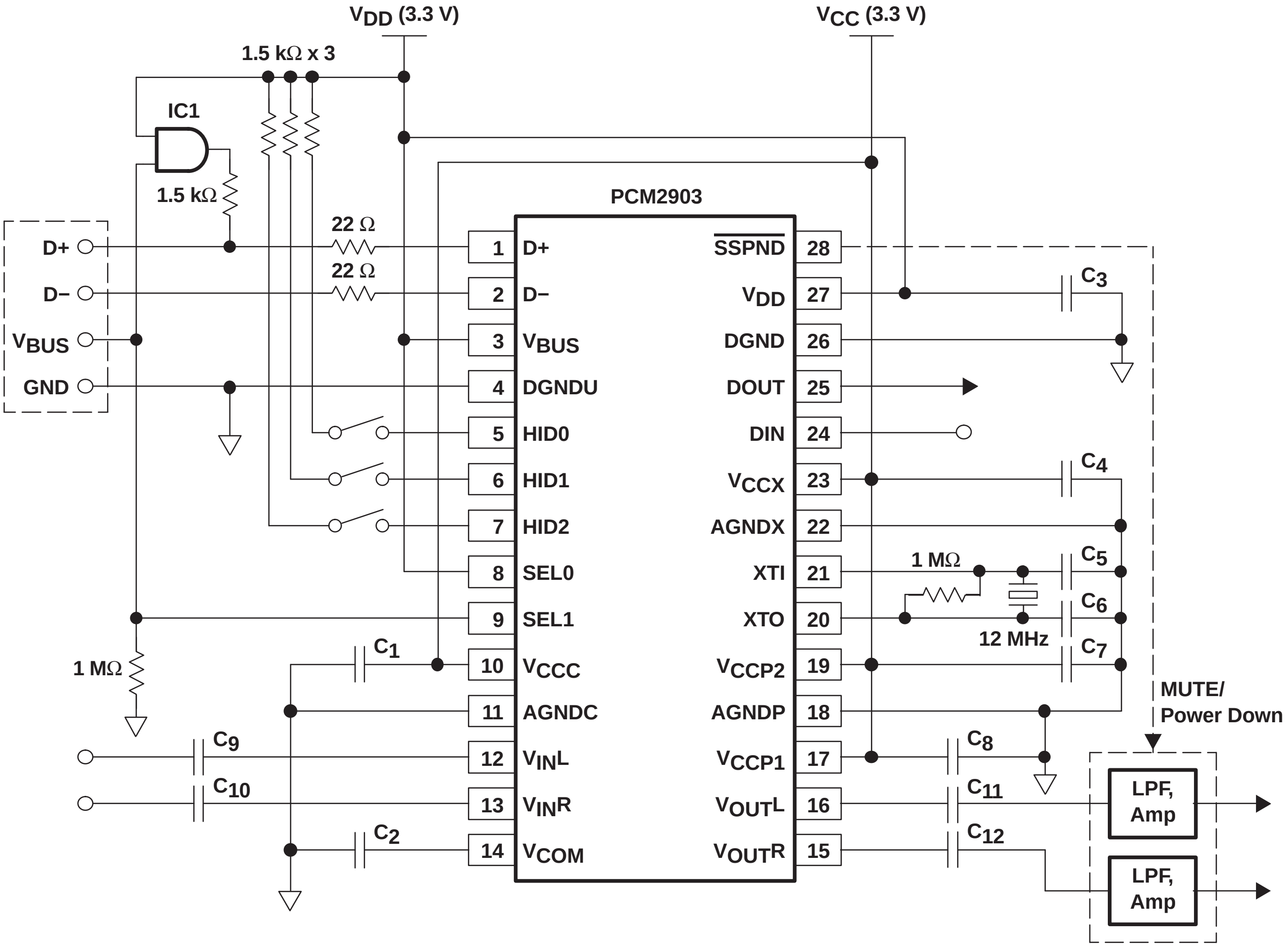
NOTE:

IC1 must be driven by V_{DD} with a 5-V tolerant input.
C_1, C_2, C_3, C_4, C_7, C_8: 10 µF
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.

Figure 40. Self-Powered Configuration

PCM2903 TYPICAL CIRCUIT CONNECTION

Figure 41 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.


VDD (3.3 V)
VCC (3.3 V)
1.5 kΩ x 3
IC1
1.5 kΩ
PCM2903
D+
D−
VBUS
GND
22 Ω
22 Ω
1 D+
2 D−
3 VBUS
4 DGNDU
5 HID0
6 HID1
7 HID2
8 SEL0
9 SEL1
10 VCCC
11 AGNDC
12 VINL
13 VINR
14 VCOM
SSPND 28
VDD 27
DGND 26
DOUT 25
DIN 24
VCCX 23
AGNDX 22
XTI 21
XTO 20
VCCP2 19
AGNDP 18
VCCP1 17
VOUTL 16
VOUTR 15
C3
C4
1 MΩ
C5
C6
12 MHz
C7
MUTE/
Power Down
C8
C11
C12
LPF,
Amp
LPF,
Amp
1 MΩ
C1
C9
C10
C2

NOTE:

IC1 must be driven by V_{DD} with a 5-V tolerant input.
C_1, C_2, C_3, C_4, C_7, C_8: 10 µF
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.

Figure 41. Self-Powered Configuration

APPLICATION INFORMATION

OPERATING ENVIRONMENT

To get the appropriate operation, one of the following operating systems must be working on the host PC that has the USB port assured by the manufacturer. If the condition is fulfilled, the operation of the PCM2901/2903 does not depend on the operating speed of the CPU.

Texas Instruments has confirmed following operating environments.

- Operating System
  - Microsoft™ Windows™ 98/98SE/Me™ Japanese/English Edition
  - Microsoft Windows 2000 Professional Japanese/English Edition
  - Microsoft Windows XP™ Home/Professional Japanese/English Edition (For Windows XP, use the latest version of the USB audio driver that is available on Windows update site)
  - Apple™ Computer Mac™ OS 9.1 or later Japanese/English Edition
  - Apple Computer Mac OS™ X 10.0 or later English Edition
  - Apple Computer Mac OS X 10.1 or later Japanese Edition (For Mac OS X 10.0 Japanese Edition, plug and play does not work for USB audio device appropriately)
- PC: Following PC-AT compatible computers for above OS (OS requirement must be met)
  - Motherboard using Intel™ 440BX or ZX chipset (using USB controller in the chipset)
  - Motherboard using Intel i810 chipset (using USB controller in the chipset)
  - Motherboard using Intel i815 chipset (using USB controller in the chipset)
  - Motherboard using Intel i820 chipset (using USB controller in the chipset)
  - Motherboard using Intel i845 chipset (using USB controller in the chipset)
  - Motherboard using Intel i850 chipset (using USB controller in the chipset)
  - Motherboard using Apollo KT133 chipset (using USB controller in the chipset)
  - Motherboard using Apollo Pro plus chipset (using USB controller in the chipset)
  - Motherboard using MVP4 or MVP3 chipset (using USB controller in the chipset)
  - Motherboard using Aladdin V chipset (using USB controller in the chipset)
  - Motherboard using SiS530 or SiS559 chipset (using USB controller in the chipset)
  - Motherboard using SiS735 chipset (using USB controller in the chipset)

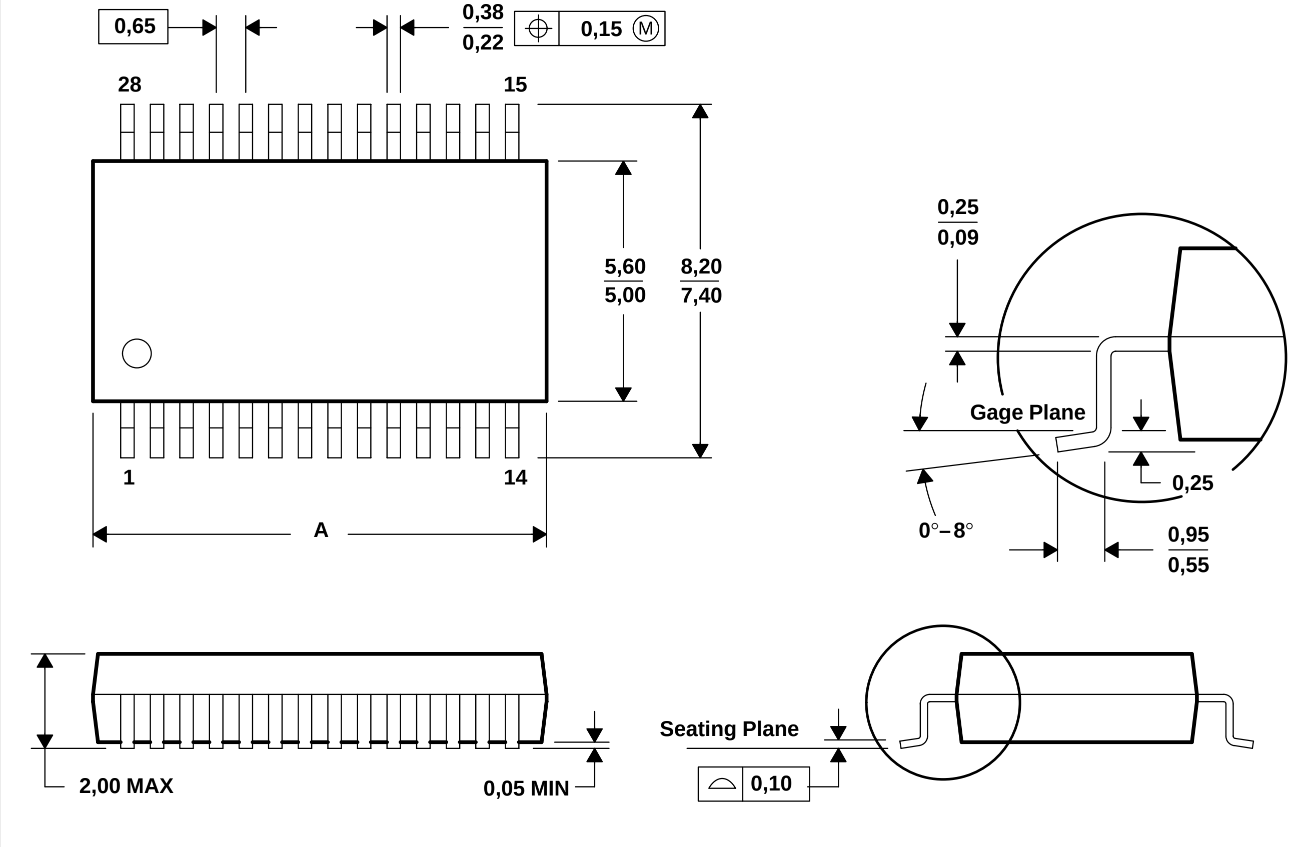
NOTE: The OSs and PCs for which the operation of the PCM2901/2903 was confirmed are listed above. The PCM2901/2903 may also work with other OSs and PCs that have not been tested. Furthermore, there is no assurance that the PCM2901/2903 will work with every PC having a compatible chipset, because other design factors of the motherboard may also cause incompatibility.

The PCM2901/2903 has been acknowledged in the USB compliance test. However, the acknowledgement is just for the PCM2901/2903 from Texas Instruments. Be careful that the acknowledgement is not for the customer’s USB system using the PCM2901/2903.

Intel is a trademark of Intel Corporation.
Microsoft, Windows, Windows Me, and Windows XP are trademarks of Microsoft Corporation.
Apple. Mac, and Mac OS are trademarks of Apple Computer, Inc.

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

28 PINS SHOWN


0,65
0,38
0,22
0,15 M
28
15
1
14
5,60
5,00
8,20
7,40
A
0,25
0,09
Gage Plane
0,25
0°–8°
0,95
0,55
2,00 MAX
0,05 MIN
Seating Plane
0,10

PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated