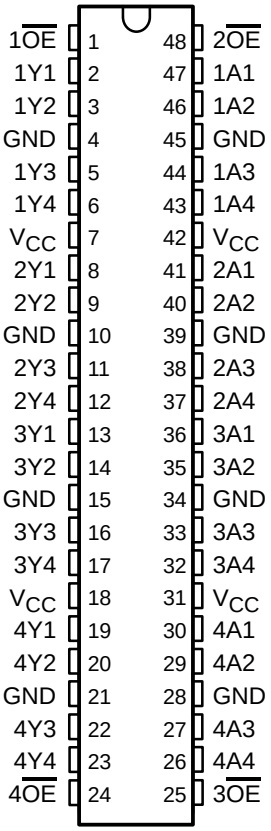
- **Member of the Texas Instruments Widebus™ Family**
- **Optimized for 1.8-V Operation and is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Sub 1-V Operable**
- **Max $t_{pd}$ of 2 ns at 1.8 V**
- **Low Power Consumption, 20-μA Max $I_{CC}$**
- **±8-mA Output Drive at 1.8 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

**DGG OR DGV PACKAGE**
**(TOP VIEW)**




## description/ordering information

This 16-bit buffer/driver is operational at 0.8-V to 2.7-V $V_{CC}$, but is designed specifically for 1.65-V to 1.95-V $V_{CC}$ operation.

The SN74AUC16240 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides inverting outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

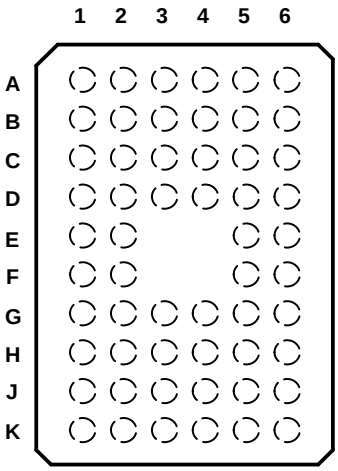
This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | TSSOP – DGG | Tape and reel | SN74AUC16240DGGR | AUC16240 |
| | TVSOP – DGV | Tape and reel | SN74AUC16240DGVR | MH240 |
| | VFBGA – GQL | Tape and reel | SN74AUC16240GQLR | MH240 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**GQL PACKAGE**
**(TOP VIEW)**




## terminal assignments

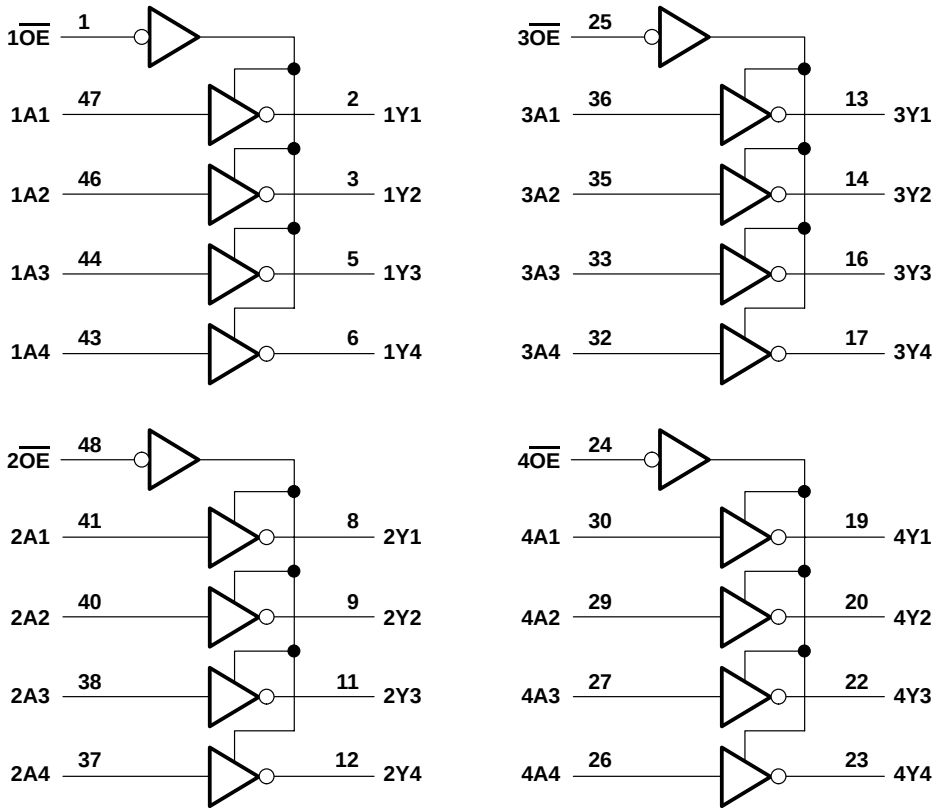
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | $1\overline{OE}$ | NC | NC | NC | NC | $2\overline{OE}$ |
| **B** | 1Y2 | 1Y1 | GND | GND | 1A1 | 1A2 |
| **C** | 1Y4 | 1Y3 | $V_{CC}$ | $V_{CC}$ | 1A3 | 1A4 |
| **D** | 2Y2 | 2Y1 | GND | GND | 2A1 | 2A2 |
| **E** | 2Y4 | 2Y3 | | | 2A3 | 2A4 |
| **F** | 3Y1 | 3Y2 | | | 3A2 | 3A1 |
| **G** | 3Y3 | 3Y4 | GND | GND | 3A4 | 3A3 |
| **H** | 4Y1 | 4Y2 | $V_{CC}$ | $V_{CC}$ | 4A2 | 4A1 |
| **J** | 4Y3 | 4Y4 | GND | GND | 4A4 | 4A3 |
| **K** | $4\overline{OE}$ | NC | NC | NC | NC | $3\overline{OE}$ |

NC – No internal connection

**FUNCTION TABLE**
**(each 4-bit buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

## logic diagram (positive logic)




Pin numbers shown are for the DGG and DGV packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 3.6 V |
| Input voltage range, $V_I$ (see Note 1) | –0.5 V to 3.6 V |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) | –0.5 V to 3.6 V |
| Output voltage range, $V_O$ (see Note 1) | –0.5 V to $V_{CC}$ + 0.5 V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0) | –50 mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0) | –50 mA |
| Continuous output current, $I_O$ | ±20 mA |
| Continuous current through $V_{CC}$ or GND | ±100 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package | 70°C/W |
| DGV package | 58°C/W |
| GQL package | 42°C/W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 0.8 | 2.7 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 0.8 V | $V_{CC}$ | | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | $0.65 \times V_{CC}$ | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 0.8 V | | 0 | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | | $0.35 \times V_{CC}$ | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| $V_I$ | Input voltage | | 0 | 3.6 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 0.8 V | | –0.7 | mA |
| | | $V_{CC}$ = 1.1 V | | –3 | |
| | | $V_{CC}$ = 1.4 V | | –5 | |
| | | $V_{CC}$ = 1.65 V | | –8 | |
| | | $V_{CC}$ = 2.3 V | | –9 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 0.8 V | | 0.7 | mA |
| | | $V_{CC}$ = 1.1 V | | 3 | |
| | | $V_{CC}$ = 1.4 V | | 5 | |
| | | $V_{CC}$ = 1.65 V | | 8 | |
| | | $V_{CC}$ = 2.3 V | | 9 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 0.8 V, 1.3 V | | 20 | ns/V |
| | | $V_{CC}$ = 1.6 V, 1.95 V | | 10 | |
| | | $V_{CC}$ = 2.7 V | | 5 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –100 µA | 0.8 V to 2.7 V | $V_{CC}$–0.1 | | | V |
| | | $I_{OH}$ = –0.7 mA | 0.8 V | | 0.55 | | |
| | | $I_{OH}$ = –3 mA | 1.1 V | 0.8 | | | |
| | | $I_{OH}$ = –5 mA | 1.4 V | 1 | | | |
| | | $I_{OH}$ = –8 mA | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = –9 mA | 2.3 V | 1.8 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 µA | 0.8 V to 2.7 V | | | 0.2 | V |
| | | $I_{OL}$ = 0.7 mA | 0.8 V | | 0.25 | | |
| | | $I_{OL}$ = 3 mA | 1.1 V | | | 0.3 | |
| | | $I_{OL}$ = 5 mA | 1.4 V | | | 0.4 | |
| | | $I_{OL}$ = 8 mA | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 9 mA | 2.3 V | | | 0.6 | |
| $I_I$ | A or $\overline{OE}$ inputs | $V_I = V_{CC}$ or GND | 0 to 2.7 V | | | ±5 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 2.7 V | 0 | | | ±10 | µA |
| $I_{OZ}$ | | $V_O = V_{CC}$ or GND | 2.7 V | | | ±10 | µA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 0.8 V to 2.7 V | | | 20 | µA |
| $C_i$ | | $V_I = V_{CC}$ or GND | 2.5 V | | 3 | 4 | pF |
| $C_o$ | | $V_O = V_{CC}$ or GND | 2.5 V | | 5.5 | 6 | pF |

† All typical values are at $T_A$ = 25°C.

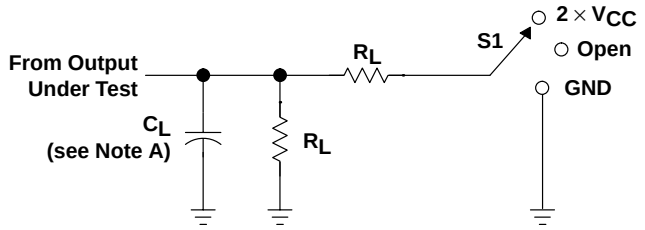
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V ± 0.1 V | | $V_{CC}$ = 1.5 V ± 0.1 V | | $V_{CC}$ = 1.8 V ± 0.15 V | | | $V_{CC}$ = 2.5 V ± 0.2 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 5.9 | 0.9 | 2.6 | 0.7 | 1.8 | 0.6 | 1.4 | 2 | 0.4 | 1.6 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | 7.9 | 1.2 | 3.8 | 0.8 | 2.5 | 0.7 | 1.5 | 2.5 | 0.7 | 2 | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | 9.3 | 2.1 | 6 | 1.5 | 4.8 | 1.8 | 2.7 | 4.5 | 0.6 | 2.3 | ns |

## operating characteristics, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V | $V_{CC}$ = 1.5 V | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | f = 10 MHz | 24 | 24 | 25 | 26 | 30 | pF |
| | | Outputs disabled | | 2 | 2 | 2 | 3 | 4 | |

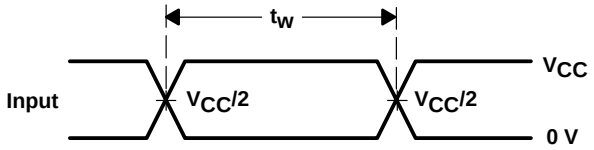
## PARAMETER MEASUREMENT INFORMATION



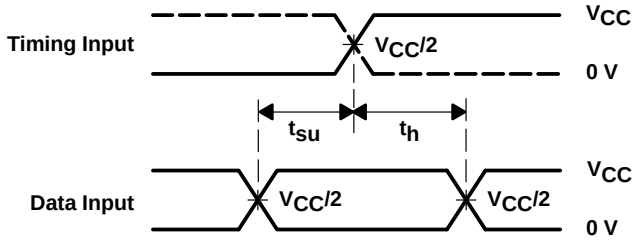

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

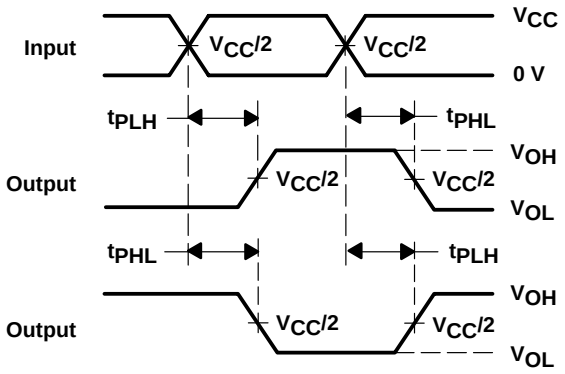
| $V_{CC}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|
| 0.8 V | 15 pF | 2 kΩ | 0.1 V |
| 1.2 V ± 0.1 V | 15 pF | 2 kΩ | 0.1 V |
| 1.5 V ± 0.1 V | 15 pF | 2 kΩ | 0.1 V |
| 1.8 V ± 0.15 V | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | 30 pF | 500 Ω | 0.15 V |



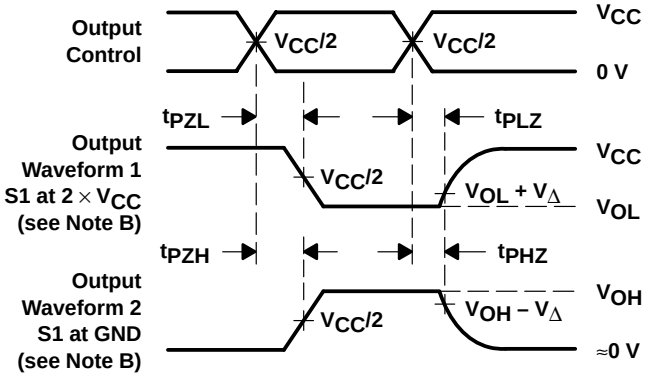

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

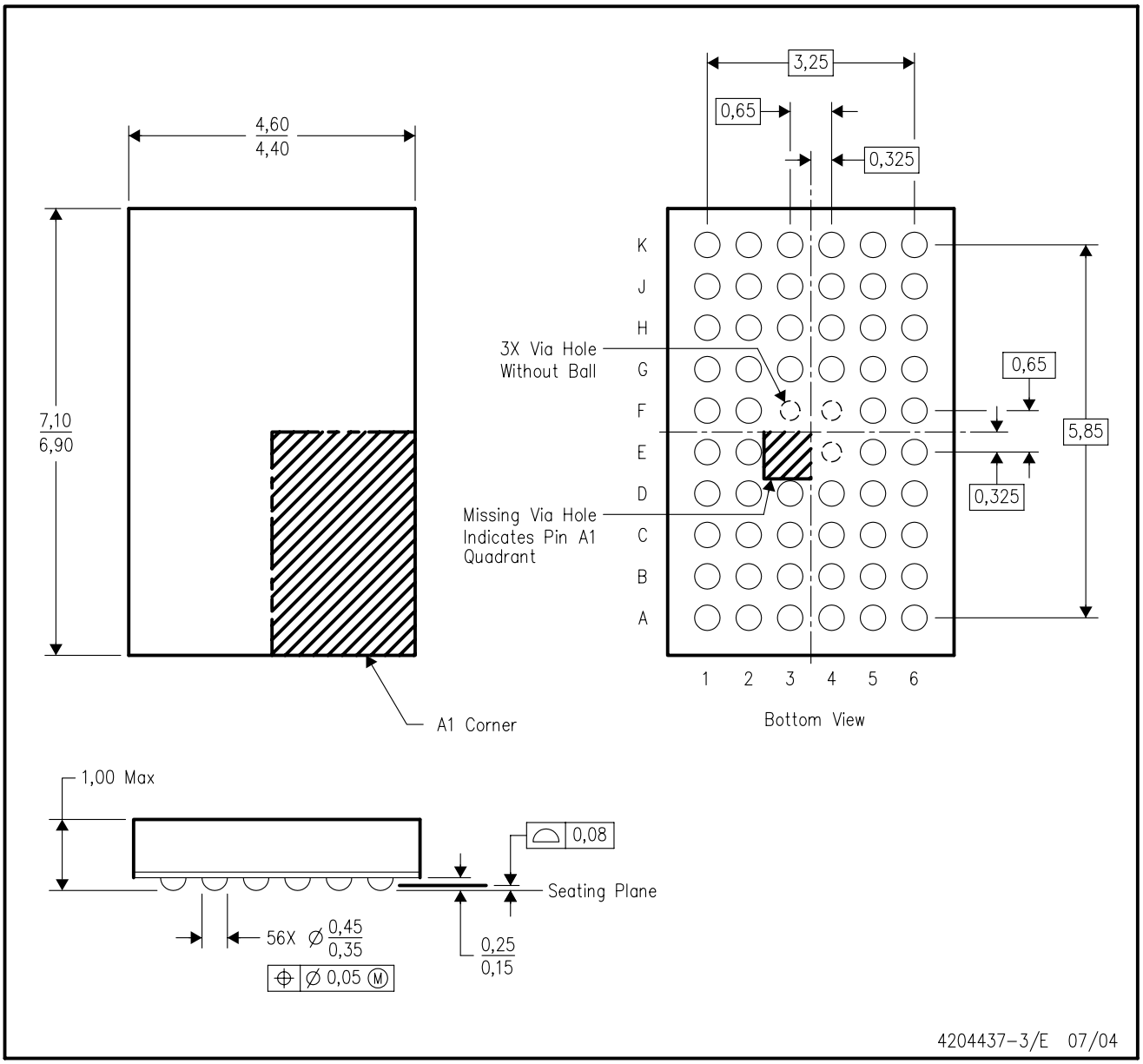



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

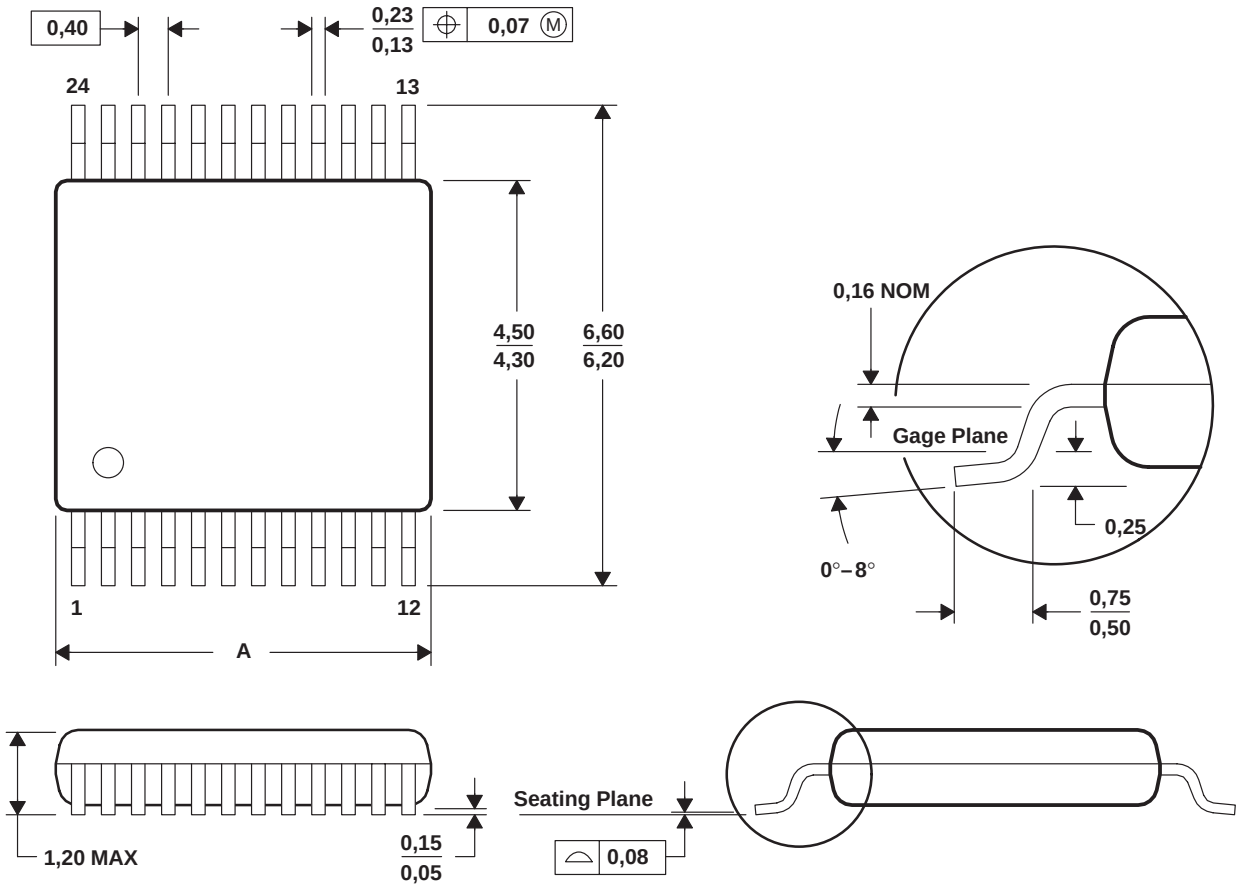
## ZQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BA.
D. This package is lead–free. Refer to the 56 GQL package (drawing 4200583) for tin–lead (SnPb).

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

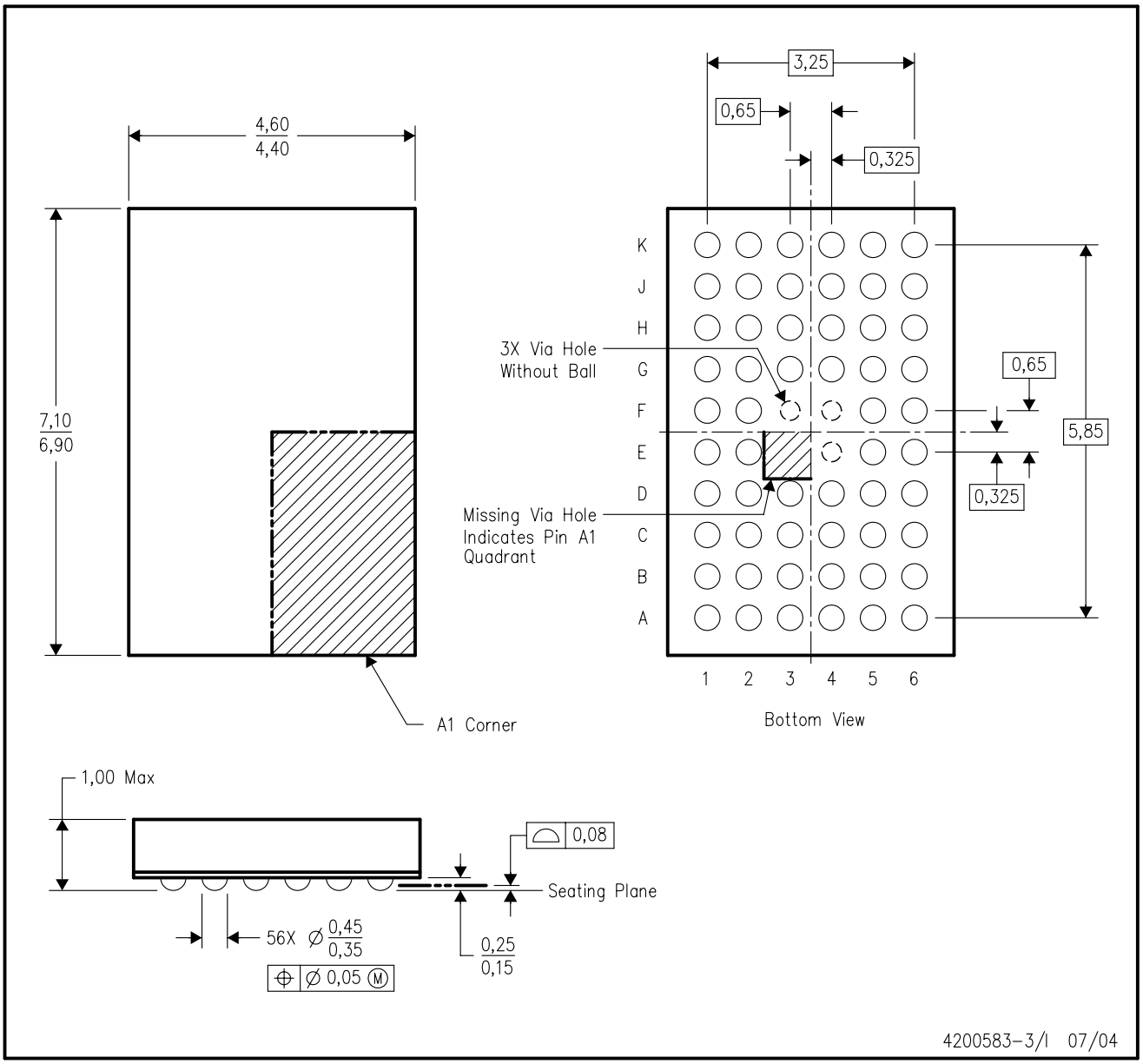



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

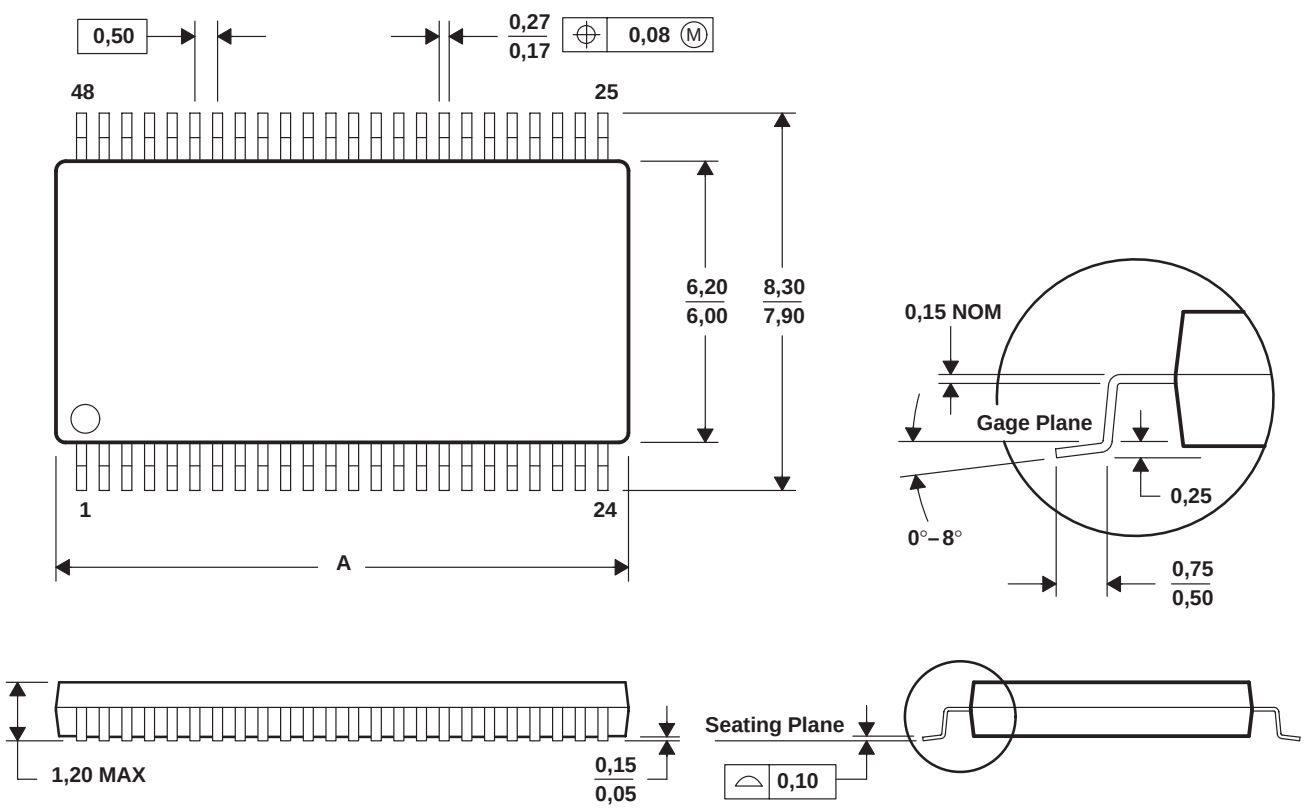
## GQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BA.
D. This package is tin–lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead–free.

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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