Burr-Brown Products
from Texas Instruments

MSC1200

SBAS289E – JUNE 2003 – REVISED NOVEMBER 2004

Precision Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) with 8051 Microcontroller and Flash Memory

FEATURES

ANALOG FEATURES

- 24-BITS NO MISSING CODES
- 22-BITS EFFECTIVE RESOLUTION AT 10Hz
  Low Noise: 75nV
- PGA FROM 1 TO 128
- PRECISION ON-CHIP VOLTAGE REFERENCE
- 8 DIFFERENTIAL/SINGLE-ENDED CHANNELS
- ON-CHIP OFFSET/GAIN CALIBRATION
- OFFSET DRIFT: 0.02ppm/°C
- GAIN DRIFT: 0.5ppm/°C
- ON-CHIP TEMPERATURE SENSOR
- SELECTABLE BUFFER INPUT
- BURNOUT DETECT
- 8-BIT CURRENT DAC

DIGITAL FEATURES

Microcontroller Core

- 8051-COMPATIBLE
- HIGH-SPEED CORE:
  4 Clocks per Instruction Cycle
- DC TO 33MHz
- ON-CHIP OSCILLATOR
- PLL WITH 32kHz CAPABILITY
- SINGLE INSTRUCTION 121ns
- DUAL DATA POINTER

Memory

- 4kB OR 8kB OF FLASH MEMORY
- FLASH MEMORY PARTITIONING
- ENDURANCE 1M ERASE/WRITE CYCLES,
  100 YEAR DATA RETENTION
- 128 BYTES DATA SRAM
- IN-SYSTEM SERIALLY PROGRAMMABLE
- FLASH MEMORY SECURITY
- 1kB BOOT ROM

Peripheral Features

- 16 DIGITAL I/O PINS
- ADDITIONAL 32-BIT ACCUMULATOR
- TWO 16-BIT TIMER/COUNTERS
- SYSTEM TIMERS
- PROGRAMMABLE WATCHDOG TIMER
- FULL DUPLEX USART
- BASIC SPI™
- BASIC I²C™
- POWER MANAGEMENT CONTROL
- INTERNAL CLOCK DIVIDER
- IDLE MODE CURRENT < 200µA
- STOP MODE CURRENT < 100nA
- DIGITAL BROWNOUT RESET
- ANALOG LOW VOLTAGE DETECT
- 20 INTERRUPT SOURCES

GENERAL FEATURES

- PACKAGE: TQFP-48
- LOW POWER: 3mW
- INDUSTRIAL TEMPERATURE RANGE:
  –40°C to +85°C
- POWER SUPPLY: 2.7V to 5.25V

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- INSTRUMENTATION
- LIQUID/GAS CHROMATOGRAPHY
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS
- WEIGH SCALES
- PRESSURE TRANSDUCERS
- INTELLIGENT SENSORS
- PORTABLE APPLICATIONS
- DAS SYSTEMS

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	FLASH MEMORY	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
MSC1200Y2	4k	TQFP-48	PFB	–40°C to +85°C	MSC1200Y2
MSC1200Y2	4k	"	"	"	"
MSC1200Y3	8k	TQFP-48	PFB	–40°C to +85°C	MSC1200Y3
MSC1200Y3	8k	"	"	"	"

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or refer to our web site at www.ti.com/msc.

ABSOLUTE MAXIMUM RATINGS(1)

Analog Inputs
- Input Current .... 100mA, Momentary
- Input Current .... 10mA, Continuous
- Input Voltage .... AGND – 0.3V to AV_{DD} + 0.3V

Power Supply
- DV_{DD} to DGND .... –0.3V to 6V
- AV_{DD} to AGND .... –0.3V to 6V
- AGND to DGND .... –0.3V to +0.3V
- V_{REF} to AGND .... –0.3V to AV_{DD} + 0.3V
- Digital Input Voltage to DGND .... –0.3V to DV_{DD} + 0.3V
- Digital Output Voltage to DGND .... –0.3V to DV_{DD} + 0.3V
- Maximum Junction Temperature .... +150°C
- Operating Temperature Range .... –40°C to +85°C
- Storage Temperature Range .... –65°C to +150°C
- Lead Temperature (soldering, 10s) .... +235°C
- Package Power Dissipation .... $(T_J$ Max – $T_{AMBIENT})/\theta_{JA}$
- Output Current All Pins 200mA
- Output Pin Short Circuit 10s
- Thermal Resistance, Junction-to-Ambient (θ_{JA}) .... 56.5°C/W
- Thermal Resistance, Junction-to-Case (θ_{JC}) .... 12.8°C/W

Digital Outputs
- Output Current .... 100mA, Continuous
- I/O Source/Sink Current 100mA
- Power Pin Maximum 300mA

NOTE: (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

MSC1200Yx FAMILY FEATURES

FEATURES(1)	MSC1200Y2(2)	MSC1200Y3(2)
Flash Program Memory (Bytes)	Up to 4k	Up to 8k
Flash Data Memory (Bytes)	Up to 2k	Up to 4k
Internal Scratchpad RAM (Bytes)	128	128

NOTES: (1) All peripheral features are the same on all devices; the flash memory size is the only difference. (2) The last digit of the part number (N) represents the onboard flash size = (2^N)kBytes.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, Bipolar, and V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise noted.

PARAMETER	CONDITION	MSC1200Yx MIN	TYP	MAX	UNITS
ANALOG INPUT (AIN0-AIN7, AINCOM)					
Analog Input Range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 50mV		AV_{DD} – 1.5	V
Full-Scale Input Voltage Range	(In+) – (In–)			$\pm V_{REF}$/PGA	V
Differential Input Impedance	Buffer OFF		7/PGA		MΩ
Input Current	Buffer ON		0.5		nA
Bandwidth					
Fast Settling Filter	–3dB		0.469 • f_{DATA}		
$Sinc^2$ Filter	–3dB		0.318 • f_{DATA}		
$Sinc^3$ Filter	–3dB		0.262 • f_{DATA}		
Programmable Gain Amplifier	User-Selectable Gain Ranges	1		128	
Input Capacitance	Buffer ON		7		pF
Input Leakage Current	Multiplexer Channel Off, T = +25°C		0.5		pA
Burnout Current Sources	Buffer ON		±2		µA
ADC OFFSET DAC					
Offset DAC Range			$\pm V_{REF}$/(2 • PGA)		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±1.0		% of Range
Offset DAC Gain Error Drift			0.6		ppm/°C

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V (Cont.)

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, Bipolar, and V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise noted.

PARAMETER	CONDITION	MSC1200Yx MIN	MSC1200Yx TYP	MSC1200Yx MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		24			Bits
ENOB			22		Bits
Output Noise		See Typical Characteristics			
No Missing Codes	$Sinc^3$ Filter	24			Bits
Integral Nonlinearity	End Point Fit, Differential Input		±0.0004	±0.0015	%FSR
Offset Error	After Calibration		1.5		ppm of FS
Offset Drift(1)	Before Calibration		0.02		ppm of FS/°C
Gain Error(2)	After Calibration		0.005		%
Gain Error Drift(1)	Before Calibration		0.5		ppm/°C
System Gain Calibration Range		80		120	% of FS
System Offset Calibration Range		–50		50	% of FS
Common-Mode Rejection	At DC	100	120		dB
	f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
	f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Power-Supply Rejection	At DC, dB = $-20\log(\Delta V_{OUT}/\Delta V_{DD})$(3)		100		dB
VOLTAGE REFERENCE INPUTS					
Reference Input Range	REF IN+, REF IN–	AGND		AV_{DD}(2)	V
V_{REF}	V_{REF} ≡ (REF IN+) – (REF IN–)	0.3	2.5	AV_{DD}	V
Common-Mode Rejection	At DC		115		dB
Input Current	V_{REF} = 2.5V, PGA = 1		1		µA
ON-CHIP VOLTAGE REFERENCE					
Output Voltage	VREFH = 1 at +25°C		2.5		V
	VREFH = 0		1.25		V
Short-Circuit Current Source			9		mA
Short-Circuit Current Sink			10		mA
Short-Circuit Duration	Sink or Source		Indefinite		
Startup Time from Power ON			0.4		ms
Temperature Sensor					
Temperature Sensor Voltage	T = +25°C		115		mV
Temperature Sensor Coefficient			375		µV/°C
IDAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current			1		mA
Maximum Short-Circuit Current Duration			Indefinite		
Compliance Voltage			AV_{DD} – 1.5		V
ANALOG POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	AV_{DD}	4.75	5.0	5.25	V
Analog Current	Analog OFF, ALVD OFF, PDADC = PDIDAC = 1		< 1		nA
ADC Current I_{ADC}	PGA = 1, Buffer OFF		170		µA
	PGA = 128, Buffer OFF		430		µA
	PGA = 1, Buffer ON		230		µA
	PGA = 128, Buffer ON		770		µA
V_{REF} Supply Current I_{VREF}	ADC ON		360		µA
I_{DAC} Supply Current I_{IDAC}	IDAC = 00_H		230		µA

NOTES: (1) Calibration can minimize these errors. (2) The gain calibration cannot have a REF IN+ of more than AV_{DD} – 1.5V with buffer ON. To calibrate gain, turn buffer off. (3) DV_{OUT} is change in digital result.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V

All specifications from T_{MIN} to T_{MAX}, AV_{DD} = +3V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, Bipolar, and V_{REF} ≡ (REF IN+) – (REF IN–) = +1.25V, unless otherwise noted.

		MSC1200Yx			
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
ANALOG INPUT (AIN0-AIN7, AINCOM)					
Analog Input Range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 50mV		AV_{DD} – 1.5	V
Full-Scale Input Voltage Range	(In+) – (In–)			$\pm V_{REF}$/PGA	V
Differential Input Impedance	Buffer OFF		7/PGA		MΩ
Input Current	Buffer ON		0.5		nA
Bandwidth					
Fast Settling Filter	–3dB		0.469 • f_{DATA}		
$Sinc^2$ Filter	–3dB		0.318 • f_{DATA}		
$Sinc^3$ Filter	–3dB		0.262 • f_{DATA}		
Programmable Gain Amplifier	User-Selectable Gain Ranges	1		128	
Input Capacitance	Buffer On		7		pF
Input Leakage Current	Multiplexer Channel Off, T = +25°C		0.5		pA
Burnout Current Sources	Buffer ON		±2		µA
ADC OFFSET DAC					
Offset DAC Range			$\pm V_{REF}$/(2 • PGA)		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±1.5		% of Range
Offset DAC Gain Error Drift			0.6		ppm/°C
SYSTEM PERFORMANCE					
Resolution		24			Bits
ENOB			22		Bits
Output Noise			See Typical Characteristics		
No Missing Codes	$Sinc^3$ Filter	24			Bits
Integral Nonlinearity	End Point Fit, Differential Input		±0.0004	±0.0015	%FSR
Offset Error	After Calibration		1.3		ppm of FS
Offset Drift(1)	Before Calibration		0.02		ppm of FS/°C
Gain Error(2)	After Calibration		0.005		%
Gain Error Drift(1)	Before Calibration		0.5		ppm/°C
System Gain Calibration Range		80		120	% of FS
System Offset Calibration Range		–50		50	% of FS
Common-Mode Rejection	At DC	100	130		dB
	f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
	f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Power-Supply Rejection	At DC, dB = –20log(DV_{OUT}/DV_{DD})(3)		88		dB
VOLTAGE REFERENCE INPUTS					
Reference Input Range	REF IN+, REF IN–	AGND		AV_{DD}(2)	V
V_{REF}	V_{REF} ≡ (REF IN+) – (REF IN–)	0.3	1.25	AV_{DD}	V
Common-Mode Rejection	At DC		110		dB
Input Current	V_{REF} = 1.25V, PGA = 1		0.5		µA
ON-CHIP VOLTAGE REFERENCE					
Output Voltage	VREFH = 0 at +25°C		1.25		V
Short-Circuit Current Source			4		mA
Short-Circuit Current Sink			5		µA
Short-Circuit Duration	Sink or Source		Indefinite		
Startup Time from Power ON			0.2		ms
Temperature Sensor					
Temperature Sensor Voltage	T = +25°C		115		mV
Temperature Sensor Coefficient			375		µV/°C
IDAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current			1		mA
Maximum Short-Circuit Current Duration			Indefinite		
Compliance Voltage			AV_{DD} – 1.5		V
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	AV_{DD}	2.7	3.0	3.6	V
Analog Current	Analog OFF, ALVD OFF, PDADC = PDIDAC = 1		< 1		nA
ADC Current I_{ADC}	PGA = 1, Buffer OFF		150		µA
	PGA = 128, Buffer OFF		380		µA
	PGA = 1, Buffer ON		200		µA
	PGA = 128, Buffer ON		610		µA
V_{REF} Supply Current I_{VREF}	ADC ON		330		µA
I_{DAC} Supply Current I_{IDAC}	IDAC = 00_H		220		µA

NOTES: (1) Calibration can minimize these errors. (2) The gain calibration cannot have a REF IN+ of more than AV_{DD} – 1.5V with buffer ON. To calibrate gain, turn buffer off. (3) DV_{OUT} is change in digital result.

DIGITAL CHARACTERISTICS: DV_{DD} = 2.7V to 5.25V

All specifications from T_{MIN} to T_{MAX}, unless otherwise specified.

		MSC1200Yx			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER-SUPPLY REQUIREMENTS					
Digital Supply Current	DV_{DD}	2.7	3.0	3.6	V
	Normal Mode, f_{OSC} = 1MHz		0.6		mA
	Normal Mode, f_{OSC} = 8MHz, All Peripherals ON		5		mA
	Internal Oscillator LF Mode (12.8MHz nominal)		7.1		mA
	Stop Mode, DBOR OFF		100		nA
	DV_{DD}	4.75	5.0	5.25	V
	Normal Mode, f_{OSC} = 1MHz		1.2		mA
	Normal Mode, f_{OSC} = 8MHz, All Peripherals ON		9		mA
	Internal Oscillator LF Mode (12.8MHz nominal)		15		mA
	Internal Oscillator HF Mode (25.6MHz nominal)		29		mA
	Stop Mode, DBOR OFF		100		nA
DIGITAL INPUT/OUTPUT (CMOS)					
Logic Level: V_{IH} (except XIN pin)		0.6 • DV_{DD}		DV_{DD}	V
V_{IL} (except XIN pin)		DGND		0.2 • DV_{DD}	V
Ports 1 and 3, Input Leakage Current, Input Mode	$V_{IH} = DV_{DD}$ or V_{IH} = 0V		0		µA
Pin XIN Input Leakage Current			0		µA
I/O Pin Hysteresis			700		mV
V_{OL}, Ports 1 and 3, All Output Modes	I_{OL} = 1mA	DGND		0.4	V
V_{OL}, Ports 1 and 3, All Output Modes	I_{OL} = 30mA, 3V (20mA)		1.5		V
V_{OH}, Ports 1 and 3, Strong Drive Output	I_{OH} = 1mA	DV_{DD} – 0.4	DV_{DD} – 0.1	DV_{DD}	V
V_{OH}, Ports 1 and 3, Strong Drive Output	I_{OH} = 30mA, 3V (20mA)		DV_{DD} – 1.5		V
Ports 1 and 3 Pull-Up Resistors			11		kΩ

FLASH MEMORY CHARACTERISTICS: DV_{DD} = 2.7V to 5.25V

t_{USEC} = 1µs, t_{MSEC} = 1ms

		MSC1200Yx			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNITS**
Flash Memory Endurance		100,000	1,000,000		cycles
Flash Memory Data Retention		100			Years
Mass and Page Erase Time	Set with FER Value in FTCON	10			ms
Flash Memory Write Time	Set with FWR Value in FTCON	30		40	µs

AC ELECTRICAL CHARACTERISTICS[1]: DV_{DD} = 2.7V to 5.25V

PARAMETER	CONDITION	MSC1200Yx MIN	TYP	MAX	UNITS
PHASE LOCK LOOP (PLL)					
Input Frequency Range	External Crystal/Clock Frequency (f_{OSC})		32.768		kHz
PLL LF Mode	PLLDIV = 449 (default)		14.7456		MHz
PLL HF Mode	PLLDIV = 899 (must be set by user)		29.4912		MHz
PLL Lock Time	Within 1%			2	ms
INTERNAL OSCILLATOR (IO)	See Typical Characteristics				
IO LF Mode			12.8		MHz
IO HF Mode			25.6		MHz
Internal Oscillator Settling Time	Within 1%			1	ms

NOTE: (1) Parameters are valid over operating temperature range, unless otherwise specified.

EXTERNAL CLOCK DRIVE CLK TIMING

SYMBOL	FIGURE	PARAMETER	2.7V to 3.6V MIN	2.7V to 3.6V MAX	4.75V to 5.25V MIN	4.75V to 5.25V MAX	UNITS
External Clock Mode							
f_{OSC}[1]	A	External Crystal Frequency (f_{OSC})	1	20	1	33	MHz
$1/t_{OSC}$[1]	A	External Clock Frequency (f_{OSC})	0	20	0	33	MHz
f_{OSC}[1]	A	External Ceramic Resonator Frequency (f_{OSC})	1	12	1	12	MHz
t_{HIGH}	A	HIGH Time[2]	15		10		ns
t_{LOW}	A	LOW Time[2]	15		10		ns
t_R	A	Rise Time[2]		5		5	ns
t_F	A	Fall Time[2]		5		5	ns

NOTES: (1) $t_{CLK} = 1/f_{OSC}$ = one oscillator clock period for clock divider = 1. (2) These values are characterized but not 100% production tested.

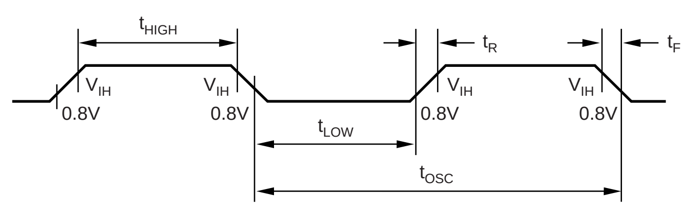


FIGURE A. External Clock Drive CLK.

SERIAL FLASH PROGRAMMING TIMING

SYMBOL	FIGURE	PARAMETER	MIN	MAX	UNIT
t_{RW}	B	RST width	2 t_{OSC}	—	ns
t_{RRD}	B	RST rise to P1.0 internal pull high	—	5	µs
t_{RFD}	B	RST falling to CPU start	—	18	ms
t_{RS}	B	Input signal to RST falling setup time	t_{OSC}	—	ns
t_{RH}	B	RST falling to P1.0 hold time	18	—	ms

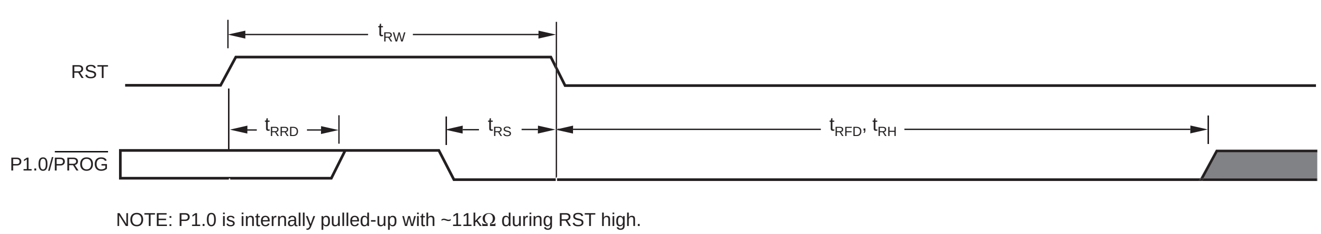
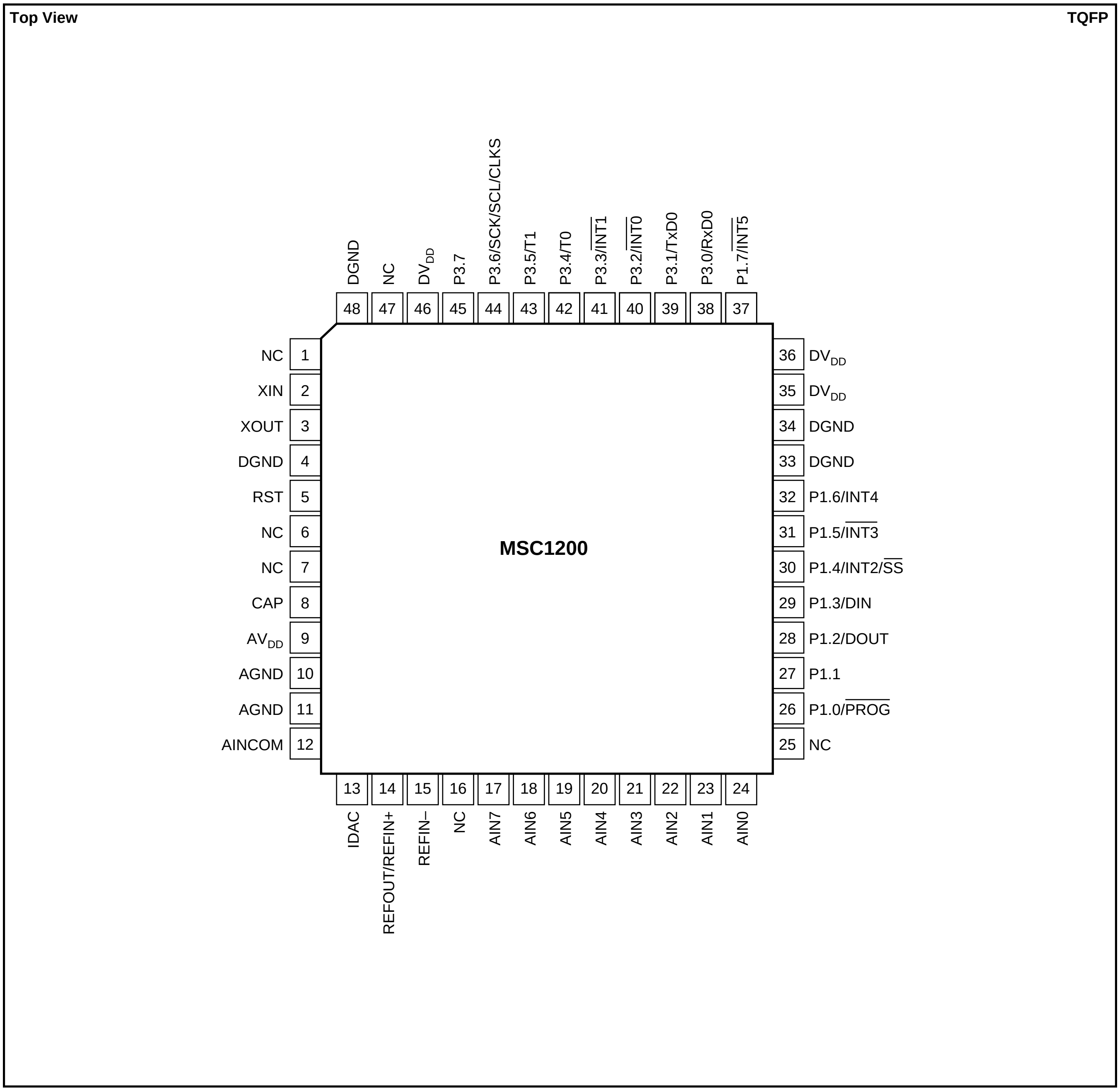


FIGURE B. Serial Flash Programming Power-On Timing.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1,6,7,16,25,47	NC	No Connection
2	XIN	The crystal oscillator pin XIN supports parallel resonant AT cut fundamental frequency crystals and ceramic resonators. XIN can also be an input if there is an external clock source instead of a crystal.
3	XOUT	The crystal oscillator pin XOUT supports parallel resonant AT cut fundamental frequency crystals and ceramic resonators. XOUT serves as the output of the crystal amplifier.
4, 33, 34, 48	DGND	Digital Ground
5	RST	A HIGH on the reset input for two t_{OSC} periods will reset the device.
8	CAP	Capacitor (220pF ceramic)
9	AV_{DD}	Analog Power Supply
10, 11	AGND	Analog Ground
12	AINCOM	Analog Input (can be analog common for single-ended inputs or analog input for differential inputs)
13	IDAC	IDAC Output
14	REFOUT/REF IN+	Internal Voltage Reference Output/Voltage Reference Positive Input
15	REF IN–	Voltage Reference Negative Input (tie to AGND for internal voltage reference)
17	AIN7	Analog Input Channel 7
18	AIN6	Analog Input Channel 6
19	AIN5	Analog Input Channel 5
20	AIN4	Analog Input Channel 4
21	AIN3	Analog Input Channel 3
22	AIN2	Analog Input Channel 2
23	AIN1	Analog Input Channel 1
24	AIN0	Analog Input Channel 0
26-32, 37	P1.0-P1.7	Port 1 is a bidirectional I/O port (refer to P1DDRL, SFR AE_H, and P1DDRH, SFR AF_H, for port pin configuration control). Port 1—Alternate Functions:

PORT	ALTERNATE	MODE
P1.0	$\overline{PROG}$	Serial Programming Mode
P1.1	N/A	
P1.2	DOUT	Serial Data Out
P1.3	DIN	Serial Data In
P1.4	INT2/$\overline{SS}$	External Interrupt 2/Slave Select
P1.5	$\overline{INT3}$	External Interrupt 3
P1.6	INT4	External Interrupt 4
P1.7	$\overline{INT5}$	External Interrupt 5

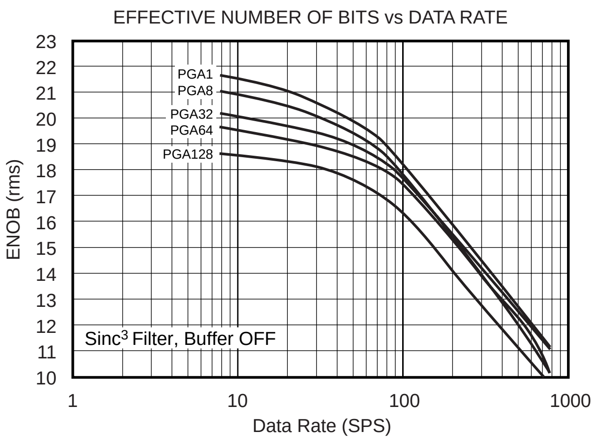
PIN #	NAME	DESCRIPTION
38-45	P3.0-P3.7	Port 3 is a bidirectional I/O port (refer to P3DDRL, SFR $B3_H$, and P3DDRH, SFR $B4_H$, for port pin configuration control). Port 3—Alternate Functions:

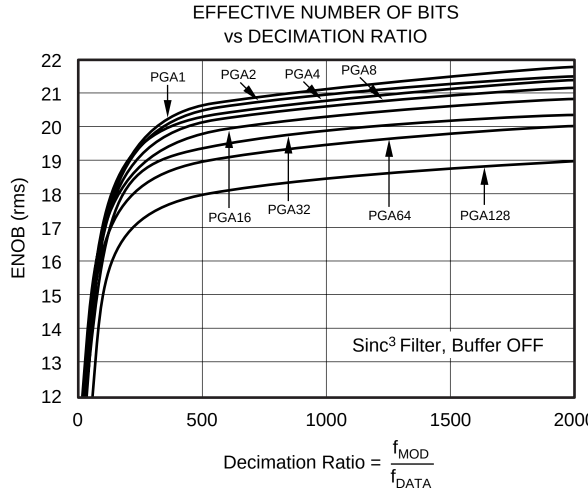
PORT	ALTERNATE	MODE
P3.0	RxD0	Serial Port 0 Input
P3.1	TxD0	Serial Port 0 Output
P3.2	$\overline{INT0}$	External Interrupt 0
P3.3	$\overline{INT1}$	External Interrupt 1
P3.4	T0	Timer 0 External Input
P3.5	T1	Timer 1 External Input
P3.6	SCK/SCL/CLKS	SCK/SCL/Various Clocks (refer to PASEL, SFR $F2_H$)
P3.7	N/A	

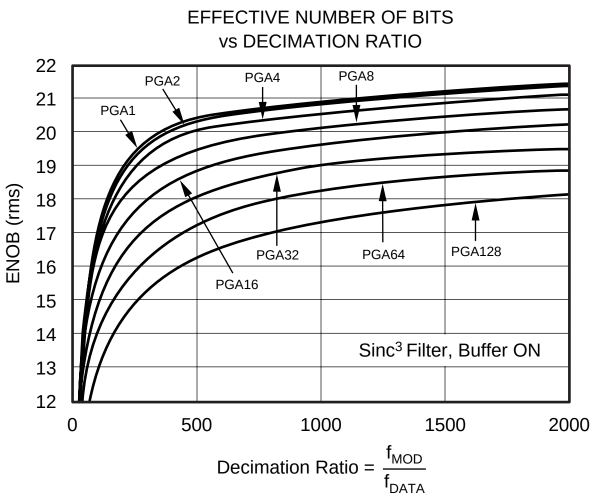
PIN #	NAME	DESCRIPTION
35, 36, 46	DV_{DD}	Digital Power Supply

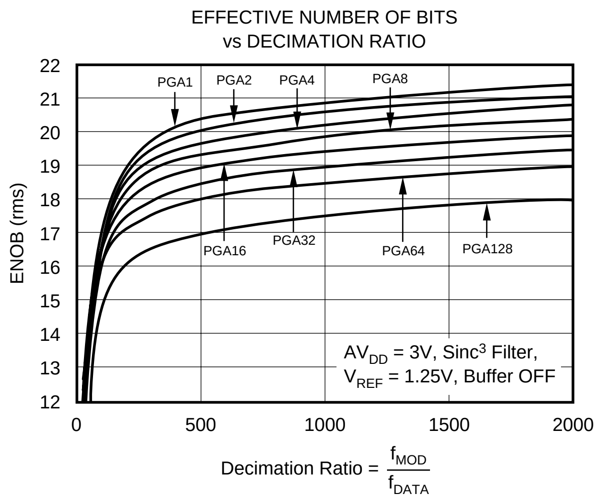
TYPICAL CHARACTERISTICS

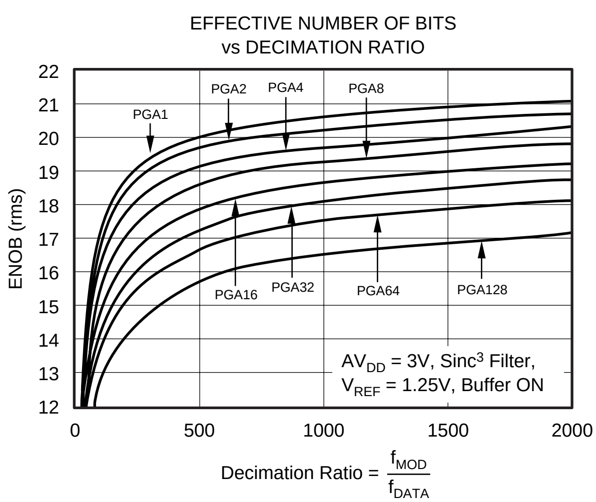
AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, Buffer ON, and V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

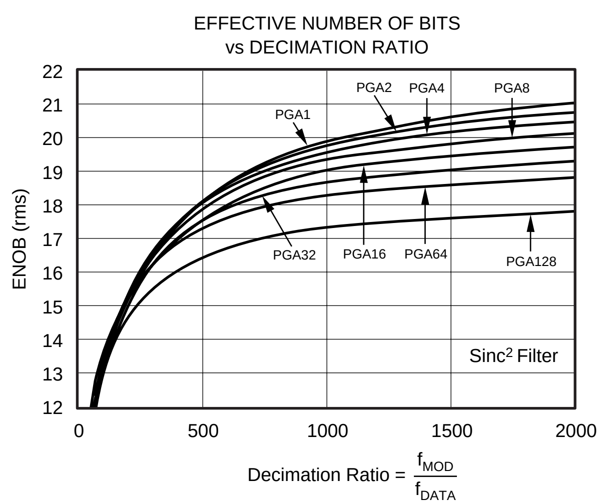






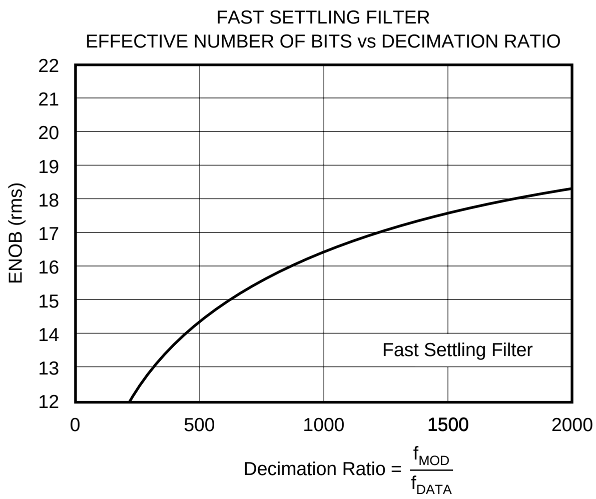


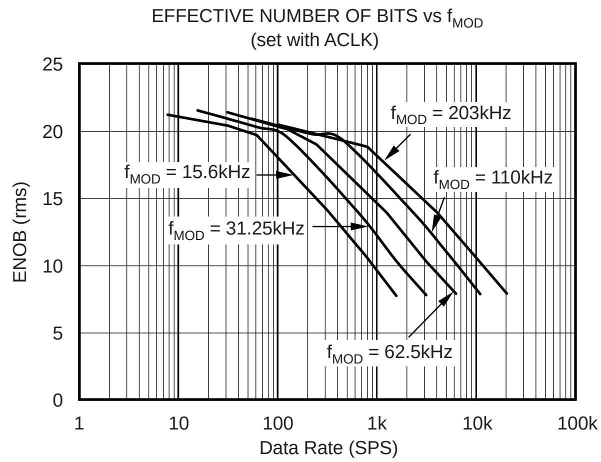


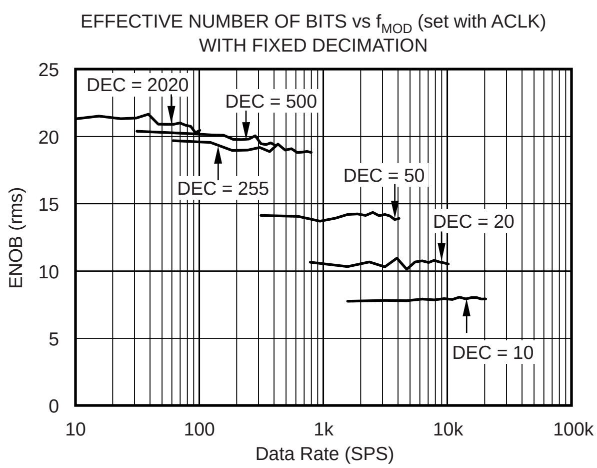


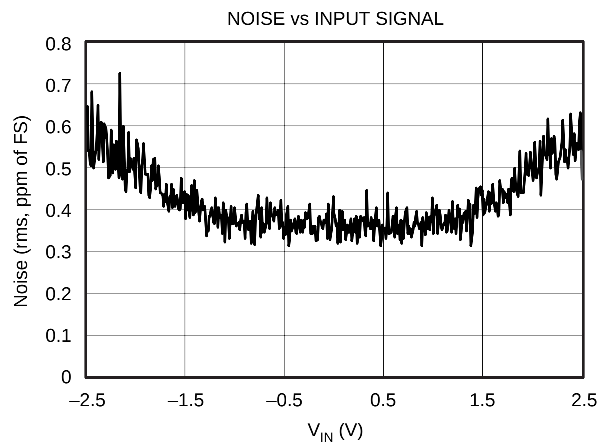
TYPICAL CHARACTERISTICS (Cont.)

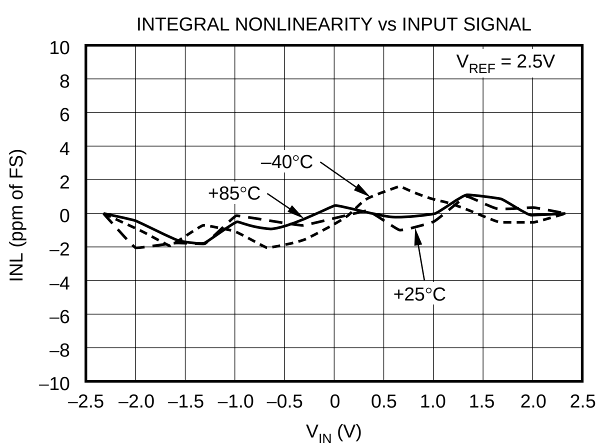
AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, Buffer ON, and V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

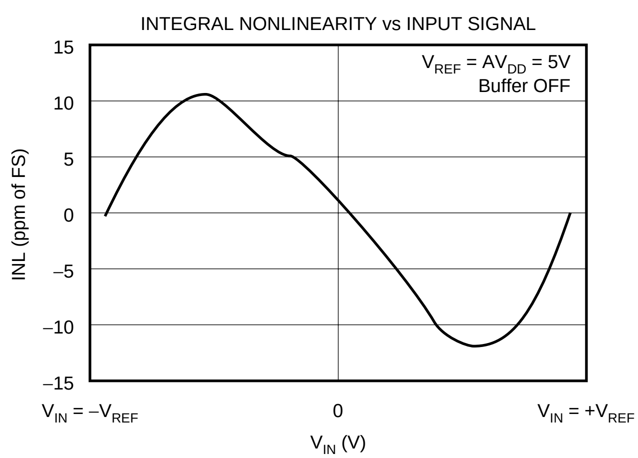






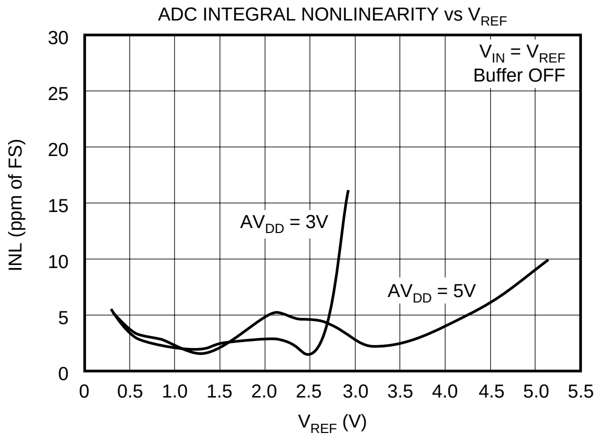


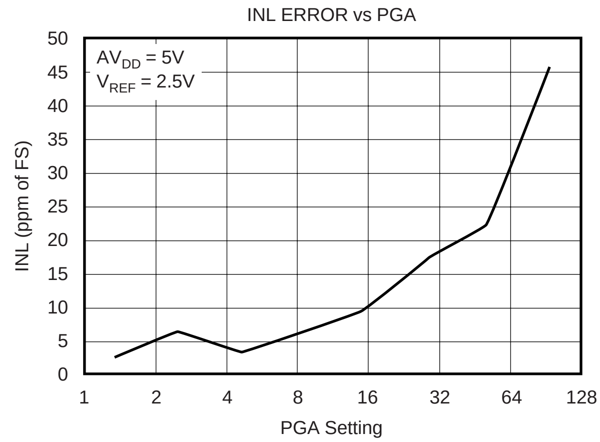


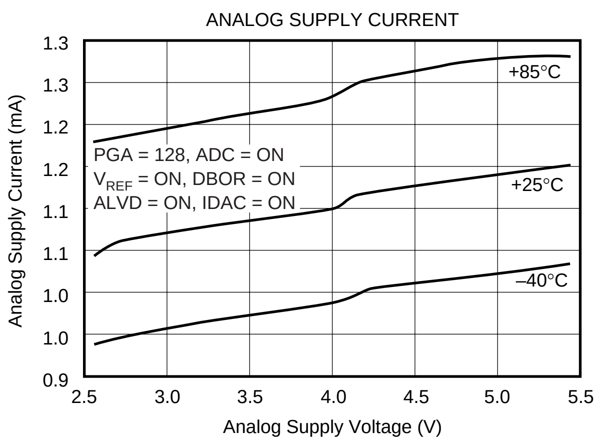


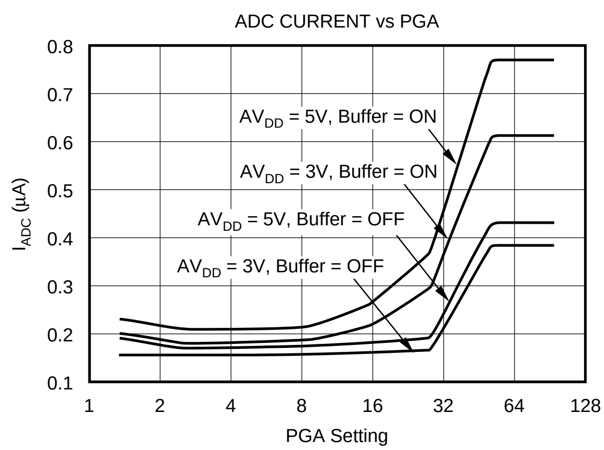
TYPICAL CHARACTERISTICS (Cont.)

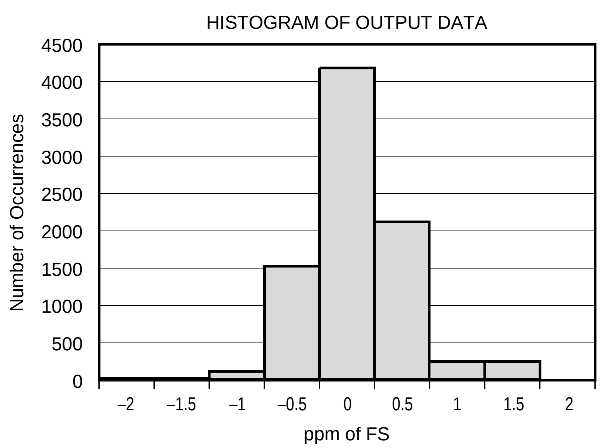
AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, Buffer ON, and V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

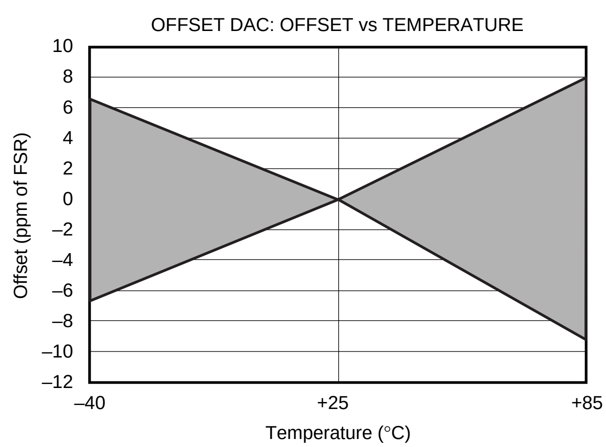






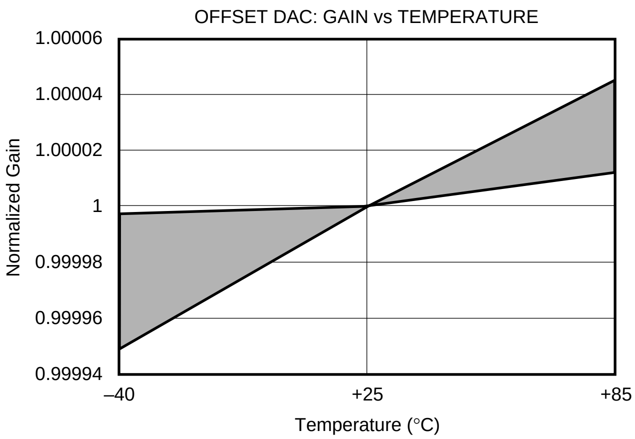


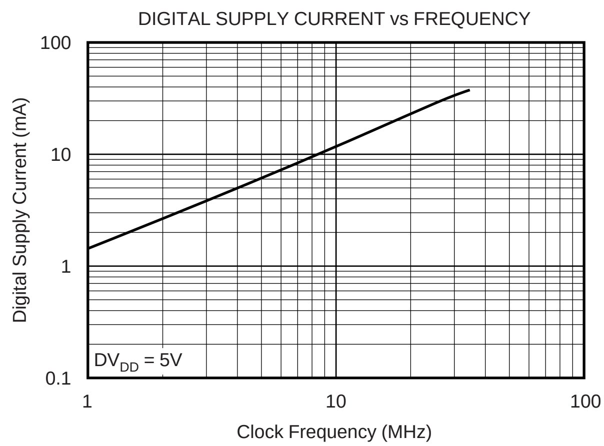


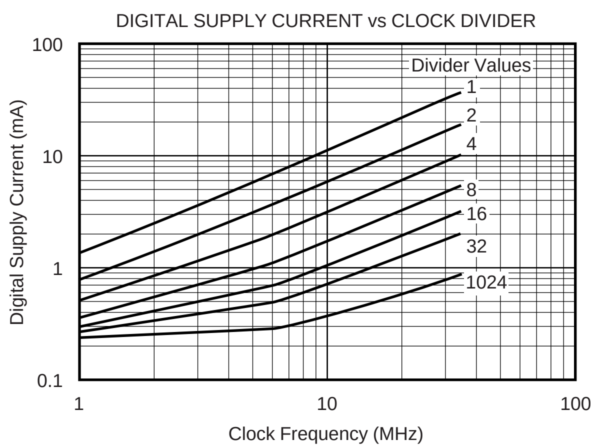


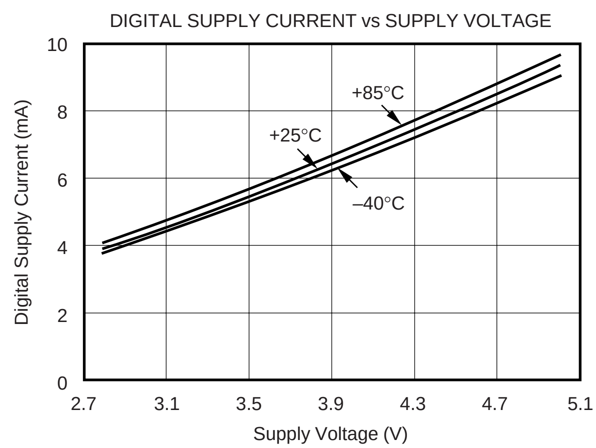
TYPICAL CHARACTERISTICS (Cont.)

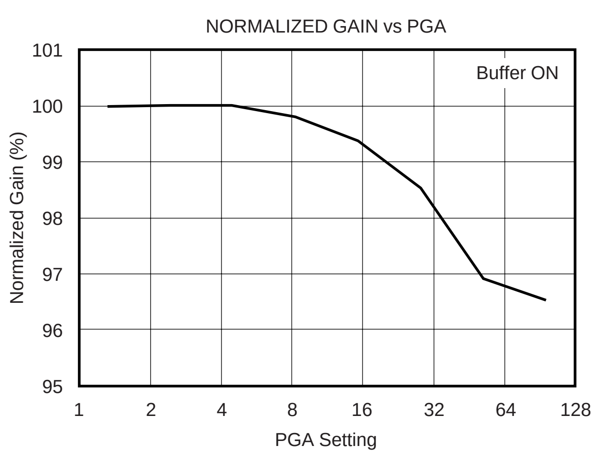
AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, Buffer ON, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

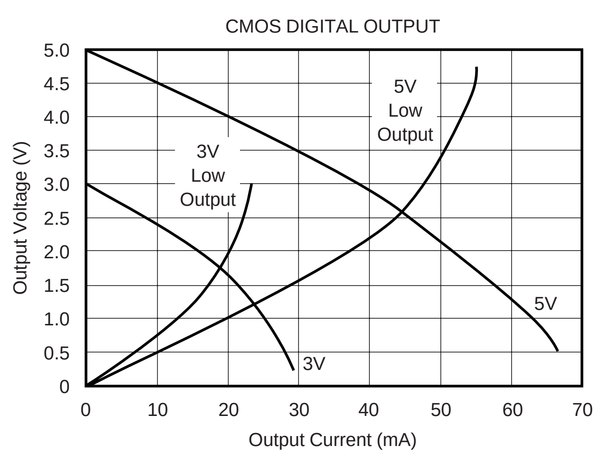






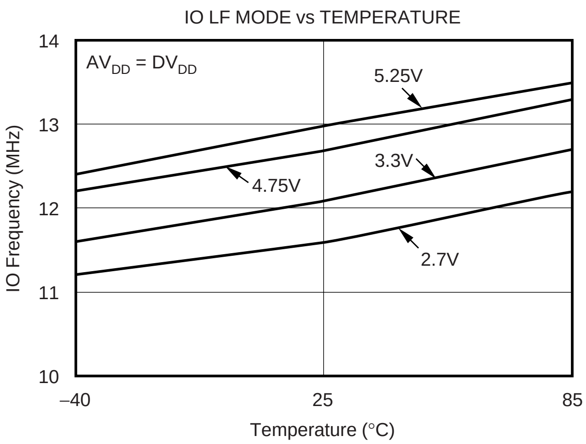


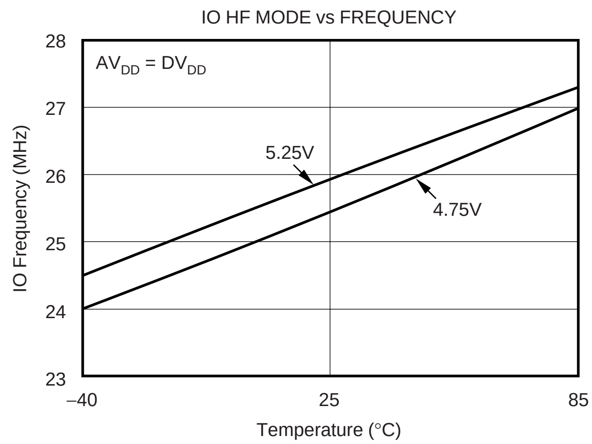




TYPICAL CHARACTERISTICS (Cont.)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, Buffer ON, and V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.





DESCRIPTION

The MSC1200Yx is a completely integrated family of mixed-signal devices incorporating a high-resolution delta-sigma ADC, 8-bit IDAC, 8-channel multiplexer, burnout detect current sources, selectable buffered input, offset DAC, programmable gain amplifier (PGA), temperature sensor, voltage reference, 8-bit microcontroller, Flash Program Memory, Flash Data Memory, and Data SRAM, as shown in Figure 1.

On-chip peripherals include an additional 32-bit accumulator, basic SPI, basic I^{2}C, USART, multiple digital input/output ports, watchdog timer, low-voltage detect, on-chip power-on reset, brownout reset, timer/counters, system clock divider, PLL, on-chip oscillator, and external interrupts.

The device accepts low-level differential or single-ended signals directly from a transducer. The ADC provides 24 bits of resolution and 24 bits of no-missing-code performance using a Sinc^3 filter with a programmable sample rate. The ADC also has a selectable filter that allows for high-resolution single-cycle conversion.

The microcontroller core is 8051 instruction set compatible. The microcontroller core is an optimized 8051 core that executes up to three times faster than the standard 8051 core, given the same clock source. This makes it possible to run the device at a lower external clock frequency and achieve the same performance at lower power than the standard 8051 core.

The MSC1200Yx allows the user to uniquely configure the Flash memory map to meet the needs of their application. The Flash is programmable down to 2.7V using serial programming. Flash endurance is typically 1M Erase/Write cycles.

The part has separate analog and digital supplies, which can be independently powered from 2.7V to +5.25V. At +3V operation, the power dissipation for the part is typically less than 4mW. The MSC1200Yx is packaged in a TQFP-48 package.

The MSC1200Yx is designed for high-resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography, and portable instrumentation.

ENHANCED 8051 CORE

All instructions in the MSC1200 family perform exactly the same functions as they would in a standard 8051. The effect on bits, flags, and registers is the same. However, the timing is different. The MSC1200 family utilizes an efficient 8051 core which results in an improved instruction execution speed of between 1.5 and 3 times faster than the original core for the same external clock speed (4 clock cycles per instruction versus 12 clock cycles per instruction, as shown in Figure 2). This translates into an effective throughput improvement of more than 2.5 times, using the same code and same external clock speed. Therefore, a device frequency of 33MHz for the MSC1200Yx actually performs at an equivalent execution speed of 82.5MHz compared to the

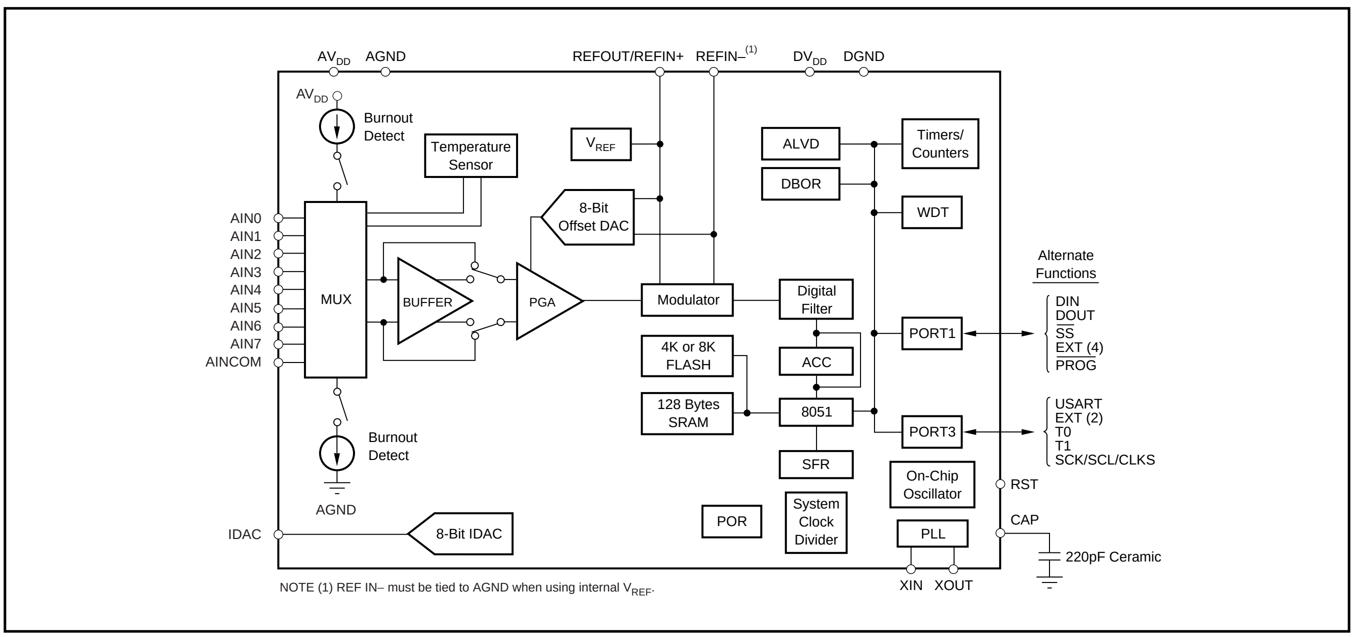


FIGURE 1. Block Diagram.

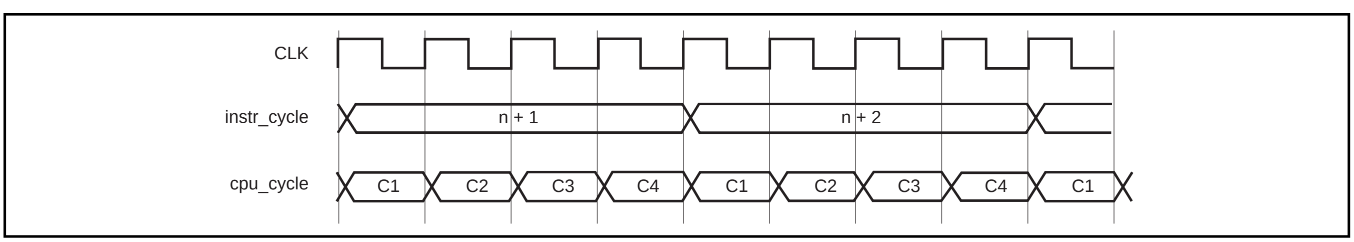


FIGURE 2. Instruction Cycle Timing.

standard 8051 core. This allows the user to run the device at slower clock speeds, which reduces system noise and power consumption, but provides greater throughput. This performance difference can be seen in Figure 3. The timing of software loops will be faster with the MSC1200. However, the timer/counter operation of the MSC1200 may be maintained at 12 clocks per increment or optionally run at 4 clocks per increment.

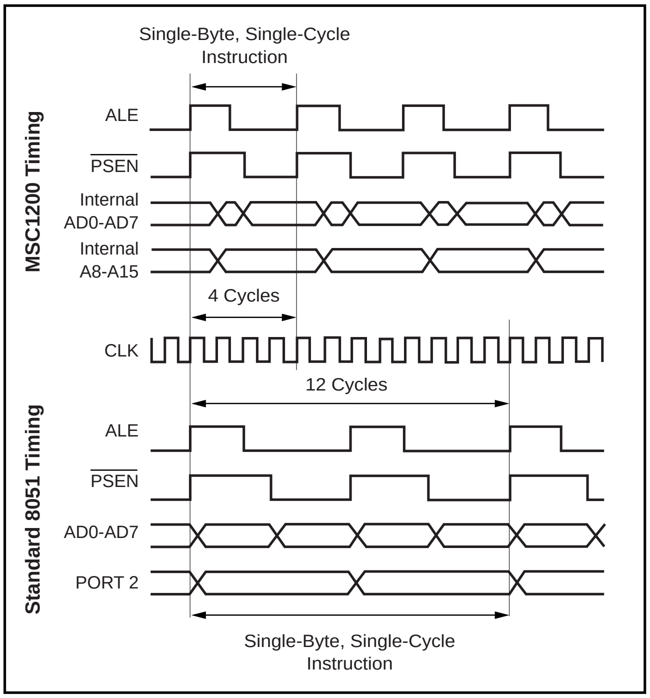


FIGURE 3. Comparison of MSC1200 Timing to Standard 8051 Timing.

The MSC1200 also provides dual data pointers (DPTRs).

Furthermore, improvements were made to peripheral features that off-load processing from the core and the user, to further improve efficiency. For instance, a 32-bit accumulator was added to significantly reduce the processing overhead for the multiple byte data from the ADC or other sources. This allows for 24-bit addition and shifting to be accomplished in a few instruction cycles, compared to hundreds of instruction cycles through software implementation.

Family Device Compatibility

The hardware functionality and pin configuration across the MSC1200 family is fully compatible. To the user, the only difference between family members is the memory configuration. This makes migration between family members simple. Code written for the MSC1200Y2 can be executed directly on an MSC1200Y3. This gives the user the ability to add or subtract software functions and to freely migrate between family members. Thus, the MSC1200 can become a standard device used across several application platforms.

Family Development Tools

The MSC1200 is fully compatible with the standard 8051 instruction set. This means that the user can develop software for the MSC1200 with existing 8051 development tools. Additionally, a complete, integrated development environment is provided with each demo board, and third-party developers also provide support.

Power Down Modes

The MSC1200 can power several of the peripherals and put the CPU into IDLE. This is accomplished by shutting off the clocks to those sections, as shown in Figure 4.

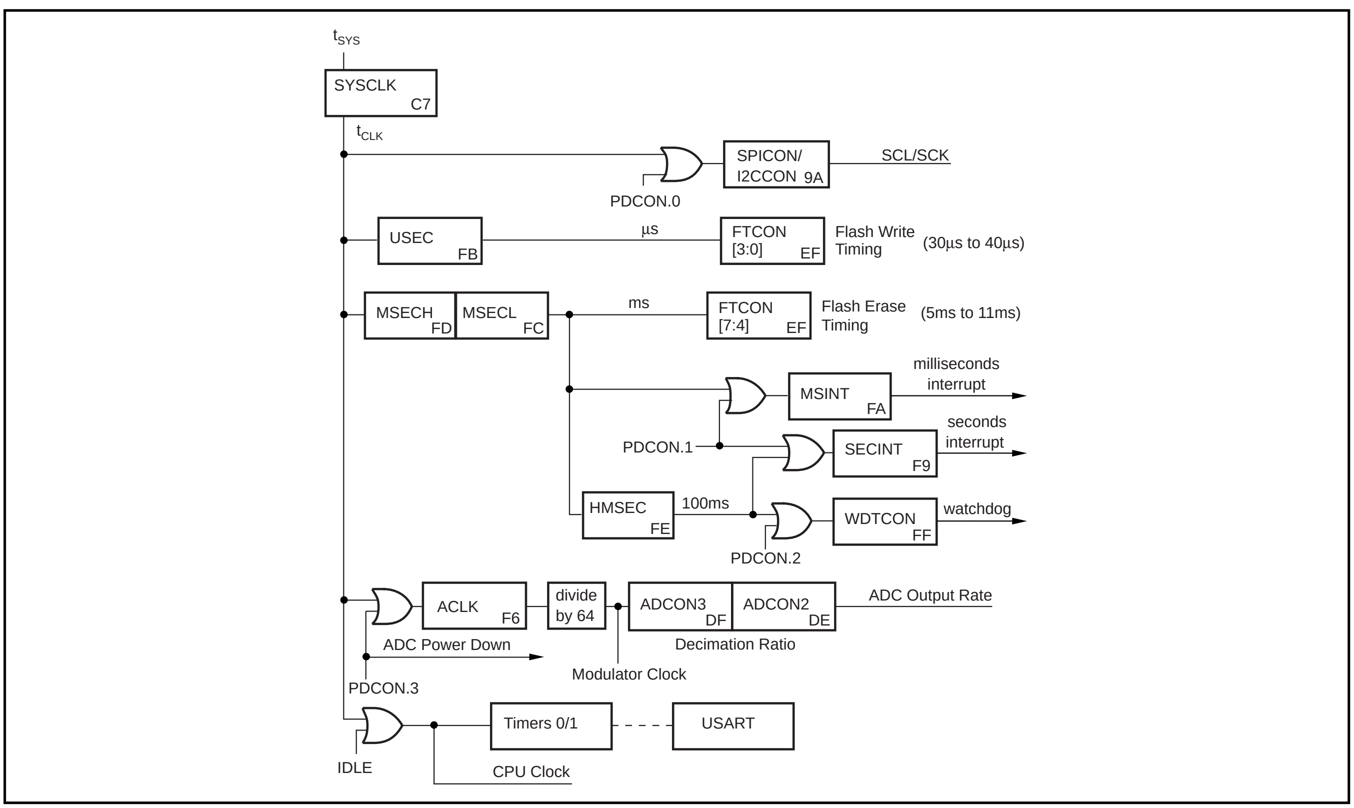


FIGURE 4. MSC1200 Timing Chain and Clock Control.

OVERVIEW

The MSC1200 ADC structure is shown in Figure 5. The figure lists the components that make up the ADC, along with the corresponding special function register (SFR) associated with each component.

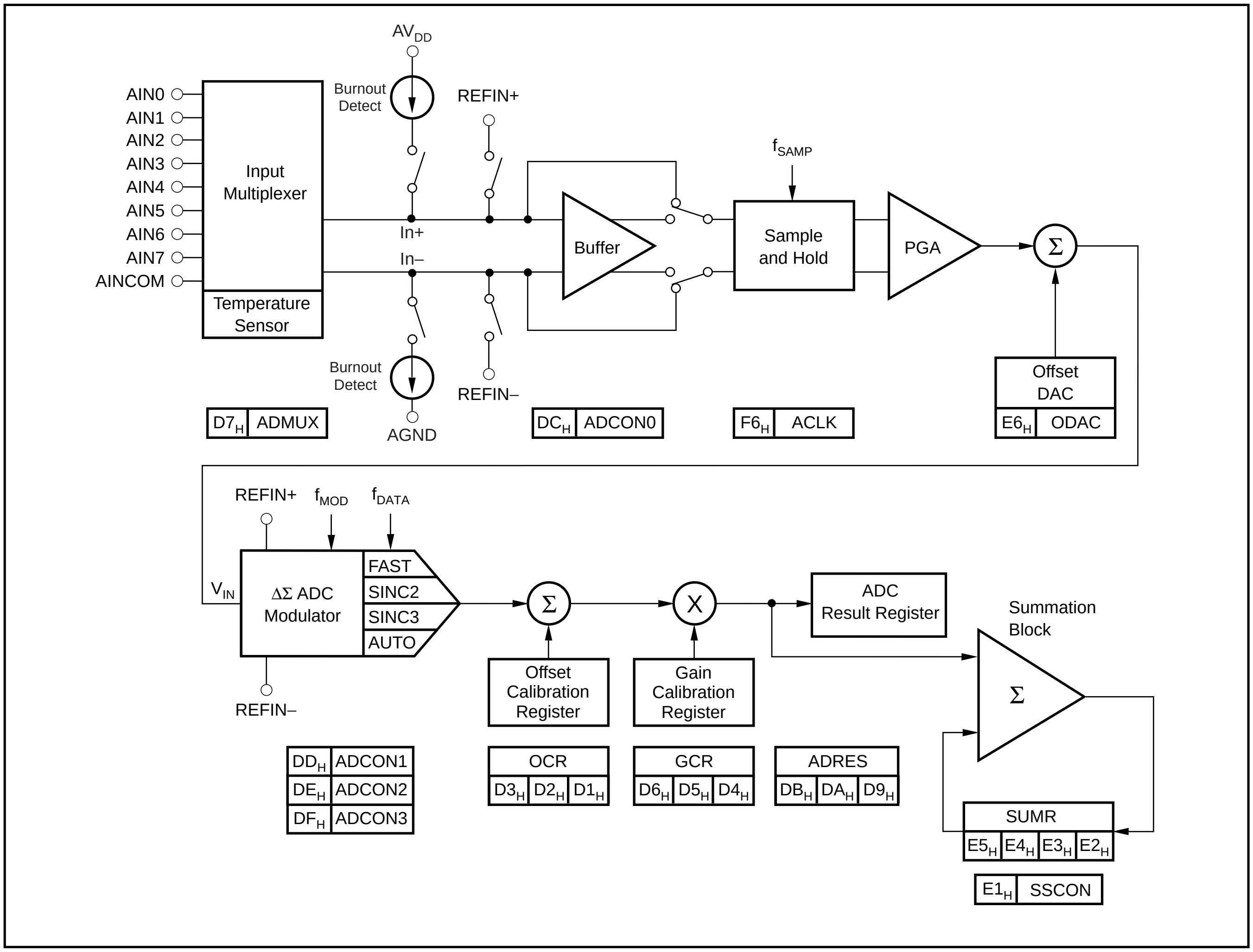


FIGURE 5. MSC1200 ADC Structure.

INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected as the input channel, as shown in Figure 6. If AIN0 is selected as the positive differential input channel, any other channel can be selected as the negative differential input channel. With this method, it is possible to have up to eight fully differential input channels. It is also possible to switch the polarity of the differential input pair to negate any offset voltages.

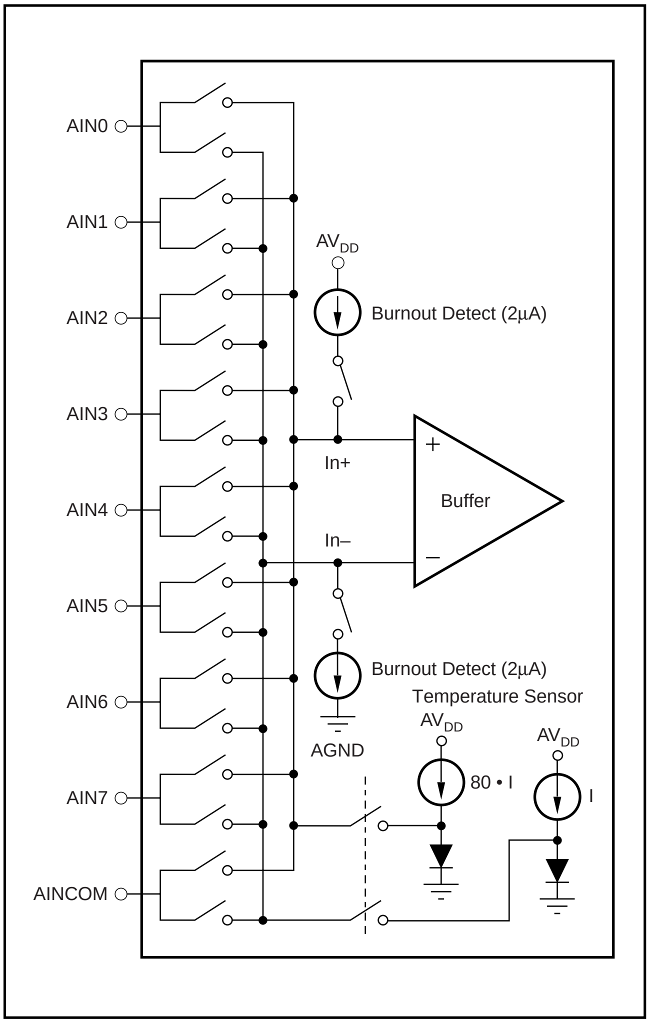


FIGURE 6. Input Multiplexer Configuration.

In addition, current sources are supplied that will source or sink current to detect open or short circuits on the pins.

TEMPERATURE SENSOR

On-chip diodes provide temperature sensing capability. When the configuration register for the input MUX is set to all 1s, the diodes are connected to the input of the ADC. All other channels are open.

BURNOUT DETECT

When the Burnout Detect (BOD) bit is set in the ADC control configuration register (ADCON0 DC_H), two current sources are enabled. The current source on the positive input channel sources approximately 2µA of current. The current source on the negative input channel sinks approximately 2µA. This allows for the detection of an open circuit (full-scale reading) or short circuit (small differential reading) on the selected input differential pair. Enabling the buffer is recommended when BOD is enabled.

INPUT BUFFER

The analog input impedance is always high, regardless of PGA setting (when the buffer is enabled). With the buffer enabled, the input voltage range is reduced and the analog power-supply current is higher. If the limitation of input voltage range is acceptable, then the buffer is always preferred.

The input impedance of the MSC1200 without the buffer is 7MΩ/PGA. The buffer is controlled by the state of the BUF bit in the ADC control register (ADCON0 DC_H).

ANALOG INPUT

When the buffer is not selected, the input impedance of the analog input changes with ACLK clock frequency (ACLK $F6_H$) and gain (PGA). The relationship is:

$$A_{IN}\ \text{Impedance}\ (\Omega) = \left(\frac{1\text{MHz}}{\text{ACLK Frequency}}\right) \bullet \left(\frac{7\text{M}\Omega}{\text{PGA}}\right)$$

where ACLK frequency (f_{ACLK}) = $\dfrac{f_{CLK}}{\text{ACLK} + 1}$

and f_{MOD} = $\dfrac{f_{ACLK}}{64}$.

Figure 7 shows the basic input structure of the MSC1200.

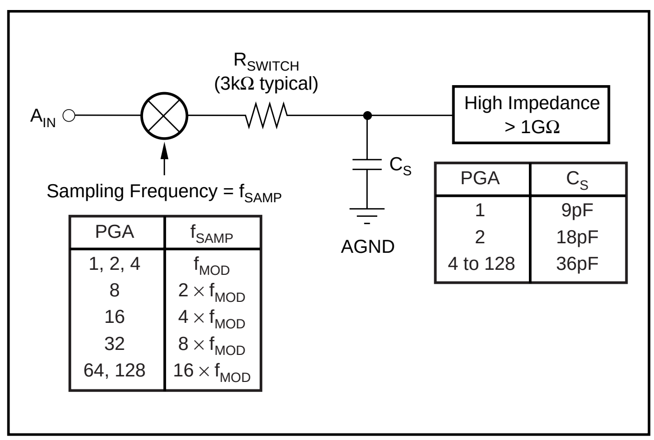


FIGURE 7. Analog Input Structure (without buffer).

PGA

The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can actually improve the effective resolution of the ADC. For instance, with a PGA of 1 on a ±2.5V full-scale range, the ADC can resolve to 1.5μV. With a PGA of 128 on a ±19mV full-scale range, the ADC can resolve to 75nV. With a PGA of 1 on a ±2.5V full-scale range, it would require a 26-bit ADC to resolve 75nV, as shown in Table I.

PGA SETTING	FULL-SCALE RANGE (V)	ENOB AT 10Hz (BITS)	RMS MEASUREMENT RESOLUTION (nV)
1	±2.5	21.7	1468
2	±1.25	21.5	843
4	±0.625	21.4	452
8	±0.313	21.2	259
16	±0.156	20.8	171
32	±0.0781	20.4	113
64	±0.039	20	74.5
128	±0.019	19	74.5

TABLE I. ENOB Versus PGA.

OFFSET DAC

The analog output from the PGA can be offset by up to half the full-scale input range of the PGA by using the ODAC register (SFR $E6_H$). The ODAC (Offset DAC) register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset. Since the ODAC introduces an analog (instead of digital) offset to the PGA, using the ODAC does not reduce the range of the ADC.

MODULATOR

The modulator is a single-loop 2nd-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from the CLK using the value in the Analog Clock register (ACLK, $F6_H$). The data output rate is:

$$\text{Data Rate} = f_{DATA} = \frac{f_{MOD}}{\text{Decimation Ratio}}$$

$$\text{where } f_{MOD} = \frac{f_{CLK}}{(ACLK + 1) \bullet 64} = \frac{f_{ACLK}}{64}$$

CALIBRATION

The offset and gain errors in the MSC1200, or the complete system, can be reduced with calibration. Calibration is controlled through the ADCON1 register (SFR DD_H), bits CAL2:CAL0. Each calibration process takes seven t_{DATA} periods (data conversion time) to complete. Therefore, it takes 14 t_{DATA} periods to complete both an offset and gain calibration.

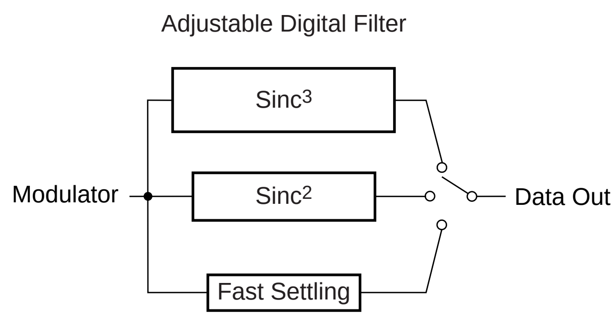
For system calibration, the appropriate signal must be applied to the inputs. The system offset calibration requires a zero-differential input signal. It then computes an offset value that will nullify offset in the system. The system gain calibration requires a positive full-scale differential input signal. It then computes a gain value to nullify gain errors in the system. Each of these calibrations will take seven t_{DATA} periods to complete.

Calibration should be performed after power on, a change in temperature, power supply, voltage reference, decimation ratio, buffer, or a change of the PGA. Calibration will remove the effects of the Offset DAC; therefore, changes to the Offset DAC register should be done after calibration.

At the completion of calibration, the ADC Interrupt bit goes high, which indicates the calibration is finished and valid data is available.

DIGITAL FILTER

The Digital Filter can use either the Fast Settling, $Sinc^2$, or $Sinc^3$ filter, as shown in Figure 8. In addition, the Auto mode changes the Sinc filter after the input channel or PGA is changed. When switching to a new channel, it will use the Fast Settling filter, for the next two conversions the first of which should be discarded. It will then use the $Sinc^2$ followed by the $Sinc^3$ filter to improve noise performance. This combines the low-noise advantage of the $Sinc^3$ filter with the quick response of the Fast Settling Time filter. The frequency response of each filter is shown in Figure 9.



FILTER SETTLING TIME

FILTER	SETTLING TIME (Conversion Cycles)
$Sinc^3$	3(1)
$Sinc^2$	2(1)
Fast	1(1)

NOTE: (1) With Synchronized Channel Changes.

AUTO MODE FILTER SELECTION

CONVERSION CYCLE			
1	2	3	4+
Discard	Fast	$Sinc^2$	$Sinc^3$

FIGURE 8. Filter Step Responses.

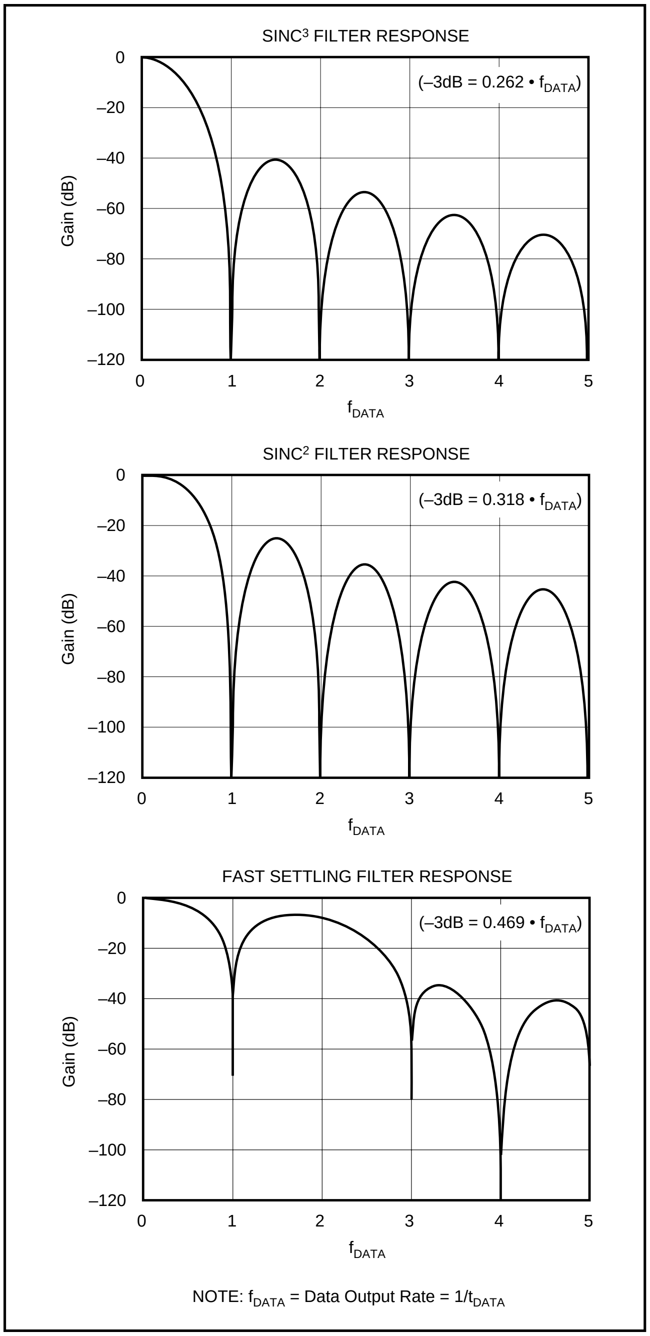


FIGURE 9. Filter Frequency Responses.

VOLTAGE REFERENCE

The MSC1200 can use either an internal or external voltage reference. The voltage reference selection is controlled via ADC Control Register 0 (ADCON0, SFR DC_H). The default power-up configuration for the voltage reference is 2.5V internal.

The internal voltage reference can be selected as either 1.25V or 2.5V. The analog power supply (AV_{DD}) must be within the specified range for the selected internal voltage reference. The valid ranges are: V_{REF} = 2.5 internal (AV_{DD} = 4.1V to 5.25V) and V_{REF} = 1.25 internal (AV_{DD} = 2.7V to 5.25V). If the internal V_{REF} is selected then AGND must be connected to REFIN–. The REFOUT/REFIN+ pin should also have a 0.1µF capacitor connected to AGND as close as possible to the pin. If the internal V_{REF} is not used, then V_{REF} should be disabled in ADCON0.

If the external voltage reference is selected it can be used as either a single-ended input of differential input, for ratiometric measures. When using an external reference, it is important to note that the input current will increase for V_{REF} with higher PGA settings and with a higher modulator frequency. The external voltage reference can be used over the input range specified in the electrical characteristics section.

IDAC

The 8-bit IDAC in the MSC1200 can be used to provide a current source that can be used for ratiometric measurements. The IDAC operates from its own voltage reference and is not dependent on the ADC voltage reference. The full-scale output current of the IDAC is approximately 1mA. The equation for the IDAC output current is:

$$IDACOUT = IDAC \cdot 3.6\mu A$$

RESET

Taking the RST pin HIGH will stop the operation of the device, and taking the RST pin LOW will initiate a reset. The device can also be reset by the power on reset circuitry, digital brownout Reset, or software reset. The timing of the reset operation is shown in the Electrical Characteristics section.

If the P1.0/$\overline{PROG}$ pin is unconnected or tied HIGH, the device will enter User Application mode on reset. If P1.0/$\overline{PROG}$ is tied LOW during reset, the device will enter Serial Programming mode.

POWER ON RESET

The on-chip Power On Reset (POR) circuitry releases the device from reset at approximately DVDD = 2.0V. The POR accommodates power-supply ramp rates as slow as 1V/10ms. To ensure proper operation, the power supply should ramp monotonically. Note that, as the device is released from reset and program execution begins, the device current consumption may increase, which may result in a power-supply voltage drop. If the power supply ramps at a slower rate, is not monotonic, or a brownout condition occurs (where the supply does not drop below the 2.0V threshold), then improper device operation may occur. The on-chip Brownout Reset (BOR) may provide benefit in these conditions. A POR circuit is shown in Figure 10.

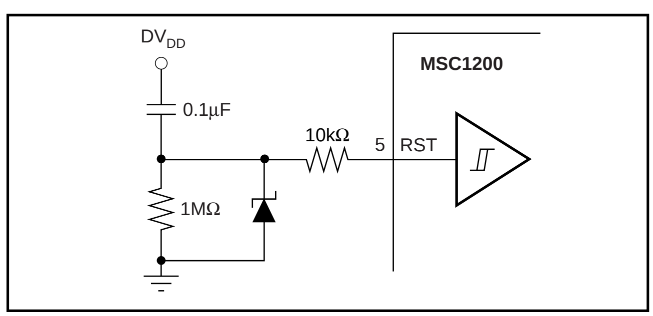


FIGURE 10. Typical Reset Circuit.

DIGITAL BROWNOUT RESET

The Digital Brownout Reset (DBOR) is enabled through Hardware Configuration Register 1 (HCR1). If the conditions for proper POR are not met or the device encounters a brownout condition which does not generate a POR, DBOR can be used to ensure proper device operation. The DBOR will hold the state of the device when the power supply drops below the threshold level programmed in HCR1 and then generate a reset when the supply rises above the threshold level. Note that, as the device is released from reset and program execution begins, the device current consumption may increase, which can result in a power-supply voltage drop, which may initiate another brownout condition. Additionally, the DBOR comparison is done against an analog reference; therefore, AV_{DD} must be within its valid operating range for DBOR to function.

The DBOR level should be chosen to match closely with the application. That is, with a high external clock frequency, the BOR level should match the minimum operating voltage range for the device, or improper operation may still occur.

ANALOG LOW VOLTAGE DETECT

The MSC1200 contains an analog low-voltage detect. When the analog supply drops below the value programmed in LVDCON (SFR $E7_H$), an interrupt is generated.

POWER-UP—SUPPLY VOLTAGE RAMP RATE

The built-in (on-chip) power-on reset circuitry was designed to accommodate analog or digital supply ramp rates as slow as 1V/10ms. To ensure proper operation, the power supply should ramp monotonically at the specified rate. If DBOR is enabled, the ramp rate can be slower.

CLOCKS

The MSC1200 can operate in three separate clock modes: internal oscillator mode (IOM), external clock mode (ECM), and PLL mode. A block diagram is shown in Figure 11. The clock mode for the MSC1200 is selected via the CLKSEL bits in HCR2. IOM is the default mode for the device.

Serial Flash Programming mode uses IO LF mode (the HCR2 and CLKSEL bits have no effect). Table II shows the active clock mode for the various startup conditions.

Internal Oscillator

In IOM, the CPU executes either in LF mode (if HCR2, CLKSEL = 111) or HF mode (if HCR2, CLKSEL = 110).

External Clock

In ECM (HCR2, CLKSEL = 011), the CPU can execute from an external crystal, external ceramic resonator, external

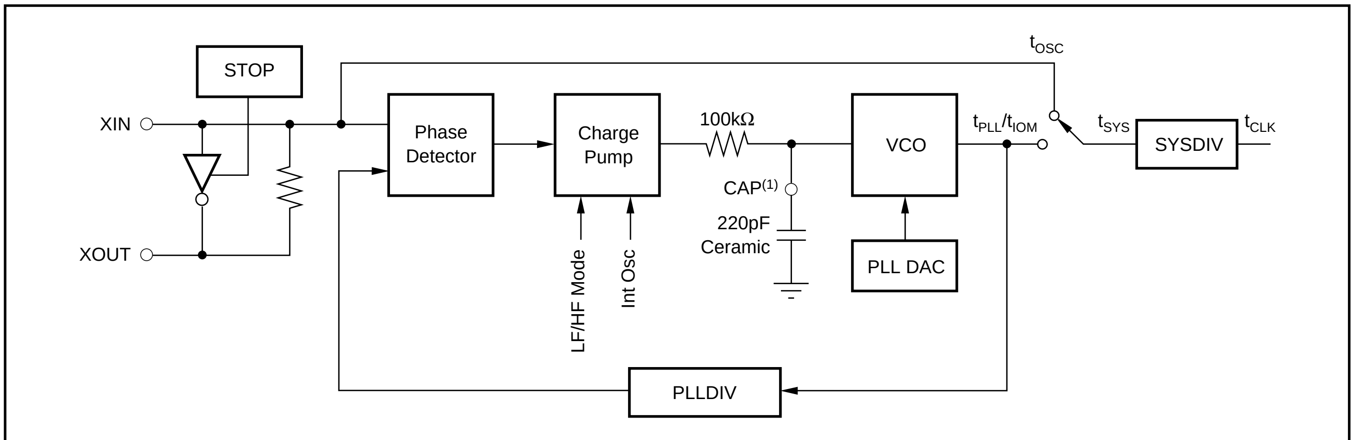


FIGURE 11. Clock Block Diagram.

SELECTED CLOCK MODE (HCR2, CLKCON2:0)	STARTUP CONDITION(1)	ACTIVE CLOCK MODE (f_{SYS})
External Clock Mode (ECM)		
	Active Clock Present at XIN	External Clock Mode
	No Clock Present at XIN	IO LF Mode
Internal Oscillator Mode (IOM)		
IO LF Mode	N/A	IO LF Mode
IO HF Mode	N/A	IO HF Mode
PLL(2)		
PLL LF Mode	Active 32.768kHz Clock at XIN	PLL LF Mode
	No Clock Present at XIN	Nominal: 50% of IO LF Mode Rate
PLL HF Mode	Active 32.768kHz Clock at XIN	PLL HF Mode
	No Clock Present at XIN	Nominal: 50% of IO HF Mode Rate

NOTES: (1) Clock detection is only done at startup; refer to Electrical Characteristics parameter t_{RFD} in Figure B.
(2) PLL operation requires that both AVDD and DVDD are within their specified operating range.

TABLE II. Active Clock Modes.

clock, or external oscillator. If an external clock is detected at startup, then the CPU will begin execution in ECM after startup. If an external clock is not detected at startup, then the device will revert to the mode shown in Table II.

PLL

In Phase Lock Loop (PLL) mode (HCR2, CLKSEL = 101 or HCR2, CLKSEL = 100), the CPU can execute from an external 32.768 kHz crystal. This mode enables the use of a phase-lock loop (PLL) circuit that synthesizes the selected clock frequencies (PLL LF mode or PLL HF mode). If an external clock is detected at startup, then the CPU will begin execution in PLL mode after startup. If an external clock is not detected at startup, then the device will revert to the mode shown in Table II. The status of the PLL can be determined by first writing the PLLLOCK bit (enable) and then reading the PLLLOCK status bit in the PLLH SFR.

The frequency of the PLL is preloaded with default trimmed values. However, the PLL frequency can be fine-tuned by writing to the PLLDIV1 and PLLDIV0 SFRs. The equation for the PLL frequency is:

$$\text{PLL Frequency} = ((\text{PLLDIV9:PLLDIV0}) + 1) \bullet f_{OSC}$$

where f_{OSC} = 32.768kHz.

The default value for PLL LF mode is automatically loaded into the PLLDIV SFR. For PLL HF mode, the user must load PLLDIV with the appropriate value (0383_H).

For different connections to external clocks, see Figures 12, 13, and 14.

SPI

The MSC1200 implements a basic SPI interface which includes the hardware for simple serial data transfers. Figure 15 shows a block digram of the SPI. The peripheral supports master and slave mode, full duplex data transfers, both clock polarities, both clock phases, bit order, and slave select.

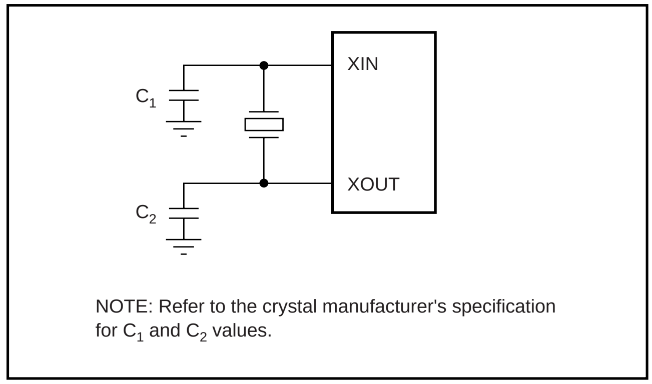


FIGURE 12. External Crystal Connection.

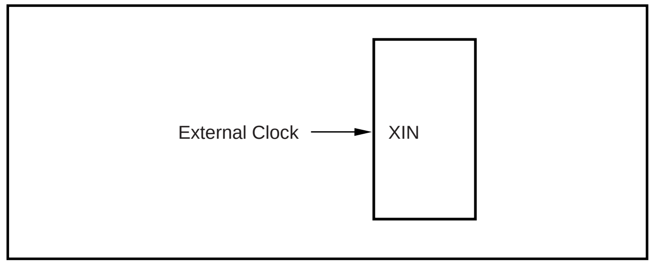


FIGURE 13. External Clock Connection.

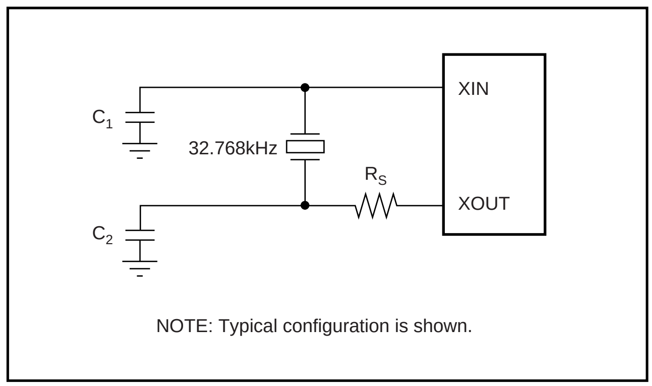


FIGURE 14. PLL Connection.

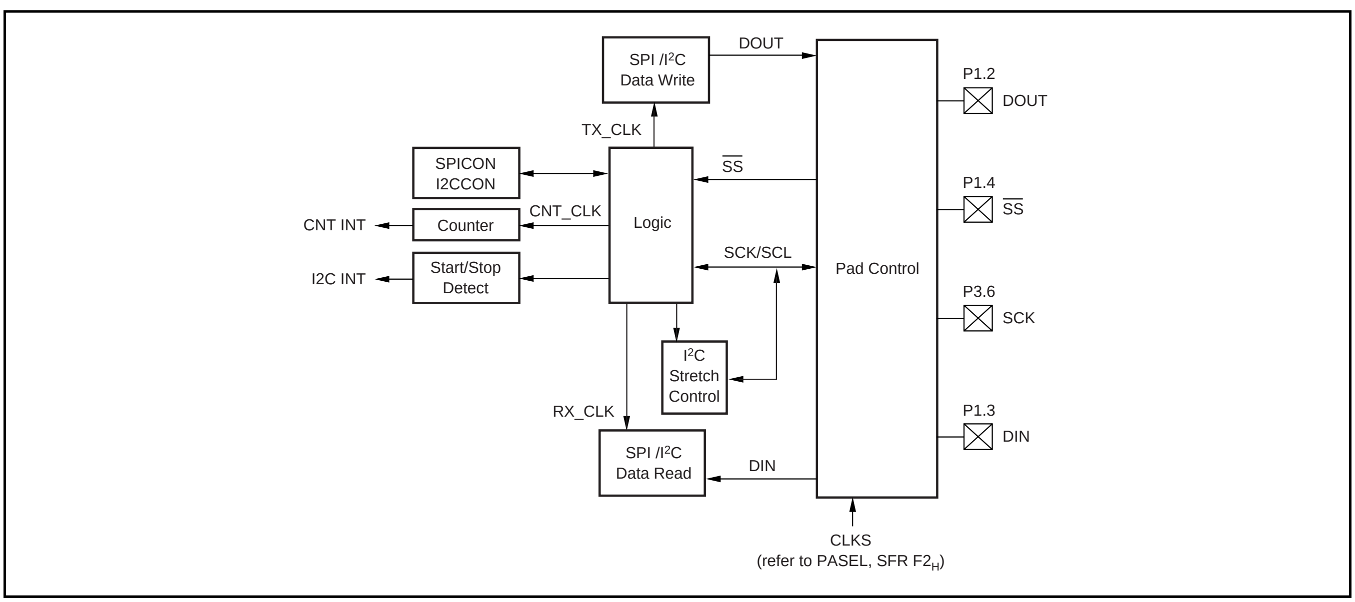


FIGURE 15. SPI/I^2C Block Diagram.

The timing diagram for supported SPI data transfers is shown in Figure 16.

The I/O pins needed for data transfer are Data In (DIN), Data Out (DOUT) and serial clock (SCK). The slave select ($\overline{SS}$) pin can also be used to control the output of data on DOUT.

The DIN pin is used for shifting data in for both master and slave modes.

The DOUT pin is used for shifting data out for both master and slave modes.

The SCK pin is used to synchronize the transfer of data for both master and slave modes. SCK is always generated by the master. The generation of SCK in master mode can be done in SW by simply toggling the port pin, or the generation of SCK can be accomplished by configuring the output on the SCK pin via PASEL (SFR $F2_H$). A list of the most common methods of generating SCK follows, but the complete list of clock sources can be found by referring to the PASEL SFR.

• Toggle SCK by setting and clearing the port pin.

• Memory Write Pulse ($\overline{WR}$) which is idle high. Whenever a external memory write command (MOVX) is executed then a pulse is seen on P3.6. This method can be used only if CPOL is set to ‘1’.

• Memory Write Pulse toggle version: In this mode, SCK toggles whenever an external write command (MOVX) is executed.

• T0_Out signal can be used as a clock. A pulse is generated on SCK whenever Timer 0 expires. The idle state of the signal is low, so this can be used only if CPOL is cleared to ‘0’.

• T0_Out Toggle: SCK toggles whenever Timer 0 expires.

• T1_Out signal can be used as a clock. A pulse is generated whenever Timer 1 expires. The idle state of the signal is low, so this can be used only if CPOL is cleared to ‘0’.

• T1_Out Toggle: SCK toggles whenever Timer 1 expires.

The $\overline{SS}$ pin can be used to control the output of data on DOUT when the MSC1200 is in slave mode. The $\overline{SS}$ function is enabled or disabled by the ESS bit of the SPICON SFR. When enabled, the $\overline{SS}$ input of a slave device must be externally asserted before a master device can exchange data with the slave device. $\overline{SS}$ must be low before data transactions and must stay low for the duration of the transaction. When $\overline{SS}$ is high then data will not be shifted into the shift register nor will the counter increment. When SPI is enabled, $\overline{SS}$ also controls the drive of the line DOUT (P1.2). When $\overline{SS}$ is low in slave mode, the DOUT pin will be driven and when $\overline{SS}$ is high then DOUT will be high impedance.

The SPI generates an interrupt ECNT (AIE.2) to indicate that the transfer/reception of the byte is complete. The interrupt goes high whenever the counter value is equal to 8 (indicating that 8 SCKs have occurred). The interrupt is cleared on reading or writing to the SPIDATA register. During the data transfer, the actual counter value can be read from the SPICON SFR.

Power Down

The SPI is powered down by the PDSPI bit in the power control register (PDCON). This bit needs to be cleared to enable the SPI function. When the SPI is powered down the pins P1.2, P1.3, P1.4, and P3.6 revert to general-purpose I/O pins.

Application Flow

Explained below are the steps of the typical application usage flow of SPI in master and slave mode:

Master Mode Application Flow

1. Configure the port pins.
2. Configure the SPI.
3. Assert $\overline{SS}$ to enable slave communications (if applicable).
4. Write data to SPIDATA.
5. Generate 8 SCKs.
6. Read the received data from SPIDATA.

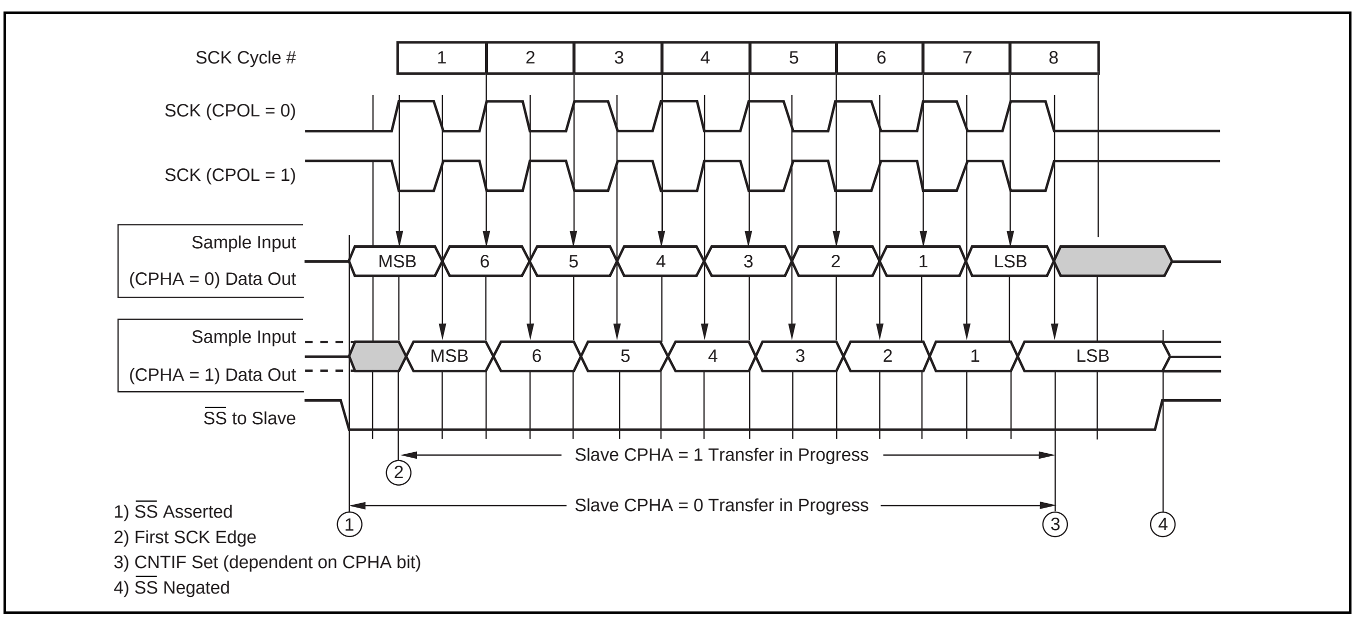


FIGURE 16. SPI Timing Diagram.

Slave Mode Application Flow

1. Configure the ports pins.
2. Enable $\overline{SS}$ (if applicable).
3. Configure the SPI.
4. Write data to SPIDATA.
5. Wait for the Count Interrupt (8 SCKs).
6. Read the data from SPIDATA.

Caution: If SPIDATA is not read before the next SPI transaction the ECNT interrupt will be removed and the previous data will be lost.

I^2C

The I/O pins needed for I^2C transfer are: serial clock (SCL) and serial data (SDA—implemented by connecting DIN and DOUT externally).

The MSC1200 I^2C supports:

1) Master or slave I^2C operation (control in software)

2) Standard or fast modes of transfer

3) Clock stretching

4) General call

When used in I^2C mode, pins DIN (P1.3) and DOUT (P1.2) should be tied together externally. The DIN pin should be configured as an input pin and the DOUT pin should be configured as open drain or standard 8051 by setting the P1DDR (DOUT should be set high so that the bus is not pulled low).

The MSC1200 I2C can generate two interrupts:

1) I2C interrupt for START/STOP interrupt (AIE.3)

2) CNT interrupt for bit counter interrupt (AIE.2)

The START/STOP interrupt is generated when a START condition or STOP condition is detected on the bus. The bit counter generates an interrupt on a complete (8-bit) data transfer and also after the transfer of the ACK/NACK.

The bit counter for serial transfer is always incremented on the falling edge of SCL and can be reset by reading or writing to I2CDATA (SFR $9B_H$) or when a START/STOP condition is detected. The bit counter can be polled or used as an interrupt. The bit counter interrupt occurs when the bit counter value is equal to 8, indicating that eight bits of data have been transferred. I^2C mode also allows for interrupt generation on one bit of data transfer (I2CCON.CNTSEL). This can be used for ACK/NACK interrupt generation. For instance, the I^2C interrupt can be configured for 8-bit interrupt detection, on the eighth bit the interrupt is generated. Following this interrupt, the clock will be stretched (SCL held low). The interrupt can then be configured for 1-bit detection. The ACK/NACK can be written by the software, which will terminate clock stretching. The next interrupt will be generated after the ACK/NACK has been latched by the receiving device. The interrupt is cleared on reading or writing to the I2CDATA register. If I2CDATA is not read before the next data transfer, the interrupt will be removed and the previous data will be lost.

Master Operation

The source for the SCL is controlled in the PASEL register or can be generated in software.

Transmit

The serial data must be stable on the bus while SCL is high. Therefore, the writing of serial data to I2CDATA must be coordinated with the generation of the SCL, since SDA transitions on the bus may be interpreted as a START or STOP while SCL is high. The START and STOP conditions on the bus must be generated in software. After the serial data has been transmitted, the generation of the ACK/NACK clock must be enabled by writing $0xFF_H$ to I2CDATA. This allows the master to read the state of ACK/NACK.

Receive

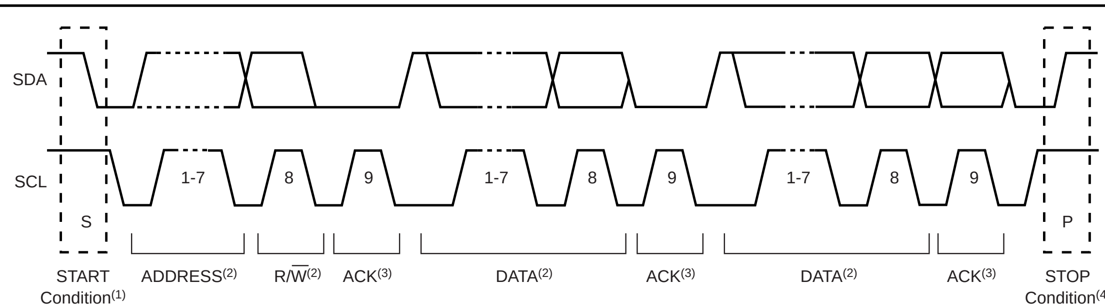
The serial data is latched into the receive buffer on the rising edge of SCL. After the serial data has been received, ACK/NACK is generated by writing $0x7F_H$ (for ACK) or $0xFF_H$ (for NACK) to I2CDATA.

Slave Operation

Slave operation is supported, but address recognition, R/$\overline{W}$ determination, and ACK/NACK must be done under software control.

Transmit

Once address recognition, R/$\overline{W}$ determination, and ACK/NACK are complete, the serial data to be transferred can be written to I2CDATA. The data is automatically shifted out based on the master SCL. After data transmission,



NOTES: (1) Generate in software; write 0x7F to I2CDATA.
(2) I2CDATA register.
(3) Generate in software. Can enable bit count = 1 interrupt prior to ACK/NACK for interrupt use. Generate ACK by writing 0x7F to I2CDATA; generate NACK by writing 0xFF to I2CDATA.
(4) Generate in software; write 0xFF to I2CDATA.

FIGURE 17. Timing Diagram for I^2C Transmission and Reception.

CNTIF is generated and SCL is stretched by the MSC1200 until the I2CDATA register is written with a $0xFF_H$. The ACK/NACK from the master can then be read.

Receive

Once address recognition, R/$\overline{W}$ determination, and ACK/NACK are complete, I2CDATA must be written with $0xFF_H$ to enable data reception. Upon completion of the data shift, the MSC1200 generates the CNT interrupt and stretches SCL. Received data can then be read from I2CDATA. After the serial data has been received, ACK/NACK is generated by writing $0x7F_H$ (for ACK) or $0xFF_H$ (for NACK) to I2CDATA. The write to I2CDATA clears the CNT interrupt and clock stretch.

MEMORY MAP

The MSC1200 contains on-chip SFR, Flash Memory, Scratchpad RAM Memory, and Boot ROM. The SFR registers are primarily used for control and status. The standard 8051 features and additional peripheral features of the MSC1200 are controlled through the SFR. Reading from undefined SFR will return zero; writing to undefined SFR registers is not recommended and may have indeterminate effects.

Flash Memory is used for both Program Memory and Data Memory. The user has the ability to select the partition size of Program and Data Memories. The partition size is set through hardware configuration bits, which are programmed through serial programming. Both Program and Data Flash Memories are erasable and writable (programmable) in user application mode. However, program execution can only occur from Program Memory. As an added precaution, a lock feature can be activated through the hardware configuration bits, which disables erase and writes to the first 4kB of Program Flash Memory or the entire Program Flash Memory in user application mode.

FLASH MEMORY

The MSC1200 uses a memory addressing scheme that separates Program Memory from Data Memory. The program and data segments can overlap since they are accessed by different instructions. Program Memory is fetched by the microcontroller automatically. There is one instruction (MOVC) that is used to explicitly read the program area. This is commonly used to read lookup tables.

The MSC1200 has three Hardware (HW) Configuration registers (HCR0, HCR1, and HCR2) that are programmable only during Flash Memory Programming mode.

The MSC1200 allows the user to partition the Flash Memory between Program Memory and Data Memory. For instance, the MSC1200Y3 contains 8kB of Flash Memory on-chip. Through the HW configuration registers, the user can define the partition between Program Memory (PM) and Data Memory (DM), as shown in Tables III and IV and Figure 18. The MSC1200 family offers two memory configurations.

HCR0	MSC1200Y2		MSC1200Y3	
DFSEL	PM	DM	PM	DM
00	2kB	2kB	4kB	4kB
01	2kB	2kB	6kB	2kB
10	3kB	1kB	7kB	1kB
11 (default)	4kB	0kB	8kB	0kB

TABLE III. MSC1200Y Flash Partitioning.

HCR0	MSC1200Y2		MSC1200Y3	
DFSEL	PM	DM	PM	DM
00	0000-07FF	0400-0BFF	0000-0FFF	0400-13FF
01	0000-07FF	0400-0BFF	0000-17FF	0400-0BFF
10	0000-0BFF	0400-07FF	0000-1BFF	0400-07FF
11 (default)	0000-0FFF	0000	0000-1FFF	0000

TABLE IV. Flash Memory Partitioning Addresses.

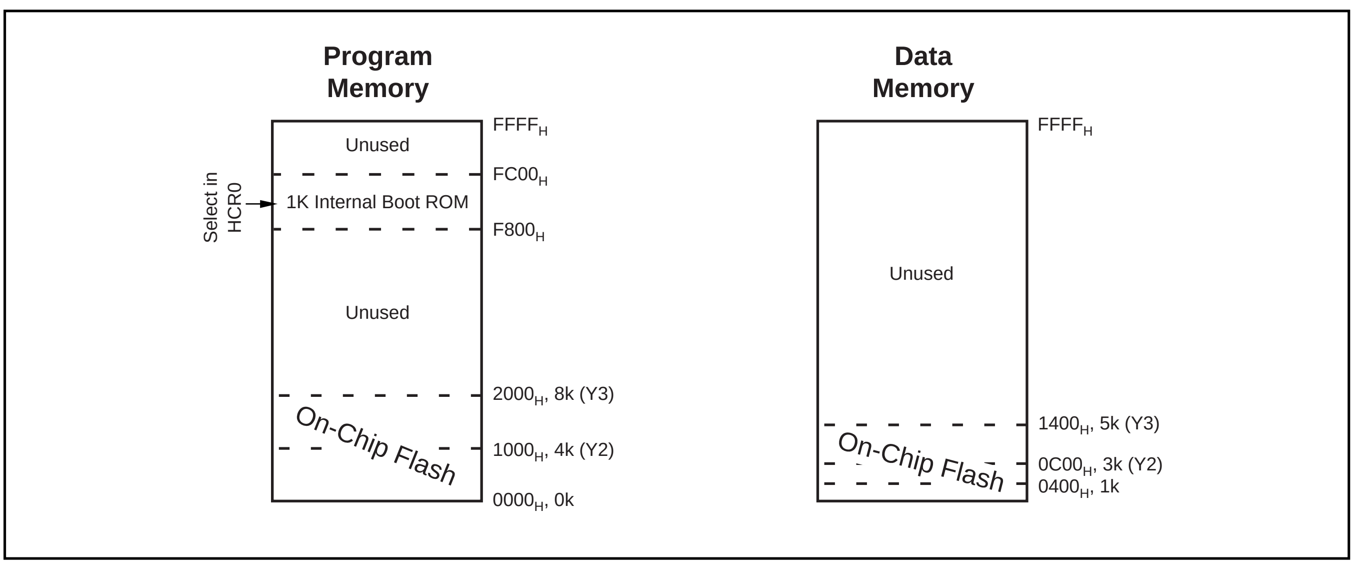


FIGURE 18. Memory Map.

It is important to note that the Flash Memory is readable and writable (depending on the MXWS bit in the MWS SFR) by the user through the MOVX instruction when configured as either Program or Data Memory. This means that the user may partition the device for maximum Flash Program Memory size (no Flash Data Memory) and use Flash Program Memory as Flash Data Memory. This may lead to undesirable behavior if the PC points to an area of Flash Program Memory that is being used for data storage. Therefore, it is recommended to use Flash partitioning when Flash Memory is used for data storage. Flash partitioning prohibits execution of code from Data Flash Memory. Additionally, the Program Memory erase/write can be disabled through hardware configuration bits (HCR0), while still providing access (read/write/erase) to Data Flash Memory.

The effect of memory mapping on Program and Data Memory is straightforward. The Program Memory is decreased in size from the top of Flash Memory. To maintain compatibility with the MSC121x, the Flash Data Memory maps to addresses 0400_H. Therefore, access to Data Memory (through MOVX) will access Flash Memory for the addresses shown in Table IV.

Data Memory

The MSC1200 has on-chip Flash Data Memory, which is readable and writable (depending on Memory Write Select register) during normal operation (full V_{DD} range). This memory is mapped into the external Data Memory space, which requires the use of the MOVX instruction to program. Note that the page size is 64 bytes for both Program and Data Memory and the page must be erased before it can be written.

REGISTER MAP

The Register Map is illustrated in Figure 19. It is entirely separate from the Program and Data Memory areas mentioned before. A separate class of instructions is used to access the registers. There are 128 register locations. In practice, the MSC1200 has 128 bytes of Scratchpad RAM and up to 128 SFRs. Thus, a direct reference to one of the upper 128 locations will be an SFR access. Direct RAM is reached at locations 0 to $7F_H$ (0 to 127).

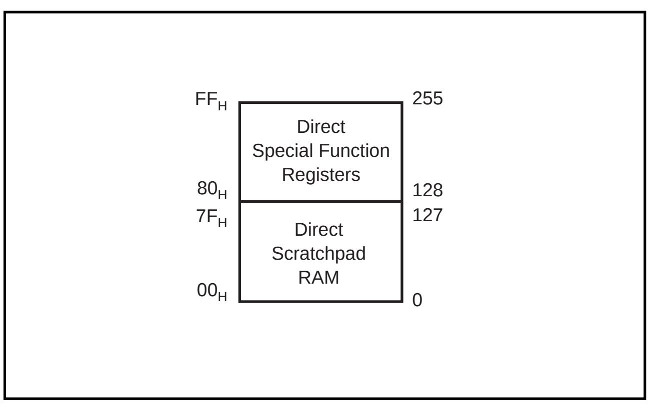


FIGURE 19. Register Map.

SFRs are accessed directly between 80_H and FF_H (128 to 255). Scratchpad RAM is available for general-purpose data storage. It is commonly used in place of off-chip RAM when the total data contents are small. Within the 128 bytes of RAM, there are several special-purpose areas.

Bit Addressable Locations

In addition to direct register access, some individual bits are also accessible. These are individually addressable bits in both the RAM and SFR area. In the Scratchpad RAM area, registers 20_H to $2F_H$ are bit addressable. This provides 128 (16 • 8) individual bits available to software. A bit access is distinguished from a full-register access by the type of instruction. In the SFR area, any register location ending in a 0_H or 8_H is bit addressable. Figure 20 shows details of the on-chip RAM addressing including the locations of individual RAM bits.

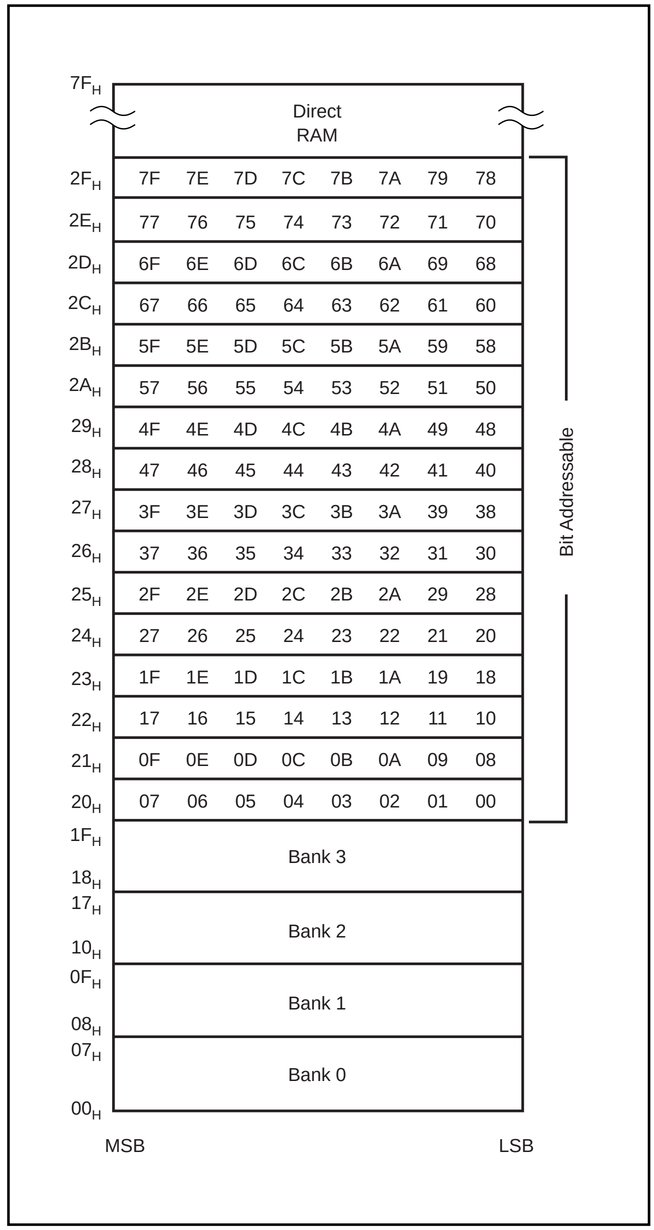


FIGURE 20. Scratchpad Register Addressing.

Working Registers

As part of the lower 128 bytes of RAM, there are four banks of Working Registers, as shown in Figure 20. The Working Registers are general-purpose RAM locations that can be addressed in a special way. They are designated R0 through R7. Since there are four banks, the currently selected bank will be used by any instruction using R0-R7. This allows software to change context by simply switching banks. This is controlled via the Program Status Word register (PSW; $0D0_H$) in the SFR area described below. The 16 bytes immediately above the R0-R7 registers are bit addressable. So any of the 128 bits in this area can be directly accessed using bit addressable instructions.

Stack

Another use of the Scratchpad area is for the programmer's stack. This area is selected using the Stack Pointer (SP; 81_H) SFR. Whenever a call or interrupt is invoked, the return address is placed on the Stack. It also is available to the programmer for variables, etc., since the Stack can be moved and there is no fixed location within the RAM designated as Stack. The Stack Pointer will default to 07_H on reset. The user can then move it as needed. The SP will point to the last used value. Therefore, the next value placed on the Stack is put at SP + 1. Each PUSH or CALL will increment the SP by the appropriate value. Each POP or RET will decrement as well.

Program Memory

After reset, the CPU begins execution from Program Memory location 0000_H. The standard internal Program Memory size for MSC1200 family members is shown in Table V. If enabled the Boot ROM will appear from address $F800_H$ to $FBFF_H$.

MODEL NUMBER	STANDARD INTERNAL PROGRAM MEMORY SIZE (BYTES)
MSC1200Y3	8k
MSC1200Y2	4k

TABLE V. MSC1200 Maximum Internal Program Memory Sizes.

Boot ROM

There is a 1kB Boot ROM that controls operation during serial programming. Additionally, the Boot ROM routines shown in Table VI can be accessed during the user mode if it is enabled. When enabled, the Boot ROM routines will be located at memory addresses $F800_H$-$FBFF_H$ during user mode.

HEX ADDRESS	ROUTINE	C DECLARATIONS	DESCRIPTION
F802	sfr_rd	char sfr_rd(void);	Return SFR value pointed to by CADDR(1)
F805	sfr_wr	void sfr_wr(char d);	Write to SFR pointed to by CADDR(1)
FBD8	monitor_isr	void monitor_isr() interrupt 6;	Push registers and call cmd_parser
FBDA	cmd_parser	void cmd_parser(void);	See SBAA076B.pdf
FBDC	put_string	void put_string(char code *string);	Output string
FBDE	page_erase	char page_erase (int faddr, char fdata, char fdm);	Erase flash page
FBE0	write_flash	Assembly only; DPTR = address, ACC = data	Flash write(2)
FBE2	write_flash_chk	char write_flash_chk (int faddr, char fdata, char fdm);	Write flash byte, verify
FBE4	write_flash_byte	void write_flash_byte (int faddr, char fdata);	Write flash byte(2)
FBE6	faddr_data_read	char faddr_data_read(char faddr);	Read HW config byte from faddr
FBE8	data_x_c_read	char data_x_c_read(int faddr, char fdm);	Read xdata or code byte
FBEA	tx_byte	void tx_byte(char);	Send byte to USART0
FBEC	tx_hex	void tx_hex(char);	Send hex value to USART0
FBEE	putx	void putx(char);	Send "x" to USART0 on R7 = 1
FBF0	rx_byte	char rx_byte(void);	Read byte from USART0
FBF2	rx_byte_echo	char rx_byte_echo(void);	Read and echo byte on USART0
FBF4	rx_hex_echo	char rx_hex_echo(void);	Read and echo hex on USART0
FBF6	rx_hex_dbl_echo	int rx_hex_dbl_echo(void);	Read int as hex and echo: USART0
FBF8	rx_hex_word_echo	int rx_hex_word_echo(void);	Read int reversed as hex and echo: USART0
FBFA	autobaud	void autobaud(void);	Set baud with received CR(3)
FBFC	putspace1	void putspace1(void);	Output 1 space to USART0
FBFE	putcr	void putcr(void);	Output CR, LF to USART0

NOTES: (1) CADDR must be set using the faddr_data_read routine.
(2) MWS register (SFR $8F_H$) defines Data Memory or Program Memory write.
(3) SFR registers CKCON and TCON must be initialized: CKCON = 0x10 and TCON = 0x00.

TABLE VI. MSC1200 Boot ROM Routines.

Serial Flash Programming Mode

Two methods of programming are available: serial programming mode and user application mode. Serial programming mode is initiated by holding the P1.0/$\overline{PROG}$ pin low during POR, as shown in Figure 21. User Application mode also allows for Flash programming. Code execution from Flash Memory cannot occur in this mode while programming, but code execution can occur from Boot ROM while programming.

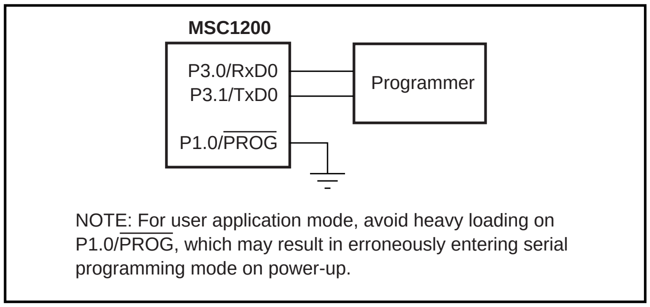


FIGURE 21. Serial Programming Mode.

INTERRUPTS

The MSC1200 uses a three-priority interrupt system. As shown in Table VII, each interrupt source has an independent priority bit, flag, interrupt vector, and enable (except that nine interrupts share the Auxiliary Interrupt (AI) at the highest priority). In addition, interrupts can be globally enabled or disabled. The interrupt structure is compatible with the original 8051 family. All of the standard interrupts are available.

HARDWARE CONFIGURATION MEMORY

The 64 configuration bytes can only be written during the program mode. The bytes are accessed through SFR registers CADDR (SFR 93_H) and CDATA (SFR 94_H). Three of the configuration bytes control Flash partitioning and system control. If the security bit is set, these bits cannot be changed except with a Mass Erase command that erases all of the Flash Memory including the 64 configuration bytes.

INTERRUPT/EVENT	INTERRUPT ADDR	INTERRUPT NUM	PRIORITY	FLAG	INTERRUPT ENABLE	CONTROL
			HIGH			
AV_{DD} Low Voltage Detect	33_H	6	0	ALVDIP (AIPOL.1)(1)	EALV (AIE.1)(1)	N/A
Count (SPI/ I²C)	33_H	6	0	CNTIP (AIPOL.2)(1)	ECNT (AIE.2)(1)	N/A
I²C Start/Stop	33_H	6	0	I2CIP (AIPOL.3)(1)	EI2C (AIE.3)(1)	N/A
Milliseconds Timer	33_H	6	0	MSECIP (AAIPOLIE.4)(1)	EMSEC (AIE.4)(1)	N/A
ADC	33_H	6	0	ADCIP (AIPOL.5)(1)	EADC (AIE .5)(1)	N/A
Summation Register	33_H	6	0	SUMIP (AIPOL.6)(1)	ESUM (AIE.6)(1)	N/A
Seconds Timer	33_H	6	0	SECIP (AIPOL.7)(1)	ESEC (AIE.7)(1)	N/A
External Interrupt 0	03_H	0	1	IE0 (TCON.1)(2)	EX0 (IE.0)(4)	PX0 (IP.0)
Timer 0 Overflow	$0B_H$	1	2	TF0 (TCON.5)(3)	ET0 (IE.1)(4)	PT0 (IP.1)
External Interrupt 1	13_H	2	3	IE1 (TCON.3)(2)	EX1 (IE.2)(4)	PX1 (IP.2)
Timer 1 Overflow	$1B_H$	3	4	TF1 (TCON.7)(3)	ET1 (IE.3)(4)	PT1 (IP.3)
Serial Port 0	23_H	4	5	RI_0 (SCON0.0) TI_0 (SCON0.1)	ES0 (IE.4)(4)	PS0 (IP.4)
External Interrupt 2	43_H	8	6	IE2 (EXIF.4)	EX2 (EIE.0)(4)	PX2 (EIP.0)
External Interrupt 3	$4B_H$	9	7	IE3 (EXIF.5)	EX3 (EIE.1)(4)	PX3 (EIP.1)
External Interrupt 4	53_H	10	8	IE4 (EXIF.6)	EX4 (EIE.2)(4)	PX4 (EIP.2)
External Interrupt 5	$5B_H$	11	9	IE5 (EXIF.7)	EX5 (EIE.3)(4)	PX5 (EIP.3)
Watchdog	63_H	12	10 LOW	WDTI (EICON.3)	EWDI (EIE.4)(4)	PWDI (EIP.4)

NOTES: (1) These interrupts set the AI flag (EICON.4) and are enabled by EAI (EICON.5). (2) If edge triggered, cleared automatically by hardware when the service routine is vectored to. If level triggered, the flag follows the state of the pin. (3) Cleared automatically by hardware when interrupt vector occurs. (4) Globally enabled by EA (IE.7).

TABLE VII. Interrupt Summary.

Hardware Configuration Register 0 (HCR0)—Accessed Using SFR Registers CADDR and CDATA.

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CADDR $3F_H$	EPMA	PML	RSL	EBR	EWDR	1	DFSEL1	DFSEL0

To read this register during normal operation, refer to the register descriptions for CADDR and CDATA.

EPMA **Enable Programming Memory Access (Security Bit).**
bit 7 0: After reset in programming modes, Flash Memory can only be accessed in UAM mode until a mass erase is done.
1: Fully Accessible (default)

PML **Program Memory Lock (PML has Priority Over RSL).**
bit 6 0: Enable all Flash Programming Modes in Program Memory; can be written in UAM.
1: Enable read only for Program Memory; cannot be written in UAM (default).

RSL **Reset Sector Lock.** The reset sector can be used to provide another method of Flash Memory programming. This
bit 5 will allow Program Memory updates without changing the jumpers for in-circuit code updates or program development. The code in this boot sector would then provide the monitor and programming routines with the ability to jump into the main Flash code when programming is finished.
0: Enable Reset Sector Writing
1: Enable Read Only Mode for Reset Sector (4kB) (default)

EBR **Enable Boot ROM.** Boot ROM is 1kB of code located in ROM, not to be confused with the 4kB Boot Sector located
bit 4 in Flash Memory.
0: Disable Internal Boot ROM
1: Enable Internal Boot ROM (default)

EWDR **Enable Watchdog Reset.**
bit 3 0: Disable Watchdog Reset
1: Enable Watchdog Reset (default)

DFSEL1-0 Data Flash Memory Size (see Table II).
bits 1-0 00: 4kB Data Flash Memory (MSC1200Y3 Only)
01: 2kB Data Flash Memory
10: 1kB Data Flash Memory
11: No Data Flash Memory (default)

Hardware Configuration Register 1 (HCR1)

	7	6	5	4	3	2	1	0
CADDR $3E_H$	1	1	1	1	1	DDB	1	1

To read this register during normal operation, refer to the register descriptions for CADDR and CDATA.

DDB **Disable Digital Brownout Detection**
bit 2 0: Enable Digital Brownout Detection (2.7V)
1: Disable Digital Brownout Detection (default)

Hardware Configuration Register 2 (HCR2)

	7	6	5	4	3	2	1	0
CADDR $3D_H$	0	0	0	0	0	CLKSEL2	CLKSEL1	CLKSEL0

To read this register during normal operation, refer to the register descriptions for CADDR and CDATA.

CLKSEL2-0 **Clock Select**
bits 2-0 000: Reserved
001: Reserved
010: Reserved
011: External Clock Mode
100: PLL High-Frequency (HF) Mode
101: PLL Low-Frequency (LF) Mode
110: Internal Oscillator High-Frequency (HF) Mode
111: Internal Oscillator Low-Frequency (LF) Mode

Configuration Memory Programming

Certain key functions such as Brownout Reset and Watchdog Timer are controlled by the hardware configuration bits. These bits are nonvolatile and can only be changed through serial flash programming. Other peripheral control and status functions, such as ADC configuration timer setup, and Flash control are controlled through the SFRs.

SFR Definitions

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUES
80_H										
81_H	SP									07_H
82_H	DPL0									00_H
83_H	DPH0									00_H
84_H	DPL1									00_H
85_H	DPH1									00_H
86_H	DPS	0	0	0	0	0	0	0	SEL	00_H
87_H	PCON	SMOD	0	1	1	GF1	GF0	STOP	IDLE	30_H
88_H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00_H
89_H	TMOD	|--------------------------Timer 1 -------------------------|				|-------------------------Timer 0 --------------------------|				00_H
		GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	
$8A_H$	TL0									00_H
$8B_H$	TL1									00_H
$8C_H$	TH0									00_H
$8D_H$	TH1									00_H
$8E_H$	CKCON	0	0	0	T1M	T0M	MD2	MD1	MD0	01_H
$8F_H$	MWS	0	0	0	0	0	0	0	MXWS	00_H
90_H	P1	P1.7 $\overline{INT5}$	P1.6 INT4	P1.5 $\overline{INT3}$	P1.4 INT2/$\overline{SS}$	P1.3 DIN	P1.2 DOUT	P1.1	P1.0	FF_H
91_H	EXIF	IE5	IE4	IE3	IE2	1	0	0	0	08_H
92_H										
93_H	CADDR									00_H
94_H	CDATA									00_H
95_H										
96_H										
97_H										
98_H	SCON0	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00_H
99_H	SBUF0									00_H
$9A_H$	SPICON I2CCON	SBIT3 SBIT3	SBIT2 SBIT2	SBIT1 SBIT1	SBIT0 SBIT0	ORDER STOP	CPHA START	ESS DCS	CPOL CNTSEL	00_H
$9B_H$	SPIDATA I2CDATA									00_H
$9C_H$										
$9D_H$										
$9E_H$										
$9F_H$										
$A0_H$										
$A1_H$										
$A2_H$										
$A3_H$										
$A4_H$	AIPOL	SECIP	SUMIP	ADCIP	MSECIP	I2CIP	CNTIP	ALVDIP	0	00_H
$A5_H$	PAI	0	0	0	0	PAI3	PAI2	PAI1	PAI0	00_H
$A6_H$	AIE	ESEC	ESUM	EADC	EMSEC	EI2C	ECNT	EALV	0	00_H
$A7_H$	AISTAT	SEC	SUM	ADC	MSEC	I2C	CNT	ALVD	0	00_H
$A8_H$	IE	EA	0	0	ES0	ET1	EX1	ET0	EX0	00_H
$A9_H$										
AA_H										
AB_H										
AC_H										
AD_H										
AE_H	P1DDRL	P13H	P13L	P12H	P12L	P11H	P11L	P10H	P10L	00_H
AF_H	P1DDRH	P17H	P17L	P16H	P16L	P15H	P15L	P14H	P14L	00_H
$B0_H$	P3	P3.7	P3.6 SCK/SCL/CLKS	P3.5 T1	P3.4 T0	P3.3 $\overline{INT1}$	P3.2 $\overline{INT0}$	P3.1 TXD0	P3.0 RXD0	FF_H
$B1_H$										
$B2_H$										
$B3_H$	P3DDRL	P33H	P33L	P32H	P32L	P31H	P31L	P30H	P30L	00_H
$B4_H$	P3DDRH	P37H	P37L	P36H	P36L	P35H	P35L	P34H	P34L	00_H
$B5_H$	IDAC									00_H
$B6_H$										
$B7_H$										
$B8_H$	IP	1	0	0	PS0	PT1	PX1	PT0	PX0	80_H
$B9_H$										
BA_H										
BB_H										
BC_H										
BD_H										
BE_H										

SFR Definitions (Cont.)

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUES
BF$_H$										
C0$_H$										
C1$_H$										
C2$_H$										
C3$_H$										
C4$_H$										
C5$_H$										
C6$_H$	EWU						EWUWDT	EWUEX1	EWUEX0	00$_H$
C7$_H$	SYSCLK	0	0	DIVMOD1	DIVMOD0	0	DIV2	DIV1	DIV0	00$_H$
C8$_H$										
C9$_H$										
CA$_H$										
CB$_H$										
CC$_H$										
CD$_H$										
CE$_H$										
CF$_H$										
D0$_H$	PSW	CY	AC	F0	RS1	RS0	OV	F1	P	00$_H$
D1$_H$	OCL								LSB	00$_H$
D2$_H$	OCM									00$_H$
D3$_H$	OCH	MSB								00$_H$
D4$_H$	GCL								LSB	5A$_H$
D5$_H$	GCM									EC$_H$
D6$_H$	GCH	MSB								5F$_H$
D7$_H$	ADMUX	INP3	INP2	INP1	INP0	INN3	INN2	INN1	INN0	01$_H$
D8$_H$	EICON	0	1	EAI	AI	WDTI	0	0	0	40$_H$
D9$_H$	ADRESL								LSB	00$_H$
DA$_H$	ADRESM									00$_H$
DB$_H$	ADRESH	MSB								00$_H$
DC$_H$	ADCON0	—	BOD	EVREF	VREFH	EBUF	PGA2	PGA1	PGA0	30$_H$
DD$_H$	ADCON1	OF_UF	POL	SM1	SM0	—	CAL2	CAL1	CAL0	00$_H$
DE$_H$	ADCON2	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	1B$_H$
DF$_H$	ADCON3	0	0	0	0	0	DR10	DR9	DR8	06$_H$
E0$_H$	ACC									00$_H$
E1$_H$	SSCON	SSCON1	SSCON0	SCNT2	SCNT1	SCNT0	SHF2	SHF1	SHF0	00$_H$
E2$_H$	SUMR0								LSB	00$_H$
E3$_H$	SUMR1									00$_H$
E4$_H$	SUMR2									00$_H$
E5$_H$	SUMR3	MSB								00$_H$
E6$_H$	ODAC									00$_H$
E7$_H$	LVDCON	ALVDIS	0	0	0	1	1	1	1	8F$_H$
E8$_H$	EIE	1	1	1	EWDI	EX5	EX4	EX3	EX2	E0$_H$
E9$_H$	HWPC0	0	0	0	0	0	0	0	MEMORY	0000_000x$_B$
EA$_H$	HWPC1	0	0	1	0	0	0	0	0	20$_H$
EB$_H$	HWVER									
EC$_H$	Reserved									
ED$_H$	Reserved									
EE$_H$	FMCON	0	PGERA	0	FRCM	0	BUSY	1	0	02$_H$
EF$_H$	FTCON	FER3	FER2	FER1	FER0	FWR3	FWR2	FWR1	FWR0	A5$_H$
F0$_H$	B									00$_H$
F1$_H$	PDCON	PDICLK	PDIDAC	PDI2C	0	PDADC	PDWDT	PDST	PDSPI	6F$_H$
F2$_H$	PASEL	PSEN4	PSEN3	PSEN2	PSEN1	PSEN0	0	0	0	00$_H$
F3$_H$	Reserved									
F4$_H$	PLLL	PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0	C1$_H$
F5$_H$	PLLH	CLKSTAT2	CLKSTAT1	CLKSTAT0	PLLLOCK	0	0	PLL9	PLL8	x1$_H$
F6$_H$	ACLK	0	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03$_H$
F7$_H$	SRST	0	0	0	0	0	0	0	RSTREQ	00$_H$
F8$_H$	EIP	1	1	1	PWDI	PX5	PX4	PX3	PX2	E0$_H$
F9$_H$	SECINT	WRT	SECINT6	SECINT5	SECINT4	SECINT3	SECINT2	SECINT1	SECINT0	7F$_H$
FA$_H$	MSINT	WRT	MSINT6	MSINT5	MSINT4	MSINT3	MSINT2	MSINT1	MSINT0	7F$_H$
FB$_H$	USEC	0	0	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03$_H$
FC$_H$	MSECL	MSECL7	MSECL6	MSECL5	MSECL4	MSECL3	MSECL2	MSECL1	MSECL0	9F$_H$
FD$_H$	MSECH	MSECH7	MSECH6	MSECH5	MSECH4	MSECH3	MSECH2	MSECH1	MSECH0	0F$_H$
FE$_H$	HMSEC	HMSEC7	HMSEC6	HMSEC5	HMSEC4	HMSEC3	HMSEC2	HMSEC1	HMSEC0	63$_H$
FF$_H$	WDTCON	EWDT	DWDT	RWDT	WDCNT4	WDCNT3	WDCNT2	WDCNT1	WDCNT0	00$_H$

Stack Pointer (SP)

	7	6	5	4	3	2	1	0	Reset Value
SFR 81_H	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	07_H

SP.7-0 bits 7-0 **Stack Pointer**. The stack pointer identifies the location where the stack will begin. The stack pointer is incremented before every PUSH or CALL operation and decremented after each POP or RET/RETI. This register defaults to 07_H after reset.

Data Pointer Low 0 (DPL0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 82_H	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0	00_H

DPL0.7-0 bits 7-0 **Data Pointer Low 0**. This register is the low byte of the standard 8051 16-bit data pointer. DPL0 and DPH0 are used to point to non-scratchpad data RAM. The current data pointer is selected by DPS (SFR 86_H).

Data Pointer High 0 (DPH0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 83_H	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0	00_H

DPH0.7-0 bits 7-0 **Data Pointer High 0.** This register is the high byte of the standard 8051 16-bit data pointer. DPL0 and DPH0 are used to point to non-scratchpad data RAM. The current data pointer is selected by DPS (SFR 86_H).

Data Pointer Low 1 (DPL1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 84_H	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0	00_H

DPL1.7-0 bits 7-0 **Data Pointer Low 1**. This register is the low byte of the auxiliary 16-bit data pointer. When the SEL bit (DPS.0) (SFR 86_H) is set, DPL1 and DPH1 are used in place of DPL0 and DPH0 during DPTR operations.

Data Pointer High 1 (DPH1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 85_H	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0	00_H

DPH1.7-0 bits 7-0 **Data Pointer High.** This register is the high byte of the auxiliary 16-bit data pointer. When the SEL bit (DPS.0) (SFR 86_H) is set, DPL1 and DPH1 are used in place of DPL0 and DPH0 during DPTR operations.

Data Pointer Select (DPS)

	7	6	5	4	3	2	1	0	Reset Value
SFR 86_H	0	0	0	0	0	0	0	SEL	00_H

SEL bit 0 **Data Pointer Select.** This bit selects the active data pointer.
0: Instructions that use the DPTR will use DPL0 and DPH0.
1: Instructions that use the DPTR will use DPL1 and DPH1.

Power Control (PCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 87_H	SMOD	0	1	1	GF1	GF0	STOP	IDLE	30_H

SMOD bit 7 — **Serial Port 0 Baud Rate Doubler Enable.** The serial baud rate doubling function for Serial Port 0.
0: Serial Port 0 baud rate will be a standard baud rate.
1: Serial Port 0 baud rate will be double that defined by baud rate generation equation.

GF1 bit 3 — **General-Purpose User Flag 1.** This is a general-purpose flag for software control.

GF0 bit 2 — **General-Purpose User Flag 0.** This is a general-purpose flag for software control.

STOP bit 1 — **Stop Mode Select.** Setting this bit will halt the oscillator and block external clocks. This bit will always read as a 0. Exit with RESET. In this mode, internal peripherals are frozen and I/O pins are held in their current state. The ADC is frozen, but IDAC and VREF remain active.

IDLE bit 0 — **Idle Mode Select.** Setting this bit will freeze the CPU, Timer 0 and 1, and the USART; other peripherals remain active. This bit will always be read as a 0. Exit with AIE ($A6_H$) and EWU ($C6_H$) interrupts (refer to Figure 4 for clocks affected during IDLE).

Timer/Counter Control (TCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 88_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00_H

TF1 bit 7 — **Timer 1 Overflow Flag.** This bit indicates when Timer 1 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow has been detected.
1: Timer 1 has overflowed its maximum count.

TR1 — **Timer 1 Run Control.** This bit enables/disables the operation of Timer 1. Halting this timer will preserve the current bit 6 count in TH1, TL1.
0: Timer is halted.
1: Timer is enabled.

TF0 bit 5 — **Timer 0 Overflow Flag.** This bit indicates when Timer 0 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow has been detected.
1: Timer 0 has overflowed its maximum count.

TR0 bit 4 — **Timer 0 Run Control.** This bit enables/disables the operation of Timer 0. Halting this timer will preserve the current count in TH0, TL0.
0: Timer is halted.
1: Timer is enabled.

IE1 bit 3 — **Interrupt 1 Edge Detect.** This bit is set when an edge/level of the type defined by IT1 is detected. If IT1 = 1, this bit will remain set until cleared in software or the start of the External Interrupt 1 service routine. If IT1 = 0, this bit will inversely reflect the state of the $\overline{INT1}$ pin.

IT1 bit 2 — **Interrupt 1 Type Select.** This bit selects whether the $\overline{INT1}$ pin will detect edge or level triggered interrupts.
0: $\overline{INT1}$ is level triggered.
1: $\overline{INT1}$ is edge triggered.

IE0 bit 3 — **Interrupt 0 Edge Detect.** This bit is set when an edge/level of the type defined by IT0 is detected. If IT0 = 1, this bit will remain set until cleared in software or the start of the External Interrupt 0 service routine. If IT0 = 0, this bit will inversely reflect the state of the $\overline{INT0}$ pin.

IT0 bit 2 — **Interrupt 0 Type Select.** This bit selects whether the $\overline{INT0}$ pin will detect edge or level triggered interrupts.
0: $\overline{INT0}$ is level triggered.
1: $\overline{INT0}$ is edge triggered.

Timer Mode Control (TMOD)

	7	6	5	4	3	2	1	0	Reset Value
	TIMER 1				TIMER 0				
SFR 89_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00_H

GATE bit 7 — **Timer 1 Gate Control.** This bit enables/disables the ability of Timer 1 to increment.
0: Timer 1 will clock when TR1 = 1, regardless of the state of pin $\overline{\text{INT1}}$.
1: Timer 1 will clock only when TR1 = 1 and pin $\overline{\text{INT1}}$ = 1.

C/$\overline{T}$ bit 6 — **Timer 1 Counter/Timer Select.**
0: Timer is incremented by internal clocks.
1: Timer is incremented by pulses on T1 pin when TR1 (TCON.6, SFR 88_H) is 1.

M1, M0 bits 5-4 — **Timer 1 Mode Select.** These bits select the operating mode of Timer 1.

M1	M0	MODE
0	0	Mode 0: 8-bit counter with 5-bit prescale.
0	1	Mode 1: 16 bits.
1	0	Mode 2: 8-bit counter with auto reload.
1	1	Mode 3: Two 8-bit counters.

GATE bit 3 — **Timer 0 Gate Control.** This bit enables/disables the ability of Timer 0 to increment.
0: Timer 0 will clock when TR0 = 1, regardless of the state of pin $\overline{\text{INT0}}$ (software control).
1: Timer 0 will clock only when TR0 = 1 and pin $\overline{\text{INT0}}$ = 1 (hardware control).

C/$\overline{T}$ bit 2 — **Timer 0 Counter/Timer Select.**
0: Timer is incremented by internal clocks.
1: Timer is incremented by pulses on pin T0 when TR0 (TCON.4, SFR 88_H) is 1.

M1, M0 bits 1-0 — **Timer 0 Mode Select.** These bits select the operating mode of Timer 0.

M1	M0	MODE
0	0	Mode 0: 8-bit counter with 5-bit prescale.
0	1	Mode 1: 16 bits.
1	0	Mode 2: 8-bit counter with auto reload.
1	1	Mode 3: Two 8-bit counters.

Timer 0 LSB (TL0)

	7	6	5	4	3	2	1	0	Reset Value
SFR $8A_H$	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0	00_H

TL0.7-0 bits 7-0 — **Timer 0 LSB.** This register contains the least significant byte of Timer 0.

Timer 1 LSB (TL1)

	7	6	5	4	3	2	1	0	Reset Value
SFR $8B_H$	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0	00_H

TL1.7-0 bits 7-0 — **Timer 1 LSB.** This register contains the least significant byte of Timer 1.

Timer 0 MSB (TH0)

	7	6	5	4	3	2	1	0	Reset Value
SFR $8C_H$	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0	00_H

TH0.7-0 bits 7-0 — **Timer 0 MSB.** This register contains the most significant byte of Timer 0.

Timer 1 MSB (TH1)

	7	6	5	4	3	2	1	0	Reset Value
SFR $8D_H$	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	00_H

TH1.7-0 **Timer 1 MSB.** This register contains the most significant byte of Timer 1.
bits 7-0

Clock Control (CKCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $8E_H$	0	0	0	T1M	T0M	MD2	MD1	MD0	01_H

T1M bit 4 — **Timer 1 Clock Select.** This bit controls the division of the system clock that drives Timer 1. Clearing this bit to 0 maintains 8051 compatibility. This bit has no effect on instruction cycle timing.
0: Timer 1 uses a divide by 12 of the crystal frequency.
1: Timer 1 uses a divide by 4 of the crystal frequency.

T0M bit 3 — **Timer 0 Clock Select.** This bit controls the division of the system clock that drives Timer 0. Clearing this bit to 0 maintains 8051 compatibility. This bit has no effect on instruction cycle timing.
0: Timer 0 uses a divide by 12 of the crystal frequency.
1: Timer 0 uses a divide by 4 of the crystal frequency.

MD2, MD1, MD0 bit 3 — **Stretch MOVX Select.** These bits select the time by which MOVX cycles are to be stretched. Since the MSC1200 does not allow external memory access, these bits should be set to 000_B to allow for the fastest flash data memory access.

	7	6	5	4	3	2	1	0	Reset Value
SFR $8F_H$	0	0	0	0	0	0	0	MXWS	00_H

Memory Write Select (MWS)

MXWS bit 0 — **MOVX Write Select.** This allows writing to the internal Flash program memory.
0: No writes are allowed to the internal Flash program memory.
1: Writing is allowed to the internal Flash program memory, unless PML (HCR0) or RSL (HCR0) are on.

Port 1 (P1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 90_H	P1.7 $\overline{\text{INT5}}$	P1.6 INT4	P1.5 $\overline{\text{INT3}}$	P1.4 INT2/$\overline{\text{SS}}$	P1.3 DIN	P1.2 DOUT	P1.1	P1.0 $\overline{\text{PROG}}$	FF_H

P1.7-0 bits 7-0 — **General-Purpose I/O Port 1.** This register functions as a general-purpose I/O port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 1 latch bit must contain a logic ‘1’ before the pin can be used in its alternate function capacity. To use the alternate function, set the appropriate mode in P1DDRL (SFR AE_H), P1DDRH (SFR AF_H).

$\overline{\text{INT5}}$ bit 7 — **External Interrupt 5.**A falling edge on this pin will cause an external interrupt 5 if enabled.

INT4 bit 6 — **External Interrupt 4.** A rising edge on this pin will cause an external interrupt 4 if enabled.

$\overline{\text{INT3}}$ bit 5 — **External Interrupt 3.** A falling edge on this pin will cause an external interrupt 3 if enabled.

INT2/$\overline{\text{SS}}$ bit 4 — **External Interrupt 2.** A rising edge on this pin will cause an external interrupt 2 if enabled. This pin can be used as slave select ($\overline{\text{SS}}$) in SPI slave mode.

DIN bit 3 — **Serial Data In.** This pin receives serial data in SPI and I^2C modes (in I^2C mode, this pin should be configured as an input) or standard 8051.

DOUT bit 2 — **Serial Data Out.** This pin transmits serial data in SPI and I^2C modes (in I^2C mode, this pin should be configured as an open drain) or standard 8051.

$\overline{\text{PROG}}$ bit 0 — **Program Mode.** When this pin is pulled low at power-up, the device enters Serial Programming mode (refer to Figure B).

External Interrupt Flag (EXIF)

	7	6	5	4	3	2	1	0	Reset Value
SFR 91_H	IE5	IE4	IE3	IE2	1	0	0	0	08_H

IE5 bit 7 — **External Interrupt 5 Flag.** This bit will be set when a falling edge is detected on $\overline{INT5}$. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE4 bit 6 — **External Interrupt 4 Flag.** This bit will be set when a rising edge is detected on INT4. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE3 bit 5 — **External Interrupt 3 Flag.** This bit will be set when a falling edge is detected on $\overline{INT3}$. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE2 bit 4 — **External Interrupt 2 Flag.** This bit will be set when a rising edge is detected on INT2. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

Configuration Address Register (CADDR) (write only)

	7	6	5	4	3	2	1	0	Reset Value
SFR 93_H									00_H

CADDR bits 7-0 — **Configuration Address Register.** This register supplies the address for reading bytes in the 64 bytes of Flash Configuration Memory. Always use the Boot ROM CADDR access routine. This register is also used for SFR read and write routines.

WARNING: If this register is written to while executing from Flash Memory, the CDATA register will be incorrect.

Configuration Data Register (CDATA)

	7	6	5	4	3	2	1	0	Reset Value
SFR 94_H									00_H

CDATA bits 7-0 — **Configuration Data Register.** This register will contain the data in the 64 bytes of Flash Configuration Memory that is located at the last written address in the CADDR register. This is a read-only register.

Serial Port 0 Control (SCON0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 98_H	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00_H

SM0-2
bits 7-5

Serial Port 0 Mode. These bits control the mode of serial Port 0. Modes 1, 2, and 3 have 1 start and 1 stop bit in addition to the 8 or 9 data bits.

MODE	SM0	SM1	SM2	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	12 p_{CLK}(1)
0	0	0	1	Synchronous	8 bits	4 p_{CLK}(1)
1	0	1	0	Asynchronous	10 bits	Timer 1 Baud Rate Equation
1	0	1	1	Asynchronous—Valid Stop Required(2)	10 bits	Timer 1 Baud Rate Equation
2	1	0	0	Asynchronous	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
2	1	0	1	Asynchronous with Multiprocessor Communication	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
3	1	1	0	Asynchronous	11 bits	Timer 1 Baud Rate Equation
3	1	1	1	Asynchronous with Multiprocessor Communication(3)	11 bits	Timer 1 Baud Rate Equation

NOTES: (1) p_{CLK} will be equal to t_{CLK}, except that p_{CLK} will stop for IDLE. (2) RI_0 will only be activated when a valid stop is received. (3) RI_0 will not be activated if bit 9 = 0.

REN_0
bit 4

Receive Enable. This bit enables/disables the serial Port 0 received shift register.
0: Serial Port 0 reception disabled.
1: Serial Port 0 received enabled (modes 1, 2, and 3). Initiate synchronous reception (mode 0).

TB8_0
bit 3

9th Transmission Bit State. This bit defines the state of the 9th transmission bit in serial Port 0 modes 2 and 3.

RB8_0
bit 2

9th Received Bit State. This bit identifies the state of the 9th reception bit of received data in serial Port 0 modes 2 and 3. In serial port mode 1, when SM2_0 = 0, RB8_0 is the state of the stop bit. RB8_0 is not used in mode 0.

TI_0
bit 1

Transmitter Interrupt Flag. This bit indicates that data in the serial Port 0 buffer has been completely shifted out. In serial port mode 0, TI_0 is set at the end of the 8th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be manually cleared by software.

RI_0
bit 0

Receiver Interrupt Flag. This bit indicates that a byte of data has been received in the serial Port 0 buffer. In serial port mode 0, RI_0 is set at the end of the 8th bit. In serial port mode 1, RI_0 is set after the last sample of the incoming stop bit subject to the state of SM2_0. In modes 2 and 3, RI_0 is set after the last sample of RB8_0. This bit must be manually cleared by software.

Serial Data Buffer 0 (SBUF0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 99_H									00_H

SBUF0
bits 7-0

Serial Data Buffer 0. Data for Serial Port 0 is read from or written to this location. The serial transmit and receive buffers are separate registers, but both are addressed at this location.

SPI Control (SPICON) (SERSEL bit determines SPICON control)

	7	6	5	4	3	2	1	0	Reset Value
SFR $9A_H$	SBIT3	SBIT2	SBIT1	SBIT0	ORDER	CPHA	ESS	CPOL	00_H

SBIT3-0 bits 7-4 — **Serial Bit Count.** Number of bits transferred (read only).

SBIT3:0	COUNT
0x00	0
0x01	1
0x03	2
0x02	3
0x06	4
0x07	5
0x05	6
0x04	7
0x0C	8

ORDER bit 3 — **Set Bit Order for Transmit and Receive.**
0: Most Significant Bits First
1: Least Significant Bits First

CPHA bit 2 — **Serial Clock Phase Control.**
0: Valid data starting from half SCK period before the first edge of SCK
1: Valid data starting from the first edge of SCK

ESS bit 1 — **Enable Slave Select.**
0: $\overline{SS}$ (P1.4) is configured as a general-purpose I/O (default).
1: $\overline{SS}$ (P1.4) is configured as $\overline{SS}$ for SPI mode. DOUT (P1.2) drives when $\overline{SS}$ is low, and DOUT (P1.2) is high-impedance when $\overline{SS}$ is high.

CPOL bit 0 — **Serial Clock Polarity.**
0: SCK idle at logic LOW
1: SCK idle at logic HIGH

I²C Control (I2CCON) (SERSEL bit determines I2CCON control)

	7	6	5	4	3	2	1	0	Reset Value
SFR $9A_H$	SBIT3	SBIT2	SBIT1	SBIT0	STOP	START	DCS	CNTSEL	00_H

SBIT3-0 bits 7-4 — **Serial Bit Count.** Number of bits transferred (read only).

SBIT3:0	COUNT
0x00	0
0x01	1
0x03	2
0x02	3
0x06	4
0x07	5
0x05	6
0x04	7
0x0C	8

STOP bit 3 — **Stop-Bit Status.**
0: No Stop
1: Stop Condition Received and I2CCNT set (cleared on write to I2CDATA)

START bit 2 — **Start-Bit Status**.
0: No Stop
1: Start or Repeated Start Condition Received and I2CCNT set (cleared on write to I2CDATA)

DCS bit 1 — **Disable Serial Clock Stretch.**
0: Enable SCL Stretch (cleared by firmware or START condition)
1: Disable SCL Stretch

CNTSEL bit 0 — **Counter Select.**
0: Counter IRQ Set for Bit Counter = 8 (default)
1: Counter IRQ Set for Bit Counter = 1

SPI Data Register (SPIDATA) / I²C Data Register (I2CDATA)

	7	6	5	4	3	2	1	0	Reset Value
SFR $9B_H$									00_H

SPIDATA bits 7-0 — **SPI Data Register.** Data for SPI is read from or written to this location. The SPI transmit and receive buffers are separate registers, but both are addressed at this location.

I2CDATA bits 7-0 — **I2C Data Register.** Data for I²C is read from or written to this location. The I²C transmit and receive buffers are separate registers, but both are addressed at this location.

Auxilliary Interrupt Poll (AIPOL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A4_H$	SECIP	SUMIP	ADCIP	MSECIP	I2CIP	CNTIP	ALVDIP	Unused	00_H

SECIP bit 7 — **Second System Timer Interrupt Poll (before IRQ masking).**
0 = Seconds System Timer Interrupt Poll Inactive
1 = Seconds System Timer Interrupt Poll Active

SUMIP bits 6 — **Accumulator Interrupt Poll (before IRQ masking).**
0 = Accumulator Interrupt Poll Inactive
1 = Accumulator Interrupt Poll Active

ADCIP bits 5 — **ADC Interrupt Poll (before IRQ masking).**
0 = ADC Interrupt Poll Inactive
1 = ADC Interrupt Poll Active

MSECIP bits 4 — **Millisecond System Timer Interrupt Poll (before IRQ masking).**
0 = Millisecond System Timer Interrupt Poll Inactive
1 = Millisecond System Timer Interrupt Poll Active

I2CIP bits 3 — **I²C Interrupt Poll (before IRQ masking).**
0 = I²C Interrupt Poll Inactive
1 = I²C Interrupt Poll Active

CNTIP bits 2 — **Serial Bit Count Interrupt Poll (before IRQ masking).**
0 = Serial Bit Count Interrupt Poll Inactive
1 = Serial Bit Count Interrupt Poll Active

ALVDIP bits 1 — **Analog Low Voltage Detect Interrupt Poll (before IRQ masking).**
0 = Analog Low Voltage Detect Interrupt Poll Inactive
1 = Analog Low Voltage Detect Interrupt Poll Active

Pending Auxiliary Interrupt (PAI)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A5_H$	0	0	0	0	PAI3	PAI2	PAI1	PAI0	00_H

PAI bits 3-0 — **Pending Auxiliary Interrupt Register.** The results of this register can be used as an index to vector to the appropriate interrupt routine. All of these interrupts vector through address 0033_H.

PAI3	PAI2	PAI1	PAI0	AUXILIARY INTERRUPT STATUS
0	0	0	0	No Pending Auxiliary IRQ
0	0	0	1	Reserved
0	0	1	0	Analog Low Voltage Detect IRQ and Possible Lower Priority Pending
0	0	1	1	I^2C IRQ and Possible Lower Priority Pending
0	1	0	0	Serial Bit Count Interrupt and Possible Lower Priority Pending
0	1	0	1	Millisecond System Timer IRQ and Possible Lower Priority Pending
0	1	1	0	ADC IRQ and Possible Lower Priority Pending
0	1	1	1	Accumulator IRQ and Possible Lower Priority Pending
1	0	0	0	Second System Timer IRQ and Possible Lower Priority Pending

Auxiliary Interrupt Enable (AIE)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A6_H$	ESEC	ESUM	EADC	EMSEC	EI2C	ECNT	EALV	0	00_H

Interrupts are enabled by EICON.4 (SFR $D8_H$). The other interrupts are controlled by the IE and EIE registers.

ESEC bit 7 — **Enable Second System Timer Interrupt (lowest priority auxiliary interrupt).**
Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **Second Timer Interrupt** mask.

ESUM bit 6 — **Enable Summation Interrupt.**
Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **Summation Interrupt** mask.

EADC bit 5 — **Enable ADC Interrupt.**
Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **ADC Interrupt** mask.

EMSEC bit 4 — **Enable Millisecond System Timer Interrupt.**
Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **Millisecond System Timer Interrupt** mask.

EI2C bit 3 — **Enable I^2C Start/Stop Bit.**
Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **I^2C Start/Stop Bit** mask.

ECNT bit 2 — **Enable Serial Bit Count Interrupt.**
Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **Serial Bit Count Interrupt** mask.

EALV bit 1 — **Enable Analog Low Voltage Interrupt.**
Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **Analog Low Voltage Detect Interrupt** mask.

Auxiliary Interrupt Status Register (AISTAT)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A7_H$	SEC	SUM	ADC	MSEC	I2C	CNT	ALVD	0	00_H

SEC **Second System Timer Interrupt Status Flag (lowest priority AI).**
bit 7
0: SEC Interrupt cleared or masked.
1: SEC Interrupt active (it is cleared by reading SECINT, SFR $F9_H$).

SUM **Summation Register Interrupt Status Flag.**
bit 6
0: SUM Interrupt cleared or masked.
1: SUM Interrupt active (it is cleared by reading the lowest byte of SUMR0, SFR $E2_H$).

ADC **ADC Interrupt Status Flag.**
bit 5
0: ADC Interrupt cleared or masked.
1: ADC Interrupt active (it is cleared by reading the lowest byte of ADRESL, SFR $D9_H$; if active, no new data will be written to the ADC Results registers).

MSEC **Millisecond System Timer Interrupt Status Flag.**
bit 4
0: MSEC Interrupt cleared or masked.
1: MSEC Interrupt active (it is cleared by reading MSINT, SFR FA_H).

I2C **I^2C Start/Stop Interrupt Status Flag.**
bit 3
0: I^2C Start/stop Interrupt cleared or masked.
1: I^2C Start/stop Interrupt active (it is cleared by writing to I2CDATA, SFR $9B_H$).

CNT **CNT Interrupt Status Flag.**
bit 2
0: CNT Interrupt cleared or masked.
1: CNT Interrupt active (it is cleared by reading from or writing to SPIDATA/I2CDATA, SFR $9B_H$).

ALVD **Analog Low Voltage Detect Interrupt Status Flag.**
bit 1
0: ALVD Interrupt cleared or masked.
1: ALVD Interrupt active (cleared in HW if AV_{DD} exceeds ALVD threshold).

NOTE: If an interrupt is masked, the status can be read in AIPOL, SFR $A4_H$.

	7	6	5	4	3	2	1	0	Reset Value
SFR $A8_H$	EA	0	0	ES0	ET1	EX1	ET0	EX0	00_H

Interrupt Enable (IE)

EA **Global Interrupt Enable.** This bit controls the global masking of all interrupts except those in AIE (SFR $A6_H$).
bit 7
0: Disable interrupt sources. This bit overrides individual interrupt mask settings for this register.
1: Enable all individual interrupt masks. Individual interrupts in this register will occur if enabled.

ES0 **Enable Serial port 0 interrupt.** This bit controls the masking of the serial Port 0 interrupt.
bit 4
0: Disable all serial Port 0 interrupts.
1: Enable interrupt requests generated by the RI_0 (SCON0.0, SFR 98_H) or TI_0 (SCON0.1, SFR 98_H) flags.

ET1 **Enable Timer 1 Interrupt.** This bit controls the masking of the Timer 1 interrupt.
bit 3
0: Disable Timer 1 interrupt.
1: Enable interrupt requests generated by the TF1 flag (TCON.7, SFR 88_H).

EX1 **Enable External Interrupt 1.** This bit controls the masking of external interrupt 1.
bit 2
0: Disable external interrupt 1.
1: Enable interrupt requests generated by the $\overline{INT1}$ pin.

ET0 **Enable Timer 0 Interrupt.** This bit controls the masking of the Timer 0 interrupt.
bit 1
0: Disable all Timer 0 interrupts.
1: Enable interrupt requests generated by the TF0 flag (TCON.5, SFR 88_H).

EX0 **Enable External Interrupt 0.** This bit controls the masking of external interrupt 0.
bit 0
0: Disable external interrupt 0.
1: Enable interrupt requests generated by the $\overline{INT0}$ pin.

Port 1 Data Direction Low Register (P1DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR AE_H	P13H	P13L	P12H	P12L	P11H	P11L	P10H	P10L	00_H

P1.3 bits 7-6 — **Port 1 bit 3 control.**

P13H	P13L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.2 bits 5-4 — **Port 1 bit 2 control.**

P12H	P12L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.1 bits 3-2 — **Port 1 bit 1 control.**

P11H	P11L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.0 bits 1-0 — **Port 1 bit 0 control.**

P10H	P10L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 1 Data Direction High Register (P1DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR AF_H	P17H	P17L	P16H	P16L	P15H	P15L	P14H	P14L	00_H

P1.7 bits 7-6 — **Port 1 bit 7 control.**

P17H	P17L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.6 bits 5-4 — **Port 1 bit 6 control.**

P16H	P16L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.5 bits 3-2 — **Port 1 bit 5 control.**

P15H	P15L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.4 bits 1-0 — **Port 1 bit 4 control.**

P14H	P14L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 3 (P3)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B0_H$	P3.7	P3.6 SCK/SCL/CLKS	P3.5 T1	P3.4 T0	P3.3 $\overline{\text{INT1}}$	P3.2 $\overline{\text{INT0}}$	P3.1 TXD0	P3.0 RXD0	FF_H

P3.7-0 bits 7-0 — **General-Purpose I/O Port 3**. This register functions as a general-purpose I/O port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 3 latch bit must contain a logic '1' before the pin can be used in its alternate function capacity.

SCK/SCL/CLKS bit 6 — **Clock Source Select.** Refer to PASEL (SFR $F2_H$).

T1 bit 5 — **Timer/Counter 1 External Input.** A 1 to 0 transition on this pin will increment Timer 1.

T0 bit 4 — **Timer/Counter 0 External Input.** A 1 to 0 transition on this pin will increment Timer 0.

$\overline{\text{INT1}}$ bit 3 — **External Interrupt 1.** A falling edge/low level on this pin will cause an external interrupt 1 if enabled.

$\overline{\text{INT0}}$ bit 2 — **External Interrupt 0.** A falling edge/low level on this pin will cause an external interrupt 0 if enabled.

TXD0 bit 1 — **Serial Port 0 Transmit.** This pin transmits the serial Port 0 data in serial port modes 1, 2, 3, and emits the synchronizing clock in serial port mode 0.

RXD0 bit 0 — **Serial Port 0 Receive.** This pin receives the serial Port 0 data in serial port modes 1, 2, 3, and is a bidirectional data transfer pin in serial port mode 0.

Port 3 Data Direction Low Register (P3DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B3_H$	P33H	P33L	P32H	P32L	P31H	P31L	P30H	P30L	00_H

P3.3 bits 7-6 — **Port 3 bit 3 control.**

P33H	P33L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.2 bits 5-4 — **Port 3 bit 2 control.**

P32H	P32L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.1 bits 3-2 — **Port 3 bit 1 control.**

P31H	P31L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.0 bits 1-0 — **Port 3 bit 0 control.**

P30H	P30L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 3 Data Direction High Register (P3DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B4_H$	P37H	P37L	P36H	P36L	P35H	P35L	P34H	P34L	00_H

P3.7 **Port 3 bit 7 control.**
bits 7-6

P37H	P37L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 3.7 also controlled by $\overline{EA}$ and Memory Access Control HCR1.1.

P3.6 **Port 3 bit 6 control.**
bits 5-4

P36H	P36L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 3.6 also controlled by $\overline{EA}$ and Memory Access Control HCR1.1.

P3.5 **Port 3 bit 5 control.**
bits 3-2

P35H	P35L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.4 **Port 3 bit 4 control.**
bits 1-0

P34H	P34L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

IDAC Register

	7	6	5	4	3	2	1	0	Reset Value
SFR $B5_H$									00_H

IDAC **IDAC Register.**
bits 7-0 $IDAC_{OUT}$ = IDAC • 3.8μA (~1mA full-scale). Setting (PDCON.PDIDAC) will shut down IDAC and float the IDAC pin.

Interrupt Priority (IP)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B8_H$	1	0	0	PS0	PT1	PX1	PT0	PX0	80_H

PS0 **Serial Port 0 Interrupt.** This bit controls the priority of the serial Port 0 interrupt.
bit 4 0 = Serial Port 0 priority is determined by the natural priority order.
1 = Serial Port 0 is a high priority interrupt.

PT1 **Timer 1 Interrupt.** This bit controls the priority of the Timer 1 interrupt.
bit 3 0 = Timer 1 priority is determined by the natural priority order.
1 = Timer 1 priority is a high priority interrupt.

PX1 **External Interrupt 1.** This bit controls the priority of external interrupt 1.
bit 2 0 = External interrupt 1 priority is determined by the natural priority order.
1 = External interrupt 1 is a high priority interrupt.

PT0 **Timer 0 Interrupt.** This bit controls the priority of the Timer 0 interrupt.
bit 1 0 = Timer 0 priority is determined by the natural priority order.
1 = Timer 0 priority is a high priority interrupt.

PX0 **External Interrupt 0.** This bit controls the priority of external interrupt 0.
bit 0 0 = External interrupt 0 priority is determined by the natural priority order.
1 = External interrupt 0 is a high priority interrupt.

Enable Wake Up (EWU) Waking Up from IDLE Mode

	7	6	5	4	3	2	1	0	Reset Value
SFR $C6_H$	—	—	—	—	—	EWUWDT	EWUEX1	EWUEX0	00_H

Auxiliary interrupts will wake up from IDLE. They are enabled with EAI (EICON.5).

EWUWDT bit 2 — **Enable Wake Up Watchdog Timer.** Wake up using watchdog timer interrupt.
0 = Don't wake up on watchdog timer interrupt.
1 = Wake up on watchdog timer interrupt.

EWUEX1 bit 1 — **Enable Wake Up External 1.** Wake up using external interrupt source 1.
0 = Don't wake up on external interrupt source 1.
1 = Wake up on external interrupt source 1.

EWUEX0 bit 0 — **Enable Wake Up External 0.** Wake up using external interrupt source 0.
0 = Don't wake up on external interrupt source 0.
1 = Wake up on external interrupt source 0.

System Clock Divider Register (SYSCLK)

	7	6	5	4	3	2	1	0	Reset Value
SFR $C7_H$	0	0	DIVMOD1	DIVMOD0	0	DIV2	DIV1	DIV0	00_H

DIVMOD1-0 bits 5-4 — **Clock Divide Mode**

Write:

DIVMOD	DIVIDE MODE
00	Normal mode (default, no divide)
01	Immediate mode: start divide immediately, return to Normal mode on IDLE wakeup condition or Normal mode write.
10	Delay mode: same as Immediate mode, except that the mode changes with the millisecond interrupt (MSINT). If MSINT is enabled, the divide will start on the next MSINT and return to normal mode on the following MSINT. If MSINT is not enabled, the divide will start on the next MSINT condition (even if masked) but will not leave the divide mode until the MSINT counter overflows, which follows a wakeup condition. Can exit on Normal mode write.
11	Manual mode: start divide immediately; exit mode only on write to DIVMOD.

Read:

DIVMOD	DIVISION MODE STATUS
00	No divide
01	Divider is in Immediate mode
10	Divider is in Delay mode
11	Reserved

DIV2-0 bit 2-0 — **Divide Mode**

DIV	DIVISOR	
000	Divide by 2 (default)	$f_{CLK} = f_{SYS}/2$
001	Divide by 4	$f_{CLK} = f_{SYS}/4$
010	Divide by 8	$f_{CLK} = f_{SYS}/8$
011	Divide by 16	$f_{CLK} = f_{SYS}/16$
100	Divide by 32	$f_{CLK} = f_{SYS}/32$
101	Divide by 1024	$f_{CLK} = f_{SYS}/1024$
110	Divide by 2048	$f_{CLK} = f_{SYS}/2048$
111	Divide by 4096	$f_{CLK} = f_{SYS}/4096$

Program Status Word (PSW)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	00_H

CY bit 7 — **Carry Flag.** This bit is set when the last arithmetic operation resulted in a carry (during addition) or a borrow (during subtraction). Otherwise it is cleared to 0 by all arithmetic operations.

AC bit 6 — **Auxiliary Carry Flag.** This bit is set to 1 if the last arithmetic operation resulted in a carry into (during addition), or a borrow (during substraction) from the high order nibble. Otherwise it is cleared to 0 by all arithmetic operations.

F0 bit 5 — **User Flag 0.** This is a bit-addressable, general-purpose flag for software control.

RS1, RS0 bits 4-3 — **Register Bank Select 1-0.** These bits select which register bank is addressed during register accesses.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00_H-07_H
0	1	1	08_H-$0F_H$
1	0	2	10_H-17_H
1	1	3	18_H-$1F_H$

OV bit 2 — **Overflow Flag.** This bit is set to 1 if the last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide). Otherwise it is cleared to 0 by all arithmetic operations.

F1 bit 1 — **User Flag 1.** This is a bit-addressable, general-purpose flag for software control.

P bit 0 — **Parity Flag.** This bit is set to 1 if the modulo-2 sum of the 8 bits of the accumulator is 1 (odd parity); and cleared to 0 on even parity.

ADC Offset Calibration Register Low Byte (OCL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D1_H$								LSB	00_H

OCL bits 7-0 — **ADC Offset Calibration Register Low Byte.** This is the low byte of the 24-bit word that contains the ADC offset calibration. A value which is written to this location will set the ADC offset calibration value.

ADC Offset Calibration Register Middle Byte (OCM)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D2_H$									00_H

OCM bits 7-0 — **ADC Offset Calibration Register Middle Byte.** This is the middle byte of the 24-bit word that contains the ADC offset calibration. A value which is written to this location will set the ADC offset calibration value.

ADC Offset Calibration Register High Byte (OCH)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D3_H$	MSB								00_H

OCH bits 7-0 — **ADC Offset Calibration Register High Byte.** This is the high byte of the 24-bit word that contains the ADC offset calibration. A value which is written to this location will set the ADC offset calibration value.

ADC Gain Calibration Register Low Byte (GCL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D4_H$								LSB	$5A_H$

GCL bits 7-0 — **ADC Gain Calibration Register Low Byte.** This is the low byte of the 24-bit word that contains the ADC gain calibration. A value which is written to this location will set the ADC gain calibration value.

ADC Gain Calibration Register Middle Byte (GCM)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D5_H$									EC_H

GCM bits 7-0 — **ADC Gain Calibration Register Middle Byte.** This is the middle byte of the 24-bit word that contains the ADC gain calibration. A value which is written to this location will set the ADC gain calibration value.

ADC Gain Calibration Register High Byte (GCH)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D6_H$	MSB								$5F_H$

GCH bits 7-0 — **ADC Gain Calibration Register High Byte.** This is the high byte of the 24-bit word that contains the ADC gain calibration. A value which is written to this location will set the ADC gain calibration value.

ADC Multiplexer Register (ADMUX)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D7_H$	INP3	INP2	INP1	INP0	INN3	INN2	INN1	INN0	01_H

INP3-0 bits 7-4 — **Input Multiplexer Positive Channel.** This selects the positive signal input.

INP3	INP2	INP1	INP0	POSITIVE INPUT
0	0	0	0	AIN0 (default)
0	0	0	1	AIN1
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	0	0	0	AINCOM
1	1	1	1	Temperature Sensor (Requires ADMUX = FF_H)

INN3-0 bits 3-0 — **Input Multiplexer Negative Channel.** This selects the negative signal input.

INN3	INN2	INN1	INN0	NEGATIVE INPUT
0	0	0	0	AIN0
0	0	0	1	AIN1 (default)
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	0	0	0	AINCOM
1	1	1	1	Temperature Sensor (Requires ADMUX = FF_H)

Enable Interrupt Control (EICON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D8_H$	0	1	EAI	AI	WDTI	0	0	0	40_H

EAI bit 5 — **Enable Auxiliary Interrupt.** The Auxiliary Interrupt accesses nine different interrupts which are masked and identified by SFR registers PAI (SFR $A5_H$), AIE (SFR $A6_H$), and AISTAT (SFR $A7_H$).
0 = Auxiliary Interrupt disabled (default).
1 = Auxiliary Interrupt enabled.

AI bit 4 — **Auxiliary Interrupt Flag.** AI must be cleared by software before exiting the interrupt service routine, after the source of the interrupt is cleared. Otherwise, the interrupt occurs again. Setting AI in software generates an Auxiliary Interrupt, if enabled.
0 = No Auxiliary Interrupt detected (default).
1 = Auxiliary Interrupt detected.

WDTI bit 3 — **Watchdog Timer Interrupt Flag.** WDTI must be cleared by software before exiting the interrupt service routine. Otherwise, the interrupt occurs again. Setting WDTI in software generates a watchdog time interrupt, if enabled. The Watchdog timer can generate an interrupt or reset. The interrupt is available only if the reset action is disabledin HCR0.
0 = No Watchdog Timer Interrupt Detected (default).
1 = Watchdog Timer Interrupt Detected.

ADC Results Register Low Byte (ADRESL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D9_H$								LSB	00_H

ADRESL bits 7-0 — **The ADC Results Low Byte.** This is the low byte of the 24-bit word that contains the ADC Results. Reading from this register clears the ADC interrupt; however, AI in EICON (SFR D8) must also be cleared.

ADC Results Register Middle Byte (ADRESM)

	7	6	5	4	3	2	1	0	Reset Value
SFR DA_H									00_H

ADRESM bits 7-0 — **The ADC Results Middle Byte.** This is the middle byte of the 24-bit word that contains the ADC Results.

ADC Results Register High Byte (ADRESH)

	7	6	5	4	3	2	1	0	Reset Value
SFR DB_H	MSB								00_H

ADRESH bits 7-0 — **The ADC Results High Byte.** This is the high byte of the 24-bit word that contains the ADC Results.

ADC Control Register 0 (ADCON0)

	7	6	5	4	3	2	1	0	Reset Value
SFR DC_H	—	BOD	EVREF	VREFH	EBUF	PGA2	PGA1	PGA0	30_H

BOD bit 6 — **Burnout Detect.** When enabled this connects a positive current source to the positive channel and a negative current source to the negative channel. If the channel is open circuit then the ADC results will be full-scale (buffer must be enabled).
0 = Burnout Current Sources Off (default).
1 = Burnout Current Sources On.

EVREF bit 5 — **Enable Internal Voltage Reference.** If an external voltage reference is used, the internal voltage reference should be disabled.
0 = Internal Voltage Reference Off.
1 = Internal Voltage Reference On (default).

VREFH bit 4 — **Voltage Reference High Select.** The internal voltage reference can be selected to be 2.5V or 1.25V.
0 = REFOUT/REFIN+ is 1.25V.
1 = REFOUT/REFIN+ is 2.5V (default).

EBUF bit 3 — **Enable Buffer.** Enable the input buffer to provide higher input impedance but limits the input voltage range and dissipates more power.
0 = Buffer disabled (default).
1 = Buffer enabled.

PGA2-0 bits 2-0 — **Programmable Gain Amplifier.** Sets the gain for the PGA from 1 to 128.

PGA2	PGA1	PGA0	GAIN
0	0	0	1 (default)
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC Control Register 1 (ADCON1)

	7	6	5	4	3	2	1	0	Reset Value
SFR DD_H	OF_UF	POL	SM1	SM0	—	CAL2	CAL1	CAL0	$x000\ 0000_B$

OF_UF bit 7 — **Overflow/Underflow.** If this bit is set, the data in the summation register is invalid. Either an overflow or an underflow occurred. The bit is cleared by writing a 0 to it.

POL bit 6 — **Polarity.** Polarity of the ADC result and Summation register.
0 = Bipolar.
1 = Unipolar.

POL	ANALOG INPUT	DIGITAL OUTPUT
0	+FSR ZERO –FSR	0x7FFFFF 0x000000 0x800000
1	+FSR ZERO –FSR	0xFFFFFF 0x000000 0x000000

SM1-0 bits 5-4 — **Settling Mode.** Selects the type of filter or auto select which defines the digital filter settling characteristics.

SM1	SM0	SETTLING MODE
0	0	Auto
0	1	Fast Settling Filter
1	0	$Sinc^2$ Filter
1	1	$Sinc^3$ Filter

CAL2-0 bits 2-0 — **Calibration Mode Control Bits.** Writing to this register initiates calibration.

CAL2	CAL1	CAL0	CALIBRATION MODE
0	0	0	No Calibration (default)
0	0	1	Self Calibration, Offset and Gain
0	1	0	Self Calibration, Offset Only
0	1	1	Self Calibration, Gain Only
1	0	0	System Calibration, Offset Only
1	0	1	System Calibration, Gain Only
1	1	0	Reserved
1	1	1	Reserved

Read Value—000_B.

ADC Control Register 2 (ADCON2)

	7	6	5	4	3	2	1	0	Reset Value
SFR DE_H	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	$1B_H$

DR7-0 bits 7-0 — **Decimation Ratio LSB (refer to ADCON3, SFR DF_H).**

ADC Control Register 3 (ADCON3)

	7	6	5	4	3	2	1	0	Reset Value
SFR DF_H	—	—	—	—	—	DR10	DR9	DR8	06_H

DR10-8 bits 2-0 — **Decimation Ratio Most Significant 3 Bits.** The output data rate = $\frac{f_{MOD}}{\text{Decimation Ratio}}$ where $f_{MOD} = \frac{f_{CLK}}{(ACLK + 1) \bullet 64}$.

Accumulator (A or ACC)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E0_H$	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00_H

ACC.7-0 bits 7-0 — **Accumulator.** This register serves as the accumulator for arithmetic and logic operations.

Summation/Shifter Control (SSCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E1_H$	SSCON1	SSCON0	SCNT2	SCNT1	SCNT0	SHF2	SHF1	SHF0	00_H

The Summation register is powered down when the ADC is powered down. If all zeroes are written to this register the 32-bit SUMR3-0 registers will be cleared. The Summation registers will do sign extend if Bipolar is selected in ADCON1.

SSCON1-0 Summation/Shift Control.
bits 7-6

SSCON1	SSCON0	SCNT2	SCNT1	SCNT0	SHF2	SHF1	SHF0	DESCRIPTION
0	0	0	0	0	0	0	0	Clear Summation Register
0	0	0	1	0	0	0	0	CPU Summation on Write to SUMR0
0	0	1	0	0	0	0	0	CPU Subtraction on Write to SUMR0
1	0	x	x	x	Note (1)	Note (1)	Note (1)	CPU Shift Only
0	1	Note (1)	Note (1)	Note (1)	x	x	x	ADC Summation Only
1	1	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	ADC Summation Completes then Shift Completes

NOTES: (1) Refer to register bit definition.

SCNT2-0 **Summation Count.** When the summation is complete an interrupt will be generated unless masked. Reading the
bits 5-3 SUMR0 register clears the interrupt.

SCNT2	SCNT1	SCNT0	SUMMATION COUNT
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

SHF2-0 **Shift Count.**
bits 2-0

SHF2	SHF1	SHF0	SHIFT	DIVIDE
0	0	0	1	2
0	0	1	2	4
0	1	0	3	8
0	1	1	4	16
1	0	0	5	32
1	0	1	6	64
1	1	0	7	128
1	1	1	8	256

Summation Register 0 (SUMR0)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E2_H$								LSB	00_H

SUMR0 **Summation Register 0.** This is the least significant byte of the 32-bit summation register or bits 0 to 7.
bits 7-0 Write: will cause values in SUMR3-0 to be added to or subtracted from the summation register.
Read: will clear the Summation Interrupt.

Summation Register 1 (SUMR1)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E3_H$									00_H

SUMR1 **Summation Register 1.** This is the most significant byte of the lowest 16 bits of the summation register or bits 8-15.
bits 7-0

Summation Register 2 (SUMR2)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E4_H$									00_H

SUMR2 **Summation Register 2.** This is the most significant byte of the lowest 24 bits of the summation register or bits 16-23.
bits 7-0

Summation Register 3 (SUMR3)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E5_H$	MSB								00_H

SUMR3 **Summation Register 3.** This is the most significant byte of the 32-bit summation register or bits 24-31.
bits 7-0

Offset DAC Register (ODAC)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E6_H$									00_H

ODAC bit7-0 — **Offset DAC Register.** This register will shift the input by up to half of the ADC full-scale input range. The offset DAC value is summed with the ADC input prior to conversion. Writing 00_H or 80_H to ODAC turns off the Offset DAC.

bit 7 — Offset DAC Sign bit.
0 = Positive
1 = Negative

bit 6-0 — $$\text{Offset} = \frac{-V_{REF}}{2 \bullet PGA} \bullet \left(\frac{ODAC[6:0]}{127}\right) \bullet (-1)^{bit\ 7}$$

NOTE: ODAC cannot be used to offset the input so that the buffer can be used for AGND signals.

Low Voltage Detect Control (LVDCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E7_H$	ALVDIS	0	0	0	1	1	1	1	$8F_H$

ALVDIS bit 7 — **Analog Low Voltage Detect Disable.**
0 = Enable Detection of Low Analog Supply Voltage (ALVD interrupt set when AVDD < 2.8V).
1 = Disable Detection of Low Analog Supply Voltage.

Extended Interrupt Enable (EIE)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E8_H$	1	1	1	EWDI	EX5	EX4	EX3	EX2	$E0_H$

EWDI bit 4 — **Enable Watchdog Interrupt.** This bit enables/disables the watchdog interrupt. The Watchdog timer is enabled by the WDTCON (SFR FF_H) and PDCON (SFR $F1_H$) registers.
0 = Disable the Watchdog Interrupt
1 = Enable Interrupt Request Generated by the Watchdog Timer

EX5 bit 3 — **External Interrupt 5 Enable.** This bit enables/disables external interrupt 5.
0 = Disable External Interrupt 5
1 = Enable External Interrupt 5

EX4 bit 2 — **External Interrupt 4 Enable.** This bit enables/disables external interrupt 4.
0 = Disable External Interrupt 4
1 = Enable External Interrupt 4

EX3 bit 1 — **External Interrupt 3 Enable.** This bit enables/disables external interrupt 3.
0 = Disable External Interrupt 3
1 = Enable External Interrupt 3

EX2 bit 0 — **External Interrupt 2 Enable.** This bit enables/disables external interrupt 2.
0 = Disable External Interrupt 2
1 = Enable External Interrupt 2

Hardware Product Code Register 0 (HWPC0)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E9_H$	0	0	0	0	0	0	0	MEMORY	0000_000x_B

HWPC0.7-0 bits 7-0 — **Hardware Product Code LSB.** Read only.

MEMORY SIZE	MODEL	FLASH MEMORY
0	MSC1200Y2	4kB
1	MSC1200Y3	8kB

Hardware Product Code Register 1 (HWPC1)

	7	6	5	4	3	2	1	0	Reset Value
SFR EA_H	0	0	1	0	0	0	0	0	20_H

HWPC1.7-0 bits 7-0 — **Hardware Product Code MSB.** Read only.

Hardware Version Register (HWVER)

	7	6	5	4	3	2	1	0	Reset Value
SFR EB_H									

Flash Memory Control (FMCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR EE_H	0	PGERA	0	FRCM	0	BUSY	1	0	02_H

PGERA bit 6 — **Page Erase.** Available in both user and program modes.
0 = Disable Page Erase Mode
1 = Enable Page Erase Mode

FRCM bit 4 — **Frequency Control Mode.** The bypass is only used for slow clocks to save power.
0 = Bypass (default)
1 = Use Delay Line. Saves power (Recommended).

BUSY bit 2 — **Write/Erase BUSY Signal.**
0 = Idle or Available
1 = Busy

Flash Memory Timing Control Register (FTCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR EF_H	FER3	FER2	FER1	FER0	FWR3	FWR2	FWR1	FWR0	$A5_H$

Refer to Flash Timing Characteristics

FER3-0 bits 7-4 — **Set Erase.** Flash Erase Time = (1 + FER) • (MSEC + 1) • t_{CLK}.
11ms industrial temperature range.
5ms commercial temperature range.

FWR3-0 bits 3-0 — **Set Write.** Flash Write Time = (1 + FWR) • (USEC + 1) • 5 • t_{CLK}.
30µs to 40µs.

B Register (B)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F0_H$									00_H

B bits 7-0 — **B Register.** This register serves as a second accumulator for certain arithmetic operations.

Power-Down Control Register (PDCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F1_H$	PDICLK	PDIDAC	PDI2C	0	PDADC	PDWDT	PDSPI	PDSPI	$6F_H$

Turning peripheral modules off puts the MSC1200 in the lowest power mode.

PDICLK bit 7 — **Internal Clock Control.**
0 = Internal Oscillator and PLL On (Internal Oscillator or PLL mode)
1 = Internal Oscillator and PLL Power Down (External Clock mode)

PDIDAC bit 6 — **IDAC Control.**
0 = IDAC On
1 = IDAC Power Down (default)

PDI2C bit 5 — **I²C Control.**
0 = I²C On (only when PDSPI = 1)
1 = I²C Power Down (default)

PDADC bit 3 — **ADC Control.**
0 = ADC On
1 = ADC, V_{REF}, and Summation registers are powered down (default).

PDWDT bit 2 — **Watchdog Timer Control.**
0 = Watchdog Timer On
1 = Watchdog Timer Power Down (default)

PDST bit 1 — **System Timer Control.**
0 = System Timer On
1 = System Timer Power Down (default)

PDSPI bit 0 — **SPI Control.**
0 = SPI System On
1 = SPI System Power Down (default)

$\overline{\text{PSEN}}$/ALE Select (PASEL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F2_H$	PSEN4	PSEN3	PSEN2	PSEN1	PSEN0	0	0	0	00_H

PSEN4-0 bits 7-3 — **$\overline{\text{PSEN}}$ Mode Select.** Defines the output on P3.6 in User Application mode or Serial Flash Programming mode.
00000: General-Purpose I/O (default)
00001: SYSCLK
00011: Internal $\overline{\text{PSEN}}$ (refer to Figure 3 for timing)
00101: Internal ALE (refer to Figure 3 for timing)
00111: f_{OSC}(buffered XIN oscillator clock)
01001: Memory $\overline{\text{WR}}$ (MOVX write)
01011: T0 Out (overflow)(1)
01101: T1 Out (overflow)(1)
01111: f_{MOD}(2)
10001: SYSCLK/2 (toggles on rising edge)(2)
10011: Internal $\overline{\text{PSEN}}$/2(2)
10101: Internal ALE/2(2)
10111: f_{OSC}/2(2)
11001: Memory $\overline{\text{WR}}$/2 (MOVX write)(2)
11011: T0 Out/2 (overflow)(2)
11101: T1 Out/2 (overflow)(2)
11111: f_{MOD}/2(2)

NOTES: (1) On period of these signals equal to t_{CLK}. (2) Duty cycle is 50%.

Phase Lock Loop Low Register (PLLL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F4_H$	PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0	$C1_H$

PLL7-0 **PLL Counter Value Least Significant Bit.**
bits 7-0

PLL Frequency = External Crystal Frequency • PLL9:0

Phase Lock Loop High Register (PLLH)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F5_H$	CLKSTAT2	CLKSTAT1	CLKSTAT0	PLLLOCK	0	0	PLL9	PLL8	$x1_H$

CLKSTAT2-0 **Active Clock Status (read only).** Derived from HCR2 setting; refer to Table II.
bits 7-5
000: Reserved
001: Reserved
010: Reserved
011: External Clock Mode
100: PLL High-Frequency (HF) Mode (must read PLLLOCK to determine active clock status)
101: PLL Low-Frequency (LF) Mode (must read PLLLOCK to determine active clock status)
110: Internal Oscillator High-Frequency (HF) Mode
111: Internal Oscillator Low-Frequency (LF) Mode

PLLLOCK **PLL Lock Status and Status Enable.**
bit 4
For Write (PLL Lock Status Enable):
0 = No Effect
1 = Enable PLL Lock Detection (must wait 20ms before PLLLOCK read status is valid).

For Read (PLL Lock Status):
0 = PLL Not Locked (PLL may be inactive; refer to Table II for active clock mode)
1 = PLL Locked (PLL is active clock)

PLL9-8 **PLL Counter Value Most Significant 2 Bits (refer to PLLL, SFR $F4_H$)**
bits 1-0

Analog Clock (ACLK)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F6_H$	0	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03_H

FREQ6-0 **Clock Frequency – 1.** This value + 1 divides the system clock to create the ADC clock.
bits 6-0

$$f_{ACLK} = \frac{f_{CLK}}{(ACLK + 1)}, \text{ where } f_{CLK} = \frac{f_{OSC}}{\text{SYSCLK Divider}}.$$

$$f_{MOD} = \frac{f_{ACLK}}{64}$$

$$\text{ADC Data Rate} = f_{DATA} = \frac{f_{MOD}}{\text{Decimation Ratio}}$$

System Reset Register (SRST)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F7_H$	0	0	0	0	0	0	0	RSTREQ	00_H

RSTREQ **Reset Request.** Setting this bit to 1 and then clearing to 0 will generate a system reset.
bit 0

Extended Interrupt Priority (EIP)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F8_H$	1	1	1	PWDI	PX5	PX4	PX3	PX2	$E0_H$

PWDI bit 4 — **Watchdog Interrupt Priority.** This bit controls the priority of the watchdog interrupt.
0 = The watchdog interrupt is low priority.
1 = The watchdog interrupt is high priority.

PX5 bit 3 — **External Interrupt 5 Priority.** This bit controls the priority of external interrupt 5.
0 = External interrupt 5 is low priority.
1 = External interrupt 5 is high priority.

PX4 bit 2 — **External Interrupt 4 Priority.** This bit controls the priority of external interrupt 4.
0 = External interrupt 4 is low priority.
1 = External interrupt 4 is high priority.

PX3 bit 1 — **External Interrupt 3 Priority.** This bit controls the priority of external interrupt 3.
0 = External interrupt 3 is low priority.
1 = External interrupt 3 is high priority.

PX2 bit 0 — **External Interrupt 2 Priority.** This bit controls the priority of external interrupt 2.
0 = External interrupt 2 is low priority.
1 = External interrupt 2 is high priority.

Seconds Timer Interrupt (SECINT)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F9_H$	WRT	SECINT6	SECINT5	SECINT4	SECINT3	SECINT2	SECINT1	SECINT0	$7F_H$

This system clock is divided by the value of the 16-bit register MSECH:MSECL. Then that 1ms timer tick is divided by the register HMSEC which provides the 100ms signal used by this seconds timer. Therefore, this seconds timer can generate an interrupt which occurs from 100ms to 12.8 seconds. Reading this register will clear the Seconds Interrupt. This Interrupt can be monitored in the AIE register.

WRT bit 7 — **Write Control.** Determines whether to write the value immediately or wait until the current count is finished.
Read = 0.
0 = Delay Write Operation. The SEC value is loaded when the current count expires.
1 = Write Immediately. The counter is loaded once the CPU completes the write operation.

SECINT6-0 bits 6-0 — **Seconds Count.** Normal operation would use 100ms as the clock interval.
Seconds Interrupt = (1 + SEC) • (HMSEC + 1) • (MSEC + 1) • t_{CLK}.

Milliseconds Interrupt (MSINT)

	7	6	5	4	3	2	1	0	Reset Value
SFR FA_H	WRT	MSINT6	MSINT5	MSINT4	MSINT3	MSINT2	MSINT1	MSINT0	$7F_H$

The clock used for this timer is the 1ms clock which results from dividing the system clock by the values in registers MSECH:MSECL. Reading this register will clear MSINT.

WRT bit 7 — **Write Control.** Determines whether to write the value immediately or wait until the current count is finished. Read = 0.
0 = Delay Write Operation. The MSINT value is loaded when the current count expires.
1 = Write Immediately. The MSINT counter is loaded once the CPU completes the write operation.

MSINT6-0 bits 6-0 — **Seconds Count.** Normal operation would use 1ms as the clock interval.
MS Interrupt Interval = (1 + MSINT) • (MSEC + 1) • t_{CLK}

One Microsecond Register (USEC)

	7	6	5	4	3	2	1	0	Reset Value
SFR FB_H	0	0	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03_H

FREQ5-0 **Clock Frequency – 1.** This value + 1 divides the system clock to create a 1µs Clock.
bits 5-0 USEC = CLK/(FREQ + 1). This clock is used to set Flash write time. See FTCON (SFR EF_H).

One Millisecond Low Register (MSECL)

	7	6	5	4	3	2	1	0	Reset Value
SFR FC_H	MSECL7	MSECL6	MSECL5	MSECL4	MSECL3	MSECL2	MSECL1	MSECL0	$9F_H$

MSECL7-0 **One Millisecond Low.** This value in combination with the next register is used to create a 1ms Clock.
bits 7-0 1ms Clock = (MSECH • 256 + MSECL + 1) • t_{CLK}. This clock is used to set Flash erase time. See FTCON (SFR EF_H).

One Millisecond High Register (MSECH)

	7	6	5	4	3	2	1	0	Reset Value
SFR FD_H	MSECH7	MSECH6	MSECH5	MSECH4	MSECH3	MSECH2	MSECH1	MSECH0	$0F_H$

MSECH7-0 **One Millisecond High.** This value in combination with the previous register is used to create a 1ms clock.
bits 7-0 1ms = (MSECH • 256 + MSECL + 1) • t_{CLK}.

One Hundred Millisecond Register (HMSEC)

	7	6	5	4	3	2	1	0	Reset Value
SFR FE_H	HMSEC7	HMSEC6	HMSEC5	HMSEC4	HMSEC3	HMSEC2	HMSEC1	HMSEC0	63_H

HMSEC7-0 **One Hundred Millisecond.** This clock divides the 1ms clock to create a 100ms clock.
bits 7-0 100ms = (MSECH • 256 + MSECL + 1) • (HMSEC + 1) • t_{CLK}.

Watchdog Timer Register (WDTCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR FF_H	EWDT	DWDT	RWDT	WDCNT4	WDCNT3	WDCNT2	WDCNT1	WDCNT0	00_H

EWDT **Enable Watchdog (R/W).**
bit 7 Write 1/Write 0 sequence sets the Watchdog Enable Counting bit.

DWDT **Disable Watchdog (R/W).**
bit 6 Write 1/Write 0 sequence clears the Watchdog Enable Counting bit.

RWDT **Reset Watchdog (R/W).**
bit 5 Write 1/Write 0 sequence restarts the Watchdog Counter.

WDCNT4-0 **Watchdog Count (R/W).**
bits 4-0 Watchdog expires in (WDCNT + 1) • HMSEC to (WDCNT + 2) • HMSEC, if the sequence is not asserted. There is an uncertainty of 1 count.

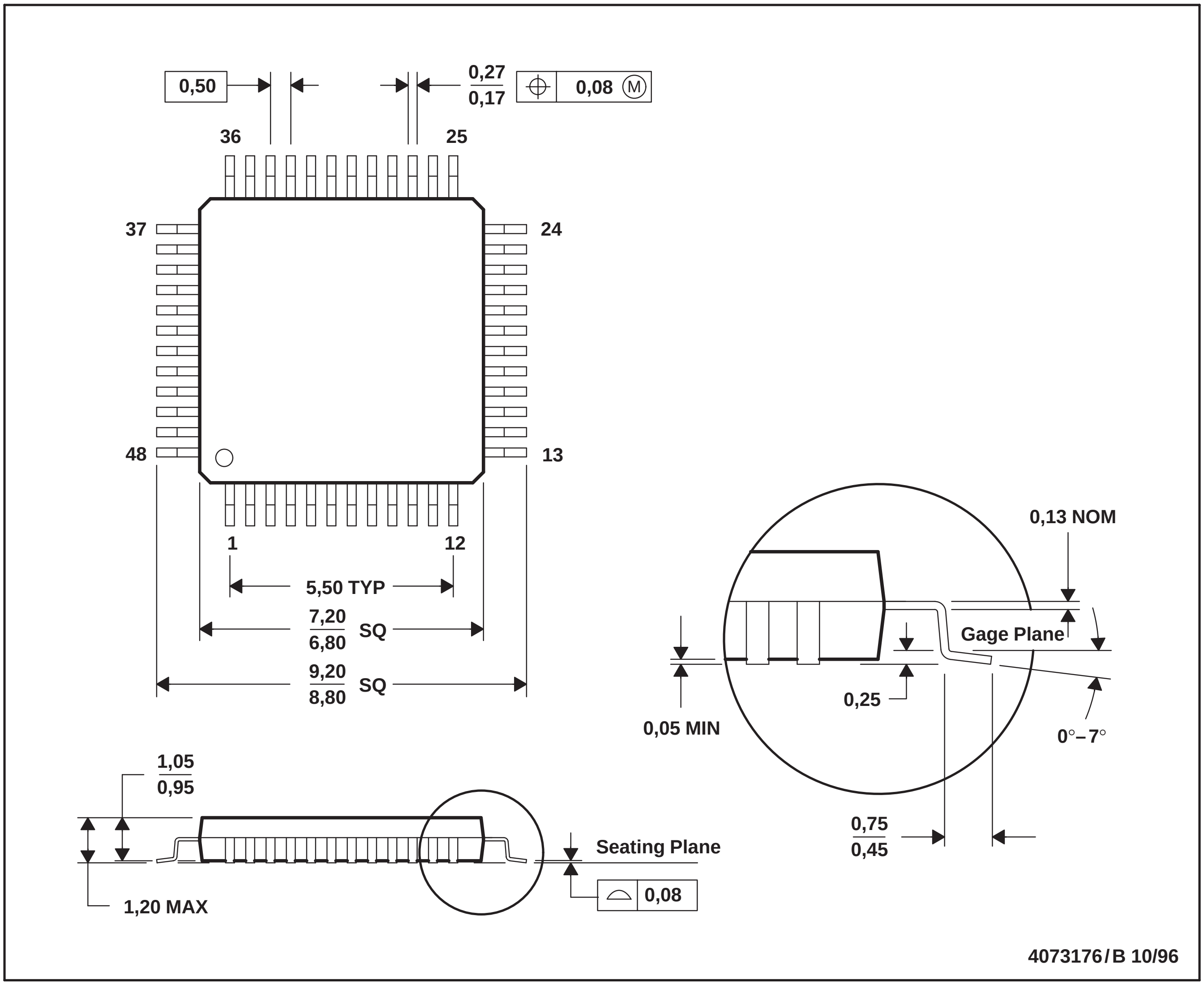
NOTE: If HCR0.3 (EWDR) is set and the watchdog timer expires, a system reset is generated. If HCR0.3 (EWDR) is cleared and the watchdog timer expires, an interrupt is generated (see Table VII).

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
MSC1200Y2PFBR	ACTIVE	TQFP	PFB	48	2000
MSC1200Y2PFBT	ACTIVE	TQFP	PFB	48	250
MSC1200Y3PFBR	ACTIVE	TQFP	PFB	48	2000
MSC1200Y3PFBT	ACTIVE	TQFP	PFB	48	250

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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