

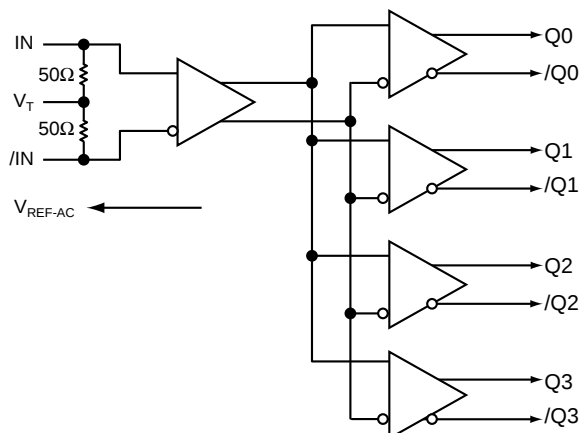
## FEATURES

- Precision 1:4, 400mV CML fanout buffer
- Guaranteed AC performance over temperature/ voltage:
  - > 6GHz  $f_{MAX}$  clock
  - < 60ps  $t_r$  /  $t_f$  times
  - < 250ps  $t_{pd}$
  - < 15ps max. skew
- Low jitter performance:
  - < 10ps<sub>(pk-pk)</sub> total jitter (clock)
  - < 1ps<sub>(rms)</sub> random jitter (data)
  - < 10ps<sub>(pk-pk)</sub> deterministic jitter (data)
- Accepts an input signal as low as 100mV
- Unique input termination and  $V_T$  pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS, and CML
- 50Ω source terminated CML outputs
- Power supply 2.5V ±5% and 3.3V ±10%
- Industrial temperature range: -40°C to +85°C
- Available in 16-pin (3mm × 3mm) MLF™ package

## APPLICATIONS

- All SONET and All GigE clock distribution
- Fibre Channel clock and data distribution
- Backplane distribution
- Data distribution: OC-48, OC-48+FEC, XAUI
- High-end, low skew, multiprocessor synchronous clock distribution

## FUNCTIONAL BLOCK DIAGRAM



Precision Edge™

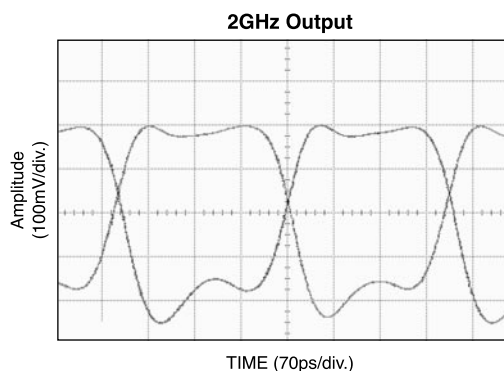
## DESCRIPTION

The SY58020U is a 2.5V/3.3V precision, high-speed, fully differential 1:4 CML fanout buffer. Optimized to provide four identical output copies with less than 15ps of skew and less than 10ps<sub>(pk-pk)</sub> total jitter, the SY58020U can process clock signals as fast as 6GHz.

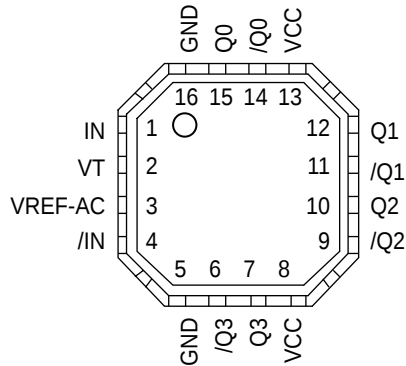
The differential input includes Micrel's unique, 3-pin input termination architecture interfaces to differential LVPECL, LVDS, and CML signals (AC-coupled or DC-coupled) as small as 100mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage ( $V_{REF-AC}$ ) is provided to bias the  $V_T$  pin. The outputs are optimized to drive 400mV typical swing into 50Ω loads, with extremely fast rise/fall times guaranteed to be less than 60ps.

The SY58020U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). For applications that require LVPECL outputs, consider the SY58021U or SY58022U 1:4 fanout buffer with 800mV and 400mV output swing, respectively. The SY58020U is part of Micrel's high-speed, Precision Edge™ product line. Data sheets and support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

## TYPICAL PERFORMANCE



## PACKAGE/ORDERING INFORMATION



16-Pin MLF™ (MLF-16)

## Ordering Information(Note 1)

| Part Number                      | Package Type | Operating Range | Package Marking |
|----------------------------------|--------------|-----------------|-----------------|
| SY58020UMI                       | MLF-16       | Industrial      | 020U            |
| SY58020UMITR <sup>(Note 2)</sup> | MLF-16       | Industrial      | 020U            |

**Note 1.** Contact factory for die availability. Die are guaranteed at  $T_A = 25^\circ\text{C}$ , DC electricals only.

**Note 2.** Tape and Reel.

## PIN DESCRIPTION

| Pin Number                        | Pin Name                                     | Pin Function                                                                                                                                                                                                                                                                                                                                                                          |
|-----------------------------------|----------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 4                              | IN, /IN                                      | Differential Input: This input pair receives the signal to be buffered. Each pin of this pair internally terminates with $50\Omega$ to the $V_T$ pin. Note that this input will default to an indeterminate state if left open. See “ <i>Input Interface Applications</i> ” section.                                                                                                  |
| 2                                 | VT                                           | Input Termination Center-Tap: Each input terminates to this pin. The $V_T$ pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See “ <i>Input Interface Applications</i> ” section.                                                                                                                                      |
| 3                                 | VREF-AC                                      | Reference Output Voltage: This output biases to $V_{CC} - 1.2\text{V}$ . It is used when AC-coupling to differential inputs. Connect $V_{REF-AC}$ directly to the $V_T$ pin. Bypass with $0.01\mu\text{F}$ low ESR capacitor to $V_{CC}$ . See “ <i>Input Interface Applications</i> ” section.                                                                                       |
| 8, 13                             | VCC                                          | Positive Power Supply: Bypass with $0.1\mu\text{F}/0.01\mu\text{F}$ low ESR capacitors as close to the pins as possible.                                                                                                                                                                                                                                                              |
| 5, 16                             | GND,<br>Exposed Pad                          | Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.                                                                                                                                                                                                                                                                                 |
| 14, 15<br>11, 12<br>9, 10<br>6, 7 | /Q0, Q0,<br>/Q1, Q1,<br>/Q2, Q2,<br>/Q3, Q3, | CML Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically $400\text{mV}$ into $50\Omega$ load. Normally terminate CML output pairs with $100\Omega$ across Q and /Q outputs at the receiving end. Unused output pairs may be left floating with no impact on jitter or skew. See “ <i>CML Output Termination</i> ” section. |

**Absolute Maximum Ratings**(Note 1)

|                                                        |                                  |
|--------------------------------------------------------|----------------------------------|
| Power Supply Voltage ( $V_{CC}$ )                      | –0.5V to +4.0V                   |
| Input Voltage ( $V_{IN}$ )                             | –0.5V to $V_{CC}$                |
| CML Output Voltage ( $V_{OUT}$ )                       | $V_{CC}$ –1.0V to $V_{CC}$ +0.5V |
| Current ( $V_T$ )                                      |                                  |
| Source or sink current on $V_T$ pin                    | ±100mA                           |
| Input Current                                          |                                  |
| Source or sink current on IN, /IN                      | ±50mA                            |
| Current ( $V_{REF}$ )                                  |                                  |
| Source or sink current on $V_{REF-AC}$ , <b>Note 4</b> | ±1.5mA                           |
| Lead Temperature Soldering, (10 seconds)               | 270°C                            |
| Storage Temperature Range ( $T_{STORE}$ )              | –65°C to +150°C                  |

**Operating Ratings**(Note 2)

|                                               |                   |
|-----------------------------------------------|-------------------|
| Supply Voltage ( $V_{CC}$ )                   | +2.375V to +3.60V |
| Operating Temperature Range ( $T_A$ )         | –40°C to +85°C    |
| Package Thermal Resistance                    |                   |
| MLF™ ( $\theta_{JA}$ )                        |                   |
| Still-Air                                     | 60°C/W            |
| 500lfpm                                       | 54°C/W            |
| MLF™ ( $\psi_{JB}$ )                          |                   |
| (Junction-to-Board Resistance), <b>Note 3</b> | 33°C/W            |

**DC ELECTRICAL CHARACTERISTICS**(Notes 5) $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ 

| Symbol         | Parameter                        | Condition                                                          | Min          | Typ          | Max           | Units |
|----------------|----------------------------------|--------------------------------------------------------------------|--------------|--------------|---------------|-------|
| $V_{CC}$       | Power Supply Voltage             | $V_{CC} = 2.5\text{V}$<br>$V_{CC} = 3.3\text{V}$                   | 2.375<br>3.0 | 2.5<br>3.3   | 2.625<br>3.60 | V     |
| $I_{CC}$       | Power Supply Current             | No load, $V_{CC} = \text{max.}$<br>(includes internal 50Ω pull-up) |              | 150          | 180           | mA    |
| $V_{IH}$       | Input HIGH Voltage               | <b>Note 6</b>                                                      | $V_{CC}-1.6$ |              | $V_{CC}$      | V     |
| $V_{IL}$       | Input LOW Voltage                |                                                                    | 0            |              | $V_{IH}-0.1$  | V     |
| $V_{IN}$       | Input Voltage Swing              | See Figure 1a                                                      | 0.1          |              | 1.7           | V     |
| $V_{DIFF\_IN}$ | Differential Input Voltage Swing | See Figure 1b                                                      | 0.2          |              | 3.4           | V     |
| $R_{IN}$       | IN-to- $V_T$ Resistance          |                                                                    | 40           | 50           | 60            | Ω     |
| $V_{REF-AC}$   | Output Reference Voltage         |                                                                    | $V_{CC}-1.3$ | $V_{CC}-1.2$ | $V_{CC}-1.1$  | V     |
| $V_{T\_IN}$    | IN-to- $V_T$ Voltage             |                                                                    |              |              | 1.28          | V     |

**CML DC ELECTRICAL CHARACTERISTICS**(Notes5) $V_{CC} = 3.3\text{V} \pm 10\%$  or  $2.5\text{V} \pm 5\%$ ;  $R_L = 100\Omega$  across each output pair or equivalent;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

| Symbol          | Parameter                         | Condition     | Min            | Typ            | Max      | Units |
|-----------------|-----------------------------------|---------------|----------------|----------------|----------|-------|
| $V_{OH}$        | Output HIGH Voltage               |               | $V_{CC}-0.020$ | $V_{CC}-0.010$ | $V_{CC}$ | V     |
| $V_{OUT}$       | Output Voltage Swing              | see Figure 1a | 325            | 400            | 500      | mV    |
| $V_{DIFF\_OUT}$ | Differential Output Voltage Swing | see Figure 1b | 650            | 800            | 1000     | mV    |
| $R_{OUT}$       | Output Source Impedance           |               | 40             | 50             | 60       | Ω     |

**Note 1.** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

**Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**Note 3.** Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

**Note 4.** Due to the limited drive capability, use for input of the same package only.

**Note 5.** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**Note 6.**  $V_{IH}$  (min.) not lower than 1.2V.

**AC ELECTRICAL CHARACTERISTICS**

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ;  $R_L = 100\Omega$  across each output pair or equivalent, unless otherwise stated.

| Symbol       | Parameter                        | Condition                        | Min | Typ | Max | Units     |
|--------------|----------------------------------|----------------------------------|-----|-----|-----|-----------|
| $f_{MAX}$    | Maximum Operating Frequency      | $V_{OUT} \geq 200mV$ Clock       | 6   |     |     | GHz       |
|              |                                  | NRZ Data                         |     | 10  |     | Gbps      |
| $t_{pd}$     | Propagation Delay                |                                  | 110 | 180 | 260 | ps        |
| $t_{CHAN}$   | Channel-to-Channel Skew          | <b>Note 7</b>                    |     | 4   | 15  | ps        |
| $t_{SKEW}$   | Part-to-Part Skew                | <b>Note 8</b>                    |     |     | 50  | ps        |
| $t_{JITTER}$ | Clock Cycle-to-Cycle Jitter      | <b>Note 9</b>                    |     |     | 1   | ps(rms)   |
|              | Total Jitter                     | <b>Note 10</b>                   |     |     | 10  | ps(pk-pk) |
|              | Data Random Jitter               | <b>Note 11</b> 2.5Gbps – 3.2Gbps |     |     | 1   | ps(rms)   |
|              | Deterministic Jitter             | <b>Note 12</b> 2.5Gbps – 3.2Gbps |     |     | 10  | ps(pk-pk) |
| $t_r, t_f$   | Output Rise/Fall Time 20% to 80% | At full swing                    | 20  | 40  | 60  | ps        |

**Note 7.** Skew is measured between outputs of the same bank under identical transitions.

**Note 8.** Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

**Note 9.** Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles,  $T_n - T_{n-1}$  where T is the time between rising edges of the output signal.

**Note 10.** Total jitter definition: With an ideal clock input of frequency  $\leq f_{MAX}$ , no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.

**Note 11.** Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps/3.2Gbps.

**Note 12.** Deterministic jitter is measured at 2.5Gbps/3.2Gbps with both K28.5 and  $2^{23}-1$  PRBS pattern

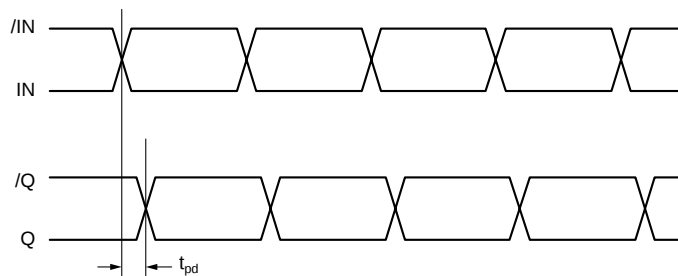
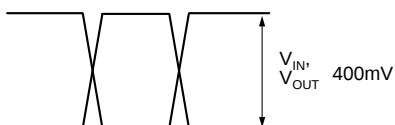
**TIMING DIAGRAM****SINGLE-ENDED AND DIFFERENTIAL SWINGS**

Figure 1a. Single-Ended Voltage Swing

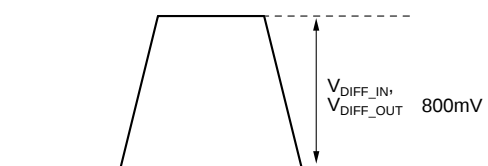
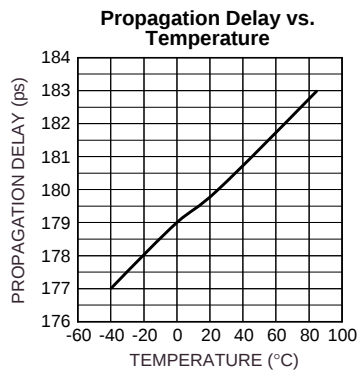
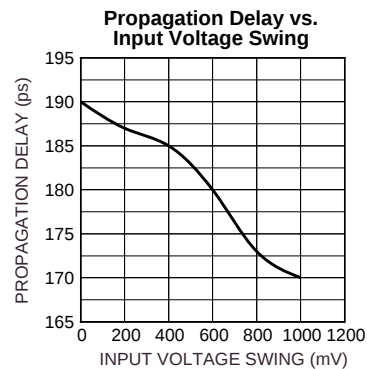
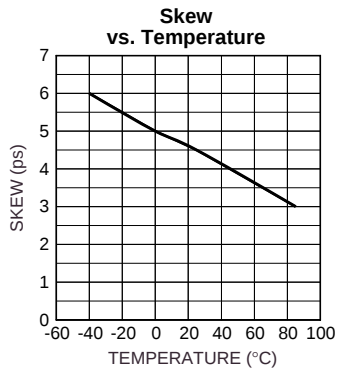
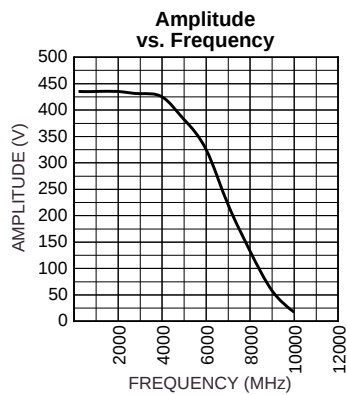


Figure 1b. Differential Voltage Swing

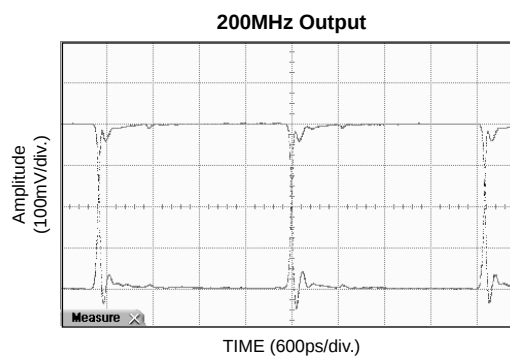
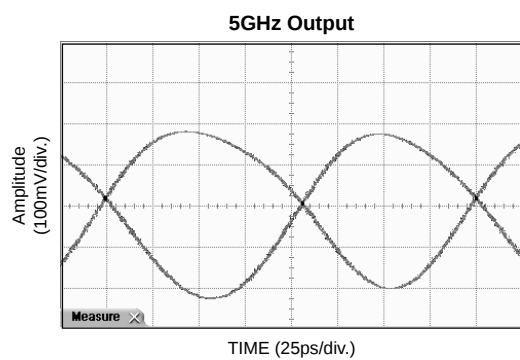
TYPICAL OPERATING CHARACTERISTICS

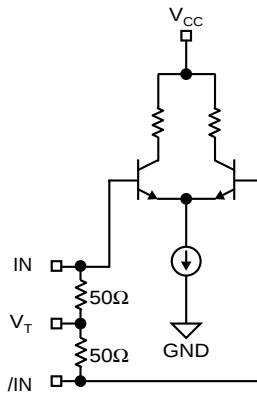
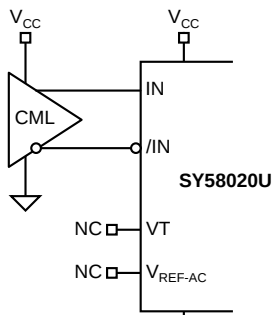
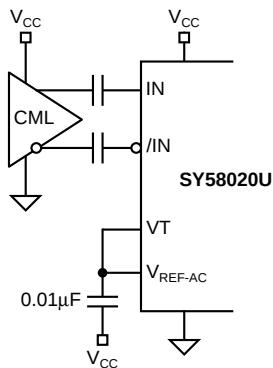
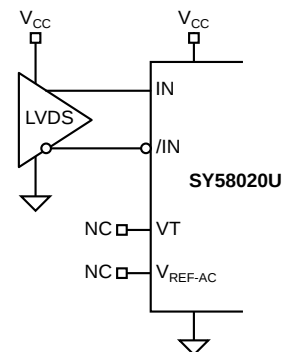
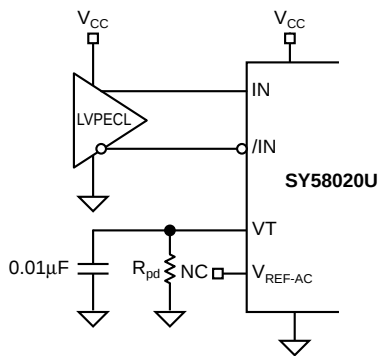
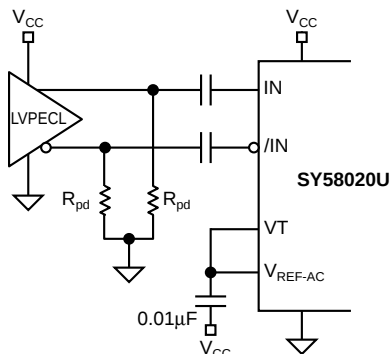
V<sub>CC</sub> = 2.5V, GND = 0, V<sub>IN</sub> = 100mV, T<sub>A</sub> = 25°C, unless otherwise stated.



**FUNCTIONAL CHARACTERISTICS**

$V_{CC} = 2.5V$ ,  $GND = 0$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^{\circ}C$ , unless otherwise stated.



**INPUT STAGE****Figure 2. Simplified Differential Input Buffer****INPUT INTERFACE APPLICATIONS**(Option: May connect  $V_T$  to  $V_{CC}$ )**Figure 3a. DC-Coupled CML Input Interface****Figure 3b. AC-Coupled CML Input Interface****Figure 3c. LVDS Input Interface**For  $V_{CC} = 2.5V$ ,  $R_{pd} = 19\Omega$   
For  $V_{CC} = 3.3V$ ,  $R_{pd} = 50\Omega$ **Figure 3d. LVPECL Input Interface** $R_{pd} = 100\Omega$  for a 3.3V system  
 $R_{pd} = 50\Omega$  for a 2.5V system**Figure 3e. AC-Coupled LVPECL Input Interface**

## CML OUTPUT TERMINATION

Figures 4 and 5 illustrate how to terminate a CML output using both the AC-coupled and DC-coupled configuration.

All outputs of the SY58020U are 50Ω with a 16mA current source.

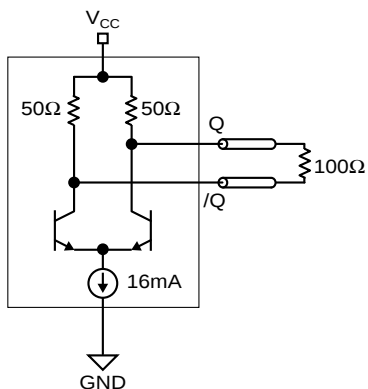


Figure 4. CML DC-Coupled

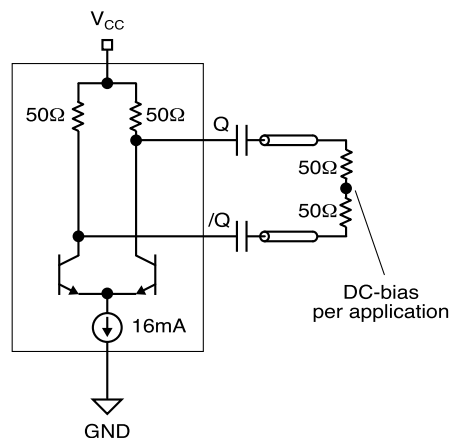
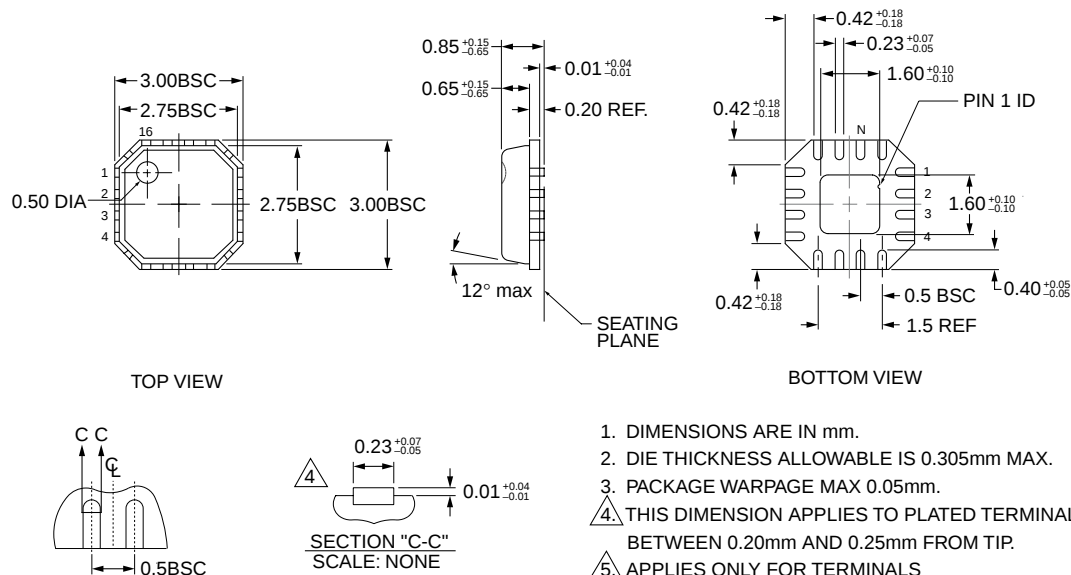


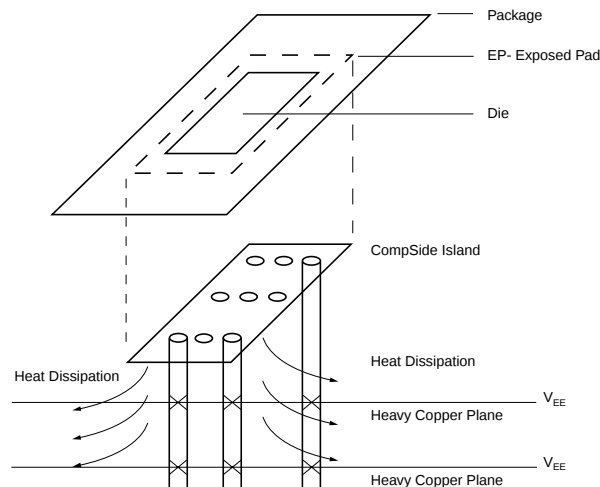
Figure 5. CML AC-Coupled Termination

## RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

| Part Number | Function                                                                                   | Data Sheet Link                                                                                                                        |
|-------------|--------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| SY58020U    | 6GHz, 1:4 CML Fanout Buffer/Translator with Internal I/O Termination                       | <a href="http://www.micrel.com/product-info/products/sy58020u.shtml">http://www.micrel.com/product-info/products/sy58020u.shtml</a>    |
| SY58021U    | 4GHz, 1:4 LVPECL Fanout Buffer/Translator with Internal Termination                        | <a href="http://www.micrel.com/product-info/products/sy58021u.shtml">http://www.micrel.com/product-info/products/sy58021u.shtml</a>    |
| SY58022U    | 5.5GHz, 1:4 Fanout Buffer/Translator w/400mV LVPECL Outputs and Internal Input Termination | <a href="http://www.micrel.com/product-info/products/sy58022u.shtml">http://www.micrel.com/product-info/products/sy58022u.shtml</a>    |
|             | 16-MLF™ Manufacturing Guidelines Exposed Pad Application Note                              | <a href="http://www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf">www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf</a> |
| M-0317      | HBW Solutions                                                                              | <a href="http://www.micrel.com/product-info/as/solutions.shtml">http://www.micrel.com/product-info/as/solutions.shtml</a>              |

**16 LEAD MicroLeadFrame™ (MLF-16)**

Rev. 02



**PCB Thermal Consideration for 16-Pin MLF™ Package**  
**(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

- Note 1.** Package meets Level 2 qualification.  
**Note 2.** All parts are dry-packaged before shipment.  
**Note 3.** Exposed pads must be soldered to a ground for proper thermal management.

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