80-mW CAPLESS STEREO HEADPHONE DRIVER

FEATURES

- **Ground-Referenced Outputs Eliminate DC-Bias Voltages on Headphone Ground Pin**
  - **No Output DC-Blocking Capacitors**
    - **Reduced Board Area**
    - **Reduced Component Cost**
    - **Improved THD+N Performance**
    - **No Degradation of Low-Frequency Response Due to Output Capacitors**
- **Wide Power Supply Range: 1.8 V to 4.5 V**
- **80-mW/Ch Output Power into 16-Ω at 4.5 V**
- **Independent Right and Left Channel Shutdown Control**
- **Short-Circuit and Thermal Protection**
- **Pop Reduction Circuitry**
- **Space Saving Pb-Free Packages**
  - **20-pin, 4 mm × 4 mm ThinQFN**
  - **16-ball, 2 mm × 2 mm WCSP (Product Preview)**

APPLICATIONS

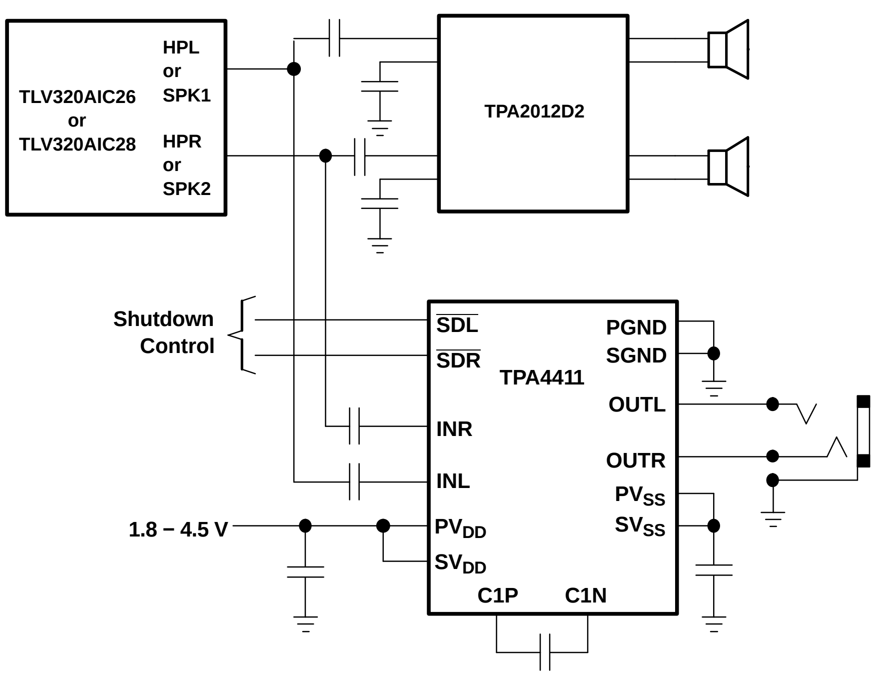
- **Notebook Computers**
- **CD / MP3 Players**
- **Smart Phones**
- **Cellular Phones**
- **PDAs**

DESCRIPTION

The TPA4411 is a stereo headphone driver designed to allow the removal of the output dc-blocking capacitors for reduced component count and cost. The TPA4411 is ideal for small portable electronics where size and cost are critical design parameters.

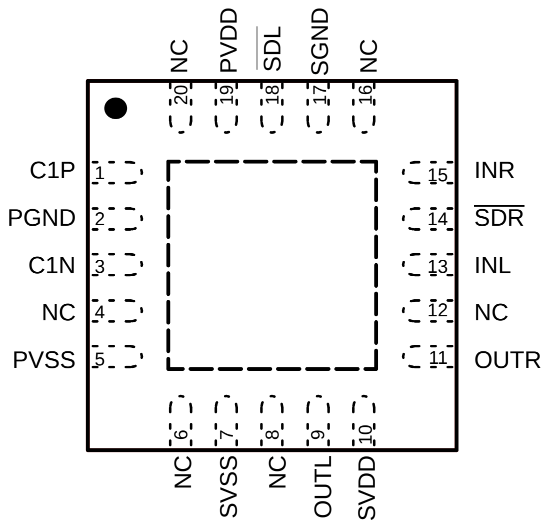
The TPA4411 is capable of driving 80 mW into a 16-Ω load at 4.5 V. The TPA4411 has a fixed gain of -1.5 V/V and headphone outputs have ±8-kV IEC ESD protection. The TPA4411 has independent shutdown control for the right and left audio channels.

The TPA4411 is available in a 20-pin, 4 mm × 4 mm ThinQFN package.



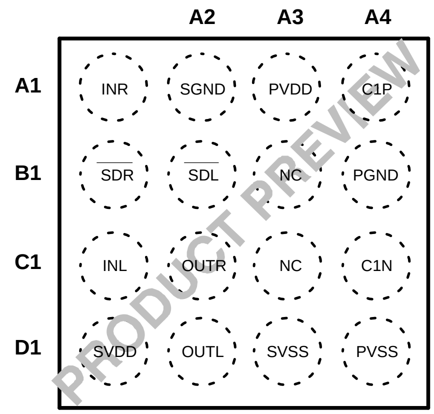
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

RTJ (QFN) PACKAGE
(TOP VIEW)



NC − No internal connection

YZH (WCSP) PACKAGE
(TOP VIEW)



NC − No internal connection

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	QFN	WCSP(1)		
C1P	1	A4	I/O	Charge pump flying capacitor positive terminal
PGND	2	B4	I	Power ground, connect to ground.
C1N	3	C4	I/O	Charge pump flying capacitor negative terminal
NC	4, 6, 8, 12, 16, 20	B3, C3		No connection
PVSS	5	D4	O	Output from charge pump.
SVSS	7	D3	I	Amplifier negative supply, connect to PVSS via star connection.
OUTL	9	D2	O	Left audio channel output signal
SVDD	10	D1	I	Amplifier positive supply, connect to PVDD via star connection.
OUTR	11	C2	O	Right audio channel output signal
INL	13	C1	I	Left audio channel input signal
SDR	14	B1	I	Right channel shutdown, active low logic.
INR	15	A1	I	Right audio channel input signal
SGND	17	A2	I	Signal ground, connect to ground.
SDL	18	B2	I	Left channel shutdown, active low logic.
PVDD	19	A3	I	Supply voltage, connect to positive supply.
Exposed Pad		-		Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground.

(1) Package not yet available

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)

			UNIT
	Supply voltage, AVDD, PVDD	-0.3 to 5.5	V
V_I	Input voltage	-0.3 to V_{DD} + 0.3	V
	Output Continuous total power dissipation	See Dissipation Rating Table	
T_A	Operating free-air temperature range	- 40 to 85	°C
T_J	Operating junction temperature range	- 40 to 150	°C
T_{stg}	Storage temperature range	-65 to 85	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS TABLE

PACKAGE	$T_A \leq$ 25°C POWER RATING	DERATING FACTOR(1)	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
RTJ	3450 mW	34.5 mW/°C	1898 mW	1380 mW
YZH(2)	TBD	TBD mW/°C	TBD	TBD

(1) Derating factor measured with High K board.
(2) Product preview

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	PART NUMBER	SYMBOL
-40°C to 85°C	20-pin, 4 mm × 4 mm QFN	TPA4411RTJ(1)	AKQ
	16-ball, 2 mm × 2mm WSCP	TPA4411YZH	AKT

(1) The RTJ package is only available taped and reeled. To order, add the suffix “R” to the end of the part number for a reel of 3000, or add the suffix “T” to the end of the part number for a reel of 250 (e.g., TPA4411RTJR).

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
	Supply voltage, AVDD, PVDD		1.8	4.5(1)	V
V_{IH}	High-level input voltage	$\overline{SDL}$, $\overline{SDR}$	1.5		V
V_{IL}	Low-level input voltage	$\overline{SDL}$, $\overline{SDR}$		0.5	V
T_A	Operating free-air temperature		- 40	85	°C

(1) Device can shut down for VDD > 4.5 V to prevent damage to the device.

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

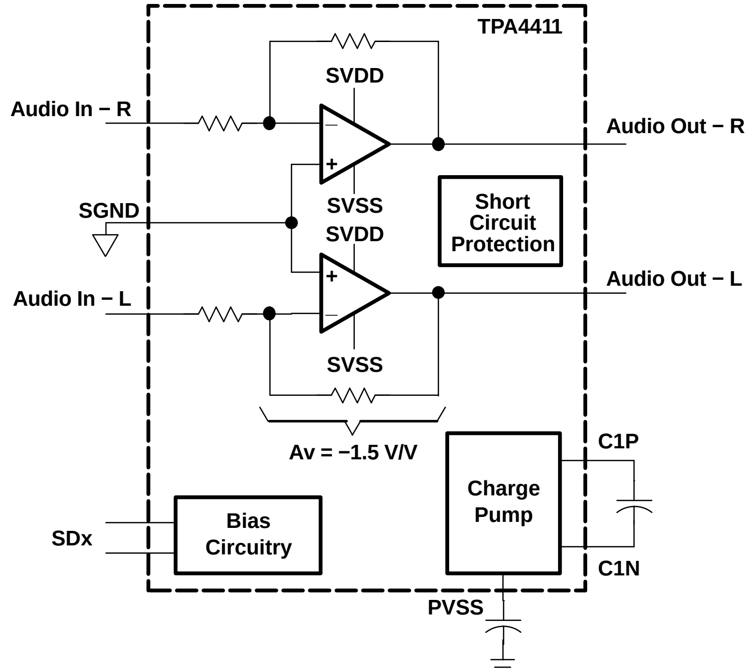
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
|VOS|	Output offset voltage	V_{DD} = 1.8 V to 4.5 V, Inputs grounded			8	mV
PSRR	Power Supply Rejection Ratio	V_{DD} = 1.8 V to 4.5 V	-69	-80		dB
V_{OH}	High-level output voltage	V_{DD} = 3 V, R_L = 16 Ω	2.2			V
V_{OL}	Low-level output voltage	V_{DD} = 3 V, R_L = 16 Ω			-1.1	V
$\|I_{IH}\|$	High-level input current ($\overline{SDL}$, $\overline{SDR}$)	V_{DD} = 4.5 V, V_I = V_{DD}			1	µA
$\|I_{IL}\|$	Low-level input current ($\overline{SDL}$, $\overline{SDR}$)	V_{DD} = 4.5 V, V_I = 0 V			1	µA
I_{DD}	Supply Current	V_{DD} = 1.8 V, No load, $\overline{SDL}$= $\overline{SDR}$ = V_{DD}		5.3	6.5	mA
		V_{DD} = 3 V, No load, $\overline{SDL}$ = $\overline{SDR}$ = V_{DD}		6.5	8.0	
		V_{DD} = 4.5 V, No load, $\overline{SDL}$ = $\overline{SDR}$ = V_{DD}		8.0	10.0	
		Shutdown mode, V_{DD} = 1.8 V to 4.5 V			1	µA

OPERATING CHARACTERISTICS

V_{DD} = 3 V , T_A = 25°C, R_L = 16 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (Outputs In Phase)	THD = 1%, V_{DD} = 3 V, f = 1 kHz		50		mW
		THD = 1%, V_{DD} = 4.5 V, f = 1 kHz		80		
		THD = 1%, V_{DD} = 3 V, f = 1 kHz, R_L = 32 Ω		40		
THD+N	Total harmonic distortion plus noise	P_O = 25 mW, f = 1 kHz		0.054%		
		P_O = 25 mW, f = 20 kHz		0.010%		
Crosstallk		P_O = 20 mW, f = 1 kHz		-83		dB
k_{SVR}	Supply ripple rejection ratio	200-mV_{pp} ripple, f = 217 Hz		-82.5		dB
		200-mV_{pp} ripple, f = 1 kHz		-70.4		
		200-mV_{pp} ripple, f = 20 kHz		-45.1		
A_v	Closed-loop voltage gain		-1.45	-1.5	-1.55	V/V
ΔA_v	Gain matching			1%		
	Slew rate			2.2		V/µs
	Maximum capacitive load			400		pF
V_n	Noise output voltage			10		µV_{RMS}
	Electrostatic discharge, IEC	OUTR, OUTL		±8		kV
f_{osc}	Charge pump switching frequency		280	320	420	kHz
	Start-up time from shutdown			450		µs
	Input impedance		12	15	18	kΩ
SNR	Signal-to-noise ratio	P_o = 40 mW (THD+N = 0.1%)		98		dB
	Thermal shutdown	Threshold	150		170	°C
		Hysteresis		15		°C

Functional Block Diagram



TYPICAL CHARACTERISTICS

$C_{(PUMP)} = C_{(PVSS)} = 2.2\ \mu F$, $C_{IN} = 1\ \mu F$ (unless otherwise noted)

Table of Graphs

		FIGURE
Total harmonic distortion + noise	vs Output power	1 - 24
Total harmonic distortion + noise	vs Frequency	25 - 32
Supply voltage rejection ratio	vs Frequency	33, 34
Power dissipation	vs Output power	35 - 42
Crosstalk	vs Frequency	43 - 46
Output power	vs Supply voltage	47 - 50
Quiescent supply current	vs Supply voltage	51
Output power	vs Load resistance	52 - 60
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TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

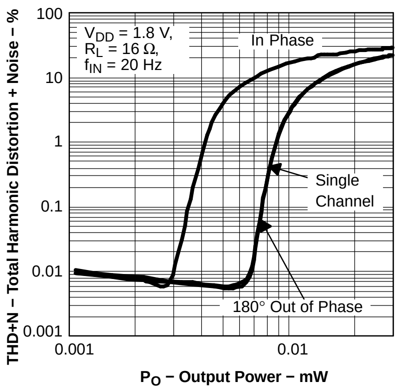


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

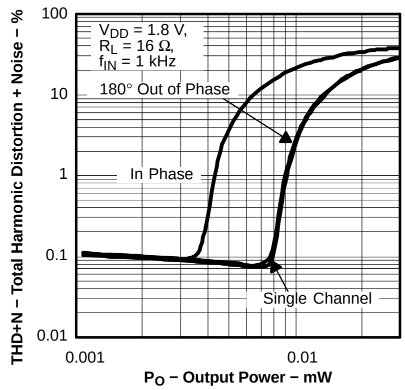


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

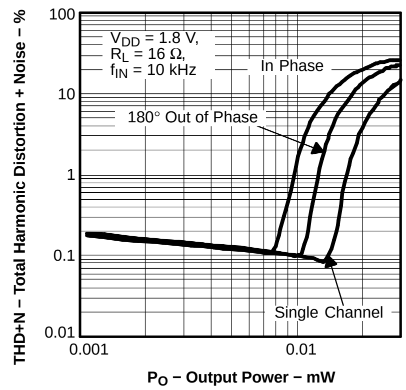


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

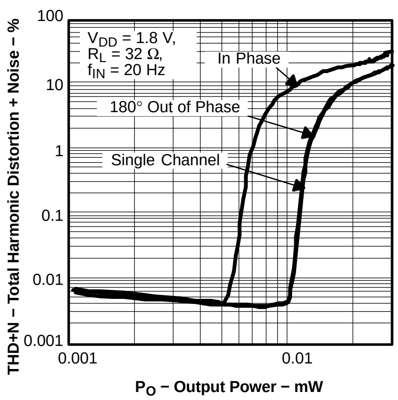


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

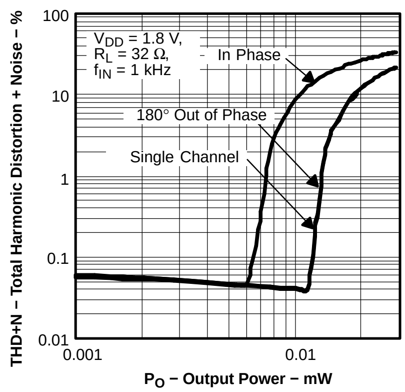


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

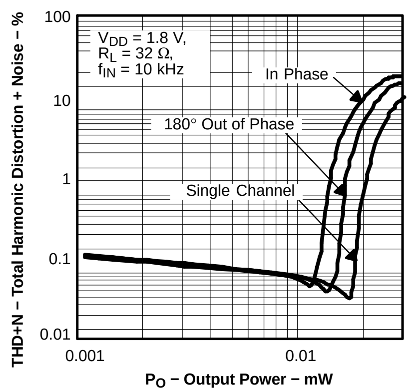


Figure 6.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

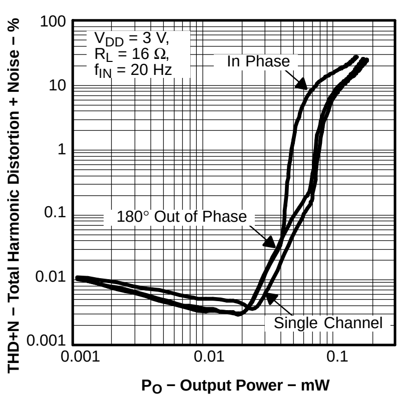


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

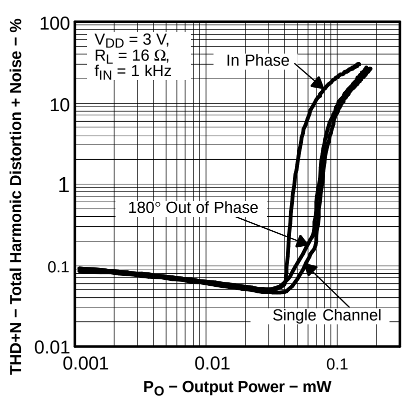


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

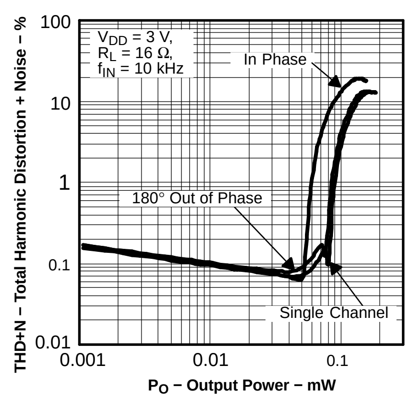


Figure 9.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

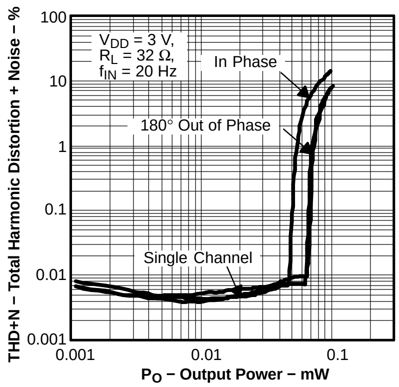


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

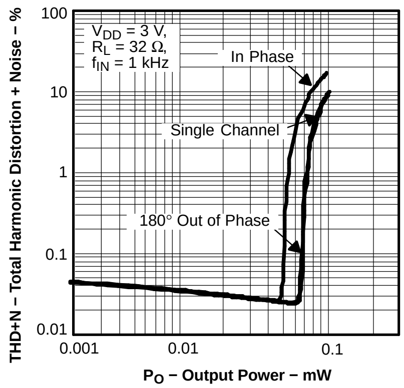


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

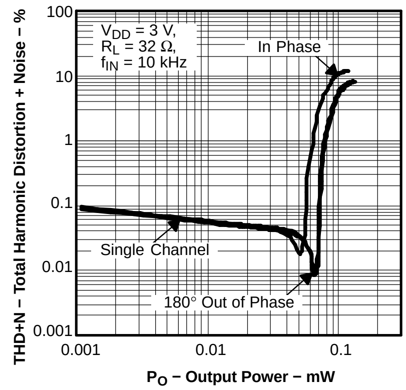


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

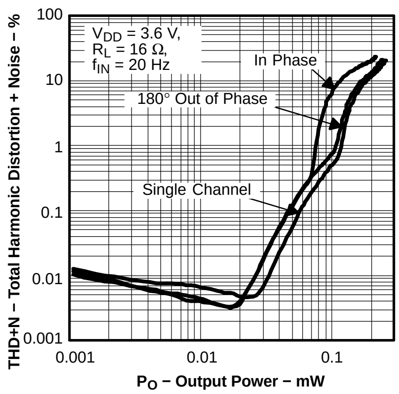


Figure 13.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

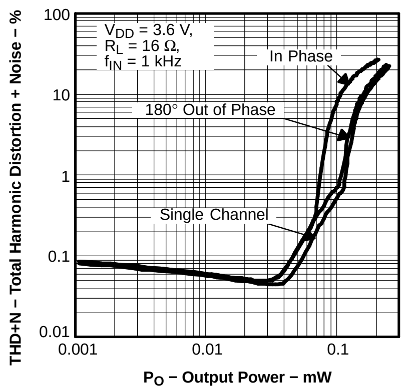


Figure 14.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

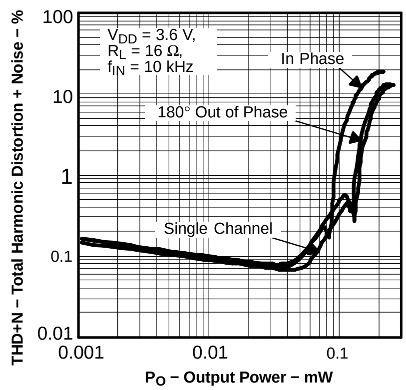


Figure 15.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

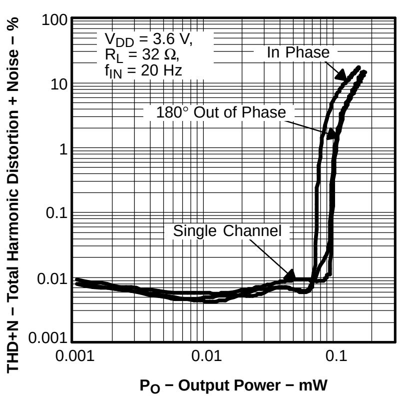


Figure 16.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

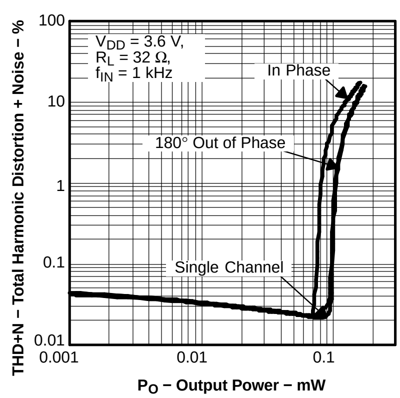


Figure 17.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

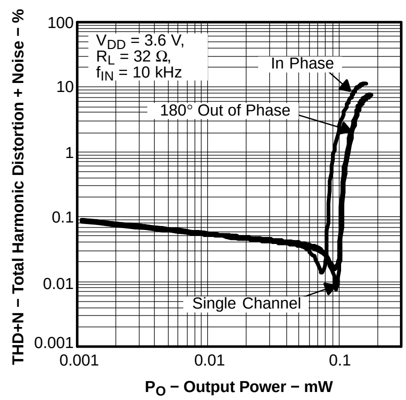


Figure 18.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

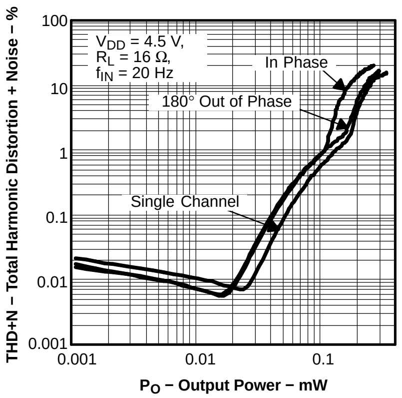


Figure 19.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

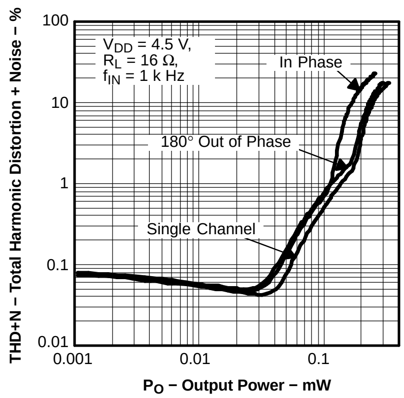


Figure 20.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

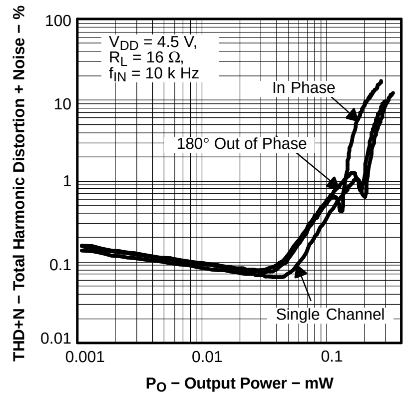


Figure 21.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

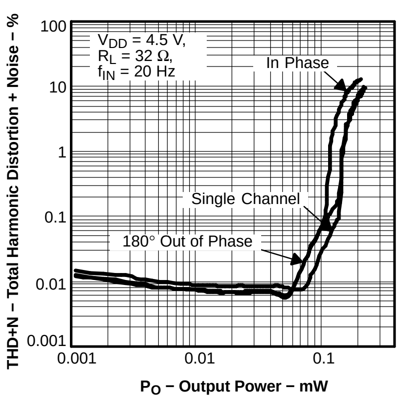


Figure 22.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

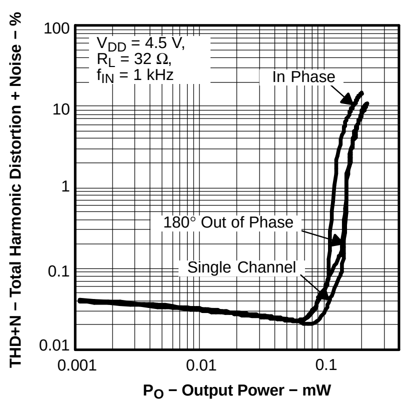


Figure 23.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

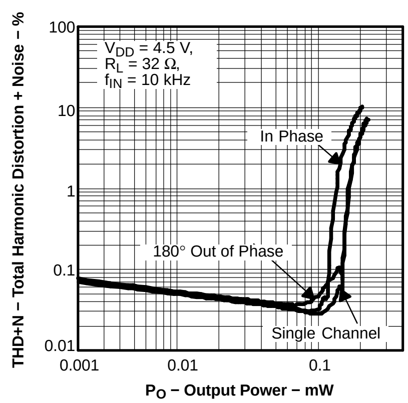


Figure 24.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

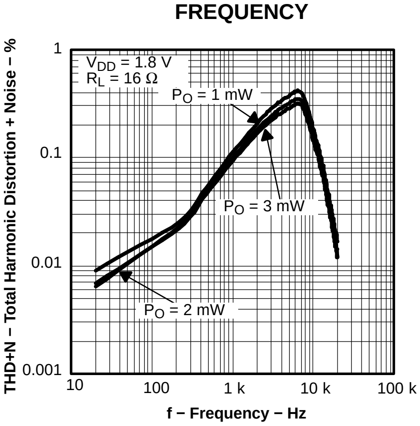


Figure 25.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

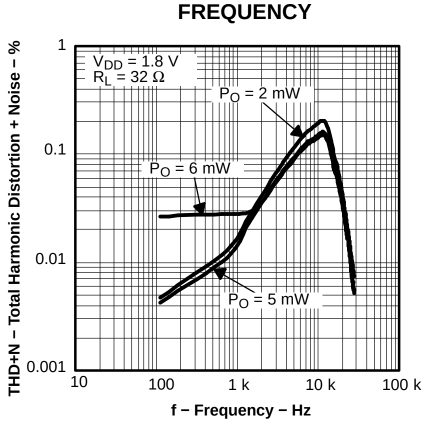


Figure 26.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

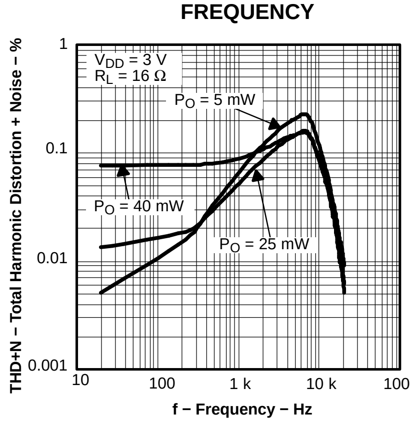


Figure 27.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

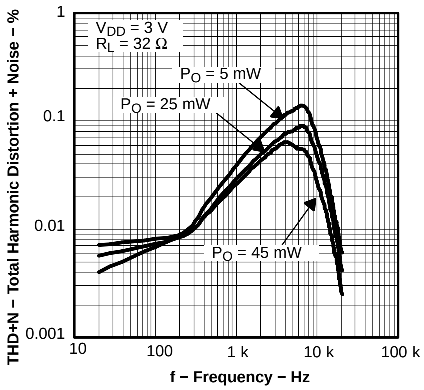


Figure 28.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

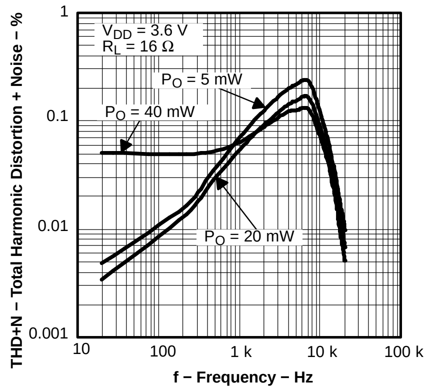


Figure 29.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

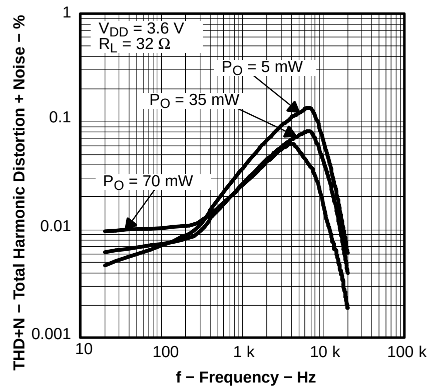


Figure 30.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

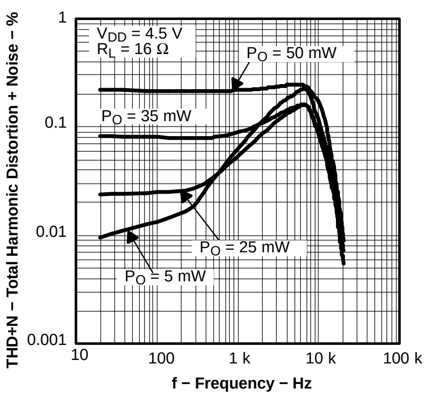


Figure 31.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

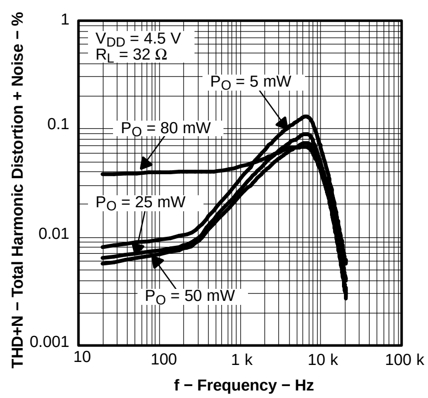


Figure 32.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

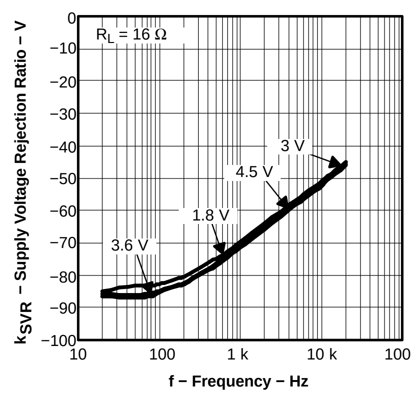


Figure 33.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

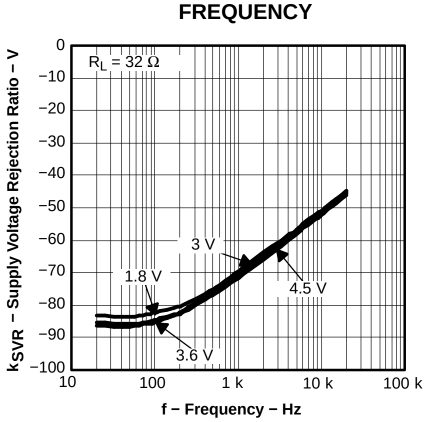


Figure 34.

POWER DISSIPATION vs OUTPUT POWER

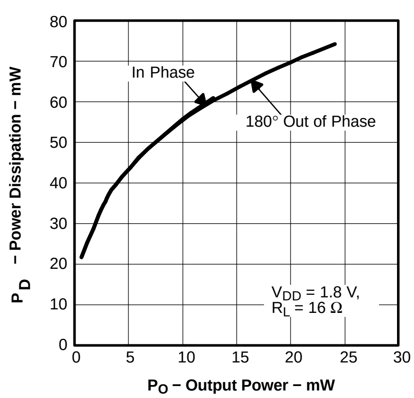


Figure 35.

POWER DISSIPATION vs OUTPUT POWER

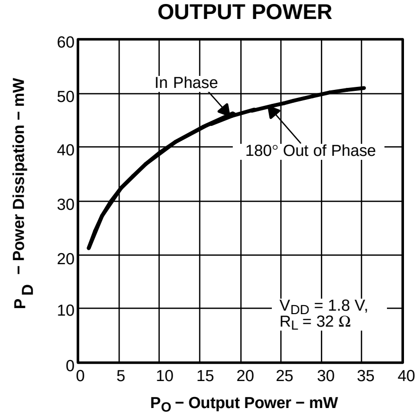


Figure 36.

**POWER DISSIPATION
vs
OUTPUT POWER**

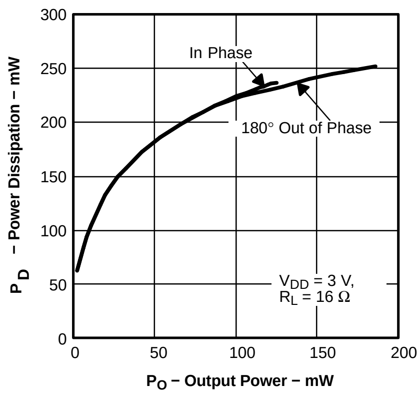


Figure 37.

**POWER DISSIPATION
vs
OUTPUT POWER**

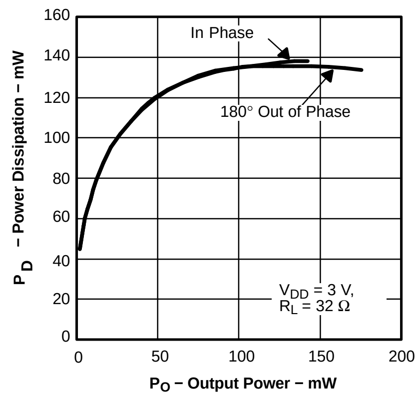


Figure 38.

**POWER DISSIPATION
vs
OUTPUT POWER**

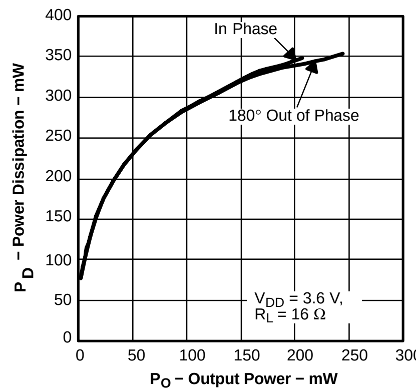


Figure 39.

**POWER DISSIPATION
vs
OUTPUT POWER**

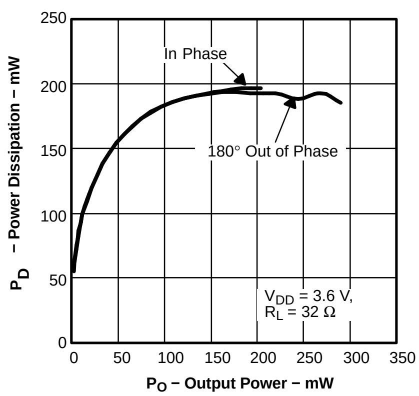


Figure 40.

**POWER DISSIPATION
vs
OUTPUT POWER**

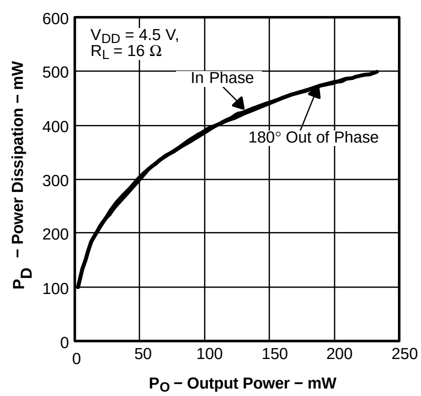


Figure 41.

**POWER DISSIPATION
vs
OUTPUT POWER**

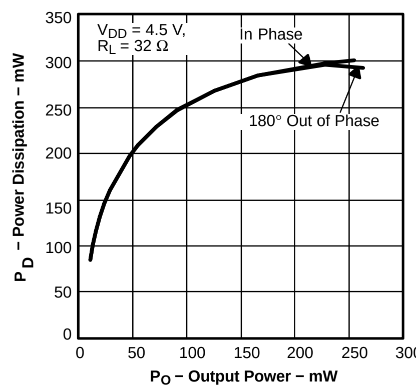


Figure 42.

**CROSSTALK
vs
FREQUENCY**

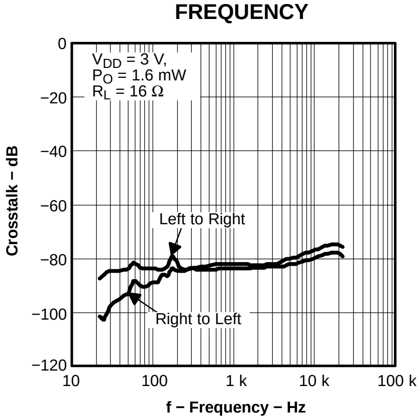


Figure 43.

**CROSSTALK
vs
FREQUENCY**

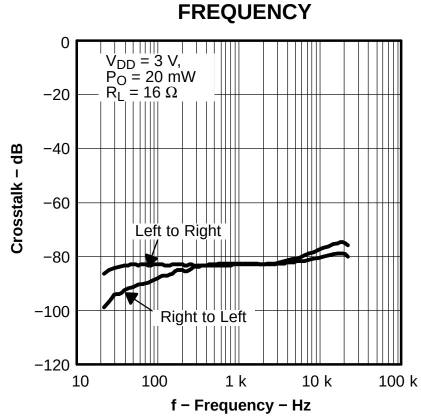


Figure 44.

**CROSSTALK
vs
FREQUENCY**

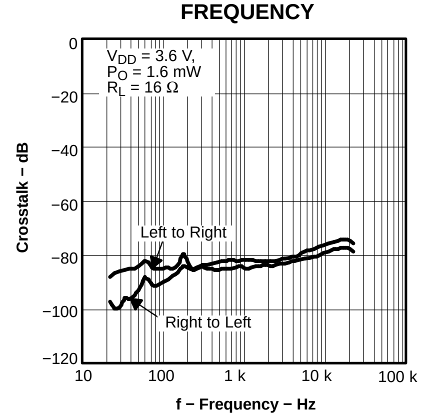


Figure 45.

CROSSTALK vs FREQUENCY

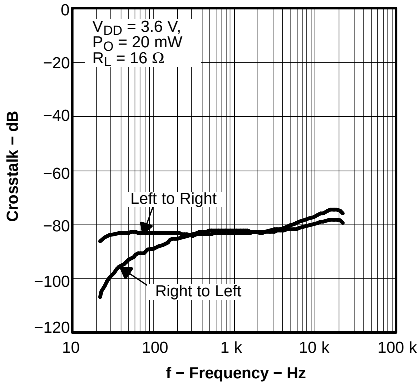


Figure 46.

OUTPUT POWER vs SUPPLY VOLTAGE

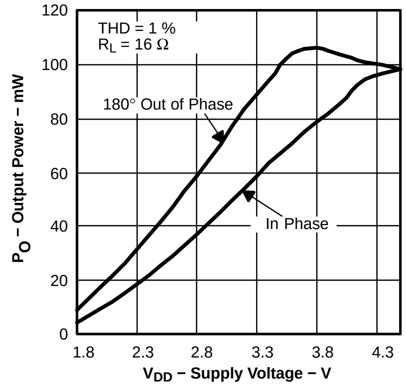


Figure 47.

OUTPUT POWER vs SUPPLY VOLTAGE

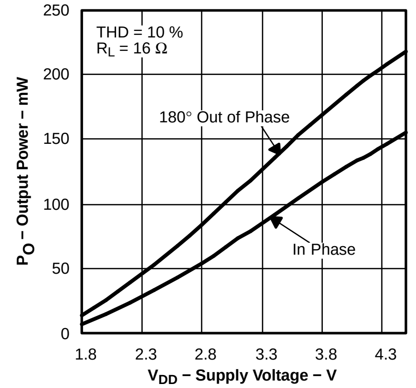


Figure 48.

OUTPUT POWER vs SUPPLY VOLTAGE

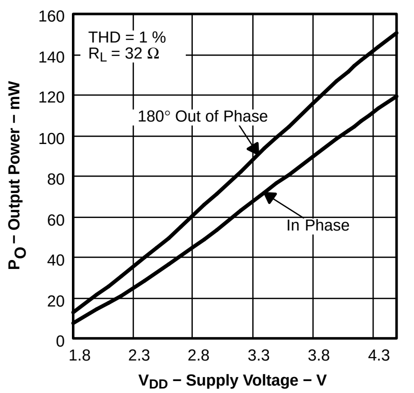


Figure 49.

OUTPUT POWER vs SUPPLY VOLTAGE

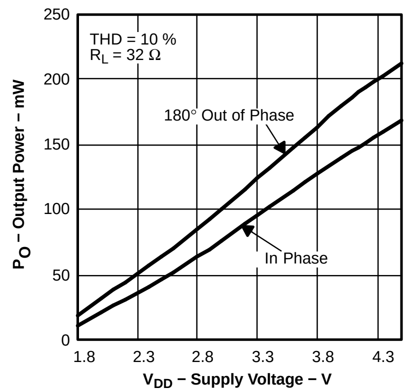


Figure 50.

QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

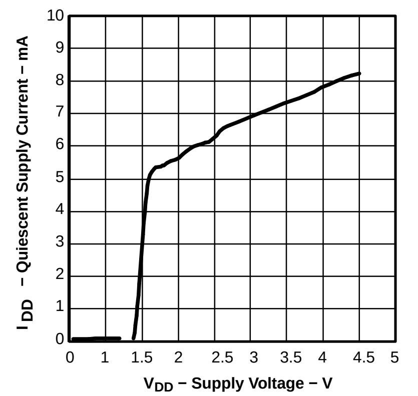


Figure 51.

OUTPUT POWER vs LOAD RESISTANCE

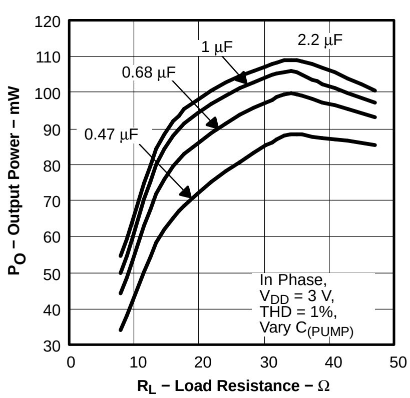


Figure 52.

OUTPUT POWER vs LOAD RESISTANCE

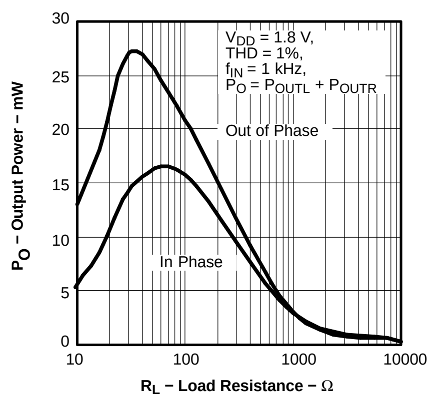


Figure 53.

OUTPUT POWER vs LOAD RESISTANCE

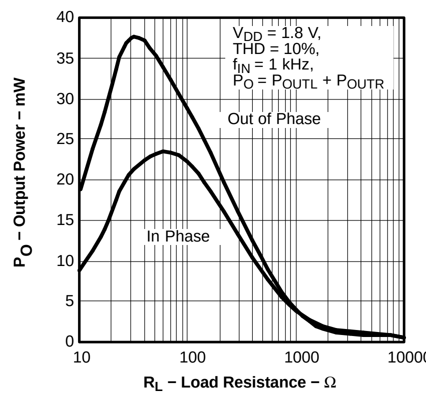


Figure 54.

**OUTPUT POWER
vs
LOAD RESISTANCE**

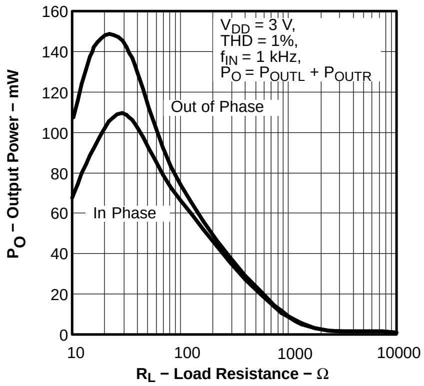


Figure 55.

**OUTPUT POWER
vs
LOAD RESISTANCE**

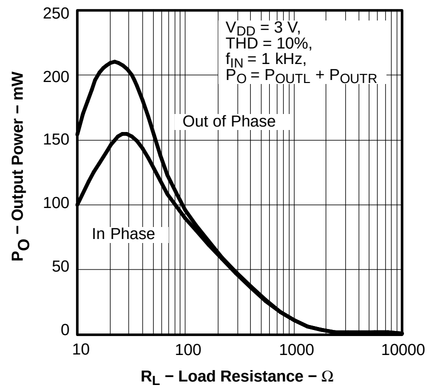


Figure 56.

**OUTPUT POWER
vs
LOAD RESISTANCE**

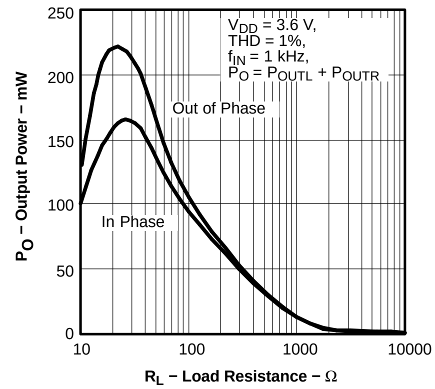


Figure 57.

**OUTPUT POWER
vs
LOAD RESISTANCE**

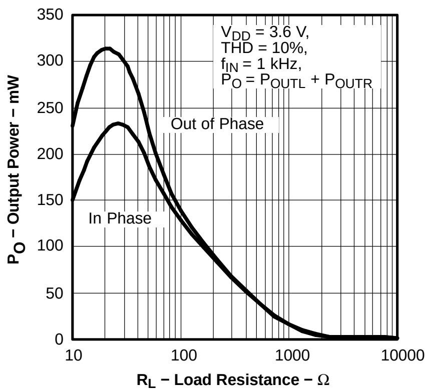


Figure 58.

**OUTPUT POWER
vs
LOAD RESISTANCE**

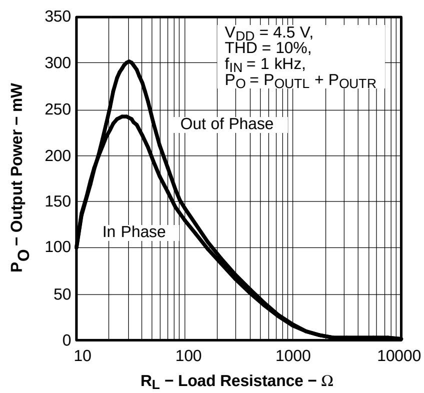


Figure 59.

**OUTPUT POWER
vs
LOAD RESISTANCE**

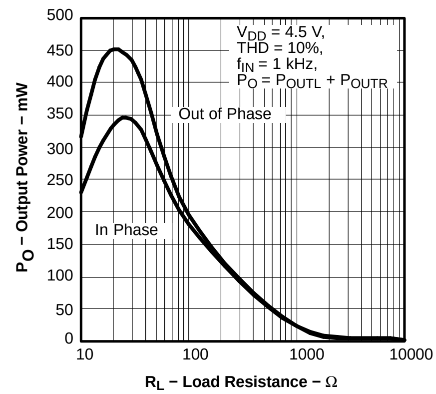


Figure 60.

OUTPUT SPECTRUM

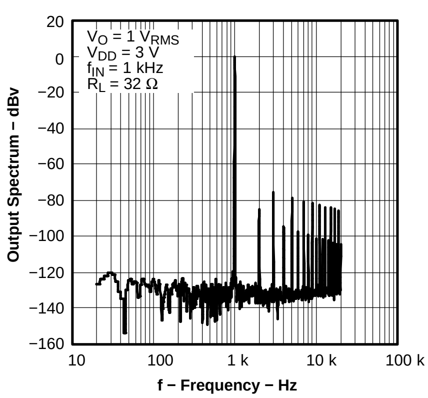


Figure 61.

**GAIN AND PHASE
vs
FREQUENCY**

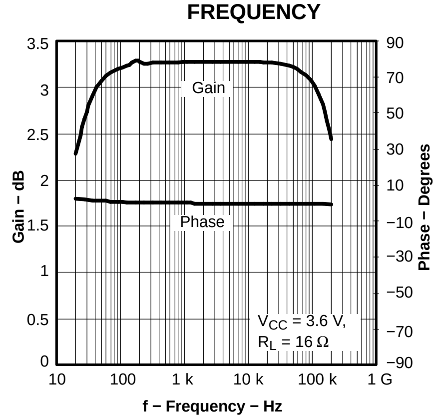


Figure 62.

**GAIN AND PHASE
vs
FREQUENCY**

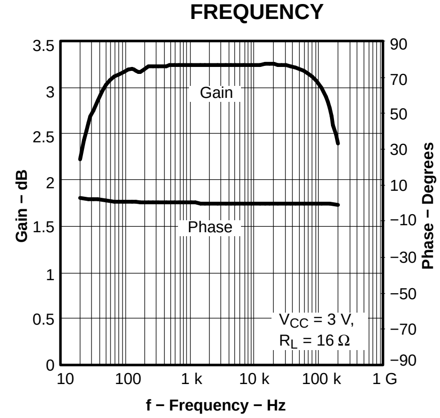


Figure 63.

APPLICATION INFORMATION

Headphone Amplifiers

For single-supply headphone amplifiers, the output architecture typically require dc-blocking capacitors to remove the mid-rail bias required to obtain symmetrical output voltage swing. These capacitors are required because most headphone jacks are ground-referenced, with respect to the shield pin. Without the capacitors, there would be a dc bias voltage across the headphone speakers. In Figure 64, the first block diagram and waveform illustrate the traditional headphone amplifier connection to the headphone jack and output signal.

These capacitors are typically large in value in order to prevent the filtering of the output audio signal. The dc-blocking capacitors form a high-pass filter with the load impedance of the headphone speakers. Treating the headphone speakers as a resistive load, typically either 16Ω or 32 Ω, the dc-blocking capacitors form a high-pass filter with the load impedance. Equation 1 shows the relationship between the load impedance (R), the capacitor (C), and the cutoff frequency.

$$f = \frac{1}{2\pi\, R\, C} \tag{1}$$

Substituting for the values in the circuit, the dc-blocking capacitors can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi\, R_L\, fc_{OUT}} \tag{2}$$

From Equation 2, the capacitor must have a large value because the resistance value is small. Large capacitance values require large package sizes which consume board area, increase cost of the assembly, and can reduce the fidelity of the audio output signal.

Two different capless headphone amplifier applications are available that allow for the removal of the output dc-blocking capacitors. The first amplifier architecture is implemented in the same manner as the traditional amplifier with the exception of the headphone jack shield pin. This amplifier provides a reference voltage, which is connected to the headphone jack shield pin. This is the voltage on which the audio output signals are centered. This voltage reference is typically half of the amplifier power supply because this allows symmetrical swing of the output voltages. The second block diagram and waveform shows the mid-supply biased capless headphone architecture.

The second amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Using this negative supply, the headphone amplifier is now a split supply amplifier (internally) and can be considered a ground-reference amplifier. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. The bottom block diagram and waveform of Figure 64 illustrate the ground-referenced capless headphone architecture.

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the TPA4411. These capacitors block the dc portion of the audio source and allow the TPA4411 inputs to be properly biased to provide maximum performace.

These capacitors form a high-pass filter with the input impedance of the TPA4411. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is input-blocking capacitor and the resistance is the input impedance of the TPA4411. Because the gain of the TPA4411 is fixed, the input impedance remains a constant value. Using the input impedance value from the operating characteristics table and Equation 2, the frequency and/or capacitance can be determined when one of the two values are given.

$$fc_{IN} = \frac{1}{2\pi\, R_{IN}\, C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi\, fc_{IN}\, R_{IN}} \tag{3}$$

- Where R_{IN} = 15 kΩ.

APPLICATION INFORMATION (continued)

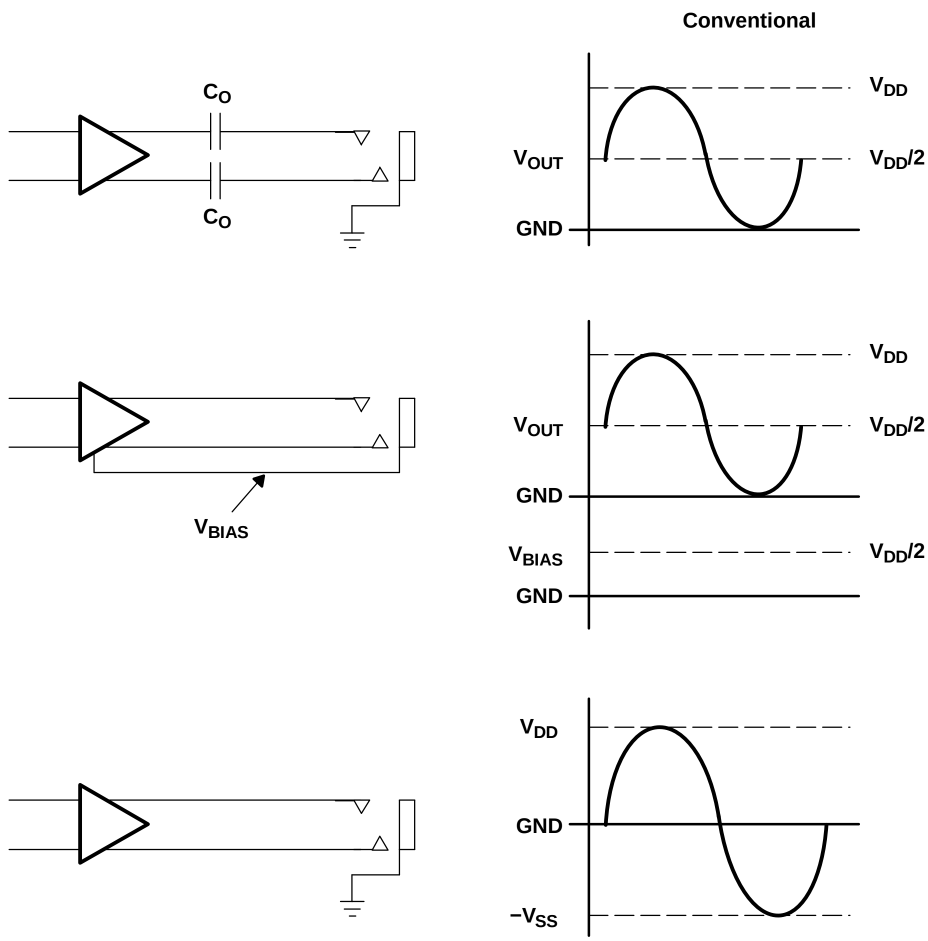


Figure 64. Amplifier Applications

Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 2.2 µF is typical. Capacitor values that are smaller than 2.2 µF can be used, but the maximum output power is reduced and the device may not operate to specifications. Figures 65 through 75 compare the performance of the TPA4411 with the recommended 2.2-µF capacitors and 1-µF capacitors.

APPLICATION INFORMATION (continued)

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

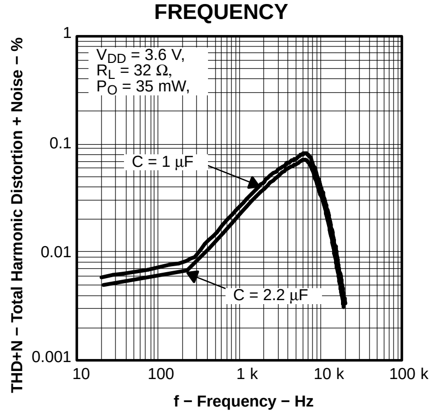


Figure 65.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

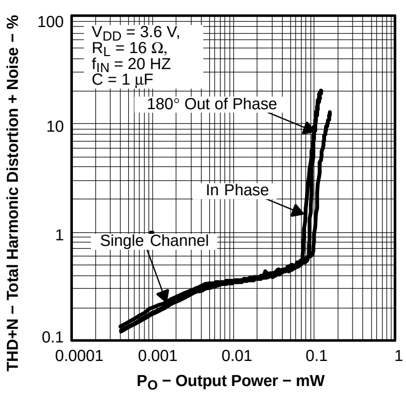


Figure 66.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

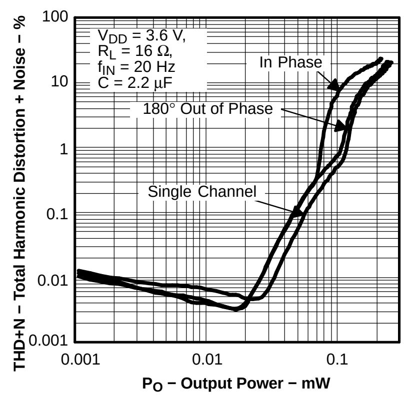


Figure 67.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

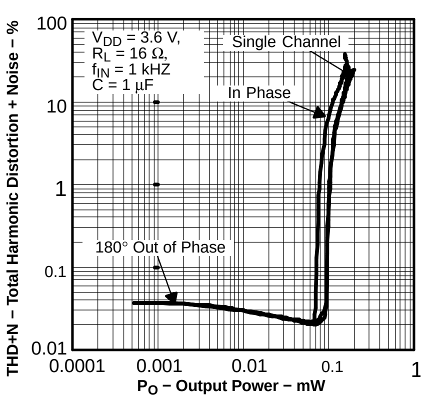


Figure 68.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

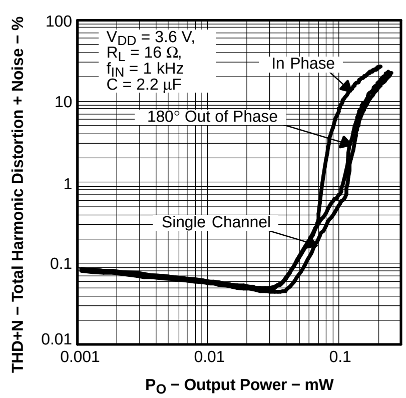


Figure 69.

APPLICATION INFORMATION (continued)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

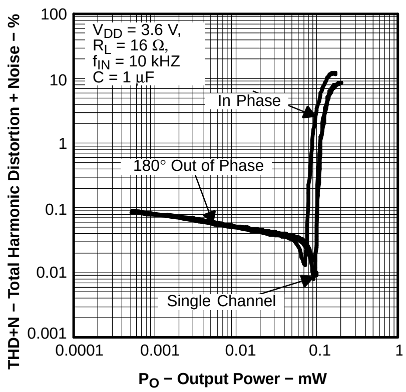


Figure 70.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

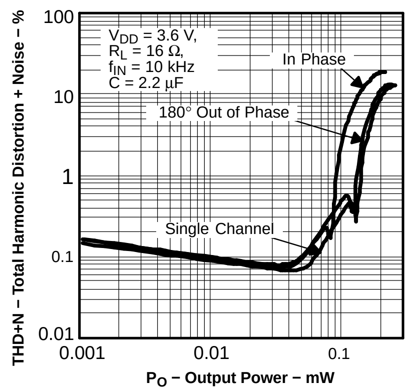


Figure 71.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

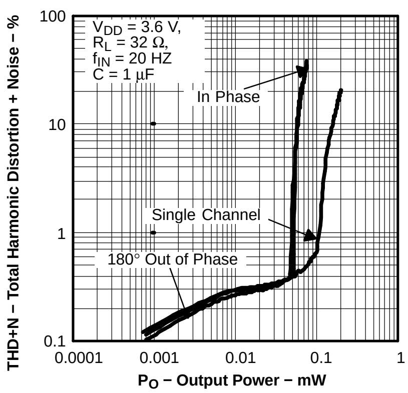


Figure 72.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

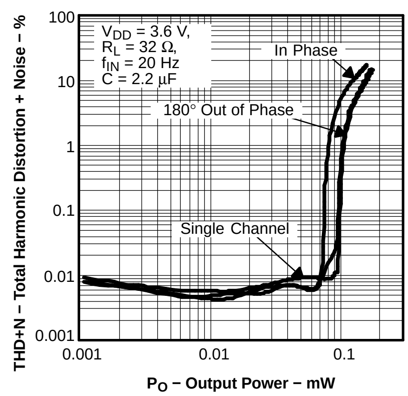


Figure 73.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

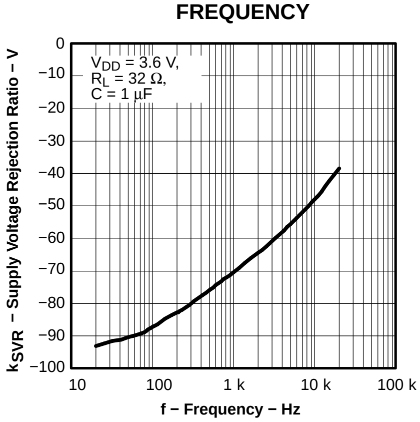


Figure 74.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

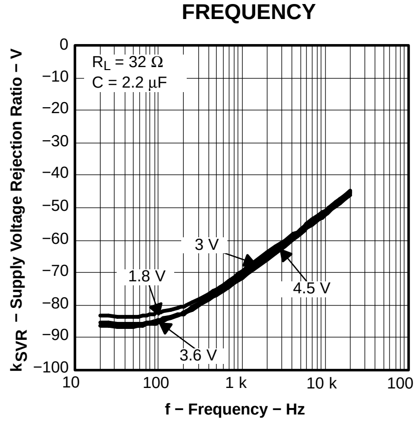


Figure 75.

APPLICATION INFORMATION (continued)

Decoupling Capacitors

The TPA4411 is a capless headphone amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 2.2 µF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the TPA4411 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Supply Voltage Limiting At 4.5 V

The TPA4411 has a built-in charge pump which serves to generate a negative rail for the headphone amplifier. Because the headphone amplifier operates from a positive voltage and negative voltage supply, circuitry has been implemented to protect the devices in the amplifier from an overvoltage condition. Once the supply is above 4.5 V, the TPA4411 can shut down in an overvoltage protection mode to prevent damage to the device. The TPA4411 resumes normal operation once the supply is reduced to 4.5 V or lower.

Layout Recommendations

Exposed Pad On TPA4411RTJ Package Option

The exposed metal pad on the TPA4411RTJ package must be soldered down to a pad on the PCB in order to maintain reliability. *The pad on the PCB should be allowed to float and not be connected to ground or power*. Connecting this pad to power or ground prevents the device from working properly because it is connected internally to PVSS.

SGND and PGND Connections

The SGND and PGND pins of the TPA4411 must be routed separately back to the decoupling capacitor in order to provide proper device operation. If the SGND and PGND pins are connected directly to each other, the part functions without risk of failure, but the noise and THD performance do not meet the specifications.

APPLICATION INFORMATION (continued)

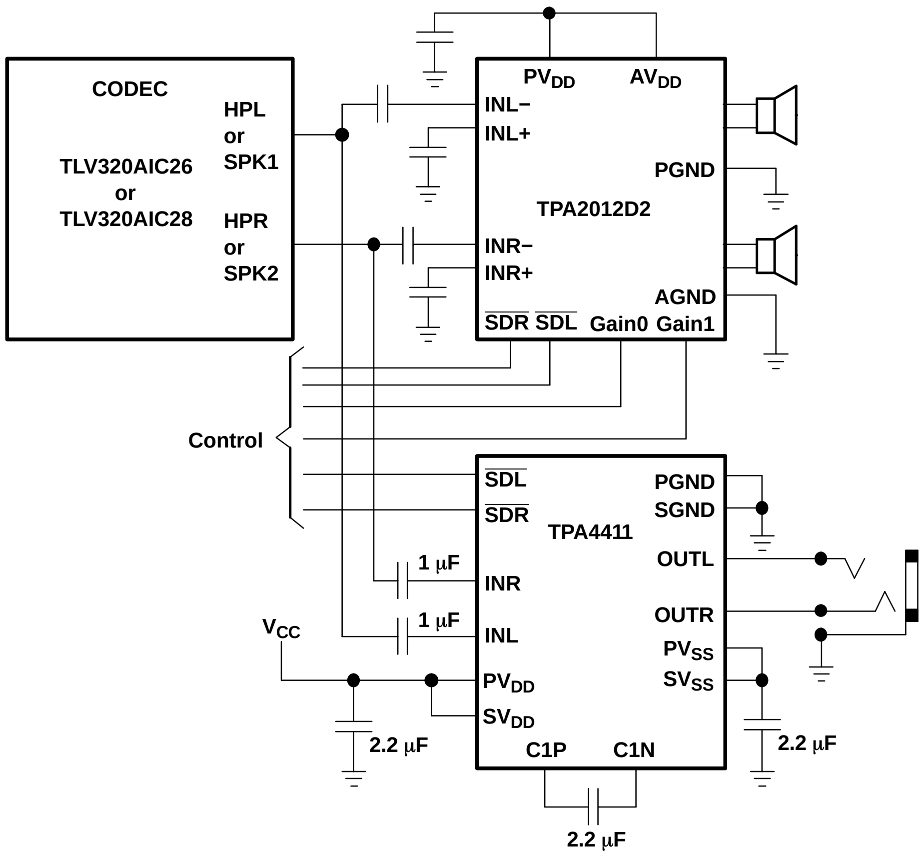
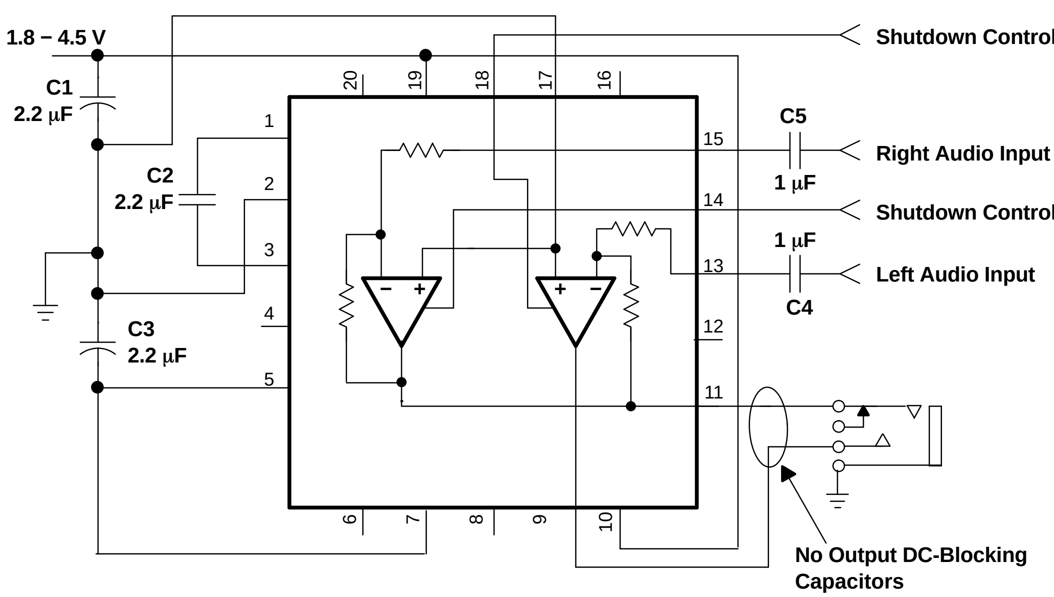


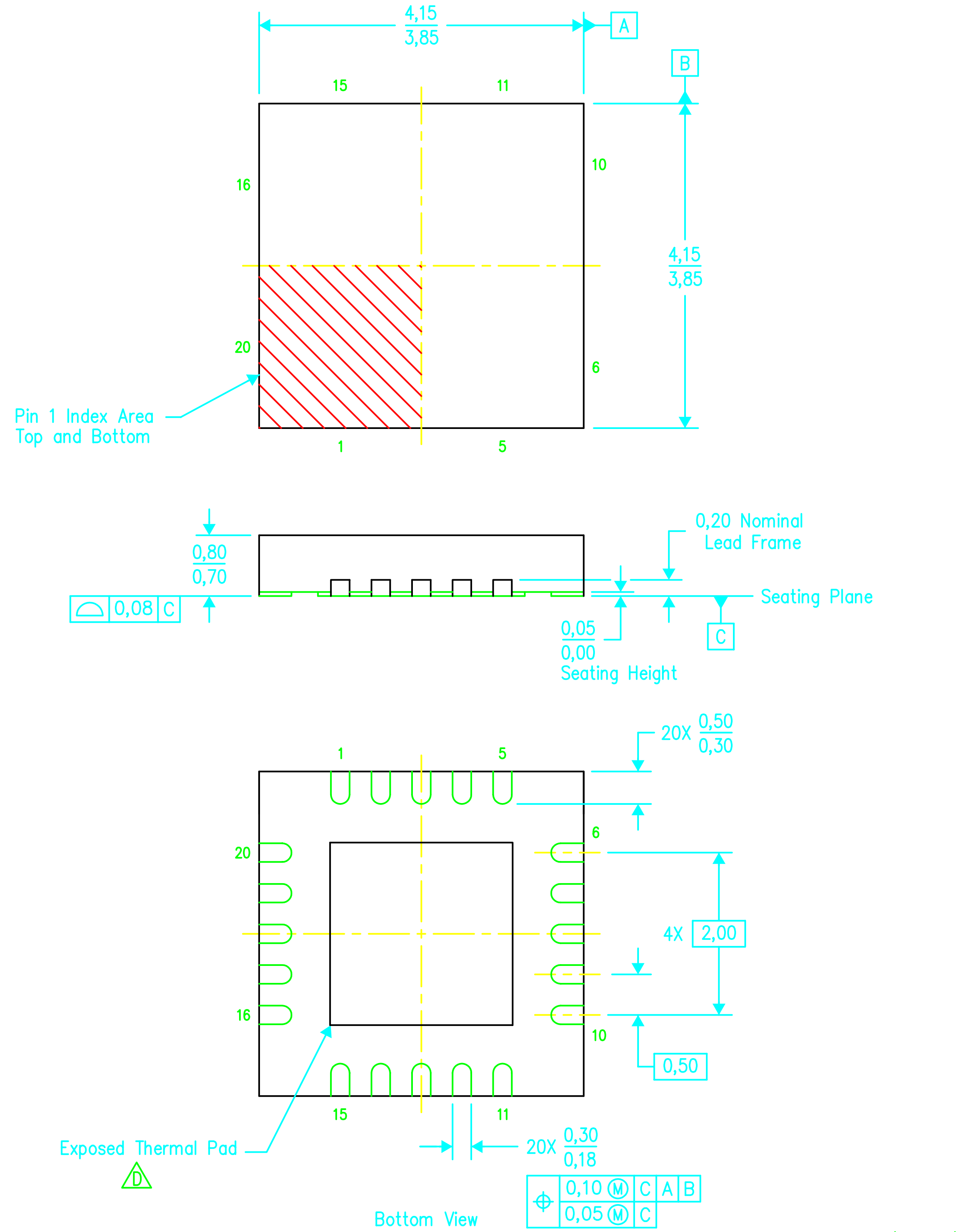
Figure 76. Application Circuit



Note: PowerPAD must be soldered down and plane must be floating.

Figure 77. Typical Circuit

RTJ (S–PQFP–N20) PLASTIC QUAD FLATPACK



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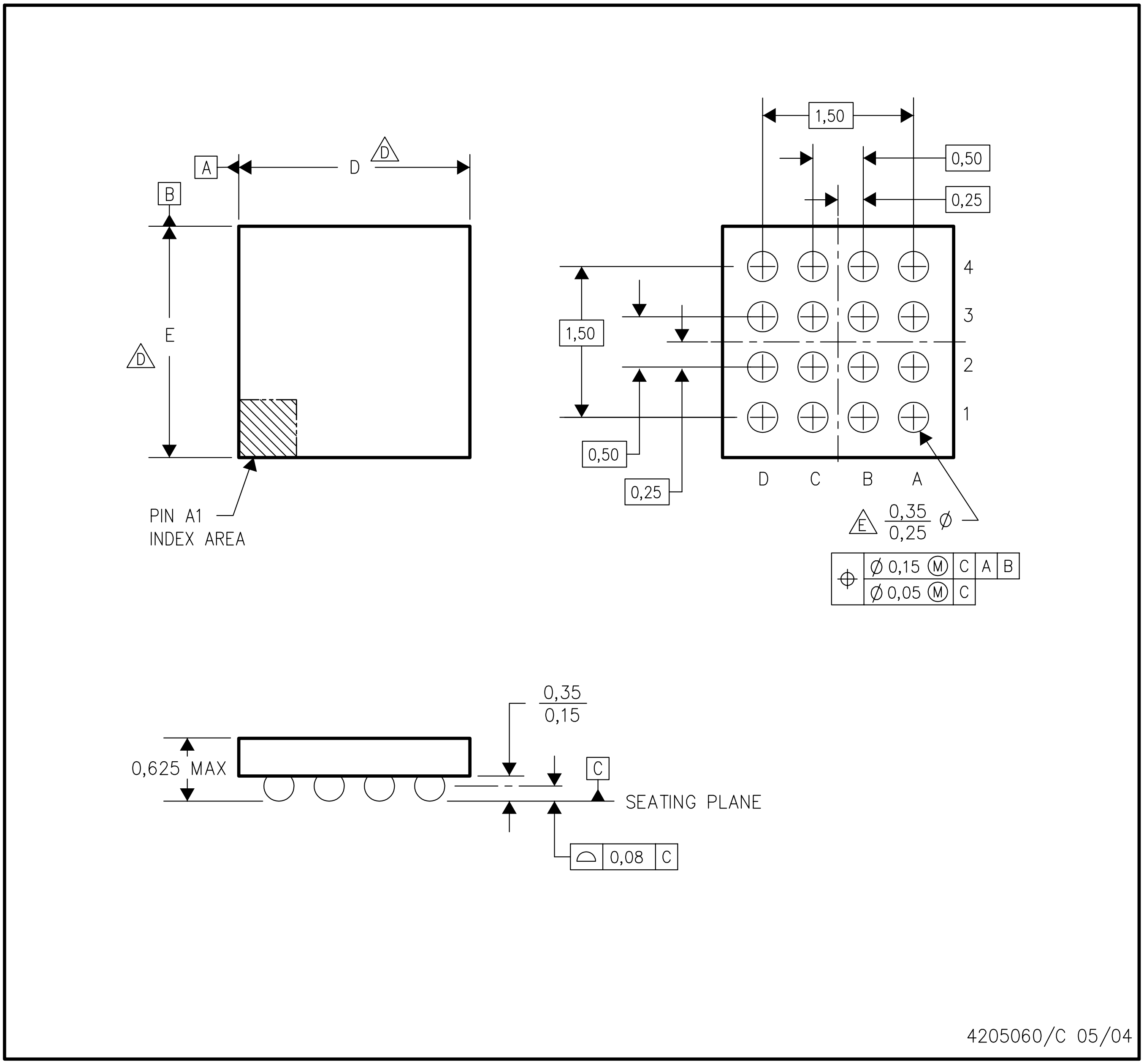
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

YZH (S–XBGA–N16) DIE–SIZE BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. Devices in YZH package can have dimension D ranging from 1.85 to 2.65 mm and dimension E ranging from 1.85 to 2.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
- E. Reference Product Data Sheet for array population. 4 x 4 matrix pattern is shown for illustration only.
- F. This package contains lead–free balls. Refer to YEH (Drawing #4204183) for tin–lead (SnPb) balls.