

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	5.5	V

TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

CAPACITANCE

($T_A = +25^\circ\text{C}$)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V, f = 1.0MHz$	20	pF
Output capacitance	C_{OUT}	$V_{OUT} = 0V, f = 1.0MHz$	20	pF

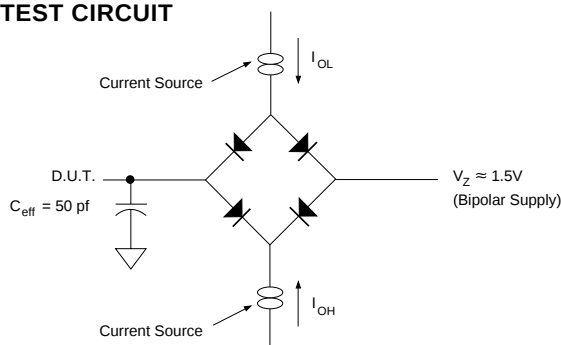
This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(VCC = 3.3V ±0.3V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{CC} = 3.3, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current (x 32 Mode)	I _{CC}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5MHz, V _{CC} = 3.3		120	mA
Standby Current	I _{SB}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, f = 5MHz, V _{CC} = 3.3		8	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Units
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 2.5$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.

LOL & LOH programmable from 0 to 16mA.

Tester Impedance $Z_0 = 75 \Omega$.

V_Z is typically the midpoint of V_{OH} and V_{OL} .

IoL & IoH are adjusted to simulate a typical resistive load circuit.

ATE tester includes jig capacitance.



AC CHARACTERISTICS

(VCC = 3.3V, TA = -55°C to +125°C)

Parameter Read Cycle	Symbol	<u>-15</u>		<u>-17</u>		<u>-20</u>		<u>-25</u>		<u>-35</u>		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	15		17		20		25		35		ns
Address Access Time	t _{AA}		15		17		20		25		35	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		0		ns
Chip Select Access Time	t _{ACS}		15		17		20		25		35	ns
Output Enable to Output Valid	t _{OE}		10		11		12		15		20	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		5		5		5		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	5		5		5		5		5		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		8		9		10		12		15	ns
Output Disable to Output in High Z	t _{OHZ} ¹		8		9		10		12		15	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

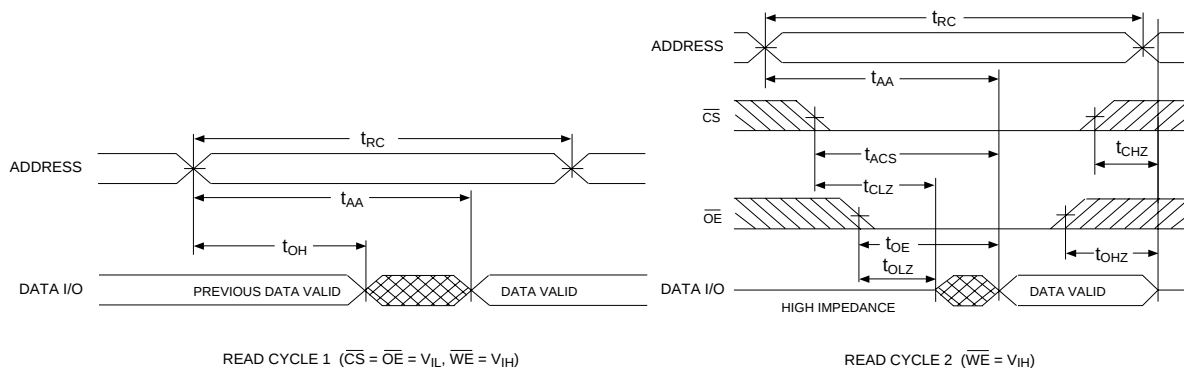
(VCC = 3.3V, TA = -55°C to +125°C)

Parameter Write Cycle	Symbol	<u>-15</u>		<u>-17</u>		<u>-20</u>		<u>-25</u>		<u>-35</u>		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	15		17		20		25		35		ns
Chip Select to End of Write	t _{CW}	13		14		15		20		30		ns
Address Valid to End of Write	t _{AW}	13		14		15		20		30		ns
Data Valid to End of Write	t _{DW}	10		11		12		15		18		ns
Write Pulse Width	t _{WP}	13		14		15		20		30		ns
Address Setup Time	t _{AS}	0		0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		0		ns
Output Active from End of Write	t _{OW} ¹	5		5		5		5		5		ns
Write Enable to Output in High Z	t _{WHZ} ¹		8		9		10		10		15	ns
Data Hold Time	t _{DH}	0		0		0		0		0		ns

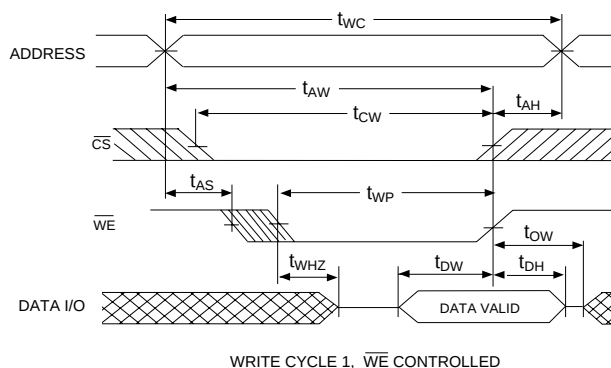
1. This parameter is guaranteed by design but not tested.



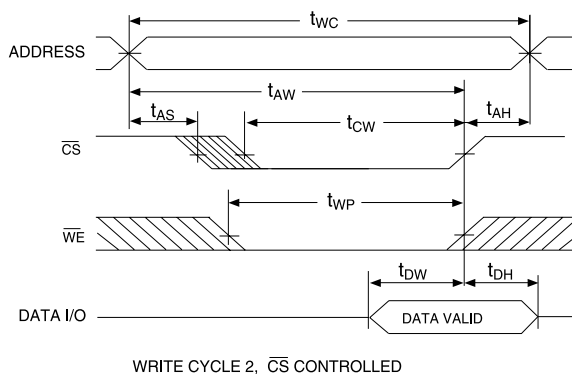
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - $\overline{WE}$ CONTROLLED

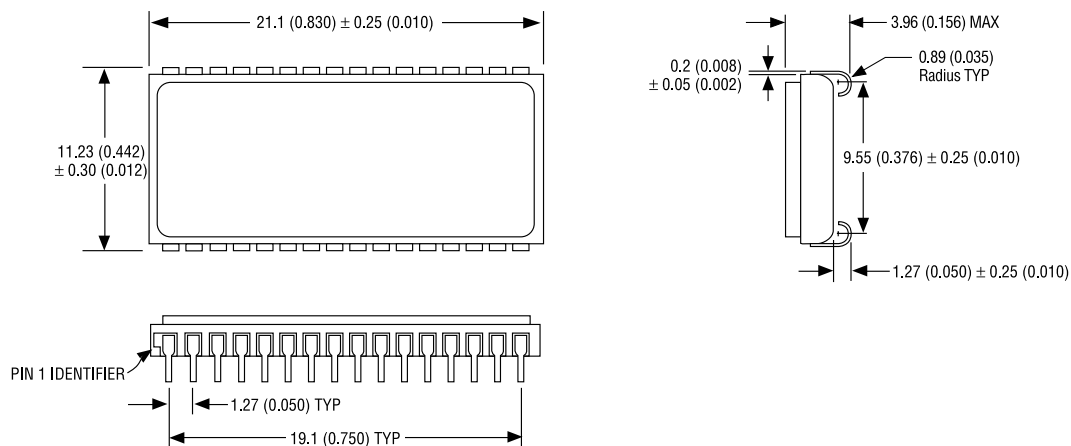


WRITE CYCLE - $\overline{CS}$ CONTROLLED



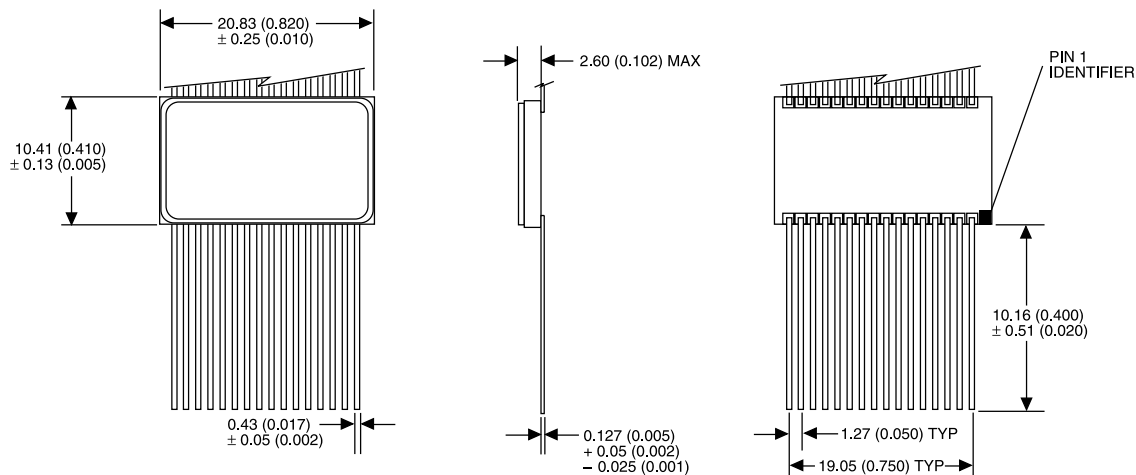


PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

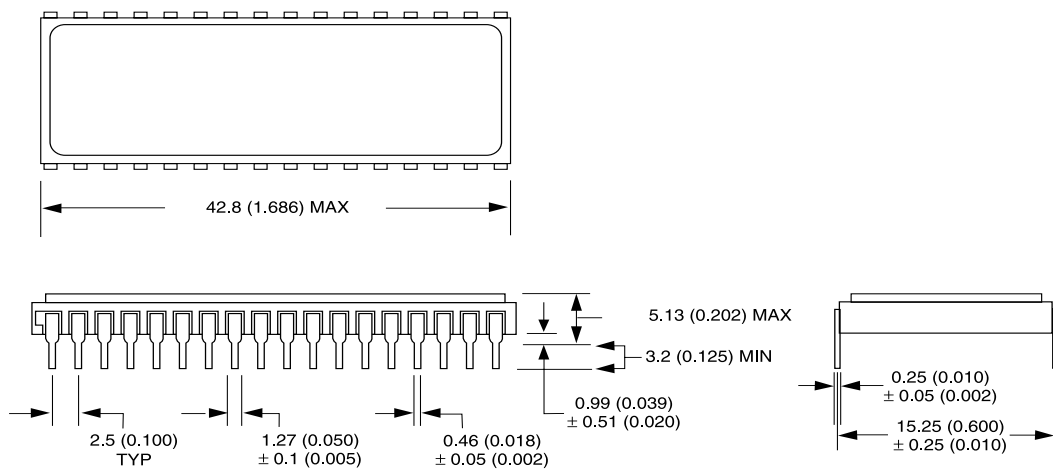
PACKAGE 220: 32 LEAD, CERAMIC FLAT PACK



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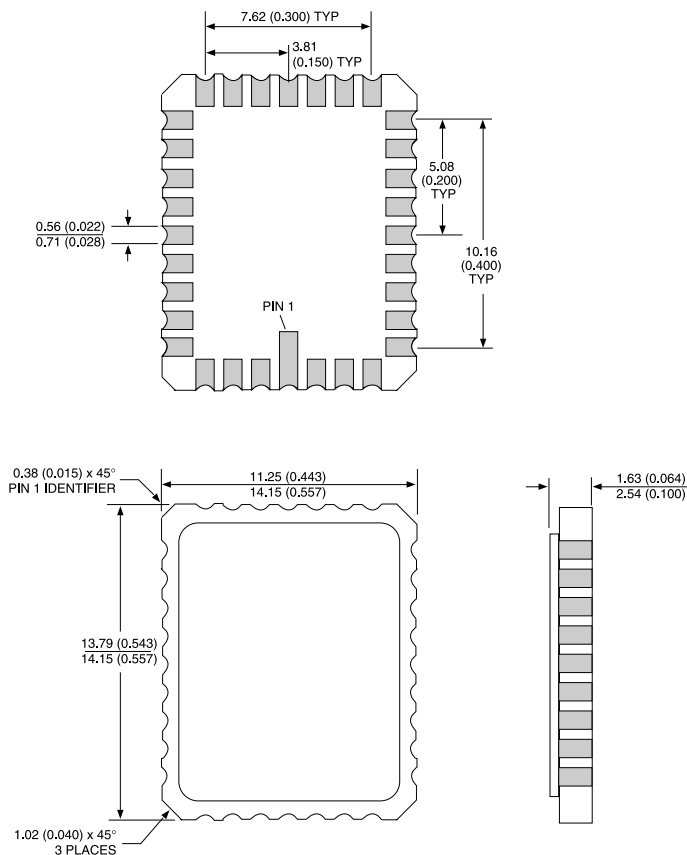
PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W M S 128K8 V - XXX X X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE:

C = 32 Pin Ceramic .600" DIP (Package 300)

CL = 32 Pin Rectangular Ceramic Leadless Chip Carrier (Package 601)

DR = 32 Lead Ceramic SOJ (Package 101) Revolutionary

FR = 32 Lead Ceramic Flat Pack (Package 220**) Revolutionary

ACCESS TIME (ns)

IMPROVEMENT MARK:

Low Voltage Supply 3.3V $\pm$ 10%

ORGANIZATION, 128K x 8

SRAM

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.

** Package under development.

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