

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90540/545 Series

MB90F543/F549/V540

■ DESCRIPTION

The MB90540/545 series with FULL-CAN*1 and FLASH ROM is specially designed for automotive and industrial applications. Its main features are two on board CAN Interfaces (one for MB90V545 series), which conform to V2.0 Part A and Part B, supporting very flexible message buffer scheme and so offering more functions than a normal full CAN approach. The instruction set by F²MC-16LX CPU core inherits an AT architecture of the F²MC*2 family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The micro controller has a 32-bit accumulator for processing long word data. The MB90540/545 series has peripheral resources of 8/10-bit A/D converters, UART(SCI), extended I/O serial interfaces, 8/16-bit timer, I/O timer (input capture(ICU), output compare (OCU)).

*1:Controller Area Network (CAN) - License of Robert Bosch GmbH.

*2:F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock

Embedded PLL clock multiplication circuit

Operating clock (PLL clock) can be selected from: divided-by-2 of oscillation or one to four times the oscillation

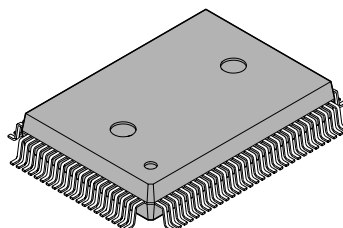
Minimum instruction execution time: 62.5 ns (operation at oscillation of 4 MHz, four times the oscillation clock, V_{CC} of 5.0V)

Subsystem Clock: 32 kHz

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■ PACKAGE

100-pin Plastic QFP



(FPT-100P-M06)

MB90540/545 Series

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- Instruction set to optimize controller applications
 - Rich data types (bit, byte, word, long word)
 - Rich addressing mode (23 types)
 - Enhanced signed multiplication/division instruction and RETI instruction functions
 - Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C language) and multi-task operations
 - Adoption of system stack pointer
 - Enhanced pointer indirect instructions
 - Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed: 4-byte Instruction queue
- Enhanced interrupt function: 8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
 - Extended intelligent I/O service function (EI²OS)
- Embedded ROM size and types
 - Flash ROM: 128 Kbytes / 256 Kbytes
 - Embedded RAM size: 6 Kbytes / 8 Kbytes (evaluation chip)
- Flash ROM
 - Supports automatic programming, Embedded Algorithm TM*
 - Write / Erase / Erase-Suspend / Resume commands
 - A flag indicating completion of the algorithm
 - Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory
 - Erase can be performed on each block
 - Block protection with external programming voltage
- Low-power consumption (stand-by) mode
 - Sleep mode (mode in which CPU operating clock is stopped)
 - Stop mode (mode in which oscillation is stopped)
 - CPU intermittent operation mode
 - Clock mode
 - Hardware stand-by mode
- Process
 - 0.5 μ m CMOS technology
- I/O port
 - General-purpose I/O ports: 81 ports
- Timer
 - Watchdog timer: 1 channel
 - 8/16-bit PPG timer: 8/16-bit $\times$ 4 channels
 - 16-bit re-load timer: 2 channels
- 16-bit I/O timer
 - 16-bit free-run timer: 1 channel
 - Input capture: 8 channels
 - Output compare: 4 channels
- Extended I/O serial interface: 1 channel
- UART 0
 - With full-duplex double buffer (8-bit length)
 - Clock asynchronous or clock synchronized (with start/stop bit) transmission can be selectively used.

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- UART 1
With full-duplex double buffer (8-bit length)
Clock asynchronized or clock synchronized serial (extended I/O serial) can be used.
- External interrupt circuit (8 channels)
A module for starting an extended intelligent I/O service (EI²OS) and generating an external interrupt which is triggered by an external input.
- Delayed interrupt generation module
Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
8/10-bit resolution can be selectively used.
Starting by an external trigger input.
Conversion time: 26.3 μ s
- FULL-CAN interfaces
MB90540 series: 2 channel
MB90545 series: 1 channel
Conforming to Version 2.0 Part A and Part B
Flexible message buffering (mailbox and FIFO buffering can be mixed)
- External bus interface: Maximum address space 16 Mbytes

*: Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

MB90540/545 Series

■ PRODUCT LINEUP

The following table provides a quick outlook of the MB90540/545 Series

Features		MB90F543	MB90F549	MB90V540
Classification		Flash ROM product		Evaluation product
ROM size		128 Kbytes Boot Block	256 Kbytes Boot Block	None
ROM size		6 K		8 K
CPU functions		The number of instructions: 351 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz) Interrupt processing time: 1.5 μ s (at machine clock frequency of 16 MHz, minimum value)		
UART 0		Clock synchronized transmission (500 K / 1M / 2 Mbps) Clock asynchronized transmission (4808 / 5208 / 9615 / 10417 / 19230 / 38460 / 62500 / 500000 bps at machine clock frequency of 16 MHz) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
UART 1 (SCI)		Clock synchronized transmission (62.5 K/ 12 K/ 250 K/ 500 K/ 1 Mbps) Clock asynchronized transmission (1202/ 2404/ 4808/ 9615/ 31250 bps) Transmission can be performed by bi-directional serial Transmission or by master / slave connection.		
8/10-bit A/D converter		Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or mode successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)		
8/16-bit PPG timers		Number of channels: 8/16 bit $\times$ 4 channels PPG operation of 8-bit or 16 bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$, 128 μ s (at oscillation of 4 MHz, f_{sys} = machine clock frequency of 16 MHz, f_{osc} = oscillation clock frequency)		
16-bit Reload timer		Number of channels:2 Operation clock frequency: $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = System clock frequency) Supports External Event Count function		
16-bit I/O timer	16-bit Output compares	Number of channels: 4 Pin input factor: A match signal of compare register		
	Input captures	Number of channels: 8 Rewriting a register value upon a pin input (rising, falling, or both edges)		

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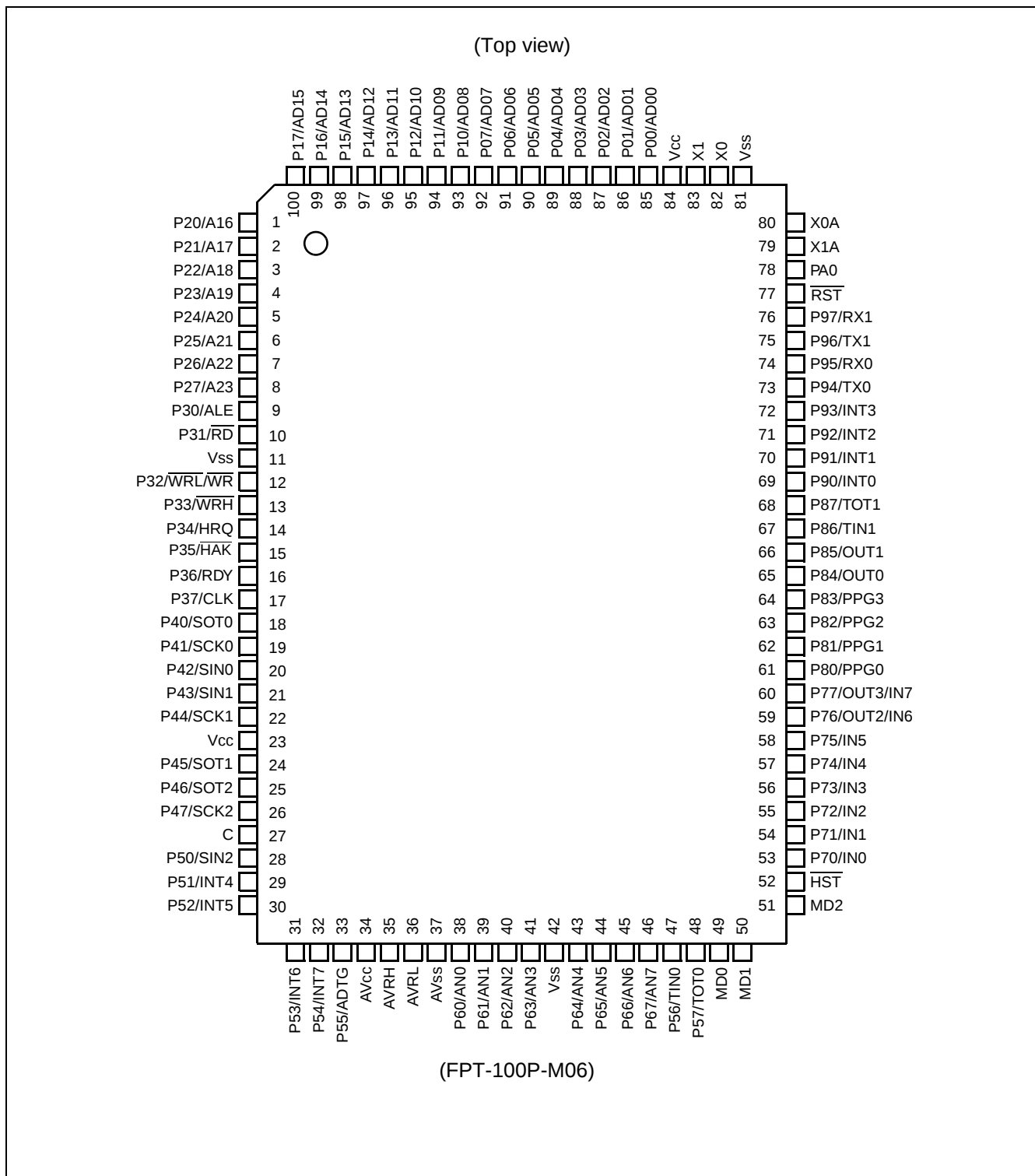
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Features	MB90F543	MB90F549	MB90V540
CAN Interface	Number of channels: 2(MB90540 series), 1(MB90545 series) Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering: Full bit compare / Full bit mask / Two partial bit masks Supports up to 1 Mbps		
External interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.		
Extended I/O serial interface	Clock synchronized transmission (31.25 K / 62.5 K / 125 K / 500 K / 1 Mbps at machine clock frequency of 16 MHz) LSB first / MSB first		
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)		
Flash Memory	Supports automatic programming, Embedded Algorithm TM and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics Inc.		
Low-power consumption (stand-by) mode	Sleep/ stop/ CPU intermittent operation/ clock timer/ hardware stand-by		
Process	CMOS		
Power supply voltage for operation	5 V $\pm$ 10 %		
Package	QFP-100		PGA-256

*: Varies with conditions such as operating frequency. (See section "■ Electrical Characteristics".)

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PIN ASSIGNMENT



(Continued)

■ PIN DESCRIPTION

No.	Pin name	Circuit type	Function
82 83	X0 X1	A (Oscillation)	High speed oscillator input pins
80 79	X0A X1A	A (Oscillation)	Low speed oscillator input pins
77	$\overline{\text{RST}}$	B	External reset request input
52	$\overline{\text{HST}}$	C	Hardware standby input
85 to 92	P00 to P07	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
93 to 100	P10 to P17	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
1 to 8	P20 to P27	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	A16 to A23		8-bit I/O pins for A16 to A23 at the external address bus. This function is enabled when the external bus is enabled.
9	P30	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
10	P31	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	$\overline{\text{RD}}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
12	P32	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output is disabled.
	$\overline{\text{WRL}}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output are enabled. $\overline{\text{WRL}}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access. $\overline{\text{WR}}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access.
	$\overline{\text{WR}}$		
13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or external bus 8-bit mode or when $\overline{\text{WRH}}$ pin output is disabled.
	$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{\text{WRH}}$ output pin is enabled.

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No.	Pin name	Circuit type	Function
14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
	HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
	$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
	RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the clock output is disabled.
	CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
	SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
19	P41	G	General I/O port. This function is enabled when UART0 disables clock output.
	SCK0		Clock I/O pin for UART0. This function is enabled when UART0 enables the clock output.
20	P42	G	General I/O port. This function is always enabled.
	SIN0		Serial data input pin for UART0. While UART0 is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
21	P43	G	General I/O port. This function is always enabled.
	SIN1		Serial data input pin for UART1. While UART1 is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
22	P44	G	General I/O port. This function is enabled when UART1 disables the clock output.
	SCK1		Clock pulse input/output pin for UART1. This function is enabled when UART1 enables the clock output.
24	P45	G	General I/O port. This function is enabled when UART1 disables the serial data output.
	SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output.

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No.	Pin name	Circuit type	Function
25	P46	G	General I/O port. This function is enabled when the Serial IO disables the serial data output.
	SOT2		Serial data output pin for the Serial IO. This function is enabled when the Serial IO enables the serial data output.
26	P47	G	General I/O port. This function is enabled when the Serial IO disables the clock output.
	SCK2		Clock pulse input/output pin for the Serial IO. This function is enabled when the Serial IO enables the clock output.
28	P50	D	General I/O port. This function is always enabled.
	SIN2		Serial data input pin for the Serial IO. While the Serial IO is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
29 to 32	P51 to P54	D	General I/O port. This function is always enabled.
	INT4 to INT7		External interrupt request input pins for INT4 to INT7. While external interrupt is allowed, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
33	P55	D	General I/O port. This function is always enabled.
	ADTG		Trigger input pin for the A/D converter. While the A/D converter is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
38 to 41	P60 to P63	E	General I/O port. This function is enabled when the analog input enable register specifies a port.
	AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies AD.
43 to 46	P64 to P67	E	General I/O port. The function is enabled when the analog input enable register specifies a port.
	AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies AD.
47	P56	D	General I/O port. This function is always enabled.
	TIN0		Event input pin for the 16-bit reload timers 0. While the 16-bit reload timer is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
48	P57	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
	TOT0		Output pin for the 16-bit reload timers 0. This function is enabled when the 16-bit reload timers 0 enables the output.

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No.	Pin name	Circuit type	Function
53 to 58	P70 to P75	D	General I/O ports. This function is always enabled.
	IN0 to IN5		Data sample input pins for input captures ICU0 to ICU5. While the ICU is for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
59 to 60	P76 to P77	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
	OUT2 to OUT3		Waveform output pins for output compares OCU2 and OCU3. This function is enabled when the OCU enables the waveform output.
	IN6 to IN7		Data sample input pin for input captures ICU6 and ICU7. While the ICU is for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
61 to 64	P80 to P83	D	General I/O ports. This function is enabled when 8/16-bit PPG disables the waveform output.
	PPG0 to PPG3		Output pins for 8/16-bit PPGs. This function is enabled when 8/16-bit PPG enables the waveform output.
65 to 66	P84 to P85	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
	OUT0 to OUT1		Waveform output pins for output compares OCU0 and OCU1. This function is enabled when the OCU enables the waveform output.
67	P86	D	General I/O port. This function is always enabled.
	TIN1		Event input pin for the 16-bit reload timers 1. While the 16-bit reload timer is operating as an input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
68	P87	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
	TOT1		Output pin for the 16-bit reload timers 1 This function is enabled when the 16-bit reload timers 1 enables the output.
69 to 72	P90 to P93	D	General I/O port. This function is always enabled.
	INT0 to INT3		External interrupt request input pins for INT0 to INT3. While external interrupt is allowed, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
73	P94	D	General I/O port. This function is enabled when CAN0 disables the output.
	TX0		TX Output pin for CAN0. This function is enabled when CAN0 enables the output.
74	P95	D	General I/O port. This function is always enabled.
	RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.

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No.	Pin name	Circuit type	Function
75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
	TX1		TX Output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540 series).
76	P97	D	General I/O port. This function is always enabled.
	RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540 series).
78	PA0	D	General I/O port. This function is always enabled.
34	AV _{cc}	Power supply	Power supply for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV _{cc} is applied to V _{cc} .
37	AV _{ss}	Power supply	Power supply for the A/D Converter.
35	AVRH	Power supply	External reference voltage input for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV _{cc} .
36	AVRL	Power supply	External reference voltage input for the A/D Converter.
49 50	MD0 MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V _{cc} or V _{ss} .
51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V _{cc} or V _{ss} .
27	C		This is the power supply stabilization capacitor pin. It should be connected externally to an 0.1 μ F ceramic capacitor.
23, 84	V _{cc}	Power supply	Input pin for power supply (5.0 V) .
11, 42, 81	V _{ss}	Power supply	Input pin for power supply (0.0 V) .

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■ I/O CIRCUIT TYPE

Circuit type	Diagram	Remarks
A	Diagram A shows a 2-input CMOS NAND gate with inputs X1 and X0. The output of the NAND gate is connected to an inverter, which is then connected back to input X1, forming an oscillation feedback loop. A standby control signal is connected to the gate's enable pin.	Oscillation feedback resistor: 1 MΩ approx.
B	Diagram B shows a hysteresis input circuit. A pull-up resistor R connects the input to Vcc. The input is also connected to a resistor R, which is then connected to the input of a hysteresis comparator (HYS).	Hysteresis input with pull-up Resistor: 50 kΩ approx.
C	Diagram C shows a hysteresis input circuit. The input is connected to a resistor R, which is then connected to the input of a hysteresis comparator (HYS).	Hysteresis input
D	Diagram D shows a CMOS level output circuit. The input is connected to the gate of a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The source of the P-ch MOSFET is connected to Vcc, and the source of the N-ch MOSFET is connected to ground. The drain of the P-ch MOSFET is connected to the drain of the N-ch MOSFET, which is also connected to a resistor R and the input of a hysteresis comparator (HYS).	- CMOS level output - Hysteresis input

Circuit type	Diagram	Remarks
E		• CMOS level output • Hysteresis input • Analog input
F		• Hysteresis input • Pull-down Resistor: 50 kΩ approx. (except FLASH devices)
G		• CMOS level output • Hysteresis input • TTL input (FLASH devices only)

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Circuit type	Diagram	Remarks
H		• CMOS level output • Hysteresis input • Programmable pullup resistor: 50 kΩ approx.
I		• CMOS level output • Hysteresis input • TTL level input (FLASH devices only) • Programmable pullup resistor: 50 kΩ approx.

■ HANDLING DEVICES

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} .
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, care must also be taken in not allowing the analog power-supply voltage (AV_{CC} , AV_{RH} , DV_{CC}) to exceed the digital power-supply voltage.

(2) Handling unused input pins

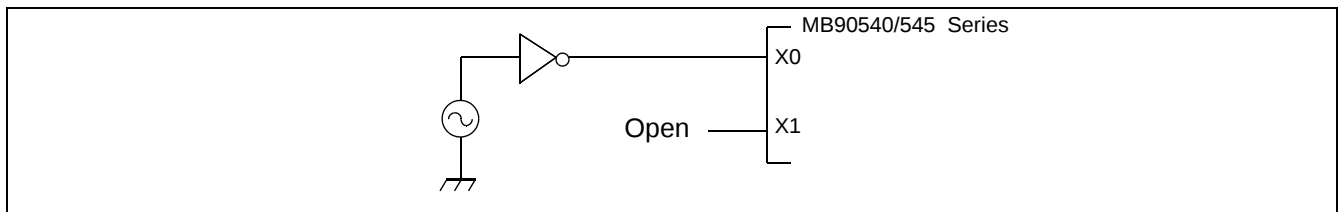
Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 k Ω .

Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.

Below is a diagram of how to use external clock.



(4) Not using subclock mode

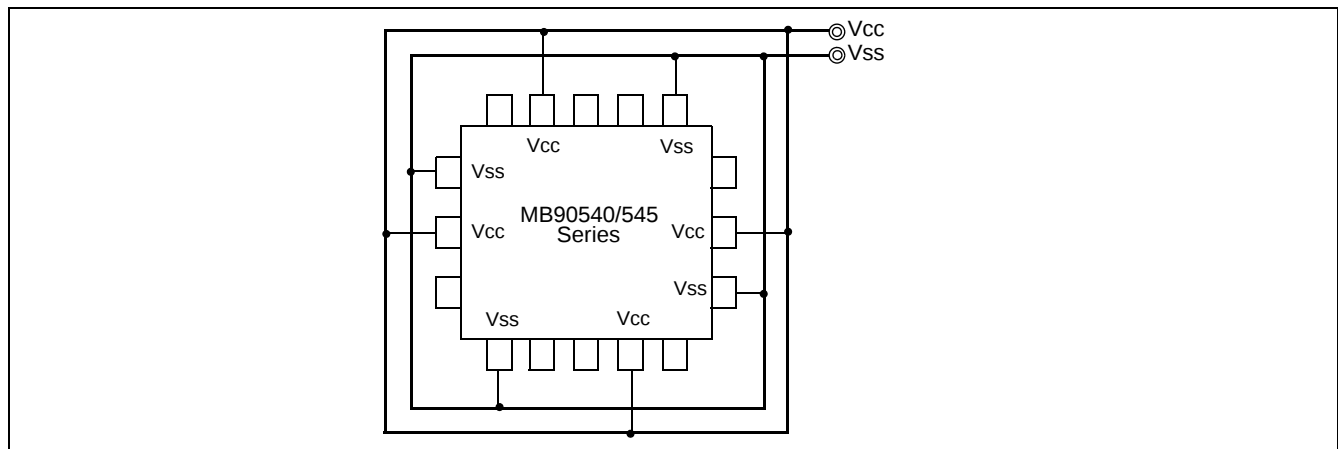
Oscillations must be connected to the X0A and X1A, even when a subclock is not used.

(5) Power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via the lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between V_{CC} and V_{SS} pins near the device.



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(6) Pull-up/down resistors

The MB90540/545 Series does not support internal pull-up/down resistors (except Port0 - Port3:pull-up resistors). Use external components where needed.

(7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a grand area for stabilizing the operation.

(8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , $AVRH$, $AVRL$) and analog inputs ($AN0$ to $AN7$) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed $AVRH$ or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

(9) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

(10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

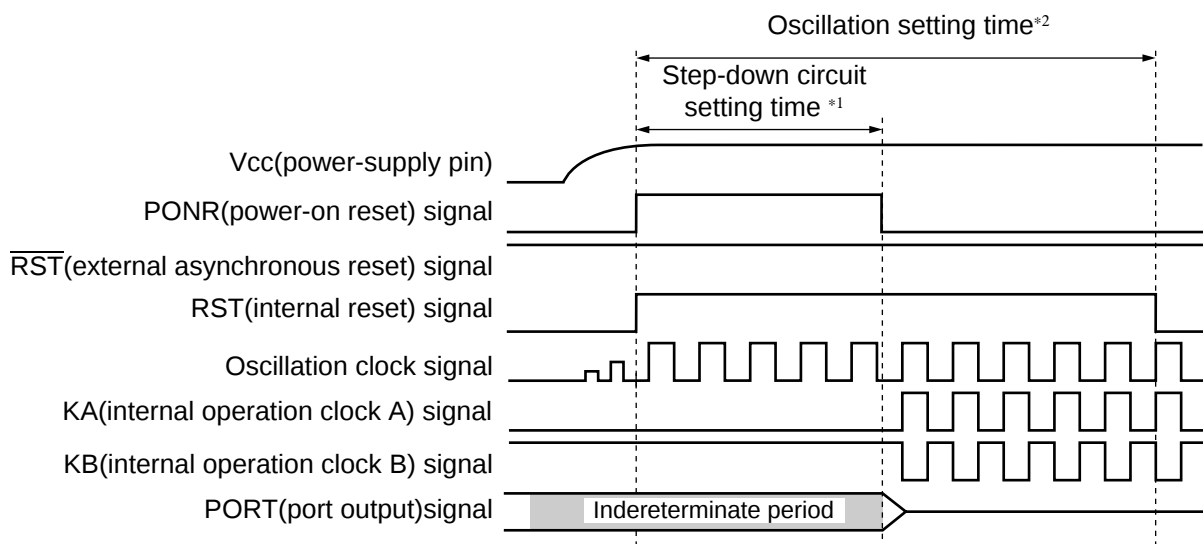
(11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V).

(12) Indeterminate outputs from ports 0 and 1

The outputs from 0 and 1 become indeterminate during a power-on reset after the power is turned on. Pay attention to the port output timing shown as follows.

• Timing chart of indeterminate outputs from ports 0 and 1



* : 1: Step-down circuit setting time : 2^{17} /oscillation clock frequency (oscillation clock frequency of 16 MHz: 8.19 ms)

* : 2: Oscillation setting time: 2^{18} /oscillation clock frequency (oscillation clock frequency of 16 MHz: 16.38 ms)

(13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(14) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00h”.

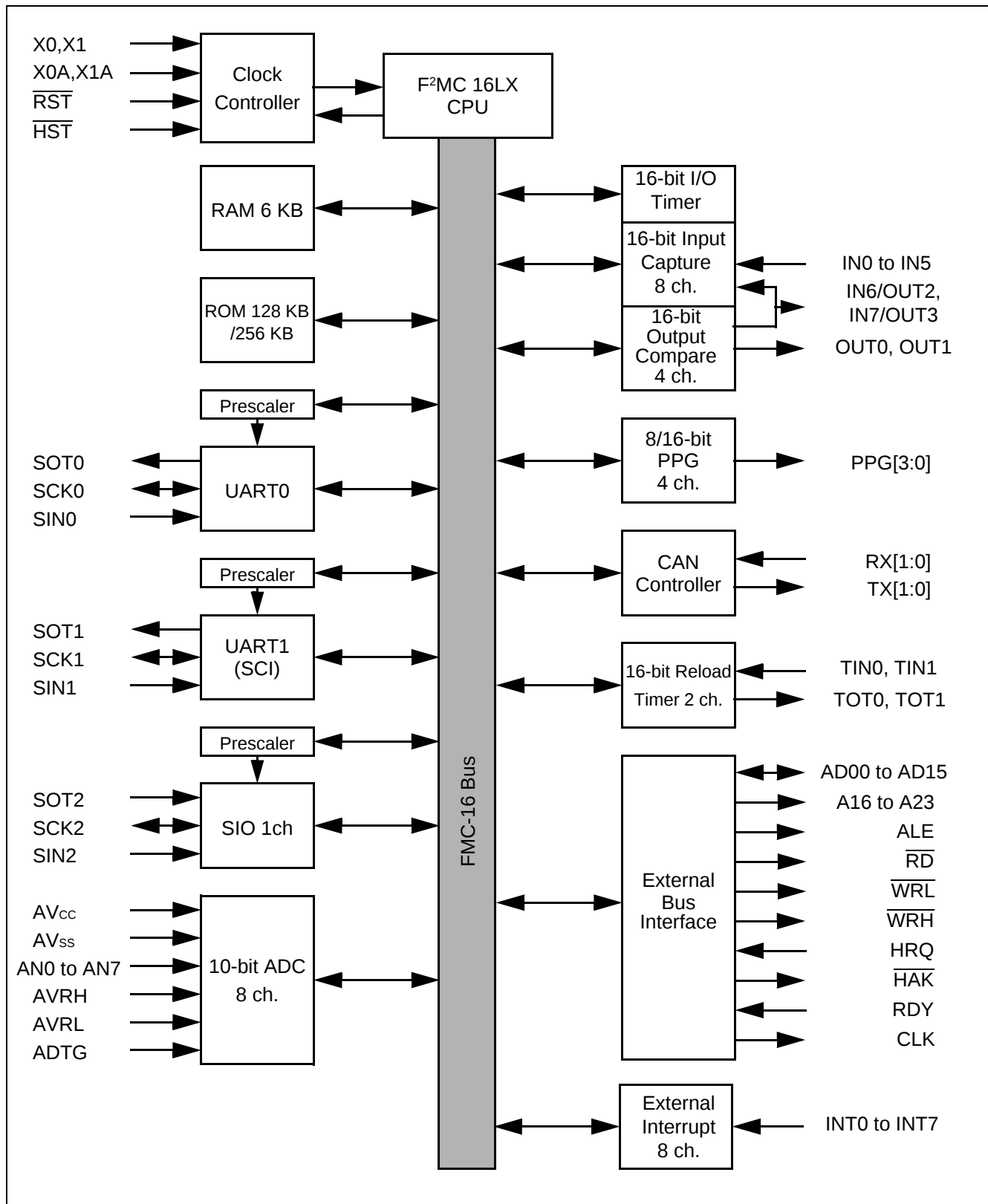
If the values of the corresponding bank registers (DTB,ADB,USB,SSB) are set to other than “00h”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(15) Using REALOS

Extended intelligent I/O service (EI²OS) can not be used, while REALOS is used.

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■ BLOCK DIAGRAM



■ MEMORY SPACE

The memory space of the MB90540/545 Series is shown below.

MB90V540		MB90F543		MB90F549	
FFFFFF _H	ROM (FF bank)	FFFFFF _H	ROM (FF bank)	FFFFFF _H	ROM (FF bank)
FF0000 _H		FF0000 _H		FF0000 _H	
FEFFFF _H	ROM (FE bank)	FEFFFF _H	ROM (FE bank)	FEFFFF _H	ROM (FE bank)
FE0000 _H		FE0000 _H		FE0000 _H	
FDFFFF _H	ROM (FD bank)	External		FDFFFF _H	ROM (FD bank)
FD0000 _H				FD0000 _H	
FCFFFF _H	ROM (FC bank)			FCFFFF _H	ROM (FC bank)
FC0000 _H				FC0000 _H	
	External				External
00FFFF _H	ROM (Image of FF bank)	00FFFF _H	ROM (Image of FF bank)	00FFFF _H	ROM (Image of FF bank)
004000 _H		004000 _H		004000 _H	
003FFF _H	Peripheral	003FFF _H	Peripheral	003FFF _H	Peripheral
003900 _H		003900 _H		003900 _H	
	External	002000 _H	External	002000 _H	External
0020FF _H					
001FF5 _H	ROM correction	0018FF _H	RAM 6K	0018FF _H	RAM 6K
001FF0 _H					
	RAM 8K				
000100 _H		000100 _H		000100 _H	
	External		External		External
0000BF _H	Peripheral	0000BF _H	Peripheral	0000BF _H	Peripheral
000000 _H		000000 _H		000000 _H	

The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the “far” specification in the pointer declaration.

For example, an attempt to access 00C000_H accesses the value at FFC000_H in ROM. The ROM area in bank FF exceeds 48 Kbytes, and its entire image cannot be shown in bank 00. The image between FF4000_H and FFFFFFF_H is visible in bank 00, while the image between FF0000_H and FF3FFF_H is visible only in bank FF.

MB90540/545 Series

■ I/O MAP

Address	Register	Abbreviation	Access	Peripheral	Initial value
00 _H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX _B
01 _H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX _B
02 _H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX _B
03 _H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX _B
04 _H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX _B
05 _H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX _B
06 _H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX _B
07 _H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX _B
08 _H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX _B
09 _H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX _B
0A _H	Port A data register	PDRA	R/W	Port A	_____X _B
0B _H to 0F _H	Reserved				
10 _H	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0 _B
11 _H	Port 1 direction register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0 _B
12 _H	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0 _B
13 _H	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0 _B
14 _H	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0 _B
15 _H	Port 5 direction register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0 _B
16 _H	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0 _B
17 _H	Port 7 direction register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0 _B
18 _H	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0 _B
19 _H	Port 9 direction register	DDR9	R/W	Port 9	0 0 0 0 0 0 0 0 _B
1A _H	Port A direction register	DDRA	R/W	Port A	_____0 _B
1B _H	Analog Input Enable	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1 _B
1C _H	Port 0 Pullup control register	PUCR0	R/W	Port 0	0 0 0 0 0 0 0 0 _B
1D _H	Port 1 Pullup control register	PUCR1	R/W	Port 1	0 0 0 0 0 0 0 0 _B
1E _H	Port 2 Pullup control register	PUCR2	R/W	Port 2	0 0 0 0 0 0 0 0 _B
1F _H	Port 3 Pullup control register	PUCR3	R/W	Port 3	0 0 0 0 0 0 0 0 _B
20 _H	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0 _B
21 _H	Serial Status Register 0	USR0	R/W		0 0 0 1 0 0 0 0 _B
22 _H	Serial Input/Output data register 0	UIDR0/ UODR0	R/W		XXXXXXXX _B
23 _H	Rate and data register 0	URD0	R/W		0 0 0 0 0 0 0 X _B

(Continued)

MB90540/545 Series

Address	Register	Abbreviation	Access	Peripheral	Initial value
24 _H	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0 _B
25 _H	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0 _B
26 _H	Serial input/output data register 1	SIDR1/ SODR1	R/W		XXXXXXXX _B
27 _H	Serial status register 1	SSR1	R/W		0 0 0 0 1 _ 0 0 _B
28 _H	UART1 prescaler control register	U1CDCR	R/W		0 _ _ 1 1 1 1 _B
29 _H	Edge selector	SES1	R/W		_ _ _ _ _ 0 _B
2A _H	Reserved				
2B _H	Serial IO prescaler	SCDCR	R/W	Serial IO	0 _ _ 1 1 1 1 _B
2C _H	Serial mode control register	SMCS	R/W		_ _ _ _ 0 0 0 0 _B
2D _H	Serial mode control register	SMCS	R/W		0 0 0 0 0 0 1 0 _B
2E _H	Serial data register	SDR	R/W		XXXXXXXX _B
2F _H	Edge selector	SES2	R/W		_ _ _ _ _ 0 _B
30 _H	External interrupt enable register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0 _B
31 _H	External interrupt request register	EIRR	R/W		XXXXXXXX _B
32 _H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 _B
33 _H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 _B
34 _H	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0 _B
35 _H	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0 _B
36 _H	A/D data register 0	ADCR0	R		XXXXXXXX _B
37 _H	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XX _B
38 _H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1 _B
39 _H	PPG1 operation mode control register	PPGC1	R/W		0 _ 0 0 0 0 0 1 _B
3A _H	PPG0 and PPG1 clock select register	PPG01	R/W		0 0 0 0 0 0 _ _ _B
3B _H	Reserved				
3C _H	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _ 1 _B
3D _H	PPG3 operation mode control register	PPGC3	R/W		0 _ 0 0 0 0 0 1 _B
3E _H	PPG2 and PPG3 Clock Select Register	PPG23	R/W		0 0 0 0 0 0 _ _ _B
3F _H	Reserved				
40 _H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1 _B
41 _H	PPG5 operation mode control register	PPGC5	R/W		0 _ 0 0 0 0 0 1 _B
42 _H	PPG4 and PPG5 clock select register	PPG45	R/W		0 0 0 0 0 0 _ _ _B
43 _H	Reserved				
44 _H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1 _B
45 _H	PPG7 operation mode control register	PPGC7	R/W		0 _ 0 0 0 0 0 1 _B
46 _H	PPG6 and PPG7 output pin control register	PPG67	R/W		0 0 0 0 0 0 _ _ _B

(Continued)

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Address	Register	Abbreviation	Access	Peripheral	Initial value
47 _H to 4B _H	Reserved				
4C _H	Input capture control status register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0 _B
4D _H	Input capture control status register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0 _B
4E _H	Input capture control status register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0 _B
4F _H	Input capture control status register 6/7	ICS67	R/W	Input Capture 6/7	0 0 0 0 0 0 0 0 _B
50 _H	Timer control status register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0 _B
51 _H	Timer control status register 0	TMCSR0	R/W		__ __ __ 0 0 0 0 _B
52 _H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXX _B
53 _H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXX _B
54 _H	Timer control status register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0 _B
55 _H	Timer control status register 1	TMCSR1	R/W		__ __ __ 0 0 0 0 _B
56 _H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXX _B
57 _H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXX _B
58 _H	Output compare control status register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 __ __ 0 0 _B
59 _H	Output compare control status register 1	OCS1	R/W		__ __ 0 0 0 0 0 0 _B
5A _H	Output compare control status register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 __ __ 0 0 _B
5B _H	Output compare control status register 3	OCS3	R/W		__ __ 0 0 0 0 0 0 _B
5C _H to 6B _H	Reserved				
6C _H	Timer Data register	TCDT	R/W	I/O Timer	0 0 0 0 0 0 0 0 _B
6D _H	Timer Data register	TCDT	R/W		0 0 0 0 0 0 0 0 _B
6E _H	Timer Control register	TCCS	R/W		0 0 0 0 0 0 0 0 _B
6F _H	ROM mirror register	ROMM	R/W	ROM Mirror	__ __ __ __ __ 1 _B
70 _H to 7F _H	Reserved for CAN 0 Interface. Refer to “CAN Controller Hardware Manual”				
80 _H to 8F _H	Reserved for CAN 1 Interface. Refer to “CAN Controller Hardware Manual”				
90 _H to 9D _H	Reserved				
9E _H	ROM correction control status register	PACSR	R/W	ROM Correction	0 0 0 0 0 0 0 0 _B
9F _H	Delayed interrupt/release register	DIRR	R/W	Delayed Interrupt	__ __ __ __ __ 0 _B
A0 _H	Low-power mode register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0 _B
A1 _H	Clock selector register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0 _B
A2 _H to A4 _H	Reserved				

(Continued)

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(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
A5 _H	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0 _B
A6 _H	External address output control register	HACR	W		0 0 0 0 0 0 0 0 _B
A7 _H	Bus control signal select register	ECSR	W		0 0 0 0 0 0 0 _ _B
A8 _H	Watchdog control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1 _B
A9 _H	Time Base Timer Control	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0 _B
AA _H	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0 _B
AB _H to AD _H	Reserved				
AE _H	Flash control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 _ _ 0 _B
AF _H	Reserved				
B0 _H	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1 _B
B1 _H	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1 _B
B2 _H	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1 _B
B3 _H	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1 _B
B4 _H	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1 _B
B5 _H	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1 _B
B6 _H	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1 _B
B7 _H	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1 _B
B8 _H	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1 _B
B9 _H	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1 _B
BA _H	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1 _B
BB _H	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1 _B
BC _H	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1 _B
BD _H	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1 _B
BE _H	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1 _B
BF _H	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1 _B
CO _H to FF _H	External				

Address	Register	Abbreviation	Access	Peripheral	Initial value
1FF0 _H	ROM Correction Address 0	PADR0	R/W	ROM correction	XXXXXXXX _B
1FF1 _H	ROM Correction Address 1	PADR0	R/W		XXXXXXXX _B
1FF2 _H	ROM Correction Address 2	PADR0	R/W		XXXXXXXX _B
1FF3 _H	ROM Correction Address 3	PADR1	R/W		XXXXXXXX _B
1FF4 _H	ROM Correction Address 4	PADR1	R/W		XXXXXXXX _B
1FF5 _H	ROM Correction Address 5	PADR1	R/W		XXXXXXXX _B

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Address	Register	Abbreviation	Access	Peripheral	Initial value
3900 _H	Reload L	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX _B
3901 _H	Reload H	PRLH0	R/W		XXXXXXXX _B
3902 _H	Reload L	PRLL1	R/W		XXXXXXXX _B
3903 _H	Reload H	PRLH1	R/W		XXXXXXXX _B
3904 _H	Reload L	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX _B
3905 _H	Reload H	PRLH2	R/W		XXXXXXXX _B
3906 _H	Reload L	PRLL3	R/W		XXXXXXXX _B
3907 _H	Reload H	PRLH3	R/W		XXXXXXXX _B
3908 _H	Reload L	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX _B
3909 _H	Reload H	PRLH4	R/W		XXXXXXXX _B
390A _H	Reload L	PRLL5	R/W		XXXXXXXX _B
390B _H	Reload H	PRLH5	R/W		XXXXXXXX _B
390C _H	Reload L	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX _B
390D _H	Reload H	PRLH6	R/W		XXXXXXXX _B
390E _H	Reload L	PRLL7	R/W		XXXXXXXX _B
390F _H	Reload H	PRLH7	R/W		XXXXXXXX _B
3910 _H to 3917 _H	Reserved				
3918 _H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
3919 _H	Input Capture 0	IPCP0	R		XXXXXXXX _B
391A _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
391B _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
391C _H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
391D _H	Input Capture 2	IPCP2	R		XXXXXXXX _B
391E _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
391F _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
3920 _H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
3921 _H	Input Capture 4	IPCP4	R		XXXXXXXX _B
3922 _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
3923 _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
3924 _H	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
3925 _H	Input Capture 6	IPCP6	R		XXXXXXXX _B
3926 _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
3927 _H	Input Capture 7	IPCP7	R		XXXXXXXX _B

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
3928 _H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
3929 _H	Output Compare 0	OCCP0	R/W		XXXXXXXX _B
392A _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
392B _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
392C _H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
392D _H	Output Compare 2	OCCP2	R/W		XXXXXXXX _B
392E _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
392F _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
3930 _H to 39FF _H	Reserved				
3A00 _H to 3AFF _H	Reserved for CAN 0 Interface. Refer to “CAN Controller Hardware Manual”				
3B00 _H to 3BFF _H	Reserved for CAN 0 Interface. Refer to “CAN Controller Hardware Manual”				
3C00 _H to 3CFF _H	Reserved for CAN 1 Interface. Refer to “CAN Controller Hardware Manual”				
3D00 _H to 3DFF _H	Reserved for CAN 1 Interface. Refer to “CAN Controller Hardware Manual”				
3E00 _H to 3FFF _H	Reserved				

Note Initial value of “_” represents unused bit, “X” represents unknown value.
 Addresses in the range 0000_H to 00FF_H, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in an “X” reading and any write access should not be performed.

MB90540/545 Series

■ CAN CONTROLLER

The MB90540 series contains two CAN controllers (CAN0 and CAN1), the MB90545 series contains only one (CAN0). The Evaluation Chip MB90V540 also has two CAN controllers.

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
 - 29-bit ID and 8-byte data
 - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as 1D acceptance mask
 - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbit/s to 1 Mbit/s (when input clock is at 16 MHz)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070 _H	000080 _H	Message buffer valid register	BVALR	R/W	00000000 00000000 _B
000071 _H	000081 _H				
000072 _H	000082 _H	Transmit request register	TREQR	R/W	00000000 00000000 _B
000073 _H	000083 _H				
000074 _H	000084 _H	Transmit cancel register	TCANR	W	00000000 00000000 _B
000075 _H	000085 _H				
000076 _H	000086 _H	Transmit complete register	TCR	R/W	00000000 00000000 _B
000077 _H	000087 _H				
000078 _H	000088 _H	Receive complete register	RCR	R/W	00000000 00000000 _B
000079 _H	000089 _H				
00007A _H	00008A _H	Remote request receiving register	RRTRR	R/W	00000000 00000000 _B
00007B _H	00008B _H				
00007C _H	00008C _H	Receive overrun register	ROVRR	R/W	00000000 00000000 _B
00007D _H	00008D _H				
00007E _H	00008E _H	Receive interrupt enable register	RIER	R/W	00000000 00000000 _B
00007F _H	00008F _H				

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003B00 _H	003D00 _H	Control status register	CSR	R/W, R	00---000 0----0-1 _B
003B01 _H	003D01 _H				
003B02 _H	003D02 _H	Last event indicator register	LEIR	R/W	----- 000-0000 _B
003B03 _H	003D03 _H				
003B04 _H	003D04 _H	Receive/transmit error counter	RTEC	R	00000000 00000000 _B
003B05 _H	003D05 _H				
003B06 _H	003D06 _H	Bit timing register	BTR	R/W	-1111111 11111111 _B
003B07 _H	003D07 _H				
003B08 _H	003D08 _H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXX _B
003B09 _H	003D09 _H				
003B0A _H	003D0A _H	Transmit RTR register	TRTRR	R/W	00000000 00000000 _B
003B0B _H	003D0B _H				
003B0C _H	003D0C _H	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXX _B
003B0D _H	003D0D _H				
003B0E _H	003D0E _H	Transmit interrupt enable register	TIER	R/W	00000000 00000000 _B
003B0F _H	003D0F _H				
003B10 _H	003D10 _H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXX _B
003B11 _H	003D11 _H				XXXXXXXX XXXXXXXX _B
003B12 _H	003D12 _H				
003B13 _H	003D13 _H				XXXXXXXX XXXXXXXX _B
003B14 _H	003D14 _H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXX _B
003B15 _H	003D15 _H				XXXXX--- XXXXXXXX _B
003B16 _H	003D16 _H				
003B17 _H	003D17 _H				XXXXX--- XXXXXXXX _B
003B18 _H	003D18 _H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXX _B
003B19 _H	003D19 _H				XXXXX--- XXXXXXXX _B
003B1A _H	003D1A _H				
003B1B _H	003D1B _H				XXXXX--- XXXXXXXX _B

MB90540/545 Series

List of Message Buffers (ID Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A00 _H to 003A1F _H	003C00 _H to 003C1F _H	General-purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
003A20 _H	003C20 _H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX _B
003A21 _H	003C21 _H				XXXXXX--- XXXXXXXX _B
003A22 _H	003C22 _H				
003A23 _H	003C23 _H				
003A24 _H	003C24 _H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXX _B
003A25 _H	003C25 _H				XXXXXX--- XXXXXXXX _B
003A26 _H	003C26 _H				
003A27 _H	003C27 _H				
003A28 _H	003C28 _H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXX _B
003A29 _H	003C29 _H				XXXXXX--- XXXXXXXX _B
003A2A _H	003C2A _H				
003A2B _H	003C2B _H				
003A2C _H	003C2C _H	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX _B
003A2D _H	003C2D _H				XXXXXX--- XXXXXXXX _B
003A2E _H	003C2E _H				
003A2F _H	003C2F _H				
003A30 _H	003C30 _H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX _B
003A31 _H	003C31 _H				XXXXXX--- XXXXXXXX _B
003A32 _H	003C32 _H				
003A33 _H	003C33 _H				
003A34 _H	003C34 _H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX _B
003A35 _H	003C35 _H				XXXXXX--- XXXXXXXX _B
003A36 _H	003C36 _H				
003A37 _H	003C37 _H				
003A38 _H	003C38 _H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX _B
003A39 _H	003C39 _H				XXXXXX--- XXXXXXXX _B
003A3A _H	003C3A _H				
003A3B _H	003C3B _H				

MB90540/545 Series

List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C _H	003C3C _H	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX _B
003A3D _H	003C3D _H				XXXXX--- XXXXXXXX _B
003A3E _H	003C3E _H				
003A3F _H	003C3F _H				
003A40 _H	003C40 _H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX _B
003A41 _H	003C41 _H				XXXXX--- XXXXXXXX _B
003A42 _H	003C42 _H				
003A43 _H	003C43 _H				
003A44 _H	003C44 _H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX _B
003A45 _H	003C45 _H				XXXXX--- XXXXXXXX _B
003A46 _H	003C46 _H				
003A47 _H	003C47 _H				
003A48 _H	003C48 _H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX _B
003A49 _H	003C49 _H				XXXXX--- XXXXXXXX _B
003A4A _H	003C4A _H				
003A4B _H	003C4B _H				
003A4C _H	003C4C _H	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX _B
003A4D _H	003C4D _H				XXXXX--- XXXXXXXX _B
003A4E _H	003C4E _H				
003A4F _H	003C4F _H				
003A50 _H	003C50 _H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX _B
003A51 _H	003C51 _H				XXXXX--- XXXXXXXX _B
003A52 _H	003C52 _H				
003A53 _H	003C53 _H				
003A54 _H	003C54 _H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX _B
003A55 _H	003C55 _H				XXXXX--- XXXXXXXX _B
003A56 _H	003C56 _H				
003A57 _H	003C57 _H				
003A58 _H	003C58 _H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX _B
003A59 _H	003C59 _H				XXXXX--- XXXXXXXX _B
003A5A _H	003C5A _H				
003A5B _H	003C5B _H				
003A5C _H	003C5C _H	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX _B
003A5D _H	003C5D _H				XXXXX--- XXXXXXXX _B
003A5E _H	003C5E _H				
003A5F _H	003C5F _H				

MB90540/545 Series

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60 _H	003C60 _H	DLC register 0	DLCR0	R/W	----XXXX _B
003A61 _H	003C61 _H				
003A62 _H	003C62 _H	DLC register 1	DLCR1	R/W	----XXXX _B
003A63 _H	003C63 _H				
003A64 _H	003C64 _H	DLC register 2	DLCR2	R/W	----XXXX _B
003A65 _H	003C65 _H				
003A66 _H	003C66 _H	DLC register 3	DLCR3	R/W	----XXXX _B
003A67 _H	003C67 _H				
003A68 _H	003C68 _H	DLC register 4	DLCR4	R/W	----XXXX _B
003A69 _H	003C69 _H				
003A6A _H	003C6A _H	DLC register 5	DLCR5	R/W	----XXXX _B
003A6B _H	003C6B _H				
003A6C _H	003C6C _H	DLC register 6	DLCR6	R/W	----XXXX _B
003A6D _H	003C6D _H				
003A6E _H	003C6E _H	DLC register 7	DLCR7	R/W	----XXXX _B
003A6F _H	003C6F _H				

MB90540/545 Series

List of Message Buffers (DLC Registers and Data Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A70 _H	003C70 _H	DLC register 8	DLCR8	R/W	----XXXX
003A71 _H	003C71 _H				
003A72 _H	003C72 _H	DLC register 9	DLCR9	R/W	----XXXX _B
003A73 _H	003C73 _H				
003A74 _H	003C74 _H	DLC register 10	DLCR10	R/W	----XXXX _B
003A75 _H	003C75 _H				
003A76 _H	003C76 _H	DLC register 11	DLCR11	R/W	----XXXX _B
003A77 _H	003C77 _H				
003A78 _H	003C78 _H	DLC register 12	DLCR12	R/W	----XXXX _B
003A79 _H	003C79 _H				
003A7A _H	003C7A _H	DLC register 13	DLCR13	R/W	----XXXX _B
003A7B _H	003C7B _H				
003A7C _H	003C7C _H	DLC register 14	DLCR14	R/W	----XXXX _B
003A7D _H	003C7D _H				
003A7E _H	003C7E _H	DLC register 15	DLCR15	R/W	----XXXX _B
003A7F _H	003C7F _H				
003A80 _H to 003A87 _H	003C80 _H to 003C87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B
003A88 _H to 003A8F _H	003C88 _H to 003C8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
003A90 _H to 003A97 _H	003C90 _H to 003C97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
003A98 _H to 003A9F _H	003C98 _H to 003C9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA0 _H to 003AA7 _H	003CA0 _H to 003CA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA8 _H to 003AAF _H	003CA8 _H to 003CAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB0 _H to 003AB7 _H	003CB0 _H to 003CB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B

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List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003AB8 _H to 003ABF _H	003CB8 _H to 003CBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC0 _H to 003AC7 _H	003CC0 _H to 003CC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC8 _H to 003ACF _H	003CC8 _H to 003CCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD0 _H to 003AD7 _H	003CD0 _H to 003CD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD8 _H to 003ADF _H	003CD8 _H to 003CDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE0 _H to 003AE7 _H	003CE0 _H to 003CE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE8 _H to 003AEF _H	003CE8 _H to 003CEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF0 _H to 003AF7 _H	003CF0 _H to 003CF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF8 _H to 003AFF _H	003CF8 _H to 003CFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

■ INTERRUPT MAP

Interrupt cause	EI ² OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC _H	—	—
INT9 instruction	N/A	#09	FFFFD8 _H	—	—
Exception	N/A	#10	FFFFD4 _H	—	—
CAN 0 RX	N/A	#11	FFFFD0 _H	ICR00	0000B0 _H
CAN 0 TX/NS	N/A	#12	FFFFCC _H		
CAN 1 RX	N/A	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS	N/A	#14	FFFFC4 _H		
External Interrupt INT0/INT1	*1	#15	FFFFC0 _H	ICR02	0000B2 _H
Time Base Timer	N/A	#16	FFFFBC _H		
16-bit Reload Timer 0	*1	#17	FFFFB8 _H	ICR03	0000B3 _H
8/10-bit A/D Converter	*1	#18	FFFFB4 _H		
I/O Timer	N/A	#19	FFFFB0 _H	ICR04	0000B4 _H
External Interrupt INT2/INT3	*1	#20	FFFFAC _H		
Serial I/O	*1	#21	FFFFA8 _H	ICR05	0000B5 _H
8/16-bit PPG 0/1	N/A	#22	FFFFA4 _H		
Input Capture 0	*1	#23	FFFFA0 _H	ICR06	0000B6 _H
External Interrupt INT4/INT5	*1	#24	FFFF9C _H		
Input Capture 1	*1	#25	FFFF98 _H	ICR07	0000B7 _H
8/16-bit PPG 2/3	N/A	#26	FFFF94 _H		
External Interrupt INT6/INT7	*1	#27	FFFF90 _H	ICR08	0000B8 _H
Watch Timer	N/A	#28	FFFF8C _H		
8/16-bit PPG 4/5	N/A	#29	FFFF88 _H	ICR09	0000B9 _H
Input Capture 2/3	*1	#30	FFFF84 _H		
8/16-bit PPG 6/7	N/A	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0	*1	#32	FFFF7C _H		
Output Compare 1	*1	#33	FFFF78 _H	ICR11	0000BB _H
Input Capture 4/5	*1	#34	FFFF74 _H		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70 _H	ICR12	0000BC _H
16-bit Reload Timer 1	*1	#36	FFFF6C _H		
UART 0 RX	*2	#37	FFFF68 _H	ICR13	0000BD _H
UART 0 TX	*1	#38	FFFF64 _H		
UART 1 RX	*2	#39	FFFF60 _H	ICR14	0000BE _H
UART 1 TX	*1	#40	FFFF5C _H		
Flash Memory	N/A	#41	FFFF58 _H	ICR15	0000BF _H
Delayed interrupt	N/A	#42	FFFF54 _H		

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*1: The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2: The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

N/A: The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

Note: • For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.

- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0V$)

Parameter	Symbol	Value		Units	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *1
	AV_{RH} , AV_{RL}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AV_{RH}/AV_{RL}$, $AV_{RH} \geq AV_{RL}$ *1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Clamp Current	I_{CLAMP}	-2.0	2.0	mA	
"L" level max. output current	I_{OL}	—	15	mA	*3
"L" level avg. output current	I_{OLAV}	—	4	mA	*4
"L" level max. overall output current	ΣI_{OL}	—	100	mA	
"L" level avg. overall output current	ΣI_{OLAV}	—	50	mA	*5
"H" level max. output current	I_{OH}	—	-15	mA	*3
"H" level avg. output current	I_{OHAV}	—	-4	mA	*4
"H" level max. overall output current	ΣI_{OH}	—	-100	mA	
"H" level avg. overall output current	ΣI_{OHAV}	—	-50	mA	*5
Power consumption	P_D	—	500	mW	MB90F543/F549
Operating temperature	T_A	-40	+85	°C	
Storage temperature	T_{STG}	-55	+150	°C	

*1: AV_{CC} , AV_{RH} and AV_{RL} should not exceed V_{CC} , and AV_{RL} should not exceed AV_{RH} .

*2: V_I and V_O should not exceed $V_{CC} + 0.3V$. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

*3: The maximum output current is a peak value for a corresponding pin.

*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

Note: Average output current = operating current $\times$ operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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2. Recommended Conditions

($V_{SS} = AV_{SS} = 0V$)

Parameter	Symbol	Value			Units	Remarks
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	
Smooth capacitor	C_S	0.022	0.1	1.0	μF	*
Operating temperature	T_A	-40		+85	$^{\circ}C$	

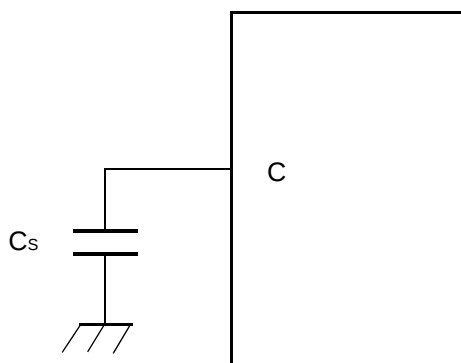
*: Use a ceramic capacitor or a capacitor of better AC characteristics. The V_{CC} Capacitor should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

• C Pin Connection Diagram



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3. DC Characteristics

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Units	Remarks
				Min.	Typ.	Max.		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHM}	MD input pin	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	—	$V_{CC} - 0.3$	—	$0.2 V_{CC}$	V	
	V_{ILM}	MD input pin	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
Output H voltage	V_{OH}	All output pins	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	V_{OL}	All output pins	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Input leak current	I_{IL}		$V_{CC} = 5.5\text{ V}$, $V_{SS} < V_I < V_{CC}$	-5	—	5	μA	
Power supply current*	I_{CC}	V_{CC}	$V_{CC} = 5.0\text{ V} \pm 10\%$, Internal frequency: 16 MHz, At normal operation	—	45	60	mA	MB90F543/F549
	I_{CCS}		$V_{CC} = 5.0\text{ V} \pm 10\%$, Internal frequency: 16 MHz, At sleep	—	13	22	mA	MB90F543/F549
	I_{CCL}		$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, At sub operation	—	0.2	1	mA	MB90F543/F549
	I_{CCLS}		$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, At sub sleep	—	10	50	μA	MB90F543/F549
	I_{CCT}		$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, At watch mode	—	10	50	μA	MB90F543/F549
	I_{CCH1}		$V_{CC} = 5.0\text{ V} \pm 10\%$, At stop, $T_A = 25\text{ }^{\circ}\text{C}$	—	5	20	μA	MB90F543/F549
	I_{CCH2}		$V_{CC} = 5.0\text{ V} \pm 10\%$, At hardware standby mode, $T_A = 25\text{ }^{\circ}\text{C}$	—	50	100	μA	MB90F543/F549
Input capacity	C_{IN}	Other than AV_{CC} , AV_{SS} , $AVRH$, $AVRL$, C , V_{CC} , V_{SS}	—	—	10	80	pF	

*: Current values are tentative. They are subject to change without notice according to improvements in the characteristics. The power supply current testing conditions are when using the external clock.

MB90540/545 Series

4. AC Characteristics

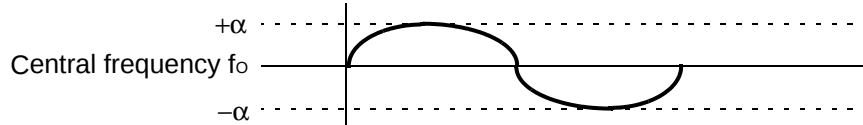
(1) Clock Timing

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

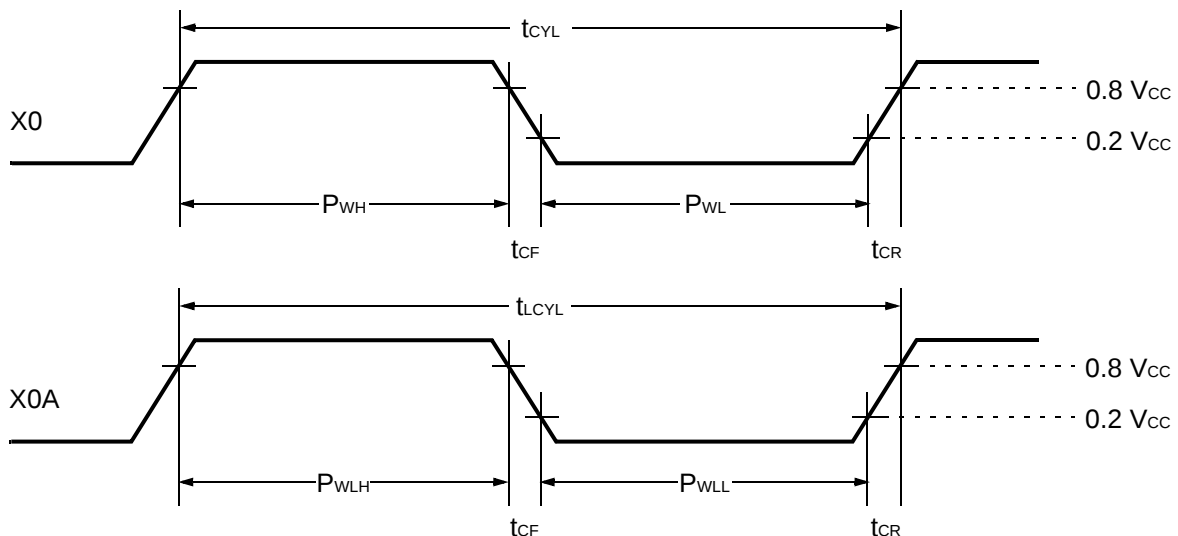
Parameter	Symbol	Pin	Value			Units	Remarks
			Min.	Typ.	Max.		
Oscillation frequency	f_c	X0, X1	3	—	16	MHz	
	f_{CL}	X0A, X1A	—	32.768	—	kHz	
Oscillation cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	μs	
Frequency deviation with PLL *	Δf	—	—	—	5	%	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	When using main clock
	f_{LCP}	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	When using main clock
	t_{LCP}	—	—	122.1	—	μs	When using sub-clock

* : Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.

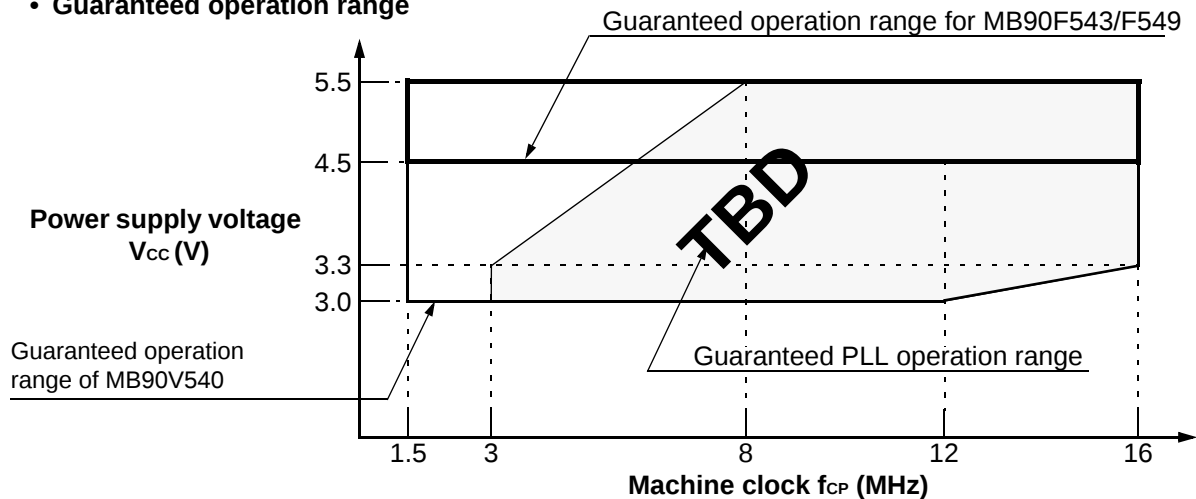
$$\Delta f = \frac{|\alpha|}{f_0} \times 100\%$$



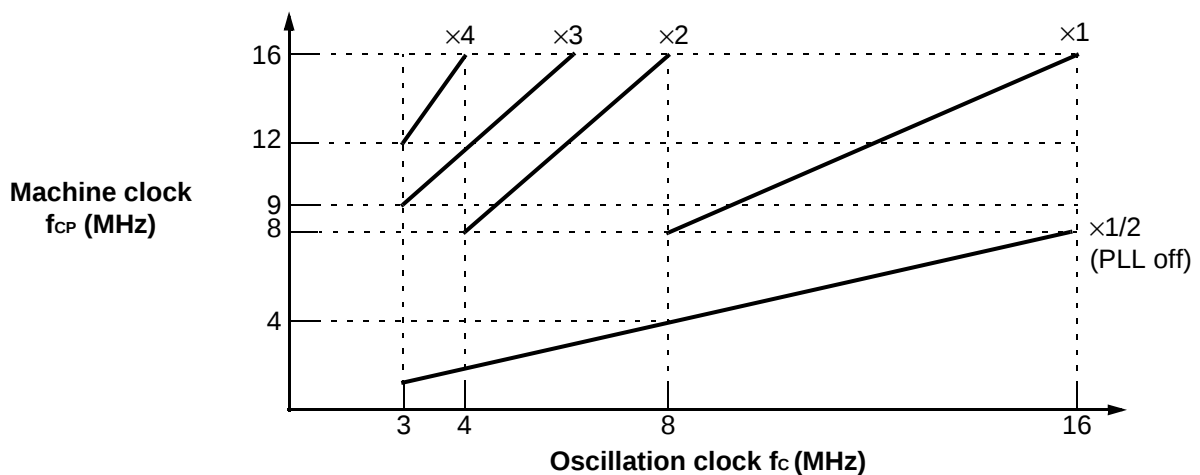
• Clock Timing



- Guaranteed operation range



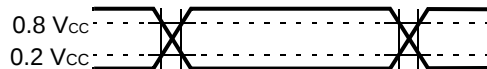
- Oscillation clock frequency and Machine clock frequency



AC characteristics are set to the measured reference voltage values below.

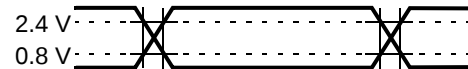
- Input signal waveform

Hysteresis Input Pin



- Output signal waveform

Output Pin

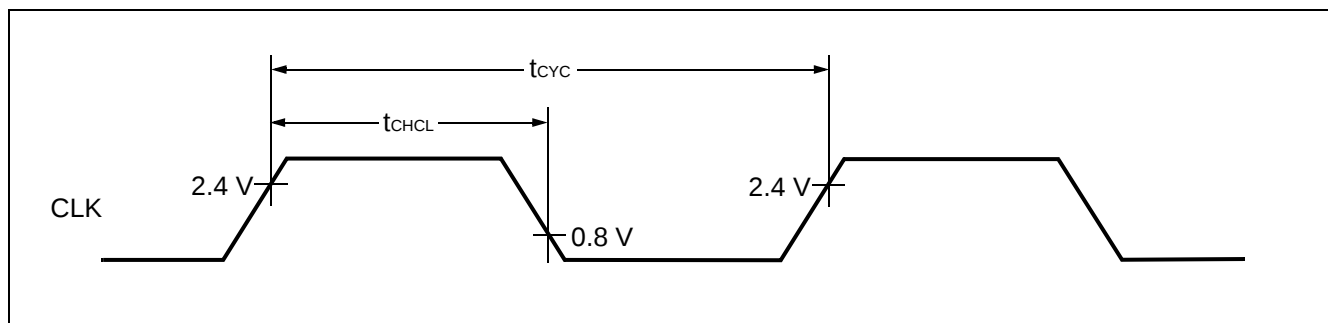


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(2) Clock Output Timing

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	$V_{CC} = 5 \text{ V} \pm 10\%$	62.5	—	ns	
CLK $\uparrow \Rightarrow$ CLK $\downarrow$	t_{CHCL}			20	—	ns	



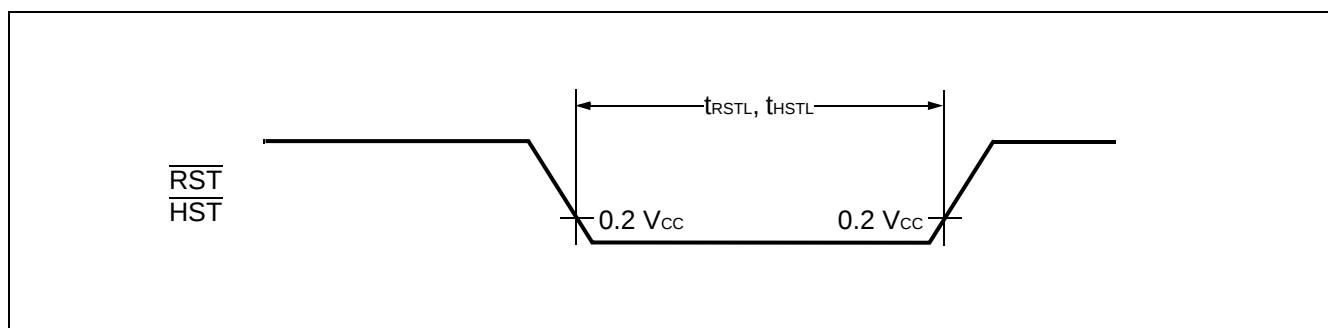
(3) Reset and Hardware Standby Input

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Value		Units	Remarks
			Min.	Max.		
Reset input time	t_{RSTL}	$\overline{\text{RST}}$	16 t_{CP}	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{\text{HST}}$	16 t_{CP}	—	ns	

" t_{cp} " represents one cycle time of the machine clock.

Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.

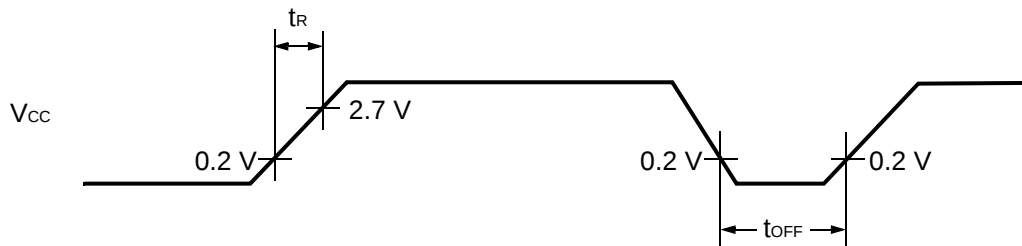


(4) Power On Reset

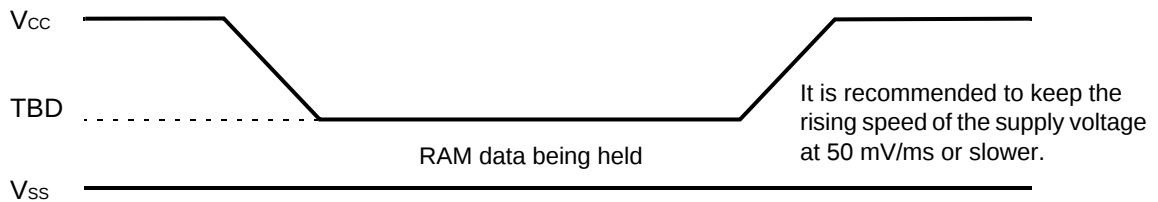
($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		50	—	ms	Due to repetitive operation

- Note
- V_{CC} must be kept lower than 0.2 V before power-on.
 - The above values are used for creating a power-on reset.
 - Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



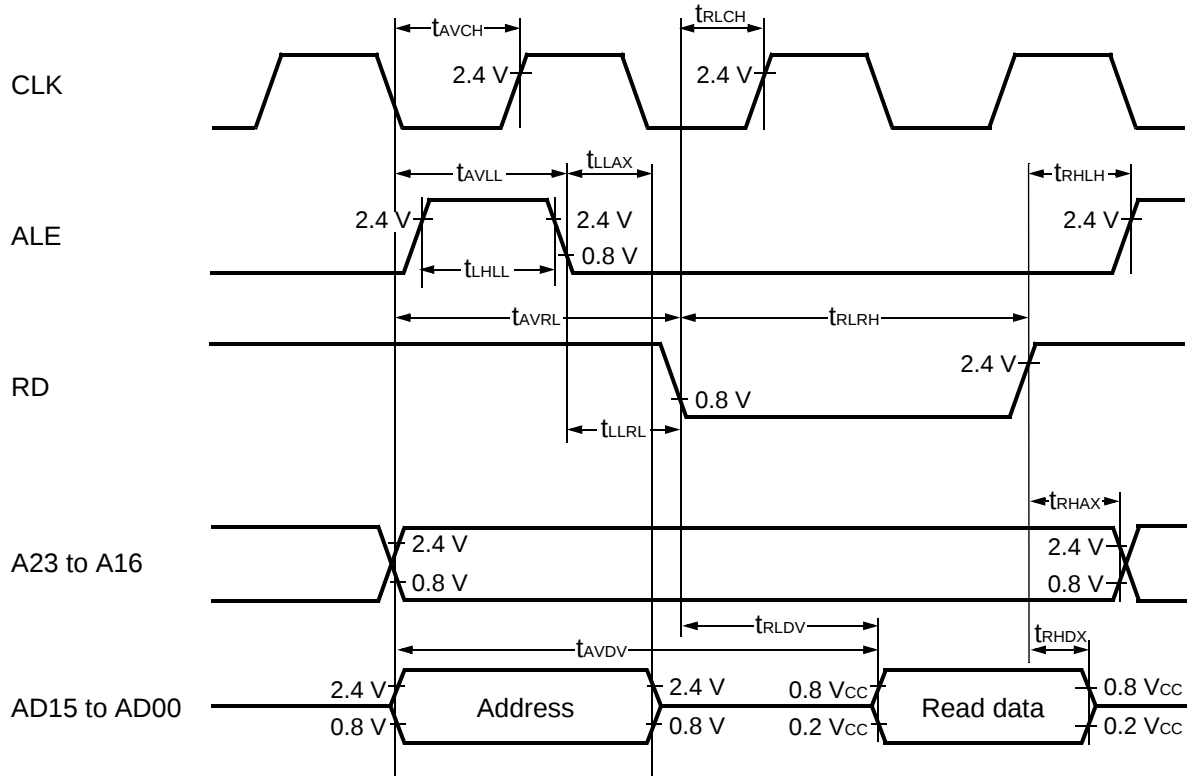
MB90540/545 Series

(5) Bus Timing (Read)

($V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 20$		ns	
Valid address $\Rightarrow$ ALE $\downarrow$ time	t_{AVLL}	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns	
ALE $\downarrow \Rightarrow$ Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns	
Valid address $\Rightarrow \overline{RD} \downarrow$ time	t_{AVRL}	A23 to A16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns	
Valid address $\Rightarrow$ Valid data input	t_{AVDV}	A23 to A16, AD15 to AD00		—	$5 t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$3 t_{CP}/2 - 20$	—	ns	
$\overline{RD} \downarrow \Rightarrow$ Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		—	$3 t_{CP}/2 - 60$	ns	
$\overline{RD} \uparrow \Rightarrow$ Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	—	ns	
$\overline{RD} \downarrow \Rightarrow$ ALE $\uparrow$ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD} \uparrow \Rightarrow$ Address valid time	t_{RHAX}	$\overline{RD}$, A23 to A16		$t_{CP}/2 - 10$	—	ns	
Valid address $\Rightarrow$ CLK $\uparrow$ time	t_{AVCH}	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 20$	—	ns	
$\overline{RD} \downarrow \Rightarrow$ CLK $\uparrow$ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 20$	—	ns	
ALE $\downarrow \Rightarrow \overline{RD} \downarrow$ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns	

• Bus Timing (Read)



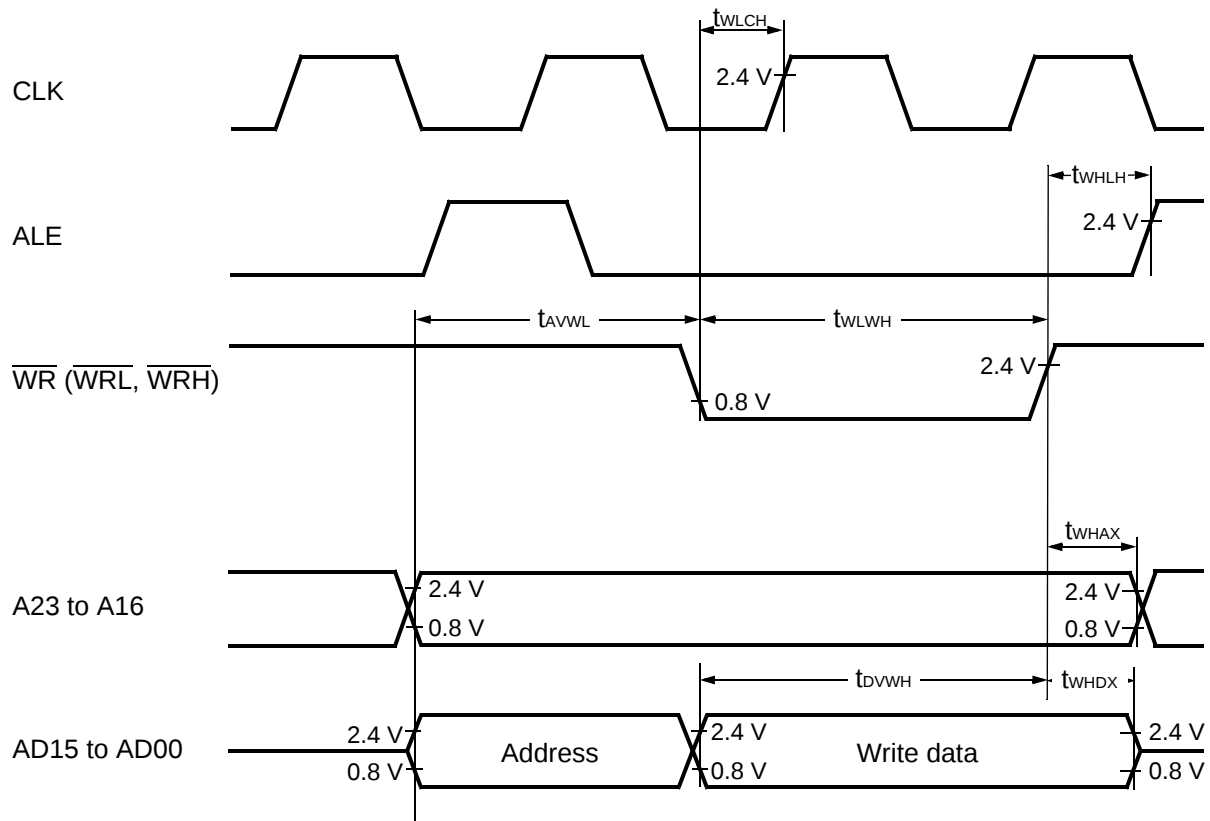
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(6) Bus Timing (Write)

($V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_A = -40^\circ \text{ C to } +85^\circ \text{ C}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Valid address $\Rightarrow \overline{\text{WR}} \downarrow$ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{\text{WR}}$	—	$t_{\text{CP}} - 15$	—	ns	
$\overline{\text{WR}}$ pulse width	t_{WLWH}	$\overline{\text{WR}}$		$3 t_{\text{CP}}/2 - 20$	—	ns	
Valid data output $\Rightarrow \overline{\text{WR}} \uparrow$ time	t_{DVWH}	AD15 to AD00, $\overline{\text{WR}}$		$3 t_{\text{CP}}/2 - 20$	—	ns	
$\overline{\text{WR}} \uparrow \Rightarrow$ Data hold time	t_{WHDX}	AD15 to AD00, $\overline{\text{WR}}$		20	—	ns	
$\overline{\text{WR}} \uparrow \Rightarrow$ Address valid time	t_{WHAX}	A23 to A16, $\overline{\text{WR}}$		$t_{\text{CP}}/2 - 10$	—	ns	
$\overline{\text{WR}} \uparrow \Rightarrow \text{ALE} \uparrow$ time	t_{WHLH}	$\overline{\text{WR}}$, ALE		$t_{\text{CP}}/2 - 15$	—	ns	
$\overline{\text{WR}} \downarrow \Rightarrow \text{CLK} \uparrow$ time	t_{WLCH}	$\overline{\text{WR}}$, CLK		$t_{\text{CP}}/2 - 20$	—	ns	

• Bus Timing (Write)



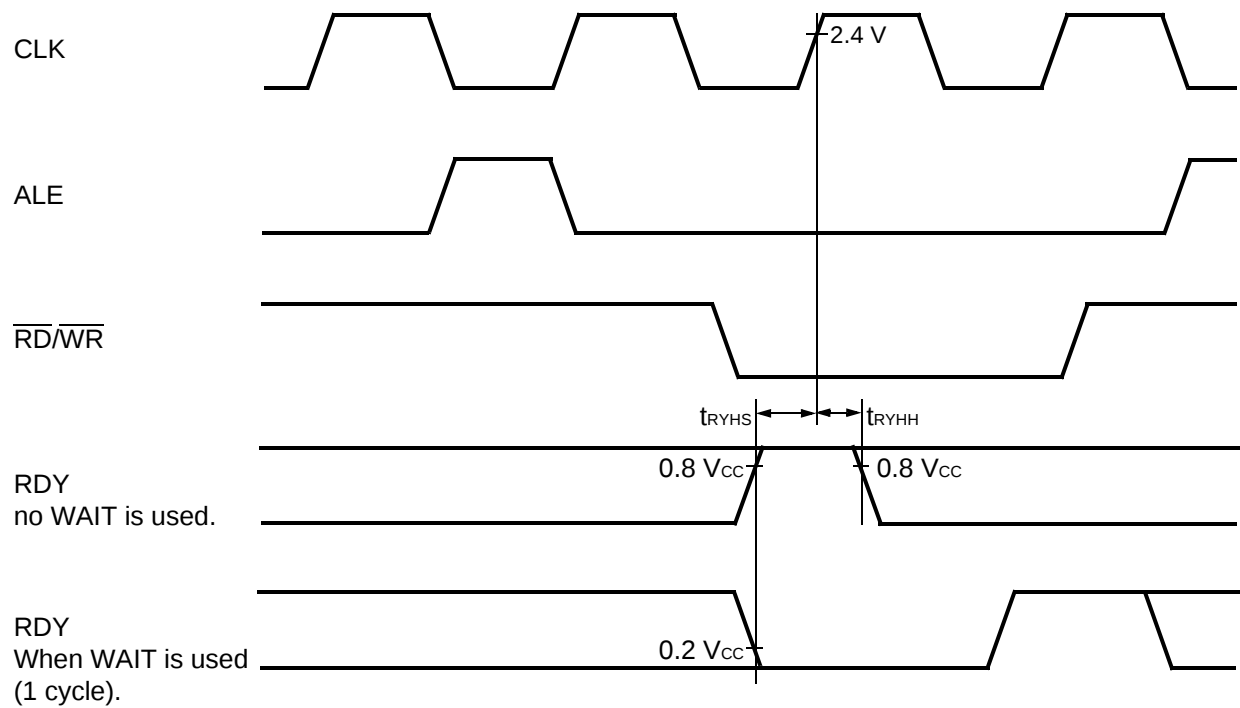
(7) Ready Input Timing

($V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note: If the RDY setup time is insufficient, use the auto-ready function.

• Ready Input Timing



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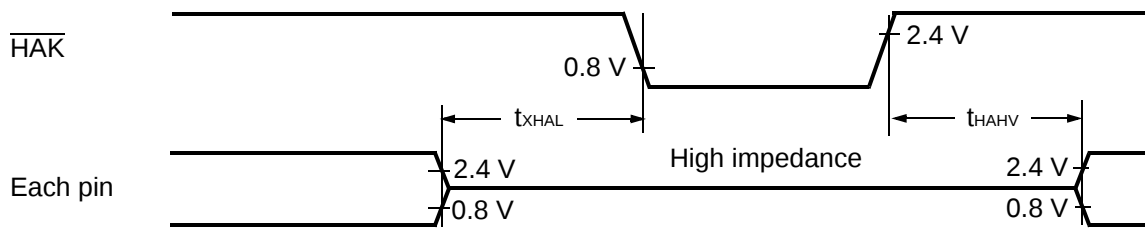
(8) Hold Timing

($V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Pin floating $\Rightarrow \overline{\text{HAK}} \downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	t_{CP}	ns	
$\overline{\text{HAK}} \uparrow$ time $\Rightarrow$ Pin valid time	t_{HAHV}	$\overline{\text{HAK}}$		t_{CP}	$2 t_{CP}$	ns	

Note: There is more than 1 cycle from the time $\overline{\text{HRQ}}$ is read to the time the $\overline{\text{HAK}}$ is changed.

• Hold Timing



(9) UART0/1, Serial I/O Timing

($V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

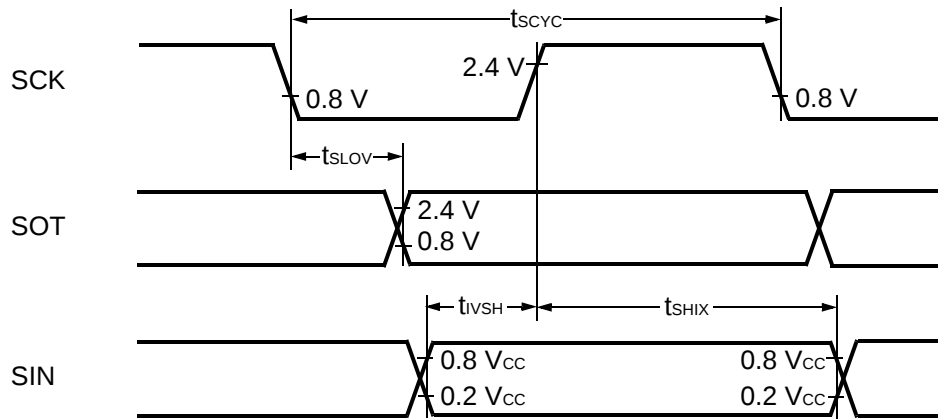
Parameter	Symbol	Pin Symbol	Condition	Value		Units	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are $C_L = 80 \text{ pF} + 1 \text{ TTL}$.	$8 t_{CP}$	—	ns	
SCK $\downarrow \Rightarrow$ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—80	80	ns	
Valid SIN $\Rightarrow$ SCK $\uparrow$	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK $\uparrow \Rightarrow$ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are $C_L = 80 \text{ pF} + 1 \text{ TTL}$.	$4 t_{CP}$	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK2		$4 t_{CP}$	—	ns	
SCK $\downarrow \Rightarrow$ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN $\Rightarrow$ SCK $\uparrow$	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK $\uparrow \Rightarrow$ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Note: 1.AC characteristic in CLK synchronized mode.

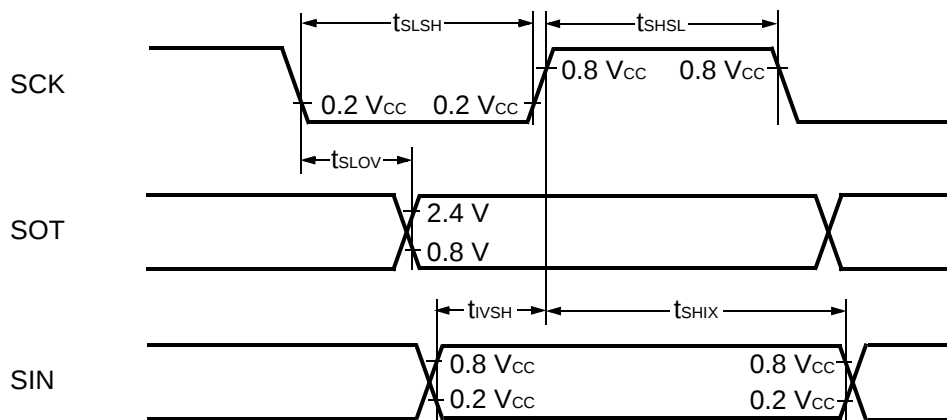
2. C_L is load capacity value of pins when testing.

3. t_{CP} is the machine cycle (Unit: ns).

• Internal Shift Clock Mode



• External Shift Clock Mode



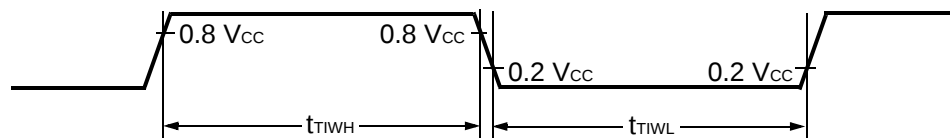
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(10) Timer Related Resource Input Timing

($V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	$4\ t_{CP}$	—	ns	
	t_{TIWL}	IN0 to IN7					

• Timer Input Timing

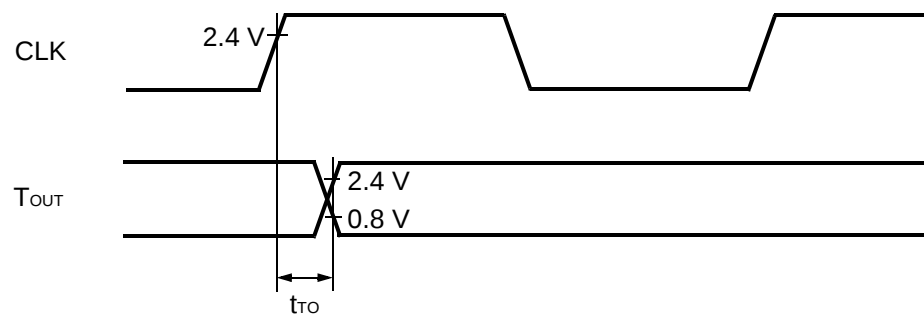


(11) Timer Related Resource Output Timing

($V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
CLK $\uparrow \Rightarrow$ T _{OUT} change time	t_{TO}	TOT0 to TOT1, PPG0 to PPG3	—	30	—	ns	

• Timer Output Timing

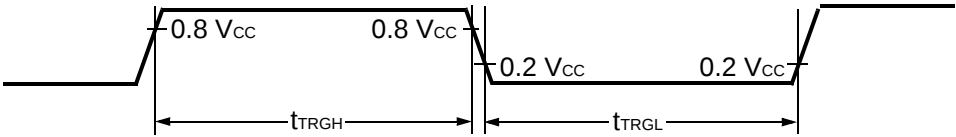


(12) Trigger Input Timing

($V_{CC} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_A = -40$ °C to $+85$ °C)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7, ADTG	—	$5 t_{CP}$	—	ns	

• Trigger Input Timing



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5. A/D Converter

($V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0\text{ V}$, $3.0\text{ V} \leq AVR_H - AVR_L$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Rated Value			Units	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—		10	bit	
Conversion error	—	—	—	—	± 5.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential nonlinearity error	—	—	—	—	± 1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN7	$AVR_L - 3.5$	$AVR_L + 0.5$	$AVR_L + 4.5$	mV	
Full scale reading voltage	V_{FST}	AN0 to AN7	$AVR_H - 6.5$	$AVR_H - 1.5$	$AVR_H + 1.5$	mV	
Conversion time	—	—	—	$352t_{CP}$	—	ns	
Sampling time	—	—	—	$64t_{CP}$	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	-10	—	10	μA	
Analog input voltage range	V_{AIN}	AN0 to AN7	AVR_L	—	AVR_H	V	
Reference voltage range	—	AVR_H	$AVR_L + 2.7$	—	AV_{CC}	V	
	—	AVR_L	0	—	$AVR_H - 2.7$	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage current	I_R	AVR_H	200	400	600	μA	
	I_{RH}	AVR_H	—	—	5	μA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

*: When not using an A/D converter, this is the current ($V_{CC} = AV_{CC} = AVR_H = 5.0\text{ V}$) when the CPU is stopped.

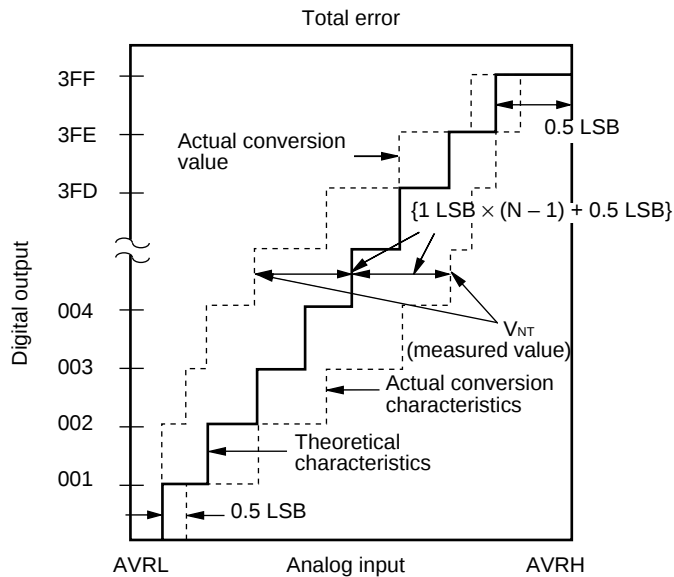
6. A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{AVRH - AVRL}{1024} \text{ [V]}$$

$$V_{OT} (\text{Theoretical value}) = AVRL + 0.5 \text{ LSB [V]}$$

$$V_{FST} (\text{Theoretical value}) = AVRH - 1.5 \text{ LSB [V]}$$

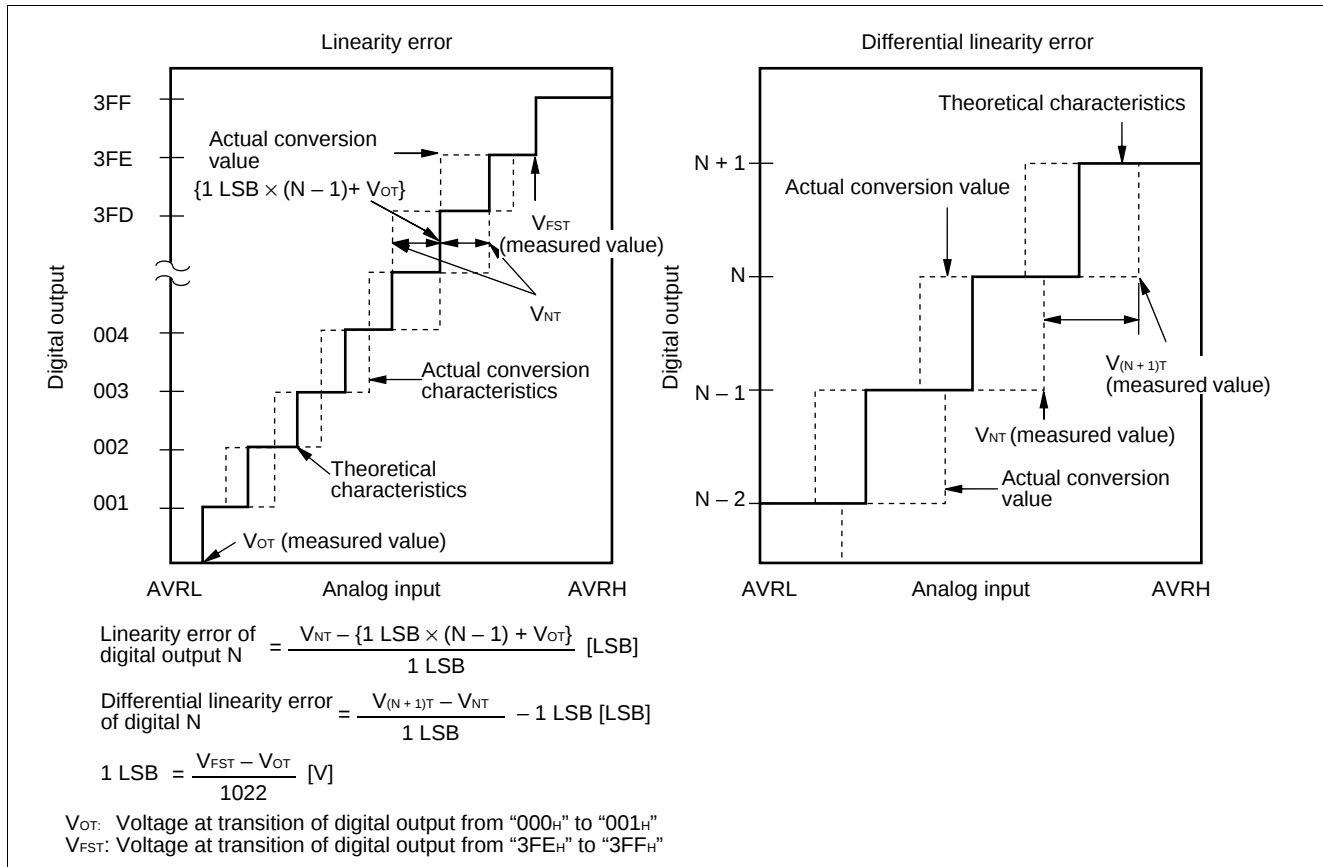
$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

V_{NT} : Voltage at a transition of digital output from $(N - 1)$ to N

(Continued)

MB90540/545 Series

(Continued)



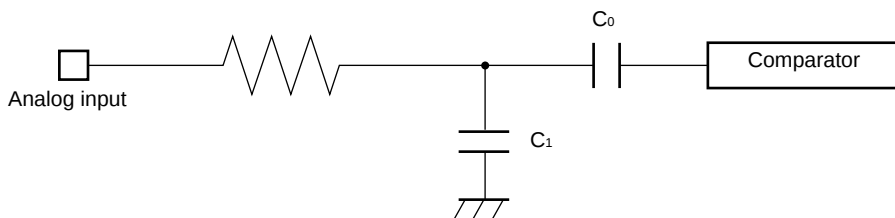
7. Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz).

• Equipment of analog input circuit model



Note: Listed values must be considered as standards.

• Error

The smaller the $|AVRH - AVRL|$, the greater the error would become relatively.

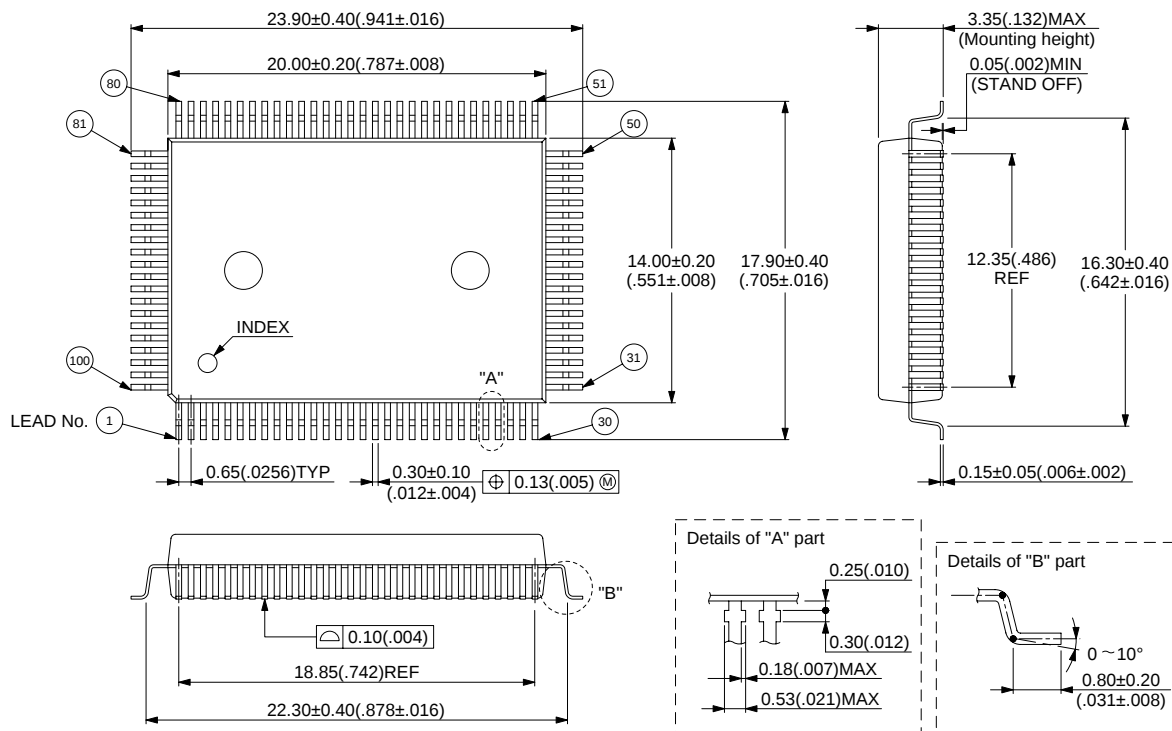
MB90540/545 Series

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F543PF MB90F549PF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V540CR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

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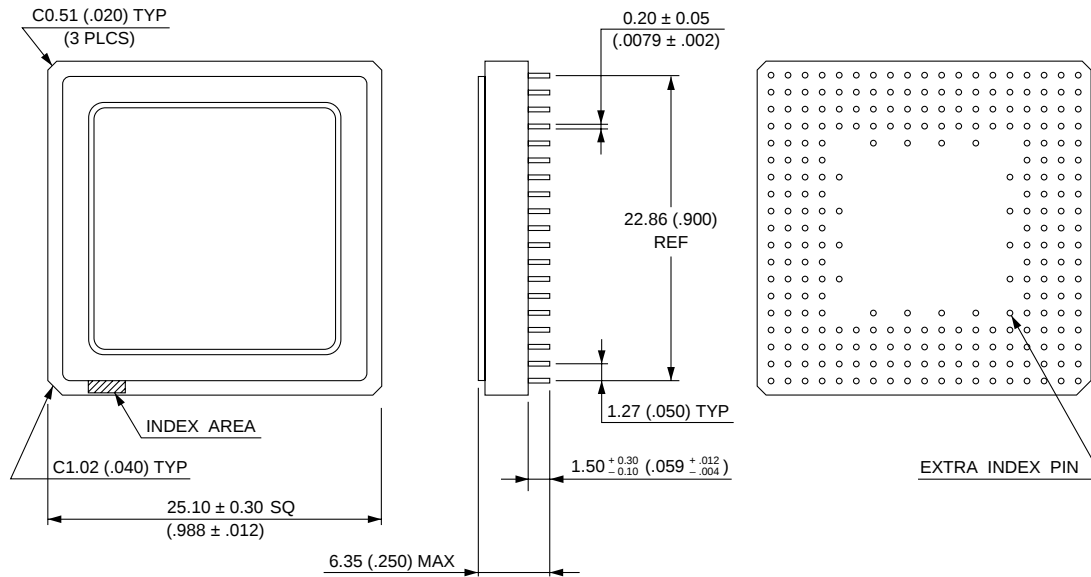
■ PACKAGE DIMENSIONS

100-pin Plastic QFP
(FPT-100P-M06)

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Dimensions in mm (inches)

250-pin Ceramic PGA (PGA-256C-A01)



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Dimensions in mm (inches)

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