I²C BUS Control 5-Input 2-Output AV Switch
Monolithic IC MM1495X

Outline

This IC is a 5-input, 2-output AV switch with I²C BUS control, developed for use in TV. This IC supports S2 and Cenelec standards.

Features

1. Serial control by I²C BUS.
2. 5 - inputs, 2 - outputs (2 of the 5 input lines can be used for either composite or Y)
3. Built-in sync separation circuit
4. Built-in Y/C mix circuit
5. Video and audio switches can be controlled independently.
6. 6dB amp built in to video and audio systems.
7. Output voltage gain can be varied by mounting an external resistor on the audio input pin.
8. Slave address can be changed: 90H or 92H
9. Built-in 3-value identification function

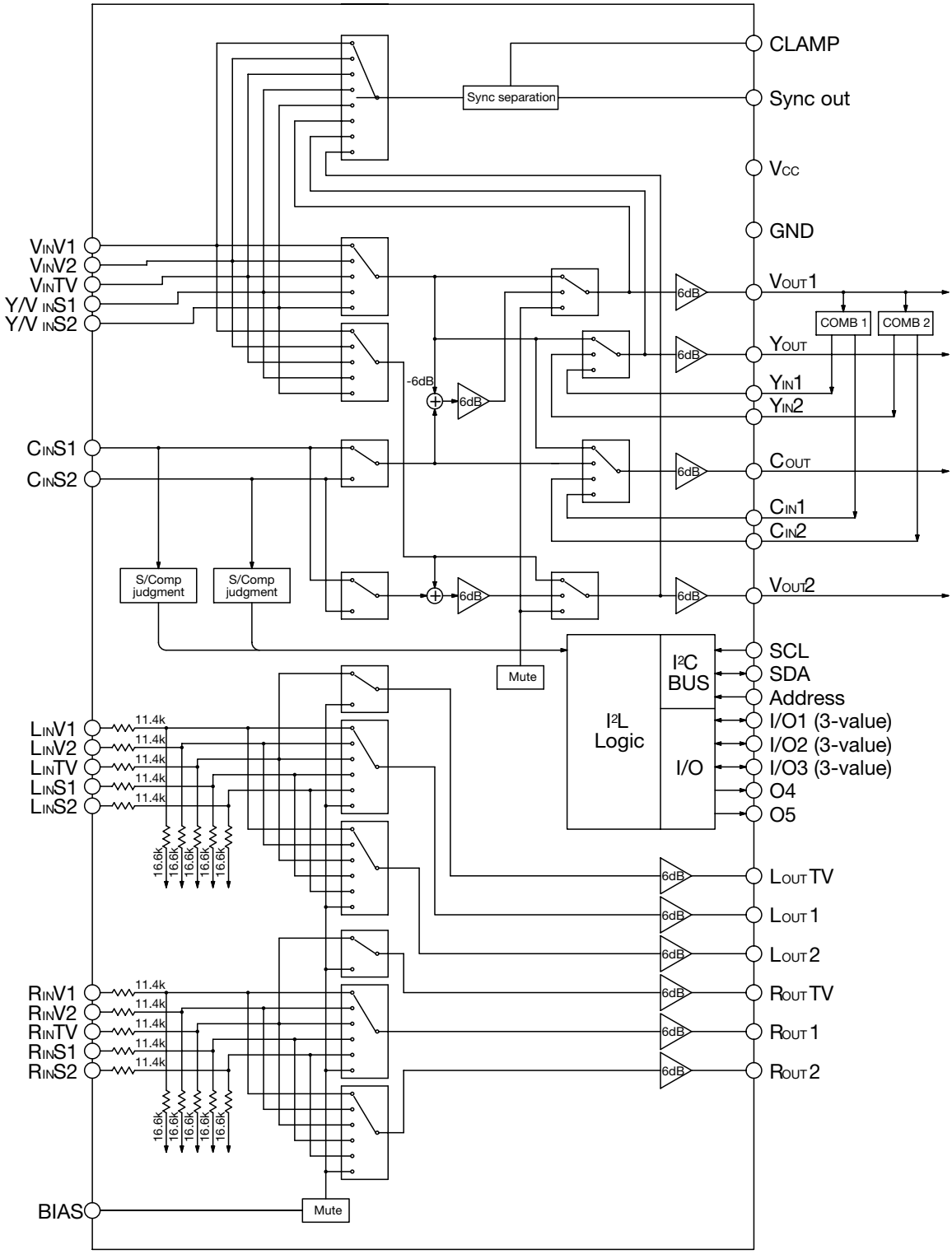
Package

SOP-44A (MM1495XF)
SDIP-42A (MM1495XD)

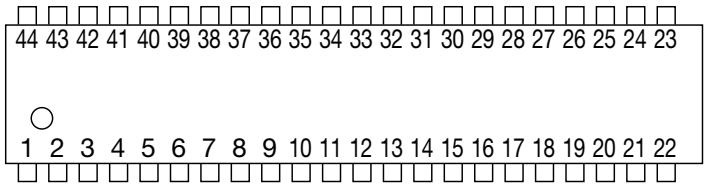
Applications

1. TV
2. Other video equipment

Block Diagram



Pin Assignment Typical model: MM1495XF

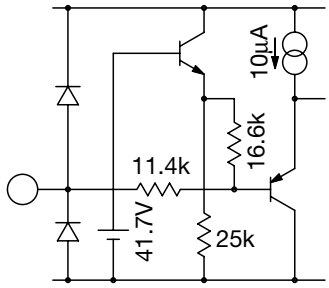
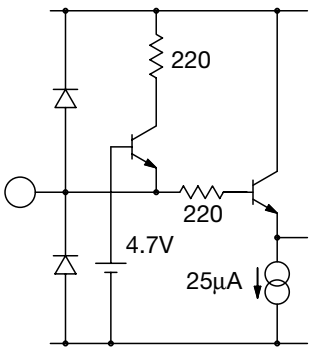


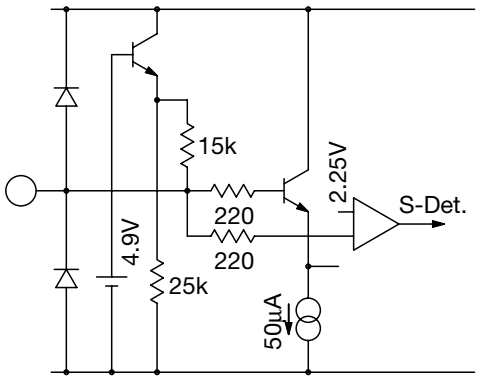
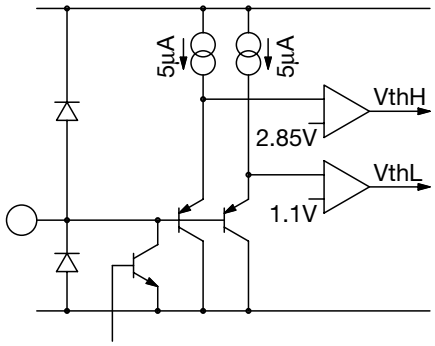
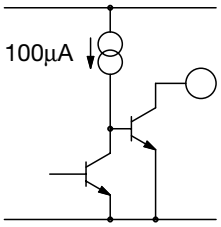
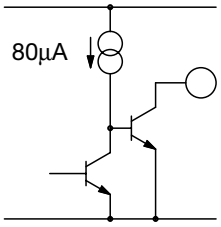
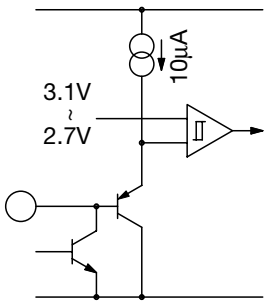
SOP-44A

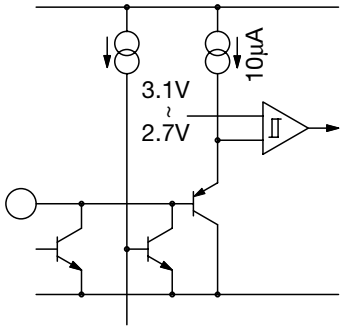
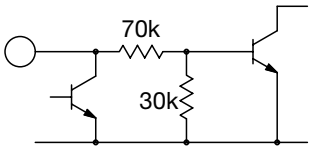
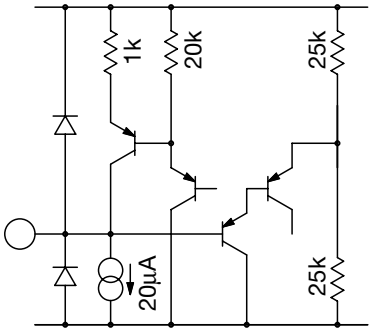
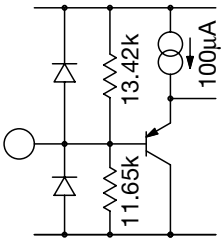
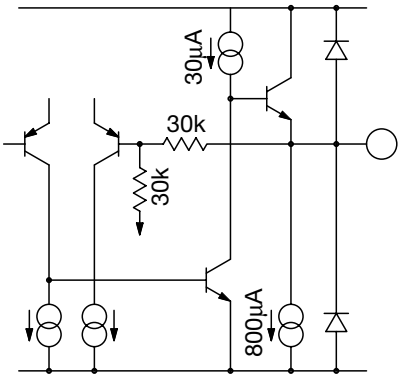
1	LINTV	12	LINS2	23	SCL	34	CIN2
2	RINTV	13	Y/VINS2	24	SDA	35	LOUT2
3	VINTV	14	RINS2	25	CLAMP	36	YIN1
4	LINV1	15	CINS2	26	BIAS	37	VCC
5	RINV1	16	I/O 2	27	Address	38	CIN1
6	VINV1	17	LINV2	28	ROUTTV	39	ROUT1
7	LINS1	18	RINV2	29	LOUTTV	40	VOUT1
8	Y/VINS1	19	VINV2	30	VOUT2	41	LOUT1
9	RINS1	20	I/O 3	31	GND	42	YOUT
10	CINS1	21	O4	32	YIN2	43	O5
11	I/O 1	22	SyncOUT	33	ROUT2	44	COUT

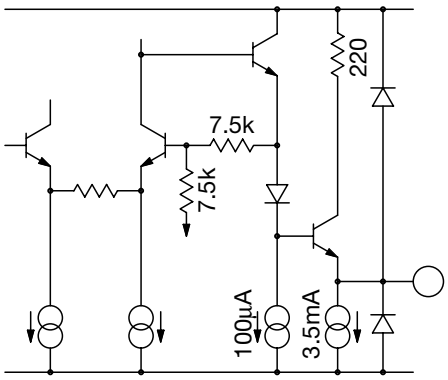
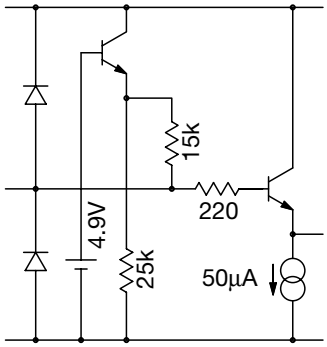
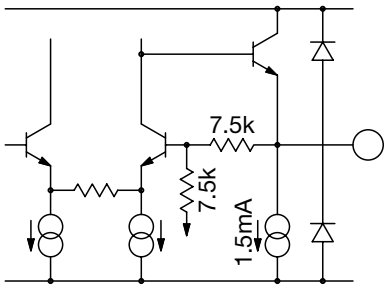
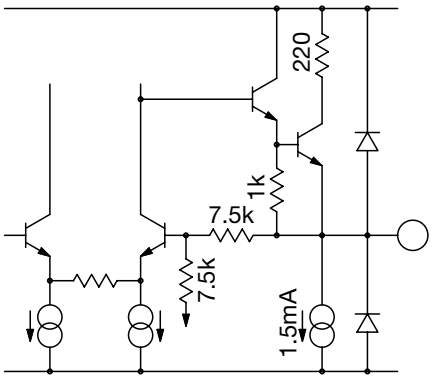
*XD has no 04 or Address pin.

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
1 2 4 5 7 9 12 14 17 18	LINTV RINTV LINV1 RINV1 LINS1 RINS1 LINS2 RINS2 LINV2 RINV2	Audio input	
3 6 8 13 19 32 36	VINTV VINV1 Y/VINS1 Y/VINS2 VINV2 YIN2 YIN1	Video input (Composite or Y) *Sync tip clamp	

Pin No.	Pin name	Function	Internal equivalent circuit diagram
10 15	CINS1 CINS2	Video input with S detector (Croma)	
11 16 20	I/O1 I/O2 I/O3	Input / Output port	
31	GND	GND	
37	VCC	VCC	
21 43	O4 O5	Output port	
22	Sync out	Sync separation output	
23	SCL	CLK input from I²C	

Pin No.	Pin name	Function	Internal equivalent circuit diagram
24	SDA	DATA input from I²C	
27	Address	Address select	
25	CLAMP	Clamp capacitor	
26	BIAS	BIAS	
28 29 33 35 39 41	ROUTTV LOUTTV ROUT2 LOUT2 ROUT1 LOUT1	Audio output	

Pin No.	Pin name	Function	Internal equivalent circuit diagram
30 40	VOUT2 VOUT1	Video output (Composite)	
34 38	CIN2 CIN1	Video input from comb-filter (Croma)	
42	YOUT	Video output (Y)	
44	COUT	Video output (Croma)	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temparature	T_{STG}	–40~+25	°C
Operating temparature	T_{OPR}	–20~+75	°C
Supply voltage	V_{CC} max.	12	V
Allowable loss	Pd	1100	mW

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temparature	T_{OPR}	–20~+75	°C
Operating voltage	V_{OP}	+8~+10	V

Electrical Characteristics Typical model: MM1495XF (Except where noted therwise, Ta=25°C, V_{CC}=9V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption		I_{CC}	No signal	41	58	75	mA
Terminal voltage							
Video input		V_{VIN}	3, 6, 8, 10, 13, 15, 19, 32, 34, 36, 38 pin	3.9	4.2	4.5	V
Composite video input		V_{VOUT}	30, 40 pin	1.9	2.1	2.3	V
S video input		V_{SOUT}	42, 44 pin	3.3	3.6	3.9	V
Audio input		V_{AIN}	1, 2, 4, 5, 7, 9, 12, 14, 17, 18 pin	3.2	3.5	3.8	V
Audio output		V_{AOUT}	28, 29, 33, 35, 39, 41 pin	3.8	4.1	4.4	V
Input impedance							
Croma input		Z_{CIN}	10, 15, 34, 38 pin	10	15	20	kΩ
Audio L input		Z_{LIN}	1, 4, 7, 12, 17 pin	22	28	34	kΩ
Audio R input		Z_{RIN}	2, 5, 9, 14, 18 pin	22	28	34	kΩ
Threshold level							
S detect of $C_{IN}S1$		$Vthc_1$		1.75	2.25	2.75	V
S detect of $C_{IN}S2$		$Vthc_2$		1.75	2.25	2.75	V
Address detect		Vth_{ADR}		1.5	2.0	2.5	V
I/O1 port detect	L	$Vthi_{1L}$		0.8	1.1	1.4	V
	H	$Vthi_{1H}$		2.70	2.85	3.00	V
I/O2 port detect	L	$Vthi_{2L}$		0.8	1.1	1.4	V
	H	$Vthi_{2H}$		2.70	2.85	3.00	V
I/O3 port detect	L	$Vthi_{3L}$		0.8	1.1	1.4	V
	H	$Vthi_{3H}$		2.70	2.85	3.00	V
$V_{OUT}1$							
Voltage gain		G_{V1}	SIN wave: 1V 100kHz	5.5	6.0	6.5	dB
Frequency characteristic		f_{V1}	SIN wave: 1V 10MHz/100kHz	–1.0	0.0	1.0	dB
Differential gain		DG_{V1}	Staircase signal 1V	–3	0	3	%
Differential phase		DP_{V1}	Staircase signal 1V	–3	0	3	°
Input dynamic range		D_{V1}	SIN wave: 100kHz THD=1.0%	1.6	1.9		V
Output impedance		Z_{V1}			(50)		Ω
Crosstalk		CT_{V1}	use test circuit 2 3.58MHz, 1V		–60	–55	dB

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
VOUT2							
Voltage gain		G_{V2}	SIN wave: 1V 100kHz	5.5	6.0	6.5	dB
Frequency characteristic		f_{V2}	SIN wave: 1V 10MHz/100kHz	–1.0	0.0	1.0	dB
Differential gain		DG_{V2}	Staircase signal 1V	–3	0	3	%
Differential phase		DP_{V2}	Staircase signal 1V	–3	0	3	°
Input dynamic range		D_{V2}	SIN wave: 100kHz THD=1.0%	1.6	1.9		V
Output impedance		Z_{V2}			(50)		Ω
Crosstalk		CT_{V2}	use test circuit 2 3.58MHz, 1V		–60	–55	dB
YOUT							
Voltage gain		G_{Y1}	SIN wave: 1V 100kHz	5.5	6.0	6.5	dB
Frequency characteristic		f_{Y1}	SIN wave: 1V 10MHz/100kHz	–1.0	0.0	1.0	dB
Differential gain		DG_{Y1}	Staircase signal 1V	–3	0	3	%
Differential phase		DP_{Y1}	Staircase signal 1V	–3	0	3	°
Input dynamic range		D_{Y1}	SIN wave: 100kHz THD=1.0%	1.6	1.9		V
Crosstalk		CT_{Y1}	use test circuit 2 3.58MHz, 1V		–60	–55	dB
COUT							
Voltage gain		G_{C1}	SIN wave: 1V 100kHz	5.5	6.0	6.5	dB
Frequency characteristic		f_{C1}	SIN wave: 1V 10MHz/100kHz	–1.0	0.0	1.0	dB
Differential gain (Note.1)		DG_{C1}	Staircase signal 1V	–3	0	3	%
Differential phase (Note.1)		DP_{C1}	Staircase signal 1V	–3	0	3	°
Input dynamic range		D_{C1}	SIN wave: 100kHz THD=1.0%	2.75	3.25		V
Crosstalk		CT_{C1}	use test circuit 2 3.58MHz, 1V		–60	–55	dB
Sync out							
Sync separation level		V_{SEPA}		30	60	90	mV
Sync out output voltage	L	V_{SOL}	Sync out: sink 2mA			0.4	V
	H	V_{SOH}		4.8			V
LOUT1							
Voltage gain		G_{L1}	SIN wave: 1V (∗1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic		f_{L1}	SIN wave: 1V (∗1) 1MHz/1kHz	–1.0	0.0	1.0	dB
Total harmonic distortion		THD_{L1}	SIN wave: 1V (∗1) 1kHz		0.03	0.1	%
Output offset voltage		V_{OFFL1}	DC offset at the switching time	–30	0	30	mV
Output dynamic range		D_{L1}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (∗1)
Crosstalk		CT_{L1}	1kHz, 1V (∗1)		–90	–80	dB
Ripple rejection		RR_{L1}	At 2.2kΩ terminal V_{CC}=9V+0.3V (100Hz: SIN wave)		–45	–40	dB
ROUT1							
Voltage gain		G_{R1}	SIN wave: 1V (∗1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic		f_{R1}	SIN wave: 1V (∗1) 1MHz/1kHz	–1.0	0.0	1.0	dB
Total harmonic distortion		THD_{R1}	SIN wave: 1V (∗1) 1kHz		0.03	0.1	%
Output offset voltage		V_{OFFR1}	DC offset at the switching time	–30	0	30	mV
Output dynamic range		D_{R1}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (∗1)
Crosstalk		CT_{R1}	1kHz, 1V (∗1)		–90	–80	dB
Ripple rejection		RR_{R1}	At 2.2kΩ terminal V_{CC}=9V+0.3V (100Hz: SIN wave)		–45	–40	dB

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
LOUT2						
Voltage gain	G_{L2}	SIN wave: 1V (★1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic	f_{L2}	SIN wave: 1V (★1) 1MHz/1kHz	–1.0	0.0	1.0	dB
Total harmonic distortion	THD_{L2}	SIN wave: 1V (★1) 1kHz		0.03	0.1	%
Output offset voltage	V_{OFFL2}	DC offset at the switching time	–30	0	30	mV
Output dynamic range	D_{L2}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (★1)
Crosstalk	CT_{L2}	1kHz, 1V (★1)		–90	–80	dB
Ripple rejection	RR_{L2}	At 2.2kΩ terminal V_{CC}=9V+0.3V (100Hz: SIN wave)		–45	–40	dB
ROUT2						
Voltage gain	G_{R2}	SIN wave: 1V (★1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic	f_{R2}	SIN wave: 1V (★1) 1MHz/1kHz	–1.0	0.0	1.0	dB
Total harmonic distortion	THD_{R2}	SIN wave: 1V (★1) 1kHz		0.03	0.1	%
Output offset voltage	V_{OFFR2}	DC offset at the switching time	–30	0	30	mV
Output dynamic range	D_{R2}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (★1)
Crosstalk	CT_{R2}	1kHz, 1V (★1)		–90	–80	dB
Ripple rejection	RR_{R2}	At 2.2kΩ terminal V_{CC}=9V+0.3V (100Hz: SIN wave)		–45	–40	dB
LOUTTV						
Voltage gain	G_{LTV}	SIN wave: 1V (★1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic	f_{LTV}	SIN wave: 1V (★1) 1MHz/1kHz	–1.0	0.0	1.0	dB
Total harmonic distortion	THD_{LTV}	SIN wave: 1V (★1) 1kHz		0.03	0.1	%
Output offset voltage	V_{OFFLTV}	DC offset at the switching time	–30	0	30	mV
Output dynamic range	D_{LTV}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (★1)
Crosstalk	CT_{LTV}	1kHz, 1V (★1)		–90	–80	dB
Ripple rejection	RR_{LTV}	At 2.2kΩ terminal V_{CC}=9V+0.3V (100Hz: SIN wave)		–45	–40	dB
ROUTTV						
Voltage gain	G_{RTV}	SIN wave: 1V (★1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic	f_{RTV}	SIN wave: 1V (★1) 1MHz/1kHz	–1.0	0.0	1.0	dB
Total harmonic distortion	THD_{RTV}	SIN wave: 1V (★1) 1kHz		0.03	0.1	%
Output offset voltage	V_{OFFRTV}	DC offset at the switching time	–30	0	30	mV
Output dynamic range	D_{RTV}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (★1)
Crosstalk	CT_{RTV}	1kHz, 1V (★1)		–90	–80	dB
Ripple rejection	RR_{RTV}	At 2.2kΩ terminal V_{CC}=9V+0.3V (100Hz: SIN wave)		–45	–40	dB

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
I²C condition (Note.2)						
Input voltage L	V_{IL}		0.0		1.5	V
Input voltage H	V_{IH}		3.0		5.0	V
Low level output voltage	V_{OL}	SDA sink 3mA	0.0		0.4	V
High level input current	I_{IH}	SDA, SCL=4.5V	–10		10	µA
Low level input current	I_{IL}	SDA, SCL=0.4V	–10		10	µA
Clock frequency	f_{SCL}				100	kHz
Data transfer wait time	t_{BUF}		4.7			µs
SCL start hold time	$t_{HD;STA}$		4.0			µs
SCL low level hold time	t_{LOW}		4.7			µs
SCL high level hold time	t_{HIGH}		4.0			µs
SCL start setup time	$t_{SU;STA}$		4.7			µs
SDA data hold time	$t_{HD;DAT}$		200			ns
SDA data setup time	$t_{SU;DAT}$		250			ns
SCL rise time	t_R				1000	ns
SCL fall time	t_F				300	ns
SCL stop setup time	$t_{SU;STO}$		4.0			µs

( ) The inside of parentheses is design guarantee value.

(*1) Effective value

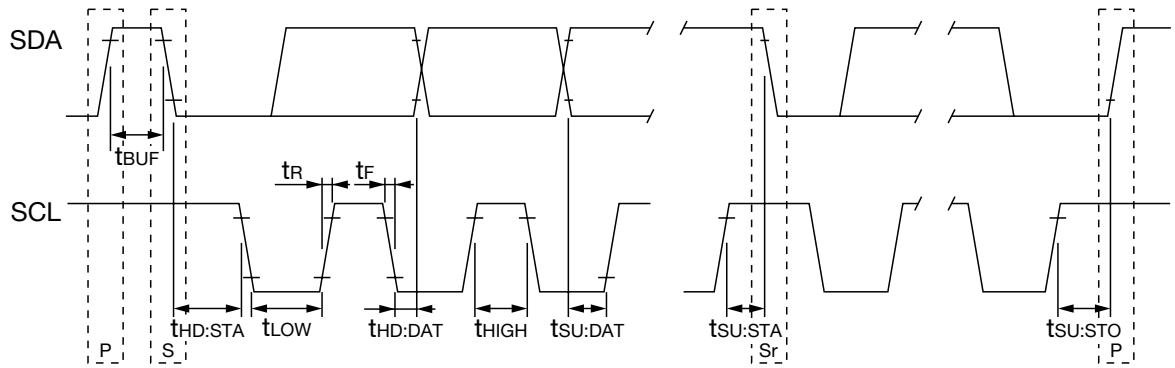
(Note.1) Differential gain and Differential phase of C_{OUT}.

The following combination is presumed as a case that a Y signal is left in the croma output terminal (C_{OUT}).

{ (1) At the time of the V-throughmode choice
{ (2) When a Y signal is left with comb-filter for $C_{IN}1$, the $C_{IN}2$ input.

Do the measurement of differential-gain and differential-phase with the C_{OUT} terminal by the above mode.

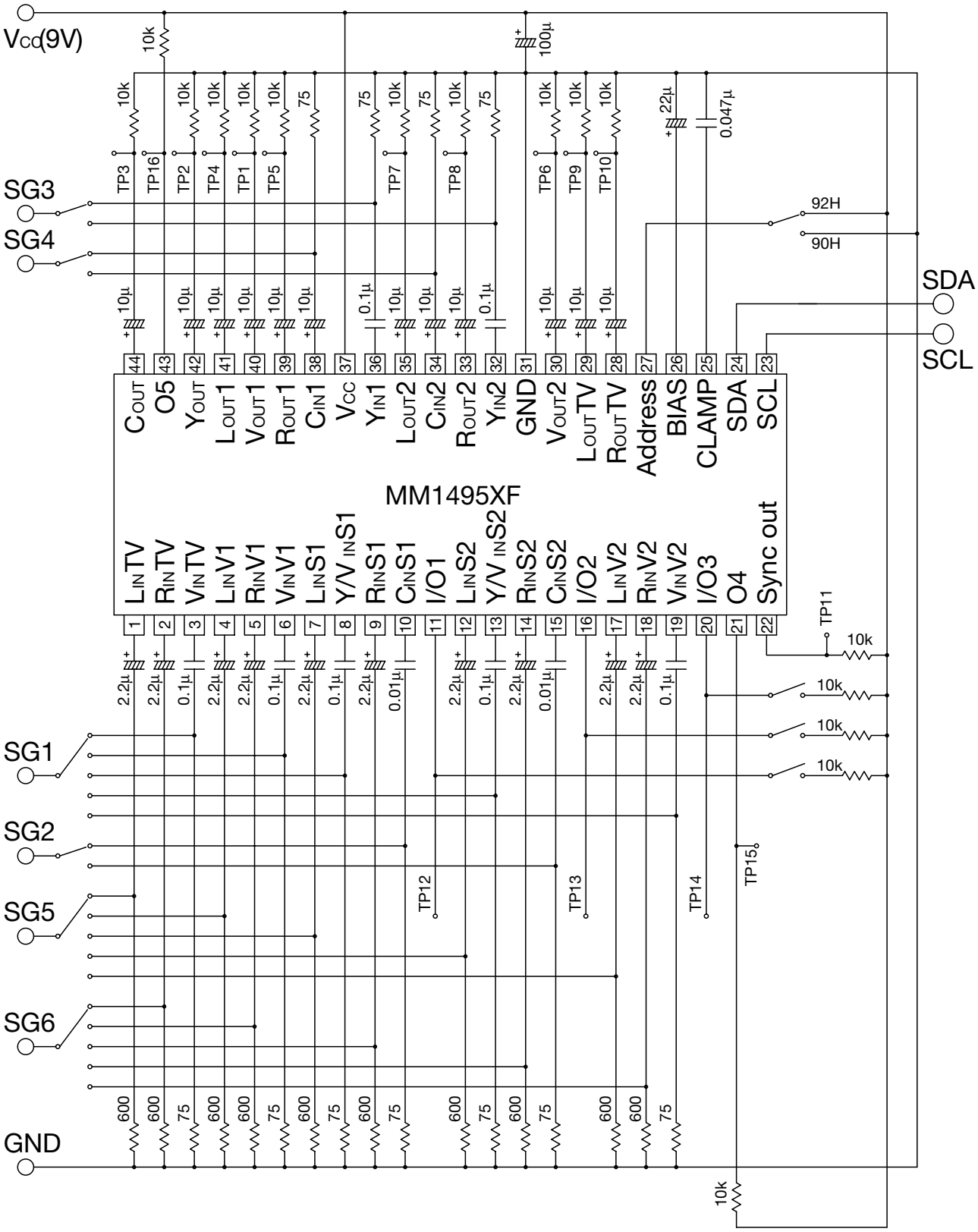
(Note.2) I²C condition



(Note.3) Video inputs

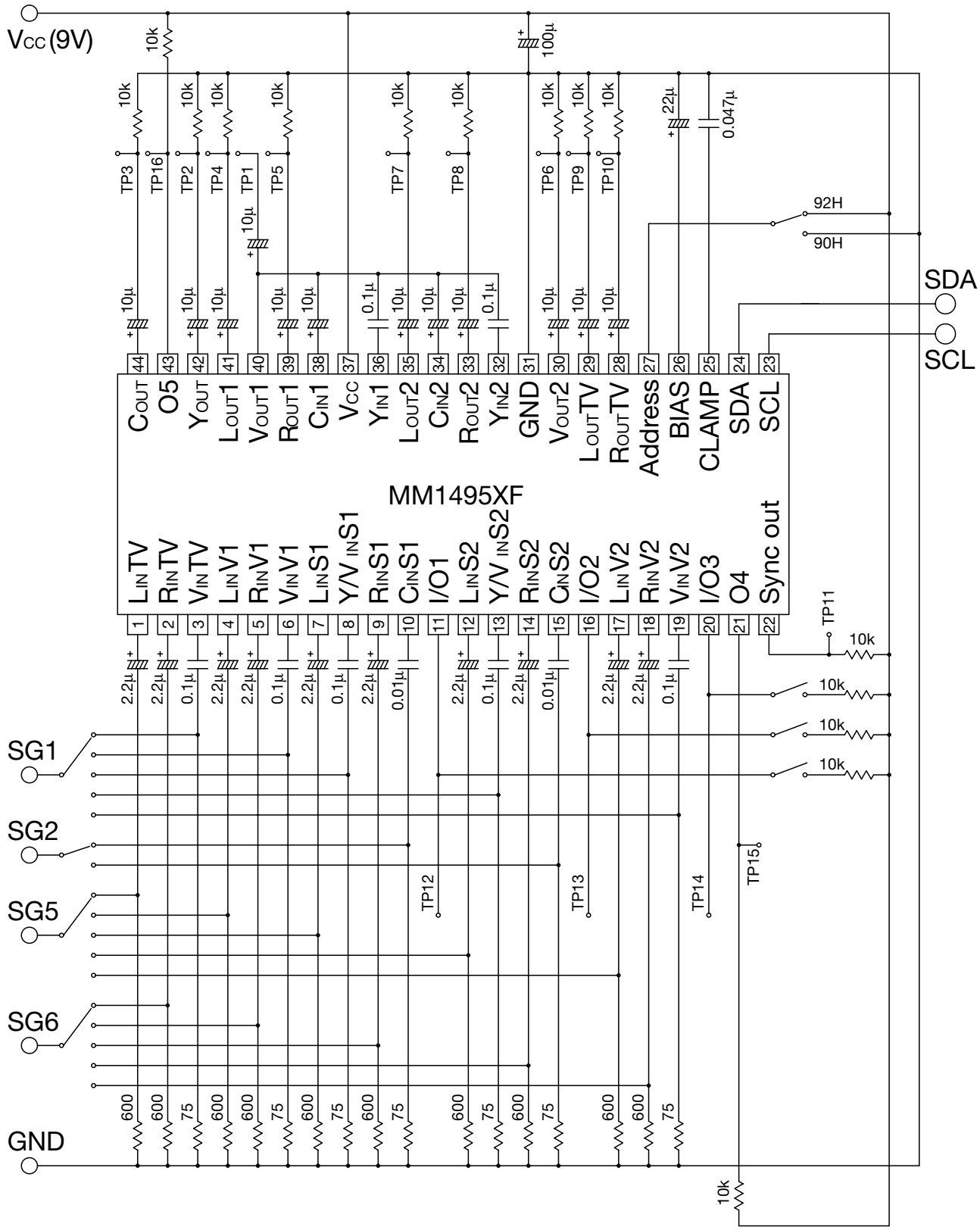
$V_{IN}V1$, $V_{IN}V2$, $V_{IN}TV$, $Y/V_{IN}S1$, $Y/V_{IN}S2$, $Y_{IN}1$ and $Y_{IN}2$ inputs are sync tip clamped, while $C_{IN}S1$, $C_{IN}S2$, $C_{IN}1$ and $C_{IN}2$ inputs are non-clamped.

Measuring Circuit 1



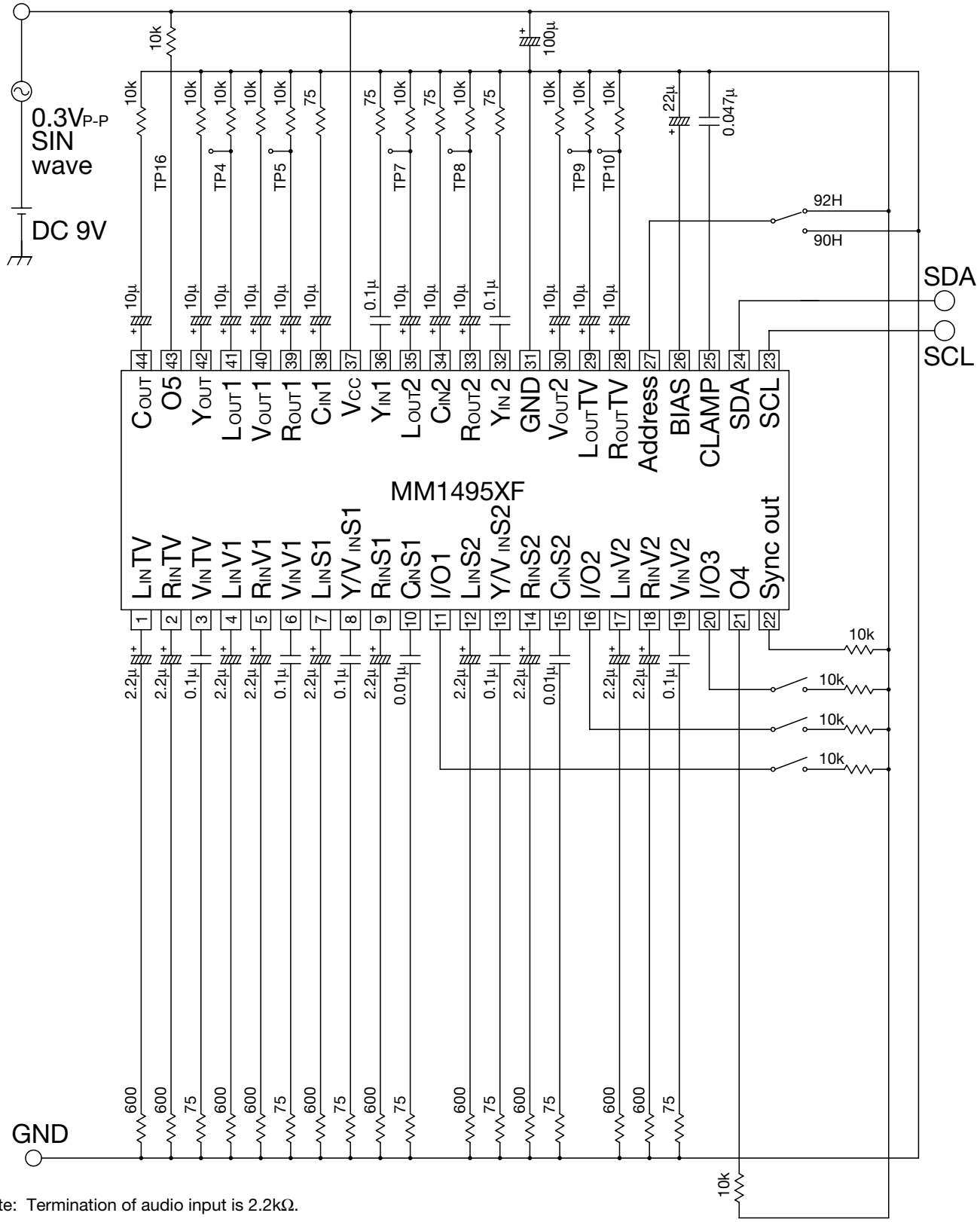
Measuring Circuit 2

For measuring crosstalk



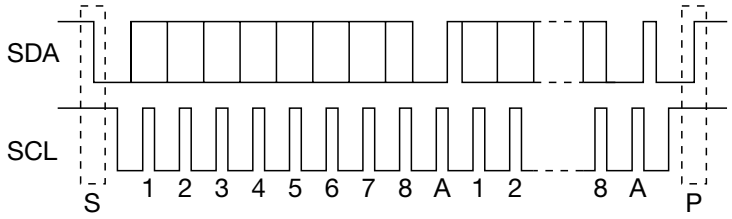
Measuring Circuit 3

For measuring ripple rejection



note: Termination of audio input is 2.2kΩ.

I²C BUS



S:Start Condition
P:Stop Condition
A:Acknowledge

I²C BUS is inter bus system controled by 2 lines (SDA, SCL).
Data are transmitted and received in the units of byte and Acknowledge.
It is transmitted by MSB first from the Start conditions.

[Control registers]

Control registers are data sent from the master for determining the switch conditions.
The data format is set as shown in the following figure.

S	Slave address							R/W	A	DATA1								A
	1	0	0	1	0	0	0/1	0		b07	b06	b05	b04	b03	b02	b01	b00	

Address byte

DATA2								A	DATA3								A	P
b17	b16	b15	b14	b13	b12	b11	b10		b27	b26	b25	b24	b23	b22	b21	b20		

Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.
Set the R/W bit to 0 when data are used control registers.
As MM1495 slave address, either 90H or 92H can be selected according to the ADR terminal conditions. When ADR terminal is L, 90H is selected.
The following figure indicates the control contents of control registers and switches.
Each bit of control registers is reset to 0, when power-on.

No.	DATA condition							
DATA1	b07	b06	b05	b04	b03	b02	b01	b00
		Y/C select		Mute		Main V select		
		Y, CIN1/2	Y, COUT	LOUT1 ROUT1	VOUT1			
DATA2	b17	b16	b15	b14	b13	b12	b11	b10
			Mute			Sub V select		
			LOUTTV ROUTTV	LOUT2 ROUT2	VOUT2			
DATA3	b27	b26	b25	b24	b23	b22	b21	b20
	Output port select					Sync sepa select		
	O5	O4	O3	O2	O1			

MM1495 consists of one address byte and three control data bytes (4bytes in total).
All data over the limited length (5th and subsequent bytes) are fully neglected.
For details of the control contents of switches, refer to the separate table.

Switch Control Table

Main V select

Mode		Output	S detect		Bus data		
					Main select		
Input	S/V	$V_{OUT}1$	CS2	CS1	b02	b01	b00
S2	V	Y/V_{IN}S2	Low	*	1	1	0
	S	Y/V_{IN}S2 +C_{IN}S2	Open				
	FV	Y/V_{IN}S2					1
S1	V	Y/V_{IN}S1	*	Low	1	0	0
	S	Y/V_{IN}S1 + C_{IN}S1		Open			
	FV	Y/V_{IN}S1					1
V2	V	V_{IN}V2	*	*	0	1	1
V1	V	V_{IN}V1	*	*	0	1	0
TV	V	V_{IN}TV	*	*	0	0	*

*: Don't care

Main L / R select

Mode	Output		Bus data		
			Main select		
Input	$L_{OUT}1$	$R_{OUT}1$	b02	b01	b00
S2	L_{IN}S2	R_{IN}S2	1	1	*
S1	L_{IN}S1	R_{IN}S1	1	0	*
V2	L_{IN}V2	R_{IN}V2	0	1	1
V1	L_{IN}V1	R_{IN}V1	0	1	0
TV	L_{IN}TV	R_{IN}TV	0	0	*

Main Y/C select

Mode		Output		Main V select mode		Bus data	
						Y/C select	
Input	Through	Y_{OUT}	C_{OUT}			b05	b06
S2	Y/C_{IN}	Y_{IN}1	C_{IN}1	S2	V or FV	0	0
		Y_{IN}2	C_{IN}2				1
	V through	Y/V_{IN}S2	Y/V_{IN}S2			1	*
	S through	Y/V_{IN}S2	C_{IN}S2		S	*	*
S1	Y/C_{IN}	Y_{IN}1	C_{IN}1	S1	V or FV	0	0
		Y_{IN}2	C_{IN}2				1
	V through	Y/V_{IN}S1	Y/V_{IN}S1			1	*
	S through	Y/V_{IN}S1	C_{IN}S1		S	*	*
V2	Y/C_{IN}	Y_{IN}1	C_{IN}1	V2	V	0	0
		Y_{IN}2	C_{IN}2				1
	V through	V_{IN}V2	V_{IN}V2			1	*
V1	Y/C_{IN}	Y_{IN}1	C_{IN}1	V1	V	0	0
		Y_{IN}2	C_{IN}2				1
	V through	V_{IN}V1	V_{IN}V1			1	*
TV	Y/C_{IN}	Y_{IN}1	C_{IN}1	TV	V	0	0
		Y_{IN}2	C_{IN}2				1
	V through	V_{IN}TV	V_{IN}TV			1	*

Sub V select

Mode		Output	S detect		Bus data		
					Main select		
Input	S/V	VOUT2	CS2	CS1	b12	b11	b10
S2	V	Y/VINS2	Low	*	1	1	0
	S	Y/VINS2 +CINS2	Open				
	FV	Y/VINS2					1
S1	V	Y/VINS1	*	Low	1	0	0
	S	Y/VINS1 +CINS1		Open			
	FV	Y/VINS1					1
V2	V	VINV2	*	*	0	1	1
V1	V	VINV1	*	*	0	1	0
TV	V	VINTV	*	*	0	0	*

Sub L / R select

Mode	Output		Bus data		
			Sub select		
Input	LOUT2	ROUT2	b12	b11	b10
S2	LINS2	RINS2	1	1	*
S1	LINS1	RINS1	1	0	*
V2	LINV2	RINV2	0	1	1
V1	LINV1	RINV1	0	1	0
TV	LINTV	RINTV	0	0	*

Video mute

Mode		Bus data	
		Video mute	
Output	Mute	b03	b13
VOUT1	ON	0	*
	OFF	1	
VOUT2	ON	*	0
	OFF		1

Audio mute

Mode		Bus data		
		Audio mute		
Output	Mute	b04	b14	b15
LOUT1 ROUT1	ON	0	*	*
	OFF	1		
LOUT2 ROUT2	ON	*	0	*
	OFF		1	
LOUTTV ROUTTV	ON	*	*	0
	OFF			1

Sync sepa select

Mode		Output	Bus data		
			Sync sepa select		
			b22	b21	b20
Video input	S2	Y/VINS2	1	1	0
	S1	Y/VINS1	1	0	0
	V2	VINV2	0	1	1
	V1	VINV1	0	1	0
	TV	VINTV	0	0	0
Video output	VOUT2	VOUT2	1	1	1
	VOUT1	VOUT1	1	0	1
	YOUT	YOUT	0	0	1

Output port switching

Mode		Bus data				
		Output port switching				
Port	Condition	b27	b26	b25	b24	b23
I/O1	Open	*	*	*	*	0
	Low					1
I/O2	Open	*	*	*	0	*
	Low				1	
I/O3	Open	*	*	0	*	*
	Low			1		
O4	Open	*	0	*	*	*
	Low		1			
O5	Open	0	*	*	*	*
	Low	1				

[Status registers]

Status registers are data to inform the master of the device status.

The data format is set as shown in the following figure.

S	Slave address							R/W	A	Status register								NA	P
	1	0	0	1	0	0	0/1	1		b37	b36	b35	b34	b33	b32	b31	b30		
	Address byte									device status									

Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.

Set the R/W bit to 1 when data are used status registers.

As MM1495 slave address, either 91H or 93H can be selected according to the ADR terminal conditions.

When ADR terminal is L, 91H is selected.

Set the confirmation acknowledgement after the end of status register to non-acknowledgement.

The following figure shows the correspondence of the output data of status registers.

b37	b36	b35	b34	b33	b32	b31	b30
Input port detect						S detect	
I/O3 Low	I/O3 High	I/O2 Low	I/O2 High	I/O1 Low	I/O1 High	CINS2	CINS1

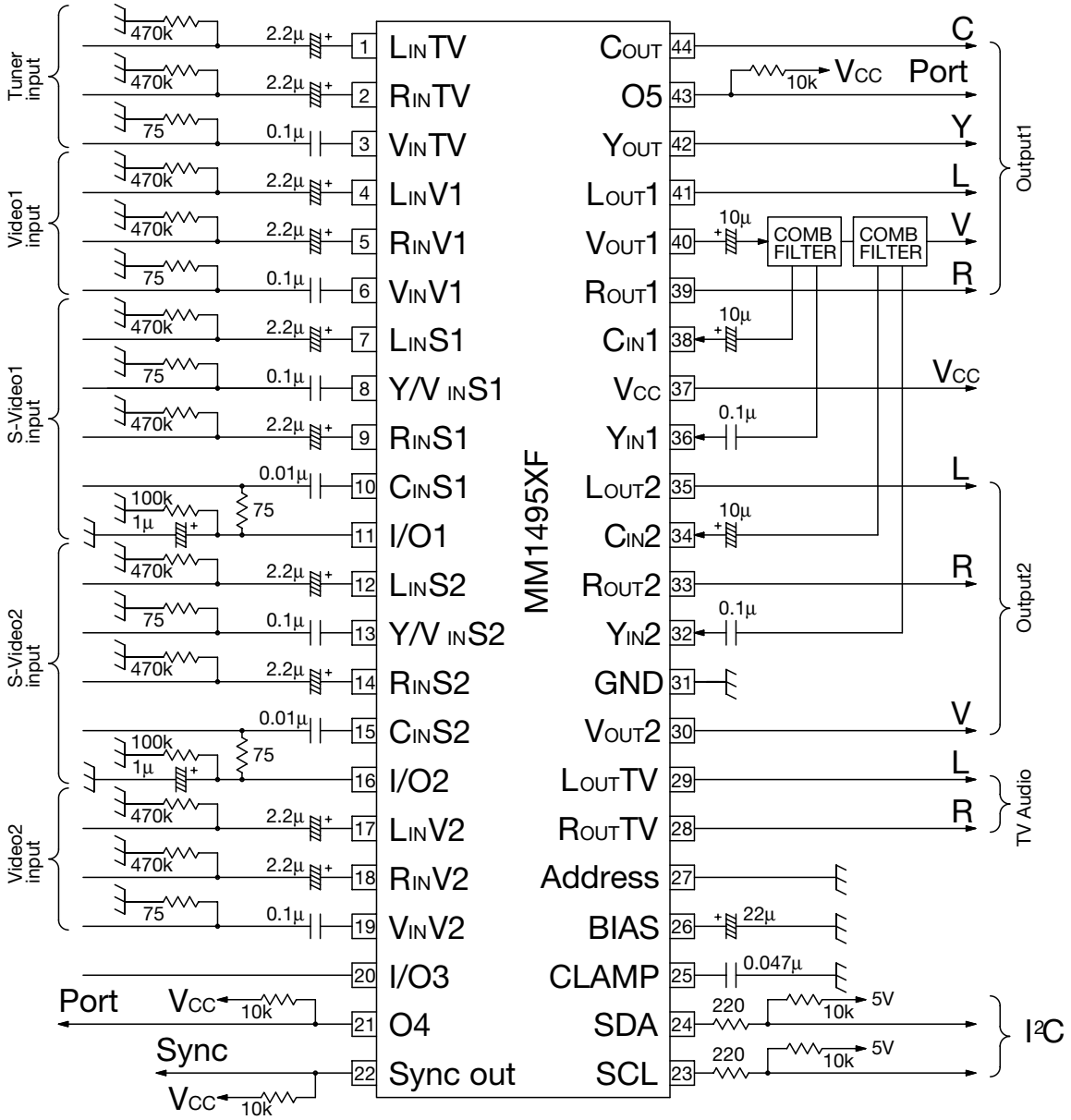
Input port detect: I/O1~3 are identified by 3 values, and output according to the combinations shown in the following table.

S detect: Judge the DC level of CINS1, the CINS2 terminal, and do the detection of the S input.

DC voltage of I/O1~3	I/O Low	I/O High
DC ≦ 0.8V	1	1
1.4V ≦ DC ≦ 2.7V	1	0
3.0V ≦ DC	0	0

CINSn condition	b31 or b30
Internal voltage	1
DC<1.75V	0

Application Circuit 1

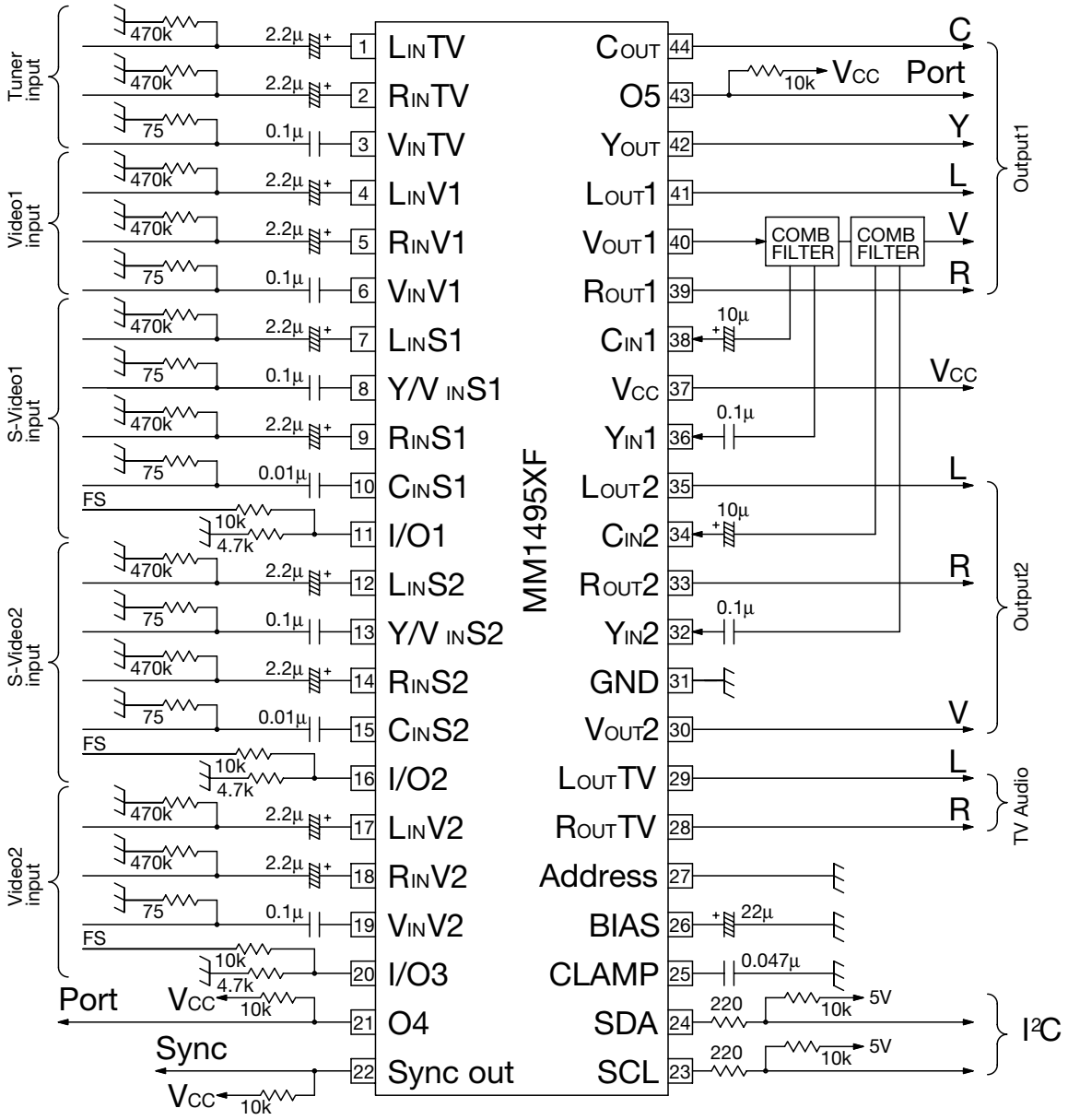


Note.

(1) VOUT is set to 2.1V, while CIN is set to 4.2V.
Be careful since the capacitor polarity may differ according to the comb filter bias.

(2) The case that a Y element is left by the Comb-filter character is presumed the condenser of CIN1, CIN2, and there is it as 10µF.
You can use 0.01µF when a Y element isn't left in the croma output of Comb-filter.

Application Circuit 2



Note.

(1) V_{OUT} is set to 2.1V, while C_{IN} is set to 4.2V.
Be careful since the capacitor polarity may differ according to the comb filter bias.

(2) The case that a Y element is left by the Comb-filter character is presumed the condenser of $C_{IN}1$, $C_{IN}2$, and there is it as 10µF.
You can use 0.01µF when a Y element isn't left in the croma output of Comb-filter.