

DATA SHEET

74LVC2GU04 Dual inverter

Product specification
Supersedes data of 2004 May 24

2004 Sep 21

Dual inverter**74LVC2GU04****FEATURES**

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- ESD protection:
 - HBM EIA/JESD22-A114-B exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V.
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C.

DESCRIPTION

The 74LVC2GU04 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Input can be driven from either 3.3 V or 5 V devices. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

The 74LVC2GU04 provides two inverters. Each inverter is a single stage with unbuffered output.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay input nA to output nY	$V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ kΩ	2.3	ns
		$V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ Ω	1.8	ns
		$V_{CC} = 2.7$ V; $C_L = 50$ pF; $R_L = 500$ Ω	2.6	ns
		$V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ Ω	2.3	ns
		$V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ Ω	1.7	ns
C_I	input capacitance		5	pF
C_{PD}	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2	7.8	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

2. The condition is $V_I = GND$ to V_{CC} .

Dual inverter

74LVC2GU04

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	nY
L	H
H	L

Note

1. H = HIGH voltage level;

L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC2GU04GW	-40 °C to +125 °C	6	SC-88	plastic	SOT363	YD
74LVC2GU04GV	-40 °C to +125 °C	6	SC-74	plastic	SOT457	VU4
74LVC2GU04GM	-40 °C to +125 °C	6	XSON6	plastic	SOT886	YD

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	GND	ground (0 V)
3	2A	data input
4	2Y	data output
5	V _{CC}	supply voltage
6	1Y	data output

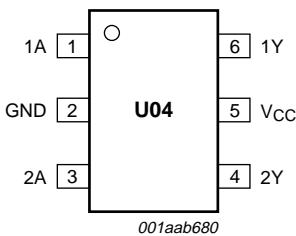
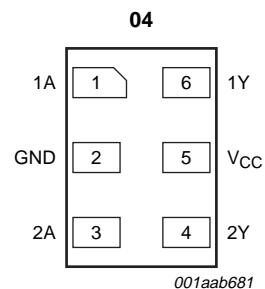


Fig.1 Pin configuration SC-88 and SC-74.



Transparent top view

Fig.2 Pin configuration XSON6.

Dual inverter

74LVC2GU04

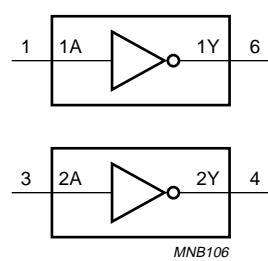


Fig.3 Logic symbol.

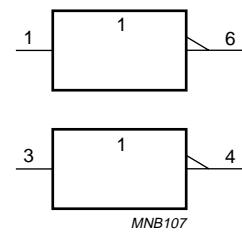


Fig.4 IEC logic symbol.

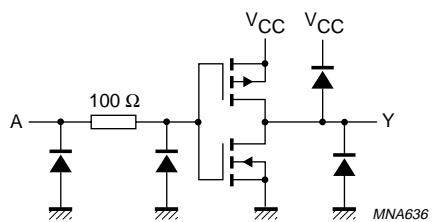


Fig.5 Logic diagram (one gate).

Dual inverter

74LVC2GU04

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	V_{CC}	V
T_{amb}	operating ambient temperature		-40	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	0	20	ns/V
		$V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0 \text{ V}$	-	-50	mA
V_I	input voltage	note 1	-0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC} \text{ or } V_O < 0 \text{ V}$	-	± 50	mA
V_O	output voltage	active mode; note 1	-0.5	$V_{CC} + 0.5$	V
I_O	output source or sink current	$V_O = 0 \text{ V to } V_{CC}$	-	± 50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	± 100	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	power dissipation	$T_{amb} = -40 \text{ °C to } +125 \text{ °C}$	-	300	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Dual inverter

74LVC2GU04

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 °C to +85 °C							
V _{IH}	HIGH-level input voltage		1.65 to 5.5	0.75 × V _{CC}	—	—	V
V _{IL}	LOW-level input voltage		1.65 to 5.5	—	—	0.25 × V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 µA I _O = 4 mA I _O = 8 mA I _O = 12 mA I _O = 24 mA I _O = 32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 4.5	— — — — — —	— — — — — —	0.1 0.45 0.3 0.4 0.55 0.55	V V V V V V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 µA I _O = -4 mA I _O = -8 mA I _O = -12 mA I _O = -24 mA I _O = -32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 4.5	V _{CC} - 0.1 1.2 1.9 2.2 2.3 3.8	— — — — — —	— — — — — —	V V V V V V
I _{LI}	input leakage current	V _I = 5.5 V or GND	5.5	—	±0.1	±5	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A	5.5	—	0.1	10	µA

Dual inverter

74LVC2GU04

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 °C to +125 °C							
V _{IH}	HIGH-level input voltage		1.65 to 5.5	0.8 × V _{CC}	—	—	V
V _{IL}	LOW-level input voltage		1.65 to 5.5	—	—	0.2 × V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 100 µA	1.65 to 5.5	—	—	0.1	V
		I _O = 4 mA	1.65	—	—	0.70	V
		I _O = 8 mA	2.3	—	—	0.45	V
		I _O = 12 mA	2.7	—	—	0.60	V
		I _O = 24 mA	3.0	—	—	0.80	V
		I _O = 32 mA	4.5	—	—	0.80	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = -100 µA	1.65 to 5.5	V _{CC} - 0.1	—	—	V
		I _O = -4 mA	1.65	0.95	—	—	V
		I _O = -8 mA	2.3	1.7	—	—	V
		I _O = -12 mA	2.7	1.9	—	—	V
		I _O = -24 mA	3.0	2.0	—	—	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	5.5	—	—	±20	µA
		V _I = V _{CC} or GND; I _O = 0 A	5.5	—	—	40	µA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Dual inverter

74LVC2GU04

AC CHARACTERISTICS

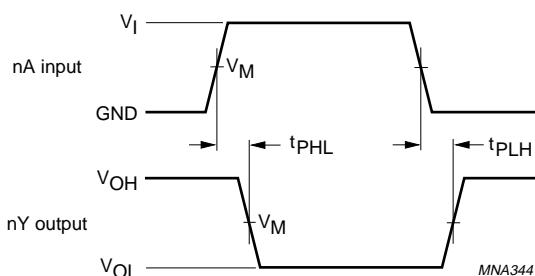
GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 °C to +85 °C							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 6 and 7	1.65 to 1.95	0.5	2.3	5.0	ns
			2.3 to 2.7	0.3	1.8	4.0	ns
			2.7	0.3	2.6	4.5	ns
			3.0 to 3.6	0.3	2.3	3.7	ns
			4.5 to 5.5	0.3	1.7	3.0	ns
T_{amb} = -40 °C to +125 °C							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 6 and 7	1.65 to 1.95	0.5	—	6.3	ns
			2.3 to 2.7	0.3	—	5.0	ns
			2.7	0.3	—	5.6	ns
			3.0 to 3.6	0.3	—	4.5	ns
			4.5 to 5.5	0.3	—	3.8	ns

Note

- All typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.

AC WAVEFORMS



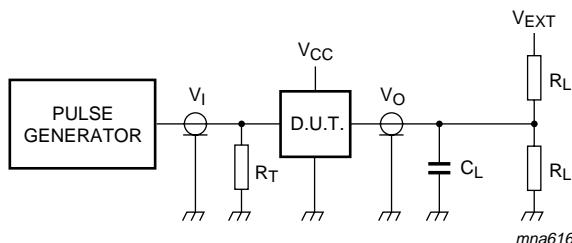
V _{CC}	V _M	INPUT	
		V _I	t _r = t _f
1.65 V to 1.95 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V _{CC}	V _{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 The input (nA) to output (nY) propagation delays.

Dual inverter

74LVC2GU04

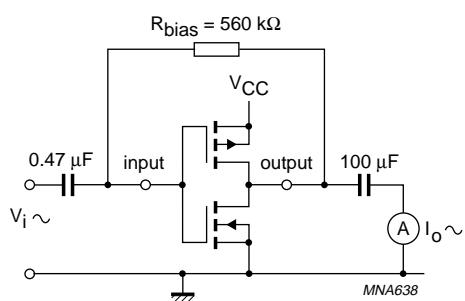


V_{CC}	V_I	C_L	R_L	V_{EXT}
				t_{PLH}/t_{PHL}
1.65 V to 1.95 V	V _{CC}	30 pF	1 kΩ	open
2.3 V to 2.7 V	V _{CC}	30 pF	500 Ω	open
2.7 V	2.7 V	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	50 pF	500 Ω	open

Definitions for test circuit:

R_L = Load resistor.C_L = Load capacitance including jig and probe capacitance.R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.



$$g_{fs} = \frac{\Delta I_o}{\Delta V_i}$$

f_i = 1 kHz.V_O is constant.

Fig.8 Test set-up for measuring forward transconductance.

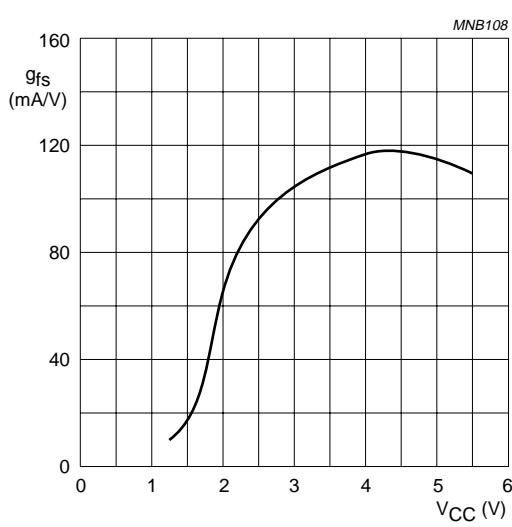


Fig.9 Typical forward transconductance as a function of supply voltage.

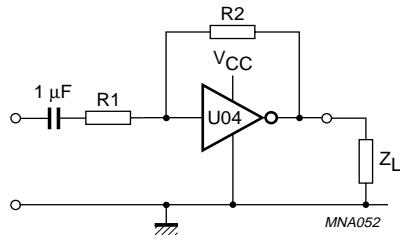
Dual inverter

74LVC2GU04

APPLICATION INFORMATION

Some applications for the 74LVC2GU04 are:

- Linear amplifier (see Fig.10)
- Crystal oscillator (see Fig.11).



$Z_L > 10 \text{ k}\Omega$, $R1 \geq 3 \text{ k}\Omega$ and $R2 \leq 1 \text{ M}\Omega$.

Open loop amplification: $A_{OL} = 20$ (typical).

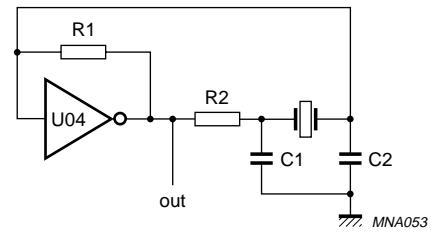
$$\text{Voltage amplification: } A_u = -\frac{A_{OL}}{1 + \frac{R1}{R2}(1 + A_{OL})}$$

Maximum output voltage: $V_{O(p-p)} = V_{CC} - 1.5 \text{ V}$ centered at $0.5 \times V_{CC}$.
Unity gain bandwidth product: $B = 5 \text{ MHz}$ (typical).

Fig.10 Linear amplifier configuration.

Remark to the application information.

All values given are typical values unless otherwise specified.



$C1 = 47 \text{ pF}$ (typical).

$C2 = 22 \text{ pF}$ (typical).

$R1 = 1 \text{ M}\Omega$ to $10 \text{ M}\Omega$ (typical).

$R2$ optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} ($I_{CC} = 2 \text{ mA}$ (typical) at $V_{CC} = 3.3 \text{ V}$ and $f = 10 \text{ MHz}$).

Fig.11 Crystal oscillator configuration.

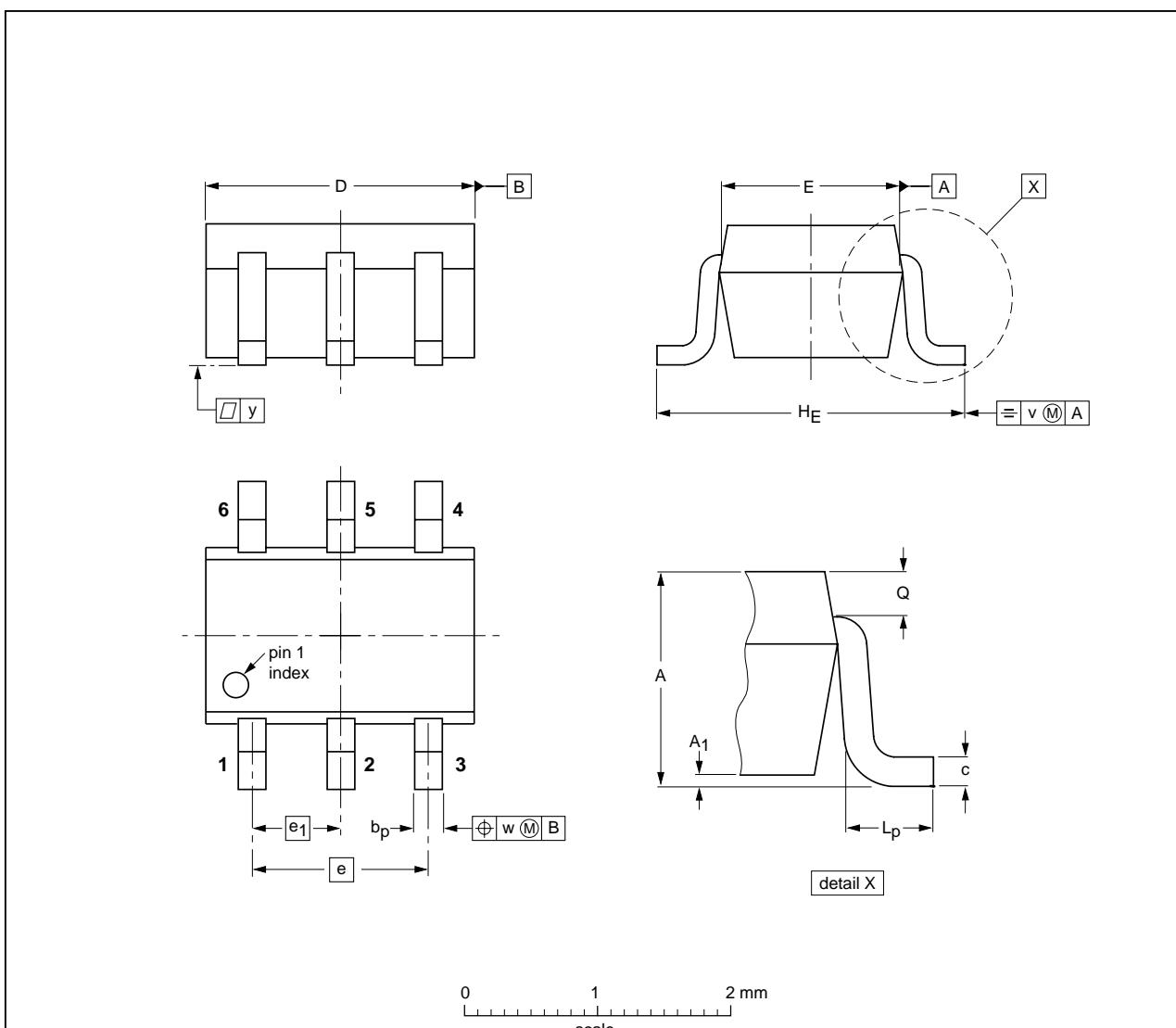
Dual inverter

74LVC2GU04

PACKAGE OUTLINES

Plastic surface mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

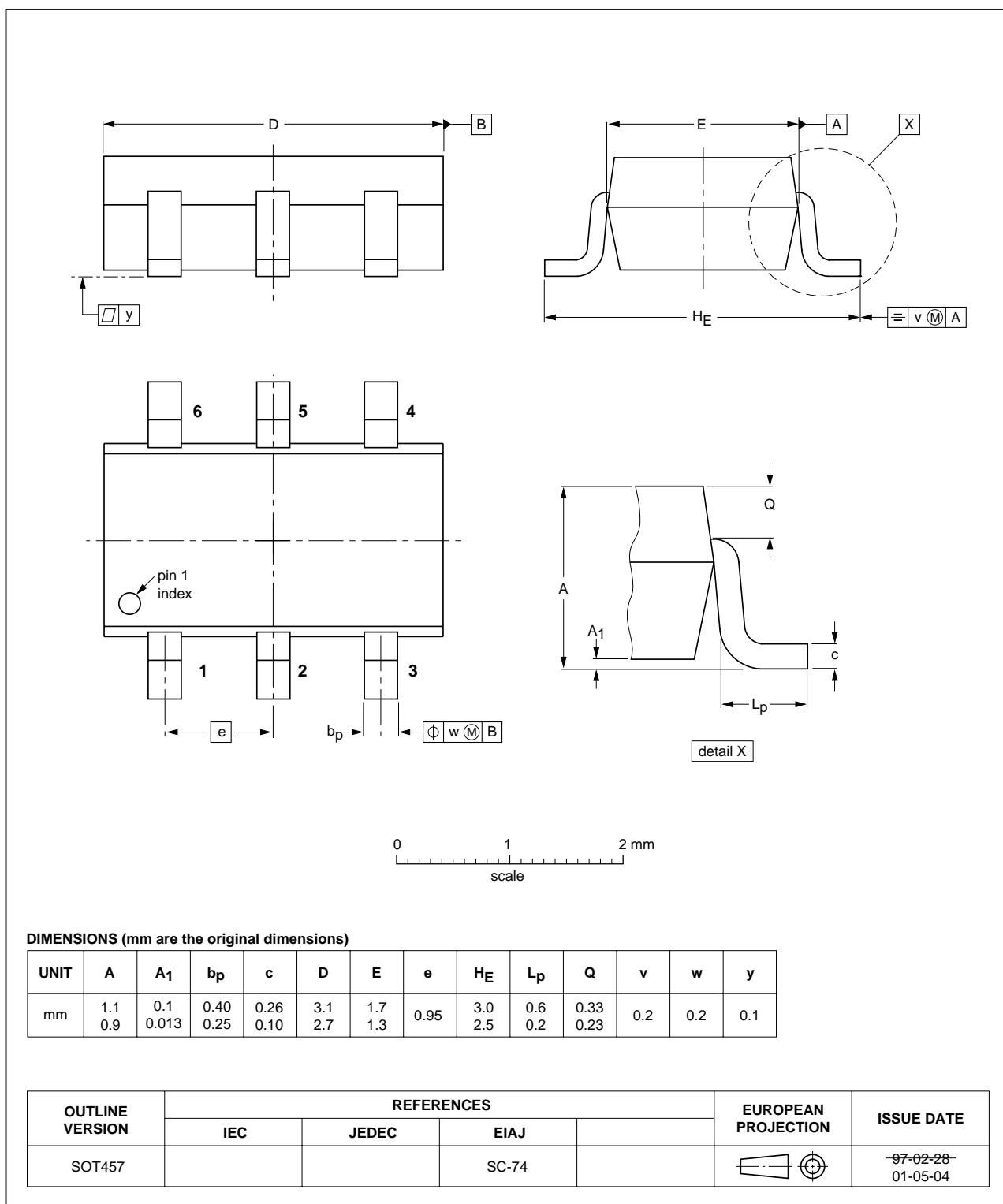
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ	SC-88		
SOT363						97-02-28

Dual inverter

74LVC2GU04

Plastic surface mounted package; 6 leads

SOT457

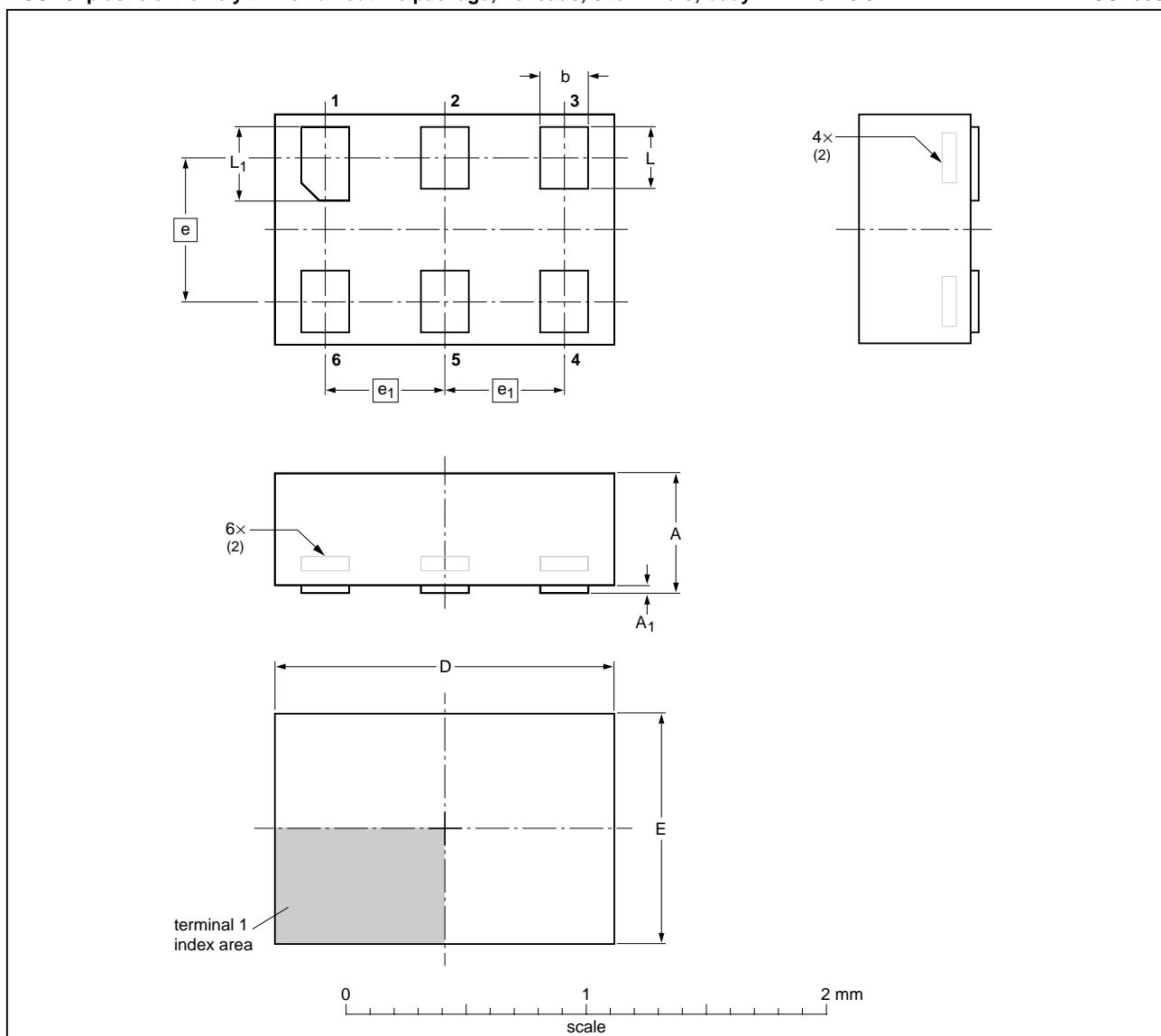


Dual inverter

74LVC2GU04

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				04-07-15 04-07-22

Dual inverter

74LVC2GU04

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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SCA76

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