FAIRCHILD
SEMICONDUCTOR®

SPT9689

DUAL ULTRAFAST VOLTAGE COMPARATOR

TECHNICAL DATA

FEBRUARY 20, 2001

FEATURES

- 650 ps propagation delay
- 100 ps propagation delay variation
- 70 dB CMRR
- Low feedthrough and crosstalk
- Differential latch control
- ECL compatible

APPLICATIONS

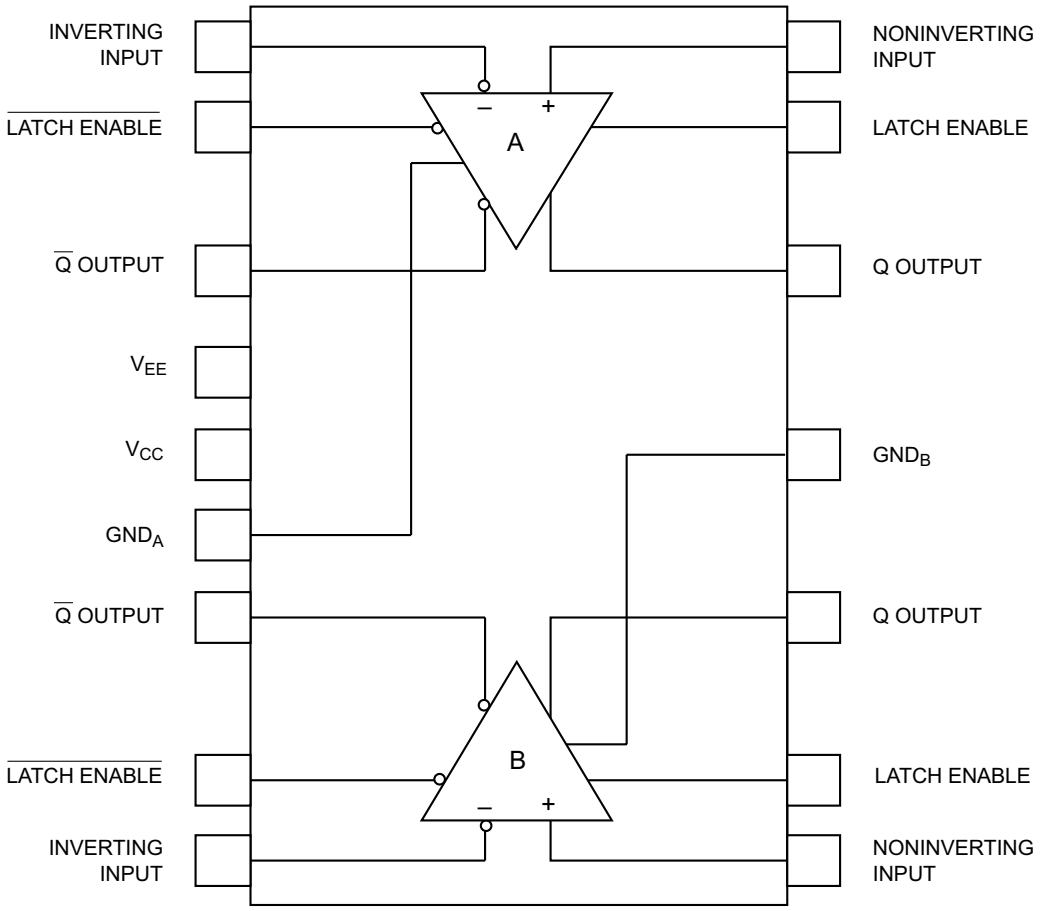
- Automated test equipment
- High-speed instrumentation
- Window comparators
- High-speed timing
- Line receivers
- High-speed triggers
- Threshold detection
- Peak detection

GENERAL DESCRIPTION

The SPT9689 is a *Sub*nanosecond monolithic dual comparator. The propagation delay variation is less than 100 ps from 5 to 50 mV input overdrive voltage. The input slew rate is 10 V/ns. The device utilizes a high precision differential input stage with a common-mode range of –2.5 V to +4.0 V.

ECL-compatible complementary digital outputs are capable of driving 50 Ω terminated transmission lines and providing 30 mA output drive. The SPT9689 is pin compatible with the SPT9687. It is available in 20-lead PLCC and 20-contact LCC packages over the industrial temperature range. The SPT9689 is also available in die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} to GND) .... –0.5 to +6.0 V
Negative Supply Voltage (V_{EE} to GND) .. –6.0 to +0.5 V
Ground Voltage Differential ..... –0.5 to +0.5 V

Input Voltages

Input Common Mode Voltage ..... –4.0 to +5.0 V
Differential Input Voltage ..... –3.0 to +3.0 V
Input Voltage, Latch Controls ..... V_{EE} to 0.5 V

Output

Output Current ..... 30 mA

Temperature

Operating Temperature, ambient ..... –40 to +85 °C
junction ..... +150 °C
Lead Temperature, (soldering 60 seconds) ..... +300 °C
Storage Temperature ..... –65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V, V_{EE} =–5.20 V, R_L = 50 Ohm to –2 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9689A MIN	SPT9689A TYP	SPT9689A MAX	SPT9689B MIN	SPT9689B TYP	SPT9689B MAX	UNITS
DC CHARACTERISTICS									
Input Offset Voltage	$V_{IN, CM}$=0, R_S=0 Ohms[1]	I	–10	±3.0	10	–25	±12	25	mV
Input Offset Voltage	$V_{IN, CM}$=0, R_S=0 Ohms[1] $T_{MIN}<T_A<T_{MAX}$	IV	–15	±4.5	15	–30	±15	30	mV
Offset Voltage Tempco		V		10			40		µV/°C
Input Bias Current		I		±8	±25		±8	±25	µA
Input Bias Current	$T_{MIN}<T_A<T_{MAX}$	IV		±12	±38		±12	±38	µA
Input Offset Current		I		±1.0	±3.0		±2.0	±5.0	µA
Input Offset Current	$T_{MIN}<T_A<T_{MAX}$	IV		±2.0	±5.0		±4.0	±7.0	µA
Positive Supply Current	Dual	I		18	30		18	35	mA
Negative Supply Current	Dual	I		40	55		40	60	mA
Positive Supply Voltage, V_{CC}		IV	4.75	5.0	5.25	4.75	5.0	5.25	V
Negative Supply Voltage, V_{EE}		IV	–4.95	–5.2	–5.45	–4.95	–5.2	–5.45	V
Input Common Mode Range		V	–2.5		+4.0	–2.5		+4.0	V
Latch Enable Common Mode Range		IV	–2.0		0	–2.0		0	V
Open Loop Gain		V		66			66		dB
Differential Input Resistance		V		500			500		kΩ
Input Capacitance		V		0.6			0.6		pF
Power Supply Sensitivity		V		70			70		dB
Common Mode Rejection Ratio	V_{CM}=–2.5 to +4.0	V		70			70		dB
Power Dissipation	Dual, Without Load	I		350	425		350	475	mW
Power Dissipation	Dual, With Load	I		400	550		400	550	mW
Output High Level	ECL 50 Ohms to –2 V	I	–1.00		–.81	–1.00		–.81	V
Output Low Level	ECL 50 Ohms to –2 V	I	–1.95		–1.54	–1.95		–1.54	V
AC CHARACTERISTICS									
Propagation Delay	20 mV O.D.	IV		650	850		750	950	ps
Latch Set-up Time		V		150	300		150	300	ps
Latch to Output Delay	250 mV O.D.	V		500	600		500	600	ps
Latch Pulse Width		V		500			500		ps
Latch Hold Time		V		0			0		ps
Rise Time	20% to 80%	V		180			180		ps
Fall Time	20% to 80%	V		80			80		ps
Slew Rate		V		10			10		V/ns
Bandwidth	–3 dB	V		900			900		MHz

[1] R_S = Source impedance

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

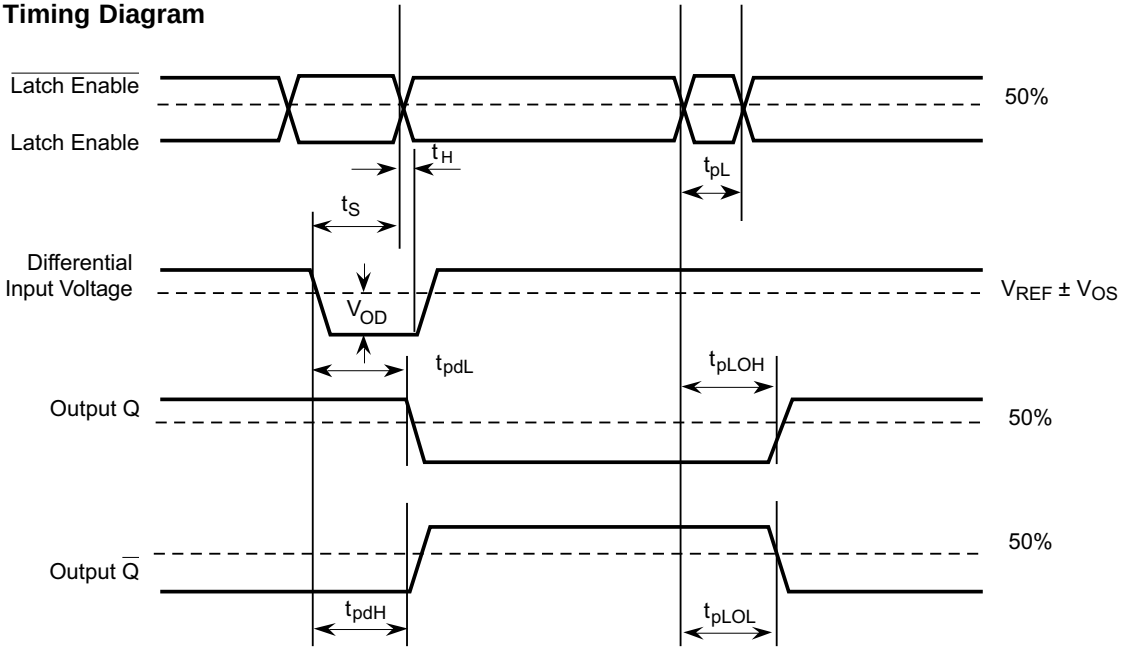
TIMING INFORMATION

The timing diagram for the comparator is shown in figure 1. If LE is high and $\overline{LE}$ low in the SPT9689, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of a 20 mV overdrive voltage) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_S (set-up time) before the LE falling edge and $\overline{LE}$ rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_S will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may not be detected.

Figure 1 – Timing Diagram



V_{IN}+=100 mV (p-p), V_{OD}=20 mV

SWITCHING TERMS (Refer to figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY – the propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output LOW to HIGH transition

t_{pdL} INPUT TO OUTPUT LOW DELAY – the propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output HIGH to LOW transition

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY – the propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition

V_{OD} VOLTAGE OVERDRIVE – the difference between the differential input and reference input voltages

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY – the propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition

t_H MINIMUM HOLD TIME – the minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH – the minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change

t_S MINIMUM SET-UP TIME – the minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs

GENERAL INFORMATION

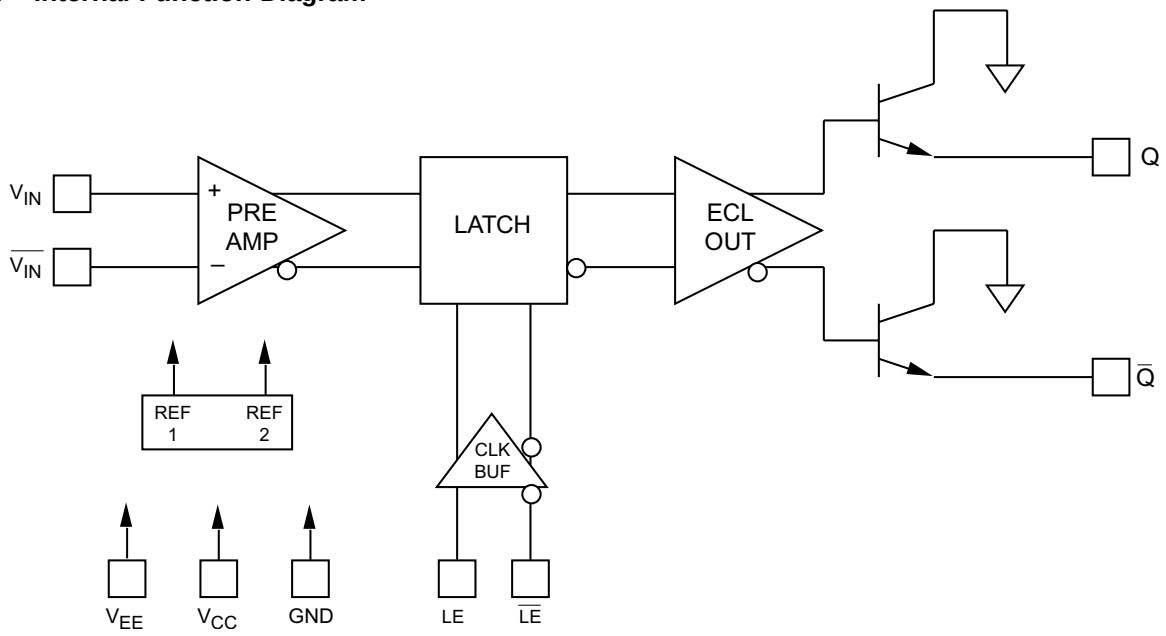
The SPT9689 is an ultrahigh-speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The SPT9689 has a complementary latch enable control for each comparator. Both should be driven by standard ECL logic levels.

The negative common mode voltage is –2.5 V. The positive common mode voltage is +4.0 V.

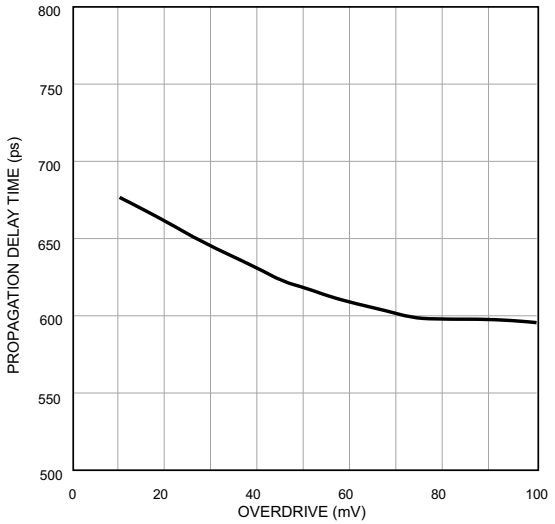
The dual comparators share the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection.

Figure 2 – Internal Function Diagram

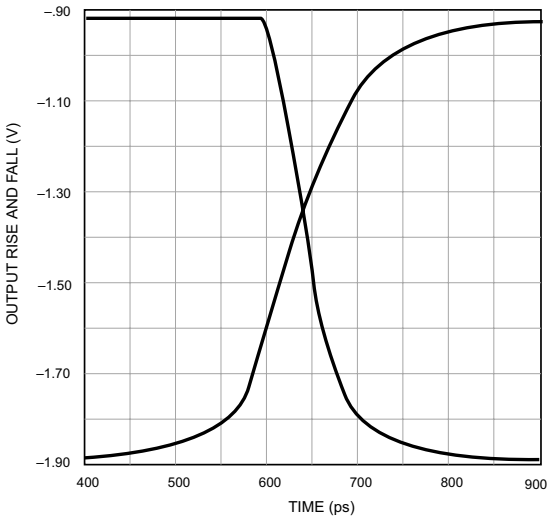


TYPICAL PERFORMANCE CHARACTERISTICS

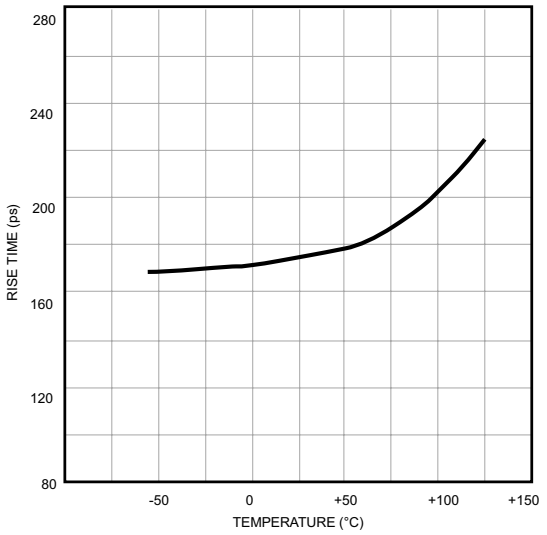
PROPAGATION DELAY VS OVERDRIVE VOLTAGE



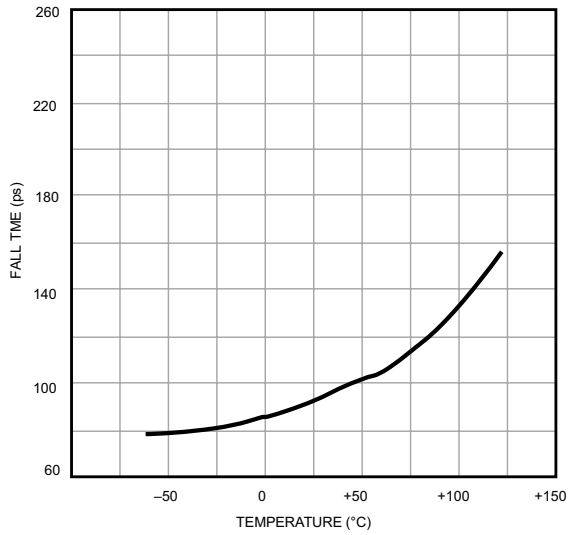
RISE AND FALL OF OUTPUTS VS TIME CROSSOVER



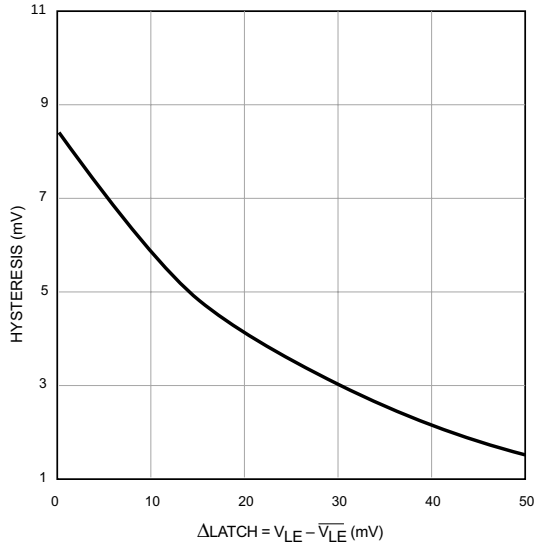
RISE TIME VS TEMPERATURE



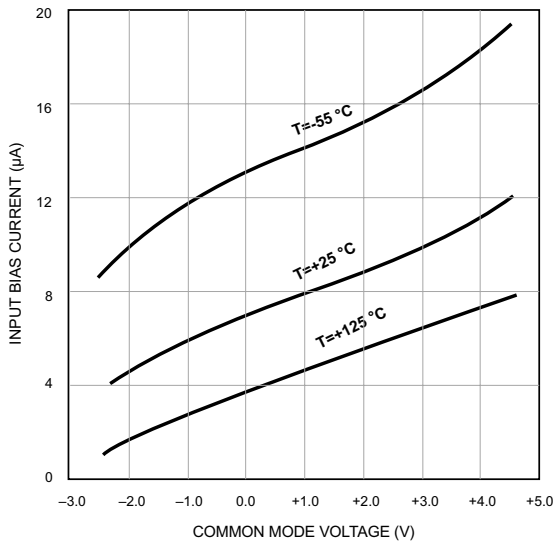
FALL TIME VS TEMPERATURE



HYSTERESIS VS ΔLATCH



INPUT BIAS CURRENT VS COMMON MODE VOLTAGE

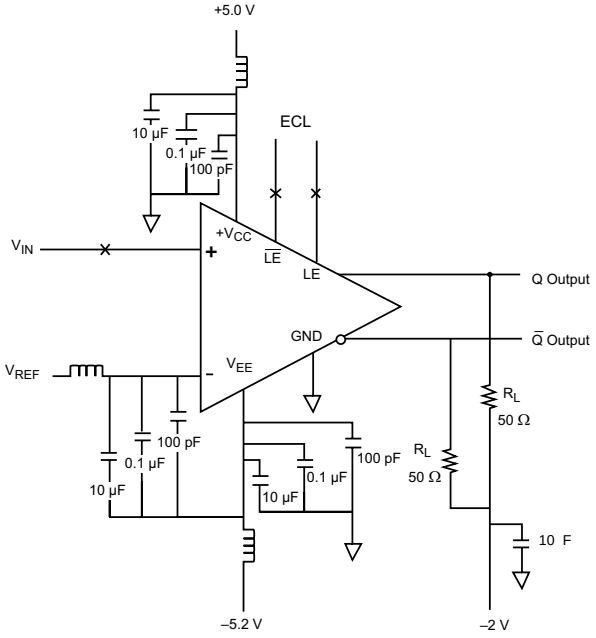


TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in figure 3. Although it needs few external components and is easy to apply, there are several conditions that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the SPT9689 comparator is a very high-frequency and high-gain device, certain layout rules must be followed to avoid oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used while the input impedance to the part is kept as low as possible to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. Both supply voltage pins should be decoupled with high-frequency capacitors as close to the device as possible. All ground pins and no connects should be soldered to a common ground plane to further improve noise immunity. If using the SPT9689 as a single comparator, the outputs of the inactive comparator can be grounded, left open, or terminated with 50 ohms to –2 V. All outputs on the active comparator, whether used or unused, should have identical terminations to minimize ground current switching transients.

Figure 3 – SPT9689 Typical Interface Circuit



NOTES:

▽ Denotes ground plane.

Ferrite bead. Fair Rite Part # 2643001501.

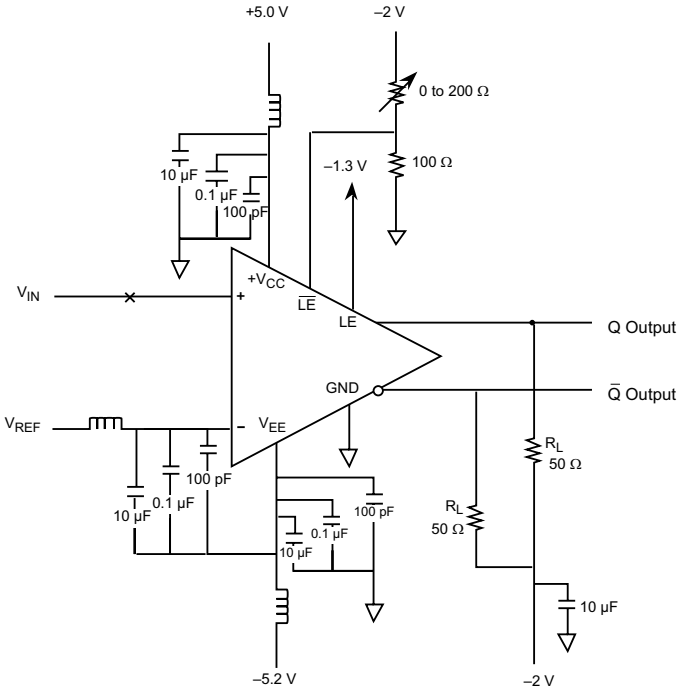
All resistors are chip type 1%.

0.1 µF and 100 pF capacitors are chip type mounted as close to the pins as possible.

10 µF tant capacitors have lead lengths <0.25" long.

Represents line termination.

Figure 4 – SPT9689 Typical Interface Circuit with Hysteresis



NOTES:

▽ Denotes ground plane.

Ferrite bead. Fair Rite Part # 2643001501.

All resistors are chip type 1%.

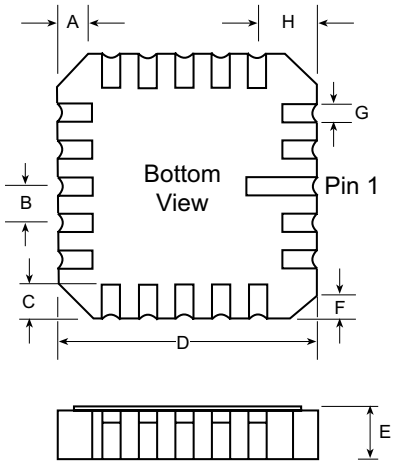
0.1 µF and 100 pF capacitors are chip type mounted as close to the pins as possible.

10 µF tant capacitors have lead lengths <0.25" long.

Represents line termination.

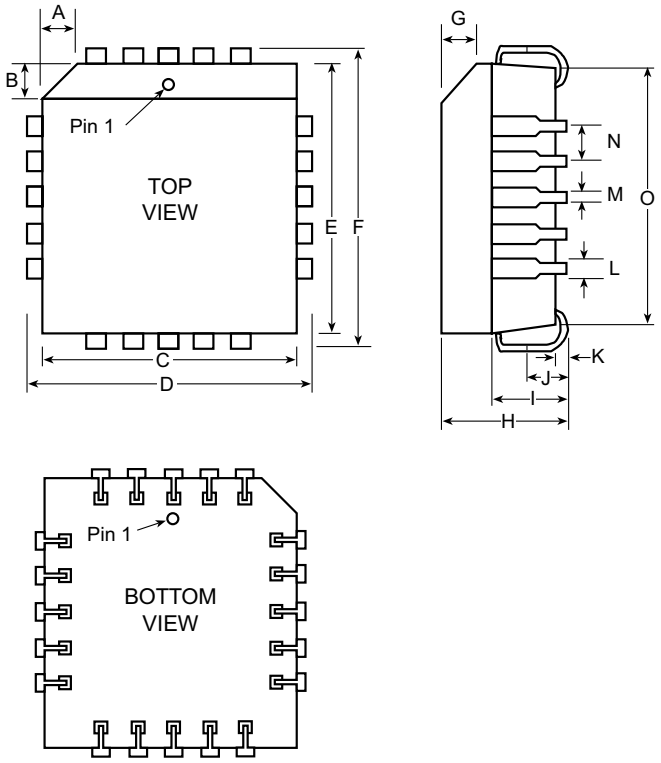
PACKAGE OUTLINES

20-Contact Leadless Chip Carrier (LCC)



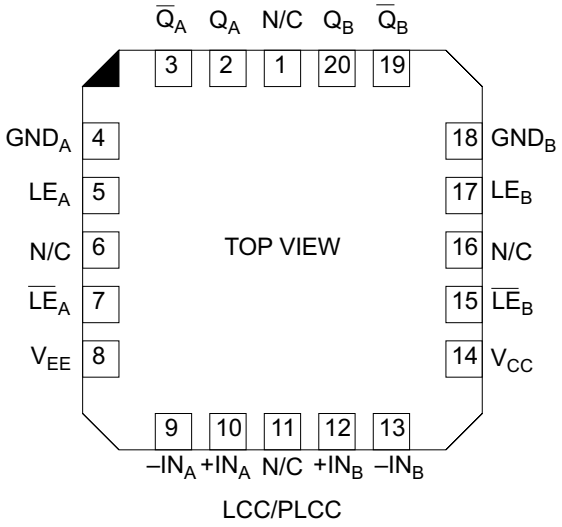
	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	.040 typ		1.02 typ	
B	.050 typ		1.27 typ	
C	0.045	0.055	1.14	1.40
D	0.345	0.360	8.76	9.14
E	0.054	0.066	1.37	1.68
F	.020 typ		0.51 typ	
G	0.022	0.028	0.56	0.71
H		0.075		1.91

20-Lead Plastic Leadless Chip Carrier (PLCC)



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	.045 typ		1.14 typ	
B	.045 typ		1.14 typ	
C	0.350	0.356	8.89	9.04
D	0.385	0.395	9.78	10.03
E	0.350	0.356	8.89	9.04
F	0.385	0.395	9.78	10.03
G	0.042	0.056	1.07	1.42
H	0.165	0.180	4.19	4.57
I	0.085	0.110	2.16	2.79
J	0.025	0.040	0.64	1.02
K	0.015	0.025	0.38	0.64
L	0.026	0.032	0.66	0.81
M	0.013	0.021	0.33	0.53
N		0.050		1.27
O	0.290	0.330	7.37	8.38

PIN ASSIGNMENTS



LCC/PLCC

PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
LE_A	Latch Enable A
$\overline{LE}_A$	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Noninverting Input A
$+IN_B$	Noninverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Latch Enabled B
$\overline{LE}_B$	Inverted Latch Enable B
GND_B	Ground B
Q_B	Output B
$\overline{Q}_B$	Inverted Output B

ORDERING INFORMATION

PART NUMBER	INPUT OFFSET	TEMPERATURE RANGE	PACKAGE TYPE
SPT9689AIC	10 mV	–40 to +85 °C	20C LCC
SPT9689BIC	25 mV	–40 to +85 °C	20C LCC
SPT9689AIP	10 mV	–40 to +85 °C	20L PLCC
SPT9689BIP	25 mV	–40 to +85 °C	20L PLCC
SPT9689ACU		+25 °C	Die*
SPT9689BCU		+25 °C	Die*

*Please see the die specification for guaranteed electrical performance.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.