



24-Bit, 20kHz, Low Power ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 24 BITS—NO MISSING CODES
- 19 BITS EFFECTIVE RESOLUTION UP TO 20kHz DATA RATE
- LOW NOISE: 1.8ppm
- FOUR DIFFERENTIAL INPUTS
- INL: 15ppm (max)
- EXTERNAL REFERENCE (0.5V to 5V)
- POWER-DOWN MODE
- SYNC MODE
- LOW POWER: 8mW at 20kHz
5mW at 10kHz

APPLICATIONS

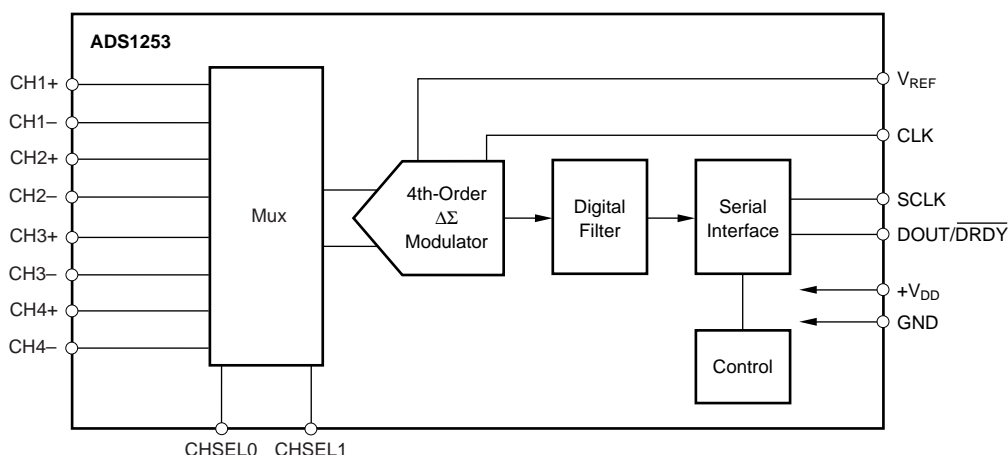
- CARDIAC DIAGNOSTICS
- DIRECT THERMOCOUPLE INTERFACES
- BLOOD ANALYSIS
- INFRARED PYROMETERS
- LIQUID/GAS CHROMATOGRAPHY
- PRECISION PROCESS CONTROL

DESCRIPTION

The ADS1253 is a precision, wide dynamic range, delta-sigma, Analog-to-Digital (A/D) converter with 24-bit resolution operating from a single +5V supply. The delta-sigma architecture is used for wide dynamic range and to guarantee 24 bits of no missing codes performance. An effective resolution of 19 bits (1.8ppm of rms noise) is achieved for conversion rates up to 20kHz.

The ADS1253 is designed for high-resolution measurement applications in cardiac diagnostics, smart transmitters, industrial process control, weight scales, chromatography, and portable instrumentation. The converter includes a flexible, two-wire synchronous serial interface for low-cost isolation.

The ADS1253 is a four-channel converter and is offered in an SSOP-16 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Analog Input: Current (Momentary)	±100mA
(Continuous)	±10mA
Voltage	GND – 0.3V to V _{DD} + 0.3V
V _{DD} to GND	–0.3V to 6V
V _{REF} Voltage to GND	–0.3V to V _{DD} + 0.3V
Digital Input Voltage to GND	–0.3V to V _{DD} + 0.3V
Digital Output Voltage to GND	–0.3V to V _{DD} + 0.3V
Lead Temperature (soldering, 10s)	+300°C
Power Dissipation (any package)	500mW



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
ADS1253E "	SSOP-16 "	322 "	–40°C to +85°C "	ADS1253E "	ADS1253E ADS1253E/2K5	Rails Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "ADS1253E/2K5" will get a single 2500-piece Tape and Reel.

ELECTRICAL CHARACTERISTICS

All specifications at T_{MIN} to T_{MAX}, V_{DD} = +5V, CLK = 8MHz, and V_{REF} = 4.096, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1253E			UNITS
		MIN	TYP	MAX	
ANALOG INPUT					
Input Voltage Range	CLK = 3,840Hz	GND		±V _{REF}	V
Input Impedance	CLK = 1MHz		260		MΩ
	CLK = 8MHz		1		MΩ
			125		kΩ
Input Capacitance			6		pF
Input Leakage	At +25°C		5	50	pA
	At T _{MIN} to T _{MAX}			1	nA
DYNAMIC CHARACTERISTICS					
Data Rate				20.8	kHz
Bandwidth	–3dB	4.24			kHz
Serial Clock (SCLK)				16	MHz
System Clock Input (CLK)				8	MHz
ACCURACY					
Integral Non-Linearity ⁽¹⁾	1kHz Input; 0.1dB below FS		±0.0002	±0.0015	% of FSR
THD			105		dB
Noise			1.8	2.7	ppm of FSR, rms
Resolution		24			Bits
No Missing Codes		24			Bits
Common-Mode Rejection	60Hz, AC	90	102		dB
Gain Error			0.1	1	% of FSR
Offset Error			±20	±100	ppm of FSR
Gain Sensitivity to V _{REF}			1:1		
Power-Supply Rejection Ratio		70	88		dB
PERFORMANCE OVER TEMPERATURE					
Offset Drift			0.07		ppm/°C
Gain Drift			0.4		ppm/°C
VOLTAGE REFERENCE					
V _{REF}		0.5	4.096	V _{DD}	V
Load Current			32		μA

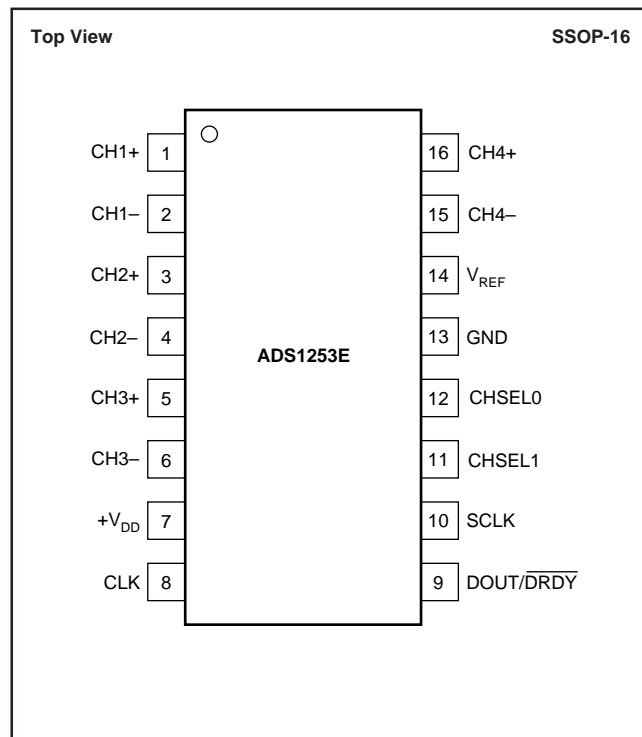
NOTE: (1) Applies to full-differential signals.

ELECTRICAL CHARACTERISTICS (Cont.)

All specifications at T_{MIN} to T_{MAX} , $V_{DD} = +5V$, $CLK = 8MHz$, and $V_{REF} = 4.096$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1253E			UNITS
		MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Level: V_{IH}		+4.0		$+V_{DD} + 0.3$	V
V_{IL}		-0.3		+0.8	V
V_{OH}		+4.5			V
V_{OL}				0.4	V
Input (SCLK, CLK, CHSEL0, CHSEL1) Hysteresis	$I_{OH} = -500\mu A$ $I_{OL} = 500\mu A$		0.6		V
Data Format		Offset Binary Two's Complement			
POWER-SUPPLY REQUIREMENTS					
Operation		+4.75	+5	+5.25	VDC
Quiescent Current			1.5	2	mA
Operating Power			7.5	10	mW
Power-Down Current			0.4	1	μA
TEMPERATURE RANGE					
Operating		-40		+85	$^{\circ}C$
Storage		-60		+100	$^{\circ}C$

PIN CONFIGURATION

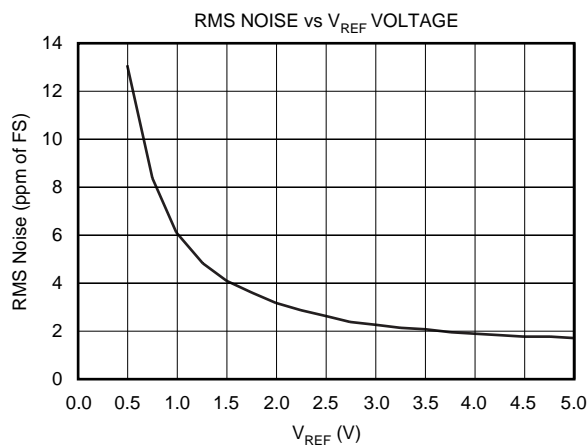
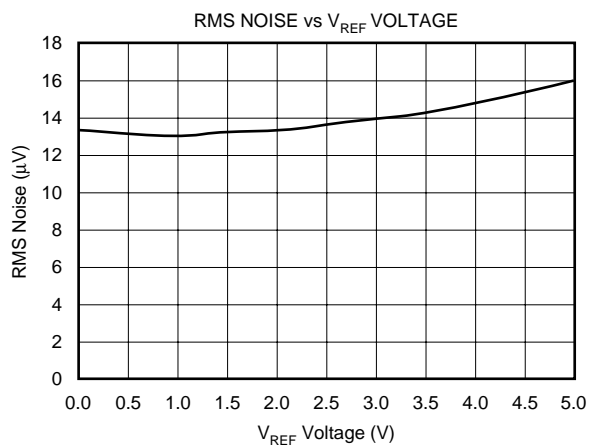
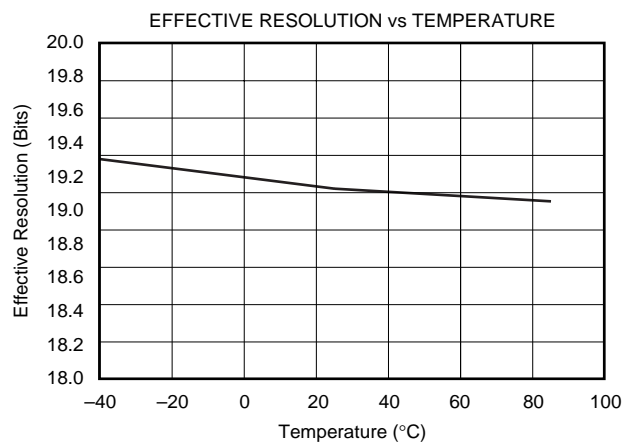
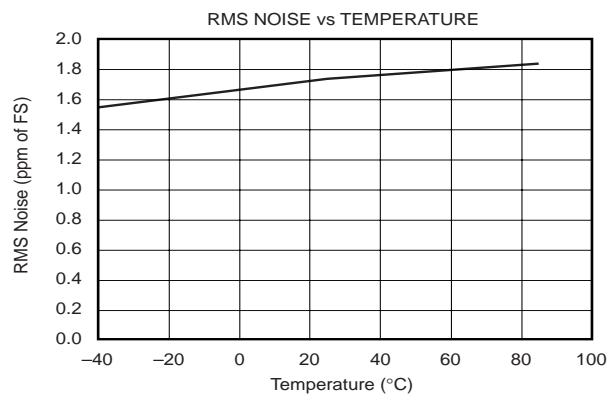
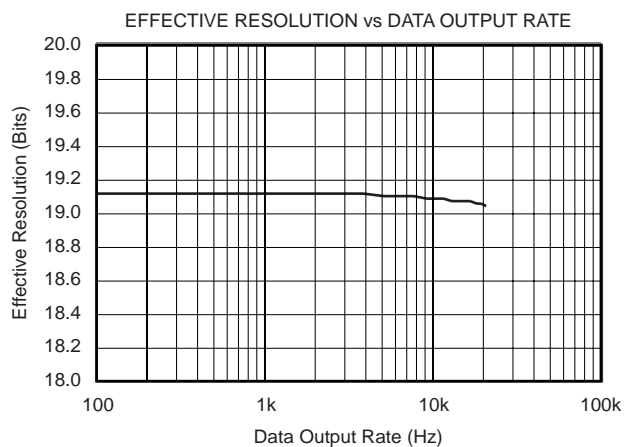
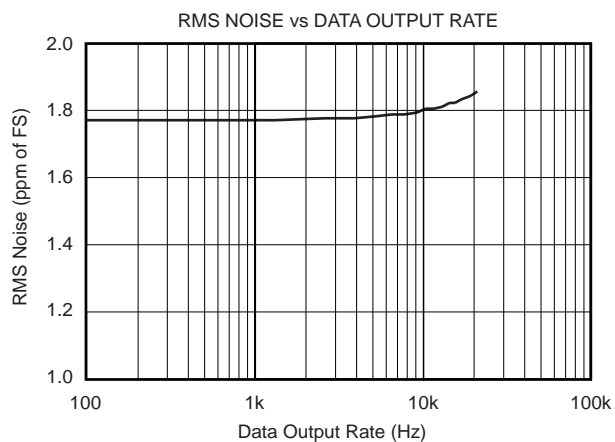


PIN DESCRIPTIONS

PIN	NAME	PIN DESCRIPTION
1	CH1+	Analog Input: Positive Input of the Differential Analog Input.
2	CH1-	Analog Input: Negative Input of the Differential Analog Input.
3	CH2+	Analog Input: Positive Input of the Differential Analog Input.
4	CH2-	Analog Input: Negative Input of the Differential Analog Input.
5	CH3+	Analog Input: Positive Input of the Differential Analog Input.
6	CH3-	Analog Input: Negative Input of the Differential Analog Input.
7	+V _{DD}	Input: Power Supply Voltage, +5V.
8	CLK	Digital Input: Device System Clock. The system clock is in the form of a CMOS-compatible clock. This is a Schmitt-Trigger input.
9	DOUT/DRDY	Digital Output: Serial Data Output/Data Ready. This output indicates that a new output word is available from the ADS1253 data output register. The serial data is clocked out of the serial data output shift register using SCLK.
10	SCLK	Digital Input: Serial Clock. The serial clock is in the form of a CMOS-compatible clock. The serial clock operates independently from the system clock, therefore, it is possible to run SCLK at a higher frequency than CLK. The normal state of SCLK is LOW. Holding SCLK HIGH will either initiate a modulator reset for synchronizing multiple converters or enter power-down mode. This is a Schmitt-Trigger input.
11	CHSEL1	Digital Input: Used to select analog input channel. This is a Schmitt-Trigger input.
12	CHSEL0	Digital Input: Used to select analog input channel. This is a Schmitt-Trigger input.
13	GND	Input: Ground.
14	V _{REF}	Analog Input: Reference Voltage Input.
15	CH4-	Analog Input: Negative Input of the Differential Analog Input.
16	CH4+	Analog Input: Positive Input of the Differential Analog Input.

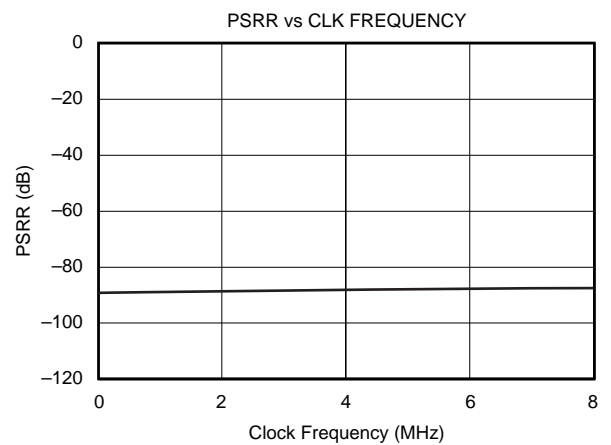
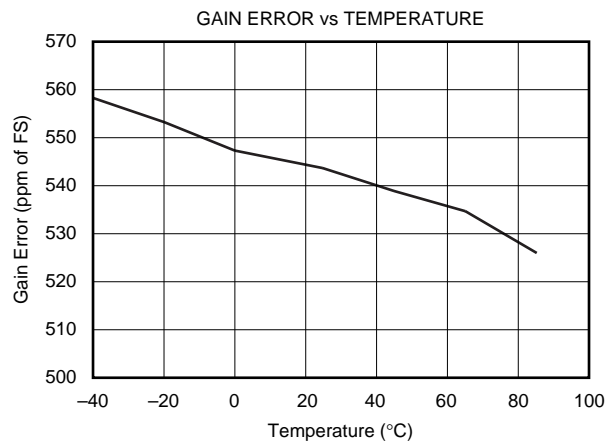
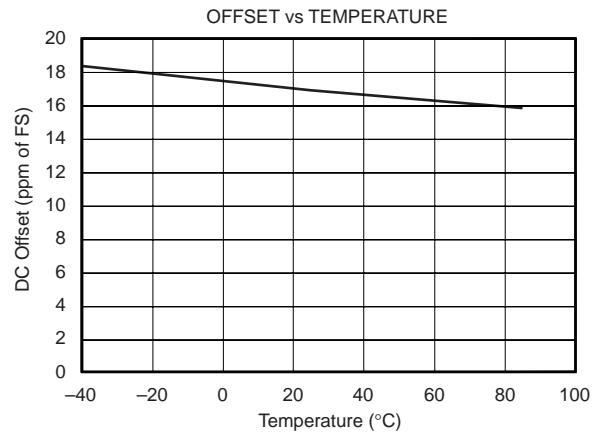
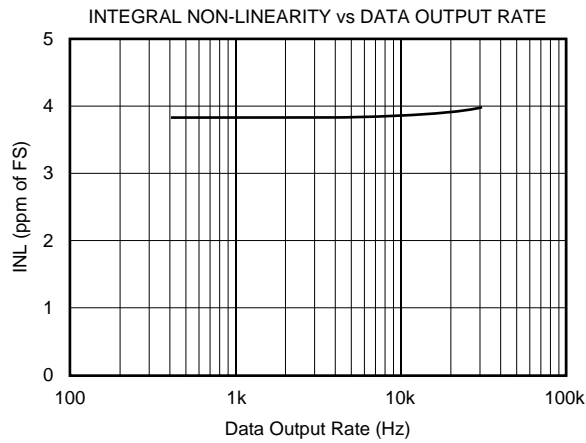
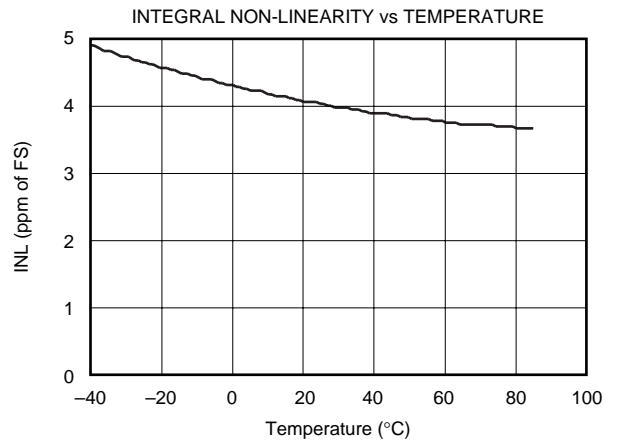
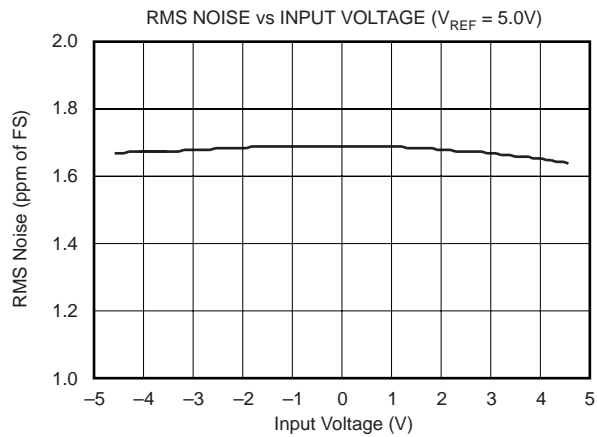
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $\text{CLK} = 8\text{MHz}$, and $V_{\text{REF}} = 4.096$, unless otherwise specified.



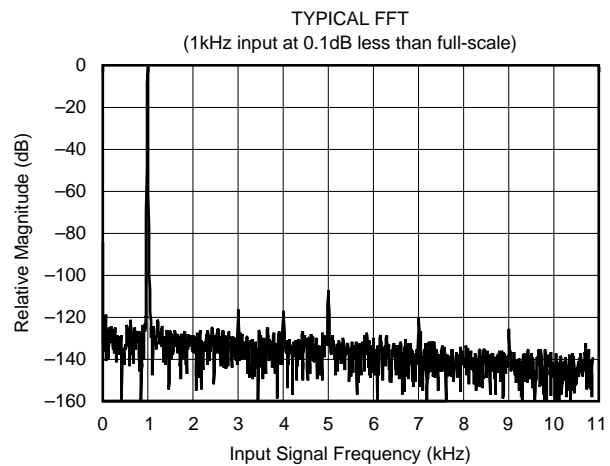
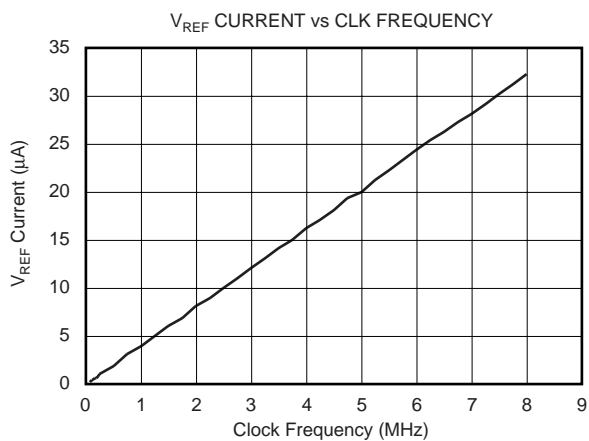
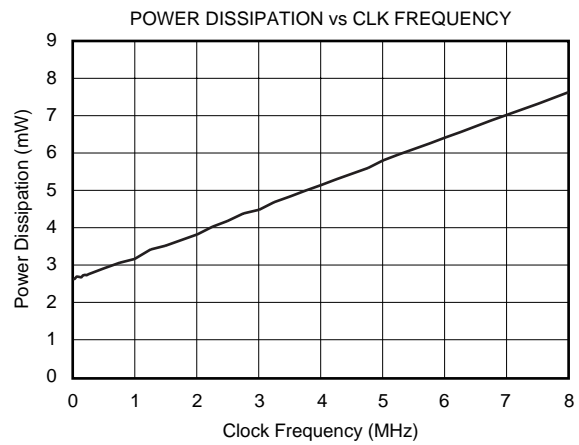
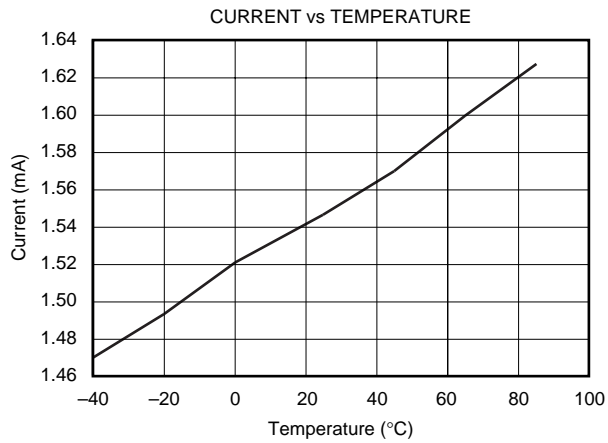
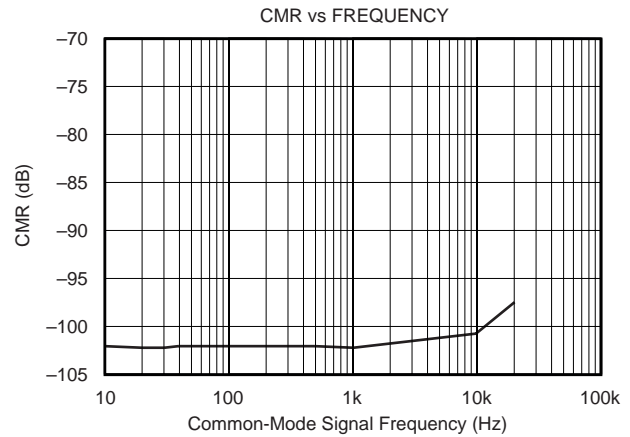
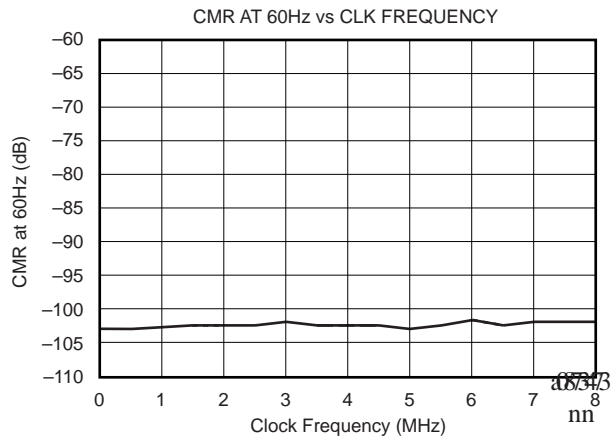
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $\text{CLK} = 8\text{MHz}$, and $V_{REF} = 4.096$, unless otherwise specified.



TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $\text{CLK} = 8\text{MHz}$, and $V_{REF} = 4.096$, unless otherwise specified.



THEORY OF OPERATION

The ADS1253 is a precision, high-dynamic range, 24-bit, delta-sigma, A/D converter capable of achieving very high-resolution digital results at high data rates. The analog-input signal is sampled at a rate determined by the frequency of the system clock (CLK). The sampled analog input is modulated by the delta-sigma A/D modulator, which is followed by a digital filter. A sinc⁵ digital low-pass filter processes the output of the delta-sigma modulator and writes the result into the data-output register. The DOUT/DRDY pin is pulled LOW, indicating that new data is available to be read by the external microcontroller/microprocessor. As shown in the block diagram, the main functional blocks of the ADS1253 are the fourth-order delta-sigma modulator, a digital filter, control logic, input multiplexer, and a serial interface. Each of these functional blocks is described below.

ANALOG INPUT

The ADS1253 contains a fully differential analog input. In order to provide low system noise, common-mode rejection of 98dB and excellent power-supply rejection, the design topology is based on a fully differential switched-capacitor architecture. The bipolar input voltage range is from -4.096 to +4.096V, when the reference input voltage equals +4.096V. The bipolar range is with respect to -V_{IN}, and not with respect to GND.

Figure 1 shows the basic input structure of the ADS1253. The impedance is directly related to the sampling frequency of the input capacitor which is set by the CLK rate. Higher CLK rates result in lower impedance, and lower CLK rates result in higher impedance.

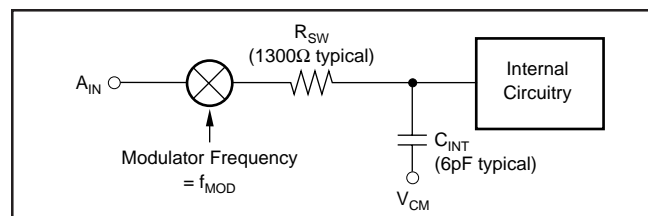


FIGURE 1. Analog-Input Structure.

The input impedance of the analog input changes with ADS1253 system clock frequency (CLK). The relationship is:

$$A_{IN} \text{ Impedance } (\Omega) = (8\text{MHz}/\text{CLK}) \cdot 125,000$$

With regard to the analog-input signal, the overall analog performance of the device is affected by three items: first, the input impedance can affect accuracy. If the source impedance of the input signal is significant, or if there is passive filtering prior to the ADS1253, a significant portion of the signal can be lost across this external impedance. The magnitude of the effect is dependent on the desired system performance.

Second, the current into or out of the analog inputs must be limited. Under no conditions should the current into or out of the analog inputs exceed 10mA.

Third, to prevent aliasing of the input signal, the analog-input signal must be band limited. The bandwidth of the A/D converter is a function of the system clock frequency. With a

system clock frequency of 8MHz, the data-output rate is 20.8kHz with a -3dB frequency of 4.24kHz. The -3dB frequency scales with the system clock frequency.

To guarantee the best linearity of the ADS1253, a fully differential signal is recommended, and the capacitance to ground must be equal on both sides.

INPUT MULTIPLEXER

The CHS1 and CHS0 pins are used to select the analog input channel as shown in Table I. The recommended method for changing channels is to change the channel after the conversion from the previous channel has been completed and read. When a channel is changed, internal logic senses the change on the falling edge of CLK and resets the conversion process. The conversion data from the new channel is valid on the first DRDY after the channel change.

When multiplexing inputs it is possible to achieve sample rates close to 4kHz. This is due to the fact that it requires five internal conversion cycles for the data to fully settle, the data also must be read before the channel is changed. The DRDY signal indicates a valid result after the five cycles have occurred

CHSEL1	CHSEL0	CHANNEL
0	0	CH1
0	1	CH2
1	0	CH3
1	1	CH4

TABLE I. Channel Selection.

BIPOLAR INPUT

Each of the differential inputs of the ADS1253 must stay between AGND - 0.3V and V_{DD} + 0.3V. With a reference voltage at less than half of V_{DD}, one input can be tied to the reference voltage, and the other input can range from 0 to 2 • V_{REF}. By using a three op amp circuit featuring a single amplifier and four external resistors, the ADS1253 can be configured to accept bipolar inputs referenced to ground. The conventional ±2.5V, ±5V, and ±10V input ranges can be interfaced to the ADS1253 using the resistor values shown in Figure 2.

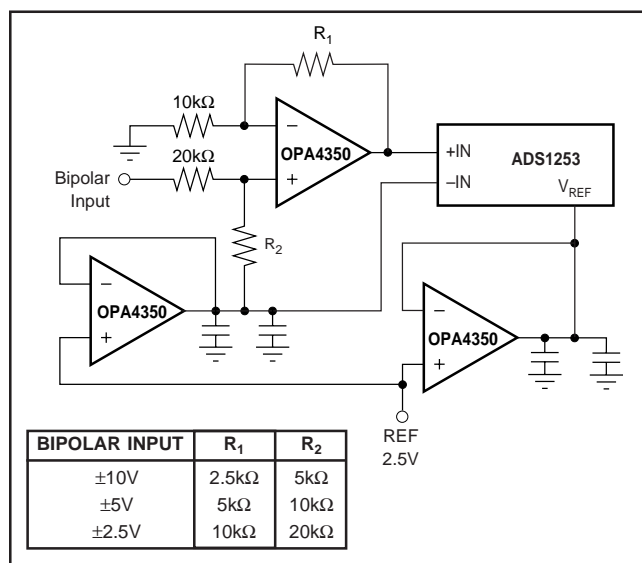


FIGURE 2. Level Shift Circuit for Bipolar Input Ranges.

DELTA-SIGMA MODULATOR

The ADS1253 operates from a nominal system clock frequency of 8MHz. The modulator frequency is fixed in relation to the system clock frequency. The system clock frequency is divided by 6 to derive the modulator frequency. Therefore, with a system clock frequency of 8MHz, the modulator frequency is 1.333MHz. Furthermore, the oversampling ratio of the modulator is fixed in relation to the modulator frequency. The oversampling ratio of the modulator is 64, and with the modulator frequency running at 1.333MHz, the data rate is 20.8kHz. Using a slower system clock frequency will result in a lower data output rate, as shown in Table II.

CLK (MHz)	DATA OUTPUT RATE (Hz)
8 ⁽¹⁾	20,833
7.372800 ⁽¹⁾	19,200
6.144000 ⁽¹⁾	16,000
6.000000 ⁽¹⁾	15,625
4.915200 ⁽¹⁾	12,800
3.686400 ⁽¹⁾	9,600
3.072000 ⁽¹⁾	8,000
2.457600 ⁽¹⁾	6,400
1.843200 ⁽¹⁾	4,800
0.921600	2,400
0.460800	1,200
0.384000	1,000
0.192000	500
0.038400	100
0.023040	60
0.019200	50
0.011520	30
0.009600	25
0.007680	20
0.006400	16.67
0.005760	15
0.004800	12.50
0.003840	10

NOTE: (1) Standard Clock Oscillator.

TABLE II. CLK Rate versus Data Output Rate.

REFERENCE INPUT

Reference input takes an average current of 32μA with a 8MHz system clock. This current will be proportional to the system clock. A buffered reference is recommended for ADS1253. The recommended reference circuit is shown in Figure 3.

Reference voltages higher than 4.096V will increase the full-scale range, while the absolute internal circuit noise of the converter remains the same. This will decrease the noise in terms of ppm of full scale, which increases the effective resolution (see the Typical Performance Curve “RMS Noise vs V_{REF} Voltage”).

DIGITAL FILTER

The digital filter of the ADS1253, referred to as a sinc⁵ filter, computes the digital result based on the most recent outputs from the delta-sigma modulator. At the most basic level, the digital filter can be thought of as simply averaging the modulator results in a weighted form and presenting this average as the digital output. The digital output rate, or data rate, scales directly with the system CLK frequency. This allows the data output rate to be changed over a very wide range (five orders of magnitude) by changing the system CLK frequency. However, it is important to note that the -3dB point of the filter is 0.2035 times the data output rate, so the data output rate should allow for sufficient margin to prevent attenuation of the signal of interest.

Since the conversion result is essentially an average, the data-output rate determines the location of the resulting notches in the digital filter (see Figure 4). Note that the first notch is located at the data-output rate frequency, and subsequent notches are located at integer multiples of the data-output rate to allow for rejection of not only the fundamental frequency, but also harmonic frequencies. In this manner, the data-output rate can be used to set specific notch frequencies in the digital filter response.

For example, if the rejection of power-line frequencies is desired, then the data-output rate can simply be set to the power-line frequency. For 50Hz rejection, the system CLK

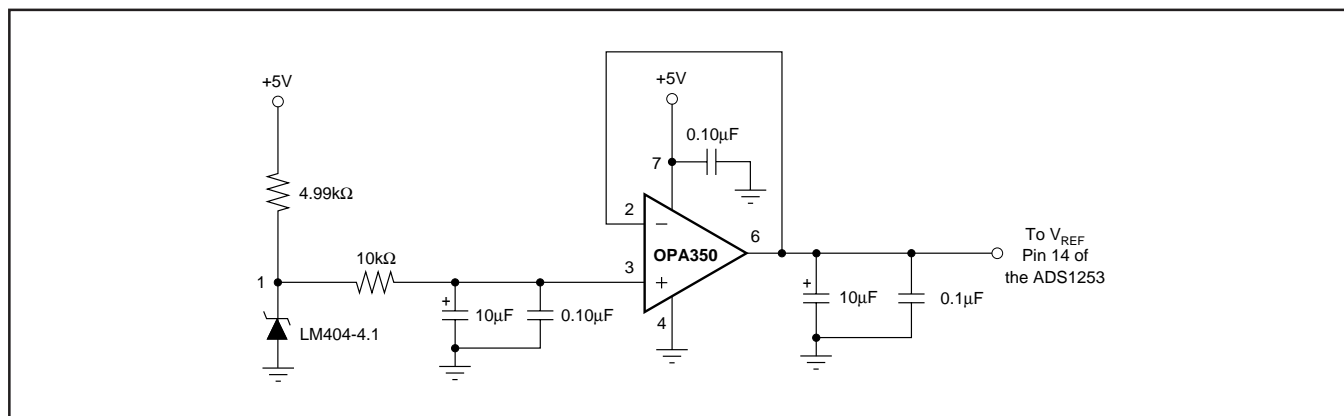


FIGURE 3. Recommended External Voltage Reference Circuit for Best Low-Noise Operation with the ADS1253.

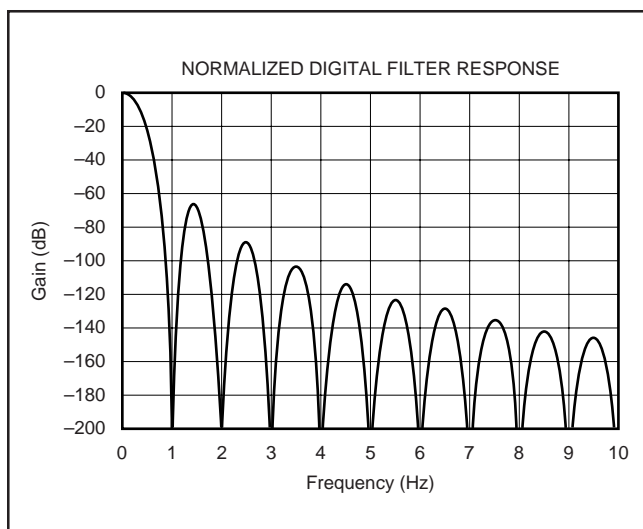


FIGURE 4. Normalized Digital Filter Response.

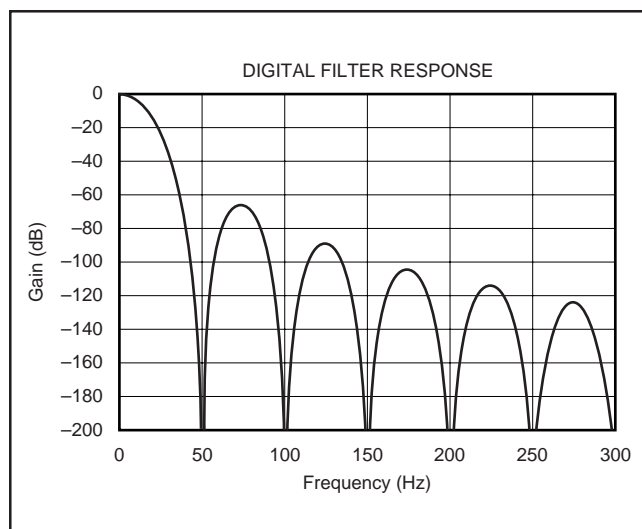


FIGURE 5. Digital Filter Response (50Hz).

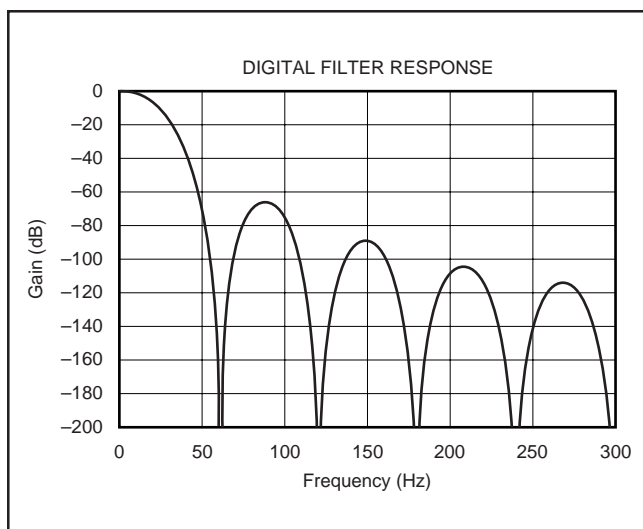


FIGURE 6. Digital Filter Response (60Hz).

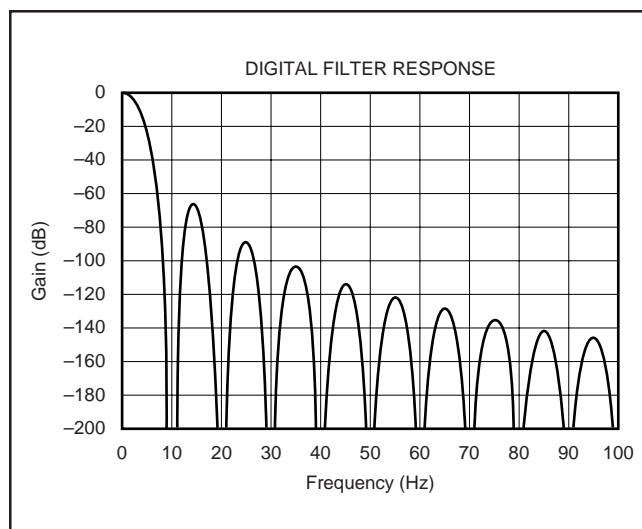


FIGURE 7. Digital Filter Response (10Hz).

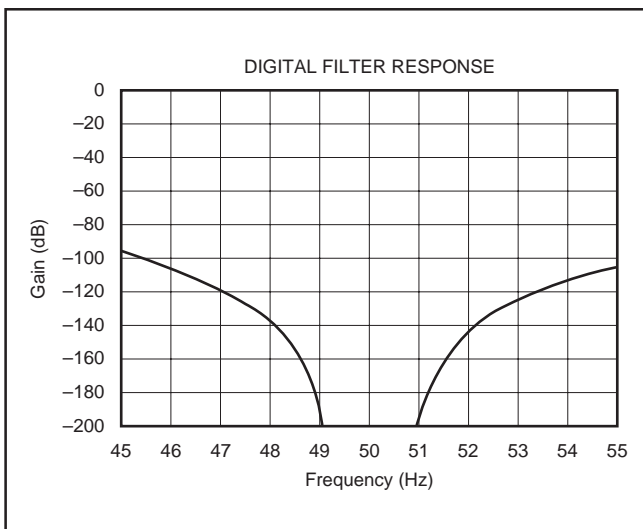


FIGURE 8. Expanded Digital Filter Response (50Hz with a 50Hz Data Output Rate).

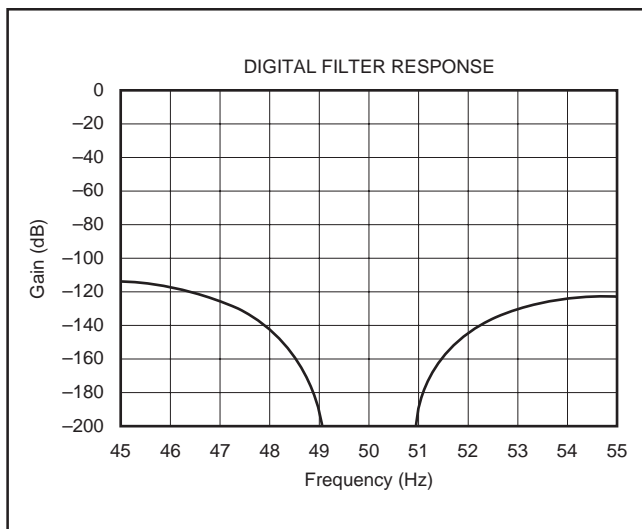


FIGURE 9. Expanded Digital Filter Response (50Hz with a 10Hz Data Output Rate).

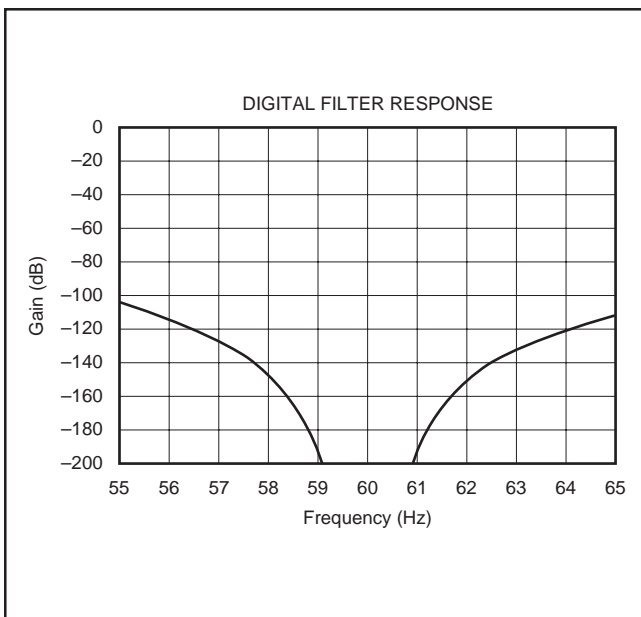


FIGURE 10. Expanded Digital Filter Response (60Hz with a 60Hz Data Output Rate).

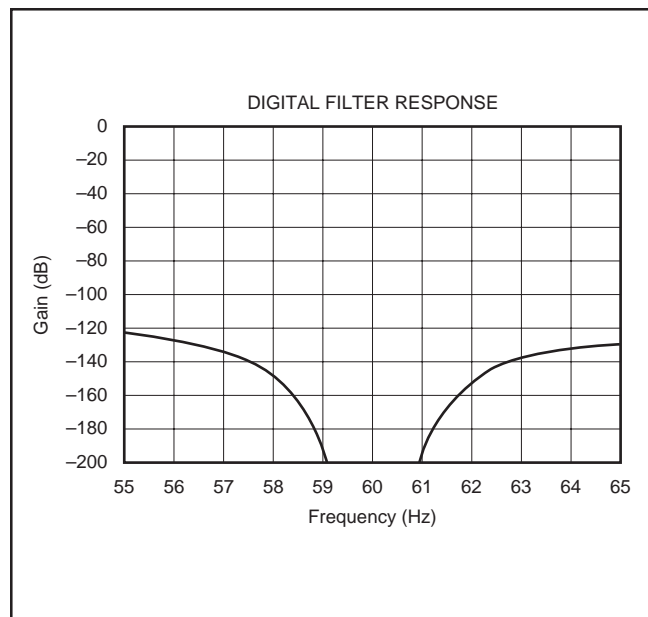


FIGURE 11. Expanded Digital Filter Response (60Hz with a 10Hz Data Output Rate).

frequency should be 19.200kHz, this will set the data-output rate to 50Hz (see Table I and Figure 5). For 60Hz rejection, the system CLK frequency should be 23.040kHz, this will set the data-output rate to 60Hz (see Table I and Figure 6). If both 50Hz and 60Hz rejection is required, then the system CLK should be 3.840kHz; this will set the data-output rate to 10Hz and reject both 50Hz and 60Hz (See Table I and Figure 7).

There is an additional benefit in using a lower data-output rate. It provides better rejection of signals in the frequency band of interest. For example, with a 50Hz data-output rate, a significant signal at 75Hz may alias back into the passband at 25Hz. This is due to the fact that rejection at 75Hz may only be 66dB in the stopband—frequencies higher than the first-notch frequency (see Figure 5). However, setting the data-output rate to 10Hz will provide 135dB rejection at 75Hz (see Figure 7). A similar benefit is gained at frequencies near the data-output rate (see Figures 8, 9, 10, and 11). For example, with a 50Hz data-output rate, rejection at 55Hz may only be 105dB (see Figure 8). However, with a 10Hz data-output rate, rejection at 55Hz will be 122dB (see Figure 9). If a slower data-output rate does not meet the system requirements, then the analog front end can be designed to provide the needed attenuation to prevent aliasing. Additionally, the data-output rate may be increased and additional digital filtering may be done in the processor or controller.

The digital filter is described by the following transfer function:

$$|H(f)| = \frac{\left| \sin\left(\frac{\pi \cdot f \cdot 64}{f_{\text{MOD}}}\right) \right|^5}{64 \cdot \sin\left(\frac{\pi \cdot f}{f_{\text{MOD}}}\right)}$$

or

$$H(z) = \left(\frac{1 - z^{-64}}{64 \cdot (1 - z^{-1})} \right)^5$$

The digital filter requires five conversions to fully settle. The modulator has an oversampling ratio of 64, therefore, it requires $5 \cdot 64$, or 320 modulator results, or clocks, to fully settle. Since the modulator clock is derived from the system clock (CLK) (modulator clock = CLK ÷ 6), the number of system clocks required for the digital filter to fully settle is $5 \cdot 64 \cdot 6$, or 1920 CLKs. This means that any significant step change at the analog input requires five full conversions to settle. However, if the step change at the analog input occurs asynchronously to the DOUT/DRDY pulse, six conversions are required to ensure full settling.

CONTROL LOGIC

The control logic is used for communications and control of the ADS1253.

Power-Up Sequence

Prior to power-up, all digital and analog-input pins must be LOW. At the time of power-up, these signal inputs can be biased to a voltage other than 0V, however, they should never exceed $+V_{DD}$.

Once the ADS1253 powers up, the DOUT/ $\overline{\text{DRDY}}$ line will pulse LOW on the first conversion for which the data is valid from the analog input signal.

DOUT/ $\overline{\text{DRDY}}$

The DOUT/ $\overline{\text{DRDY}}$ output signal alternates between two modes of operation. The first mode of operation is the Data Ready mode ($\overline{\text{DRDY}}$) to indicate that new data has been loaded into the data-output register and is ready to be read. The second mode of operation is the Data Output (DOUT) mode and is used to serially shift data out of the Data Output Register (DOR). See Figure 12 for the time domain partitioning of the $\overline{\text{DRDY}}$ and DOUT function.

See Figure 14 for the basic timing of DOUT/ $\overline{\text{DRDY}}$. During the time defined by t_2 , t_3 , and t_4 , the DOUT/ $\overline{\text{DRDY}}$ pin functions in $\overline{\text{DRDY}}$ mode. The state of the DOUT/ $\overline{\text{DRDY}}$ pin would be HIGH prior to the internal transfer of new data to the DOR. The result of the A/D conversion would be written to the DOR from MSB to LSB in the time defined by t_1 (see Figures 12 and 14). The DOUT/ $\overline{\text{DRDY}}$ line would then pulse LOW for the time defined by t_2 , and then pulse HIGH for the time defined by t_3 to indicate that new data was available to be read. At this point, the function of the DOUT/ $\overline{\text{DRDY}}$ pin would change to DOUT mode. Data would be shifted out on the pin after t_7 . The device communicating with the ADS1253 can provide SCLKs to the ADS1253 after the time defined by t_6 . The normal mode of reading data from the ADS1253 would be for the device reading the ADS1253 to latch the data on the rising edge of SCLK (since data is shifted out of the ADS1253 on the falling edge of SCLK). In order to retrieve valid data, the entire DOR must be read before the DOUT/ $\overline{\text{DRDY}}$ pin reverts back to $\overline{\text{DRDY}}$ mode.

If SCLKs were not provided to the ADS1253 during the DOUT mode, the MSB of the DOR would be present on the DOUT/ $\overline{\text{DRDY}}$ line until the time defined by t_4 . If an incomplete read of the ADS1253 took place while in DOUT mode (i.e., less than 24 SCLKs were provided), the state of the last bit read would be present on the DOUT/ $\overline{\text{DRDY}}$ line until the

time defined by t_4 . If more than 24 SCLKs were provided during DOUT mode, the DOUT/ $\overline{\text{DRDY}}$ line would stay LOW until the time defined by t_4 .

The internal data pointer for shifting data out on DOUT/ $\overline{\text{DRDY}}$ is reset on the falling edge of the time defined by t_1 and t_4 . This ensures that the first bit of data shifted out of the ADS1253 after $\overline{\text{DRDY}}$ mode is always the MSB of new data.

SYNCHRONIZING MULTIPLE CONVERTERS

The normal state of SCLK is LOW, however, by holding SCLK HIGH, multiple ADS1253s can be synchronized. This is accomplished by holding SCLK HIGH for at least four, but less than twenty, consecutive DOUT/ $\overline{\text{DRDY}}$ cycles (see Figure 15). After the ADS1253 circuitry detects that SCLK has been held HIGH for four consecutive DOUT/ $\overline{\text{DRDY}}$ cycles, the DOUT/ $\overline{\text{DRDY}}$ pin will pulse LOW for 3 CLK cycles and then be held HIGH, and the modulator will be held in a reset state. The modulator will be released from reset and synchronization will occur on the falling edge of SCLK. With multiple converters the falling edge transition of SCLK must occur simultaneously on all devices. It is important to note that prior to synchronization, the DOUT/ $\overline{\text{DRDY}}$ pulse of multiple ADS1253s in the system could have a difference in timing up to one $\overline{\text{DRDY}}$ period. Therefore to ensure synchronization, the SCLK should be held HIGH for at least five $\overline{\text{DRDY}}$ cycles. The first DOUT/ $\overline{\text{DRDY}}$ pulse after the falling edge of SCLK will occur at t_{14} . The first DOUT/ $\overline{\text{DRDY}}$ pulse indicates valid data.

POWER-DOWN MODE

The normal state of SCLK is LOW, however, by holding SCLK HIGH, the ADS1253 will enter power-down mode. This is accomplished by holding SCLK HIGH for at least twenty consecutive DOUT/ $\overline{\text{DRDY}}$ periods (see Figure 15). After the ADS1253 circuitry detects that SCLK has been held HIGH for four consecutive DOUT/ $\overline{\text{DRDY}}$ cycles, the DOUT/ $\overline{\text{DRDY}}$ pin will pulse LOW for 3 CLK cycles and then be held HIGH, and the modulator will be held in a reset state. If SCLK is held HIGH for an additional sixteen DOUT/ $\overline{\text{DRDY}}$ periods, the ADS1253 will enter power-down mode. The part will be released from power-down mode on the falling edge of SCLK. It is important to note that the DOUT/ $\overline{\text{DRDY}}$ pin will be held HIGH after four DOUT/ $\overline{\text{DRDY}}$ cycles, but power-down mode will not be entered for an additional sixteen DOUT/ $\overline{\text{DRDY}}$ periods. The first DOUT/ $\overline{\text{DRDY}}$ pulse after the falling edge of SCLK will occur at t_{16} and will indicate valid data. Subsequent DOUT/ $\overline{\text{DRDY}}$ pulses will occur normally.

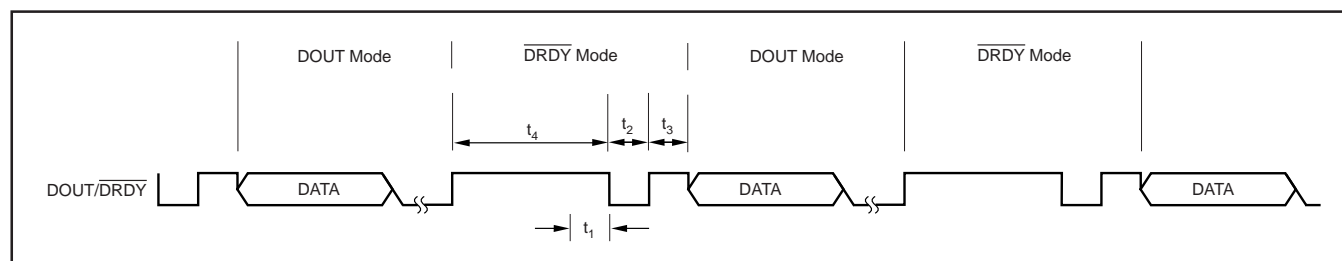


FIGURE 12. DOUT/ $\overline{\text{DRDY}}$ Partitioning.

SERIAL INTERFACE

The ADS1253 includes a simple serial interface which can be connected to microcontrollers and digital signal processors in a variety of ways. Communications with the ADS1253 can commence on the first detection of the $\overline{\text{DOUT}}/\overline{\text{DRDY}}$ pulse after power up.

It is important to note that the data from the ADS1253 is a 24-bit result transmitted MSB-first in Offset Two's Complement format, as shown in Table IV.

The data must be clocked out before the ADS1253 enters $\overline{\text{DRDY}}$ mode to ensure reception of valid data, as described in the $\overline{\text{DOUT}}/\overline{\text{DRDY}}$ section of this data sheet.

ISOLATION

The serial interface of the ADS1253 provides for simple isolation methods. The CLK signal can be local to the ADS1253, which then only requires two signals (SCLK, and $\overline{\text{DOUT}}/\overline{\text{DRDY}}$) to be used for isolated data acquisition. The channel select signals (CHS0, CHS1) will also need to be isolated unless a counter is used to auto multiplex the channels.

DIFFERENTIAL VOLTAGE INPUT	DIGITAL OUTPUT (HEX)
+Full Scale	7FFFFFFH
Zero	000000H
-Full Scale	800000H

TABLE IV. ADS1253 Data Format (Offset Two's Complement).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{OSC}	CLK Period	125			ns
t_{DRDY}	Conversion Cycle		$384 \cdot t_{\text{OSC}}$		ns
$\overline{\text{DRDY}}$ Mode	$\overline{\text{DRDY}}$ Mode		$36 \cdot t_{\text{OSC}}$		ns
$\overline{\text{DOUT}}$ Mode	$\overline{\text{DOUT}}$ Mode		$348 \cdot t_{\text{OSC}}$		ns
t_1	DOR Write Time		$6 \cdot t_{\text{OSC}}$		ns
t_2	$\overline{\text{DOUT}}/\overline{\text{DRDY}}$ LOW Time		$6 \cdot t_{\text{OSC}}$		ns
t_3	$\overline{\text{DOUT}}/\overline{\text{DRDY}}$ HIGH Time (Prior to Data Out)		$6 \cdot t_{\text{OSC}}$		ns
t_4	$\overline{\text{DOUT}}/\overline{\text{DRDY}}$ HIGH Time (Prior to Data Ready)		$24 \cdot t_{\text{OSC}}$		ns
t_5	Rising Edge of CLK to Falling Edge of $\overline{\text{DOUT}}/\overline{\text{DRDY}}$			30	ns
t_6	End of $\overline{\text{DRDY}}$ Mode to Rising Edge of First SCLK	30			ns
t_7	End of $\overline{\text{DRDY}}$ Mode to Data Valid (Propagation Delay)			30	ns
t_8	Falling Edge of SCLK to Data Valid (Hold Time)	5			ns
t_9	Falling Edge of SCLK to Next Data Out Valid (Propagation Delay)			30	ns
t_{10}	SCLK Setup Time for Synchronization or Power Down	30			ns
t_{11}	$\overline{\text{DOUT}}/\overline{\text{DRDY}}$ Pulse for Synchronization or Power Down		$3 \cdot t_{\text{OSC}}$		ns
t_{12}	Rising Edge of SCLK Until Start of Synchronization	$1537 \cdot \text{CLK}$		$7679 \cdot \text{CLK}$	ns
t_{13}	Synchronization Time	$0.5 \cdot \text{CLK}$		$6143.5 \cdot \text{CLK}$	ns
t_{14}	Falling Edge of CLK (After SCLK Goes Low) Until Start of $\overline{\text{DRDY}}$ Mode		$2042.5 \cdot t_{\text{OSC}}$		ns
t_{15}	Rising Edge of SCLK Until Start of Power Down	$7681 \cdot \text{CLK}$			ns
t_{16}	Falling Edge of CLK (After SCLK Goes Low) Until Start of $\overline{\text{DRDY}}$ Mode		$2318.5 \cdot t_{\text{OSC}}$		ns
t_{17}	Falling Edge of Last $\overline{\text{DOUT}}/\overline{\text{DRDY}}$ to Start of Power Down		$6144.5 \cdot t_{\text{OSC}}$		ns
t_{18}	$\overline{\text{DOUT}}/\overline{\text{DRDY}}$ High Time After Mux Change.		$2043.5 \cdot t_{\text{OSC}}$		ns

TABLE III. Digital Timing.

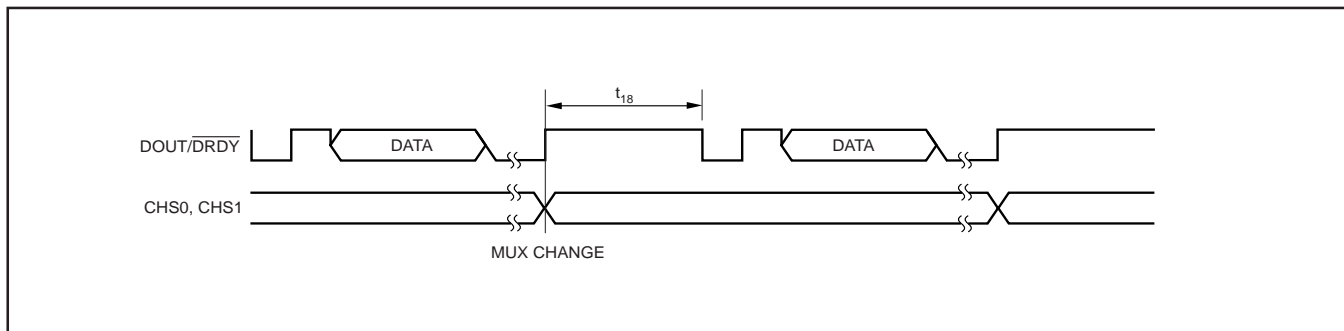


FIGURE 13. Multiplexer Operation.

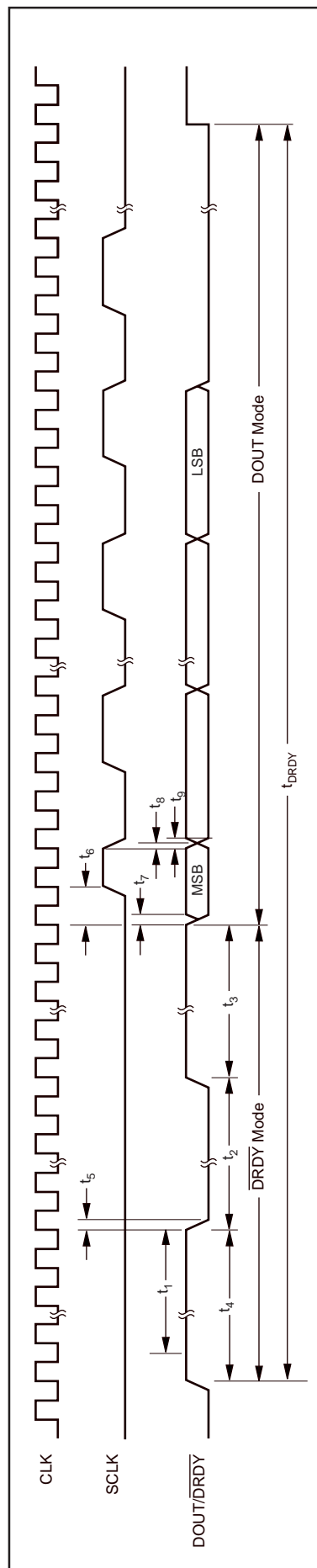


FIGURE 14. DOUT/DRDY Timing.

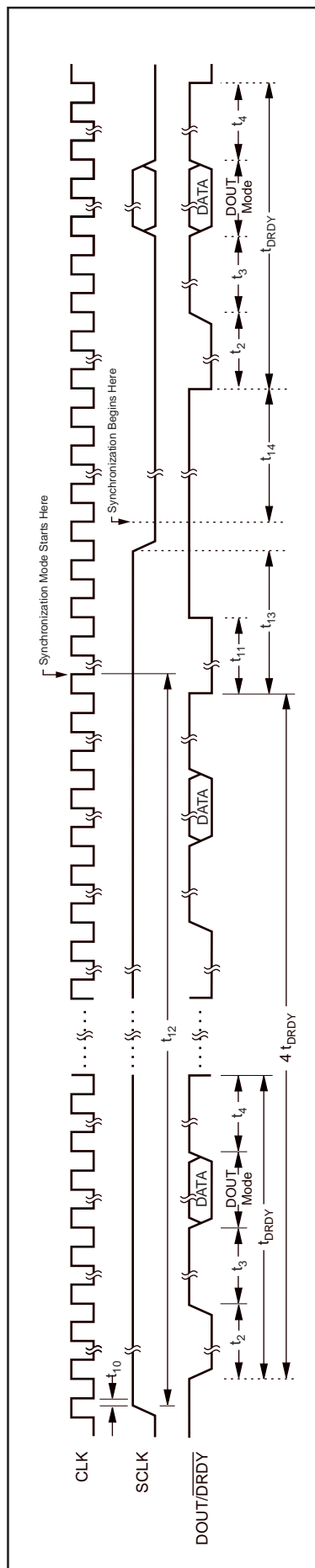


FIGURE 15. Synchronization Mode.

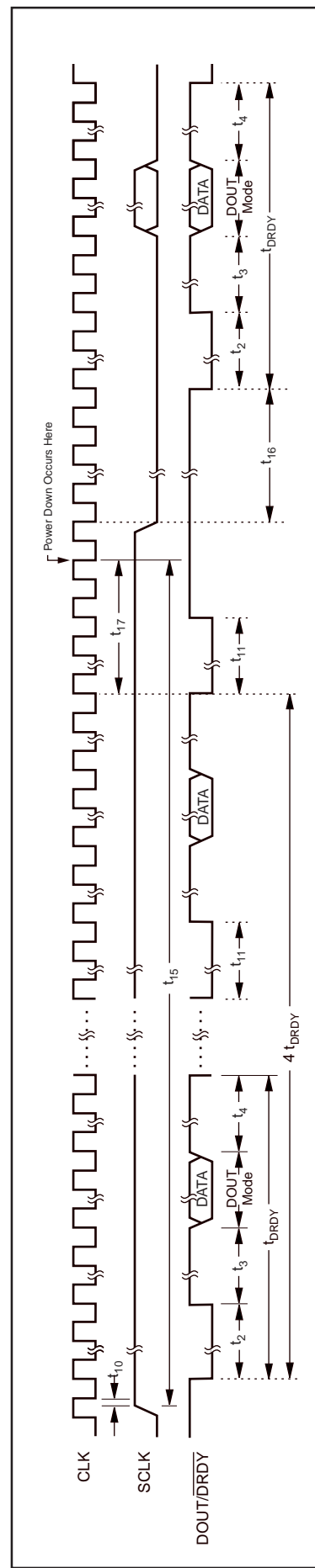


FIGURE 16. Power-Down Mode.

LAYOUT

POWER SUPPLY

The power supply should be well regulated and low noise. For designs requiring very high resolution from the ADS1253, power-supply rejection will be a concern. Avoid running digital lines under the device as they may couple noise onto the die. High-frequency noise can capacitively couple into the analog portion of the device and will alias back into the passband of the digital filter, affecting the conversion result. This clock noise will cause an offset error.

GROUNDING

The analog and digital sections of the system design should be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. GND should be connected to the analog ground plane, as well as all other analog grounds. Do not join the analog and digital ground planes on the board, but instead connect the two with a moderate signal trace. For multiple converters, connect the two ground planes at one location as central to all of the converters as possible. In some cases, experimentation may be required to find the best point to connect the two planes together. The printed circuit board can be designed to provide different analog/digital ground connections via short jumpers. The initial prototype can be used to establish which connection works best.

DECOUPLING

Good decoupling practices should be used for the ADS1253 and for all components in the design. All decoupling capacitors, and specifically the 0.1μF ceramic capacitors, should be placed as close as possible to the pin being decoupled. A 1μF to 10μF capacitor, in parallel with a 0.1μF ceramic capacitor, should be used to decouple V_{DD} to GND.

SYSTEM CONSIDERATIONS

The recommendations for power supplies and grounding will change depending on the requirements and specific design of the overall system. Achieving 24 bits of noise performance is a great deal more difficult than achieving 12 bits of noise performance. In general, a system can be broken up into four different stages:

- Analog Processing
- Analog Portion of the ADS1253
- Digital Portion of the ADS1253
- Digital Processing

For the simplest system consisting of minimal analog signal processing (basic filtering and Gain), a microcontroller, and one clock source, one can achieve high resolution by powering all components by a common power supply. In addition, all components could share a common ground plane. Thus, there would be no distinctions between “analog” power and ground, and “digital” power and ground. The layout should still include a power plane, a ground plane, and careful decoupling. In a more extreme case, the design

could include:

- Multiple ADS1253s
- Extensive Analog Signal Processing
- One or More Microcontrollers, Digital Signal Processors, or Microprocessors
- Many Different Clock Sources
- Interconnections to Various Other Systems

High resolution will be very difficult to achieve for this design. The approach would be to break the system into as many different parts as possible. For example, each ADS1253 may have its own “analog” processing front end.

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog-Input Differential Voltage—for an analog signal that is fully differential, the voltage range can be compared to that of an instrumentation amplifier. For example, if both analog inputs of the ADS1253 are at 2.048V, the differential voltage is 0V. If one analog input is at 0V and the other analog input is at 4.096V, then the differential voltage magnitude is 4.096V. This is the case regardless of which input is at 0V and which is at 4.096V. The digital-output result, however, is quite different. The analog-input differential voltage is given by the following equation:

$$+V_{IN} - (-V_{IN})$$

A positive digital output is produced whenever the analog-input differential voltage is positive, while a negative digital output is produced whenever the differential is negative. For example, a positive full-scale output is produced when the converter is configured with a 4.096V reference, and the analog-input differential is 4.096V. The negative full-scale output is produced when the differential voltage is -4.096V. In each case, the actual input voltages must remain within the -0.3V to + V_{DD} range.

Actual Analog-Input Voltage—the voltage at any one analog input relative to GND.

Full-Scale Range (FSR)—as with most ADC's, the full-scale range of the ADS1253 is defined as the “input” which produces the positive full-scale digital output minus the “input” which produces the negative full-scale digital output. For example, when the converter is configured with a 4.096V reference, the differential full-scale range is:

$$[4.096V \text{ (positive full scale)} - (-4.096V) \text{ (negative full scale)}] = 8.192V$$

Least Significant Bit (LSB) Weight—this is the theoretical amount of voltage that the differential voltage at the analog input would have to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full-Scale Range}}{2^N - 1} = \frac{2 \cdot V_{REF}}{2^N - 1}$$

where N is the number of bits in the digital output.

Conversion Cycle—as used here, a conversion cycle refers to the time period between DOUT/DRDY pulses.

Effective Resolution (ER)—of the ADS1253 in a particular configuration can be expressed in two different units: bits rms (referenced to output) and μVrms (referenced to input). Computed directly from the converter's output data, each is a statistical calculation based on a given number of results. Noise occurs randomly; the rms value represents a statistical measure which is one standard deviation. The ER in bits can be computed as follows:

$$\text{ER in bits rms} = \frac{20 \cdot \log \left(\frac{2 \cdot V_{\text{REF}}}{V_{\text{rms noise}}} \right)}{6.02}$$

The $2 \cdot V_{\text{REF}}$ figure in each calculation represents the full-scale range of the ADS1253. This means that both units are absolute expressions of resolution—the performance in different configurations can be directly compared, regardless of the units.

f_{MOD} —frequency of the modulator and the frequency the input is sampled.

$$f_{\text{MOD}} = \frac{\text{CLK Frequency}}{6}$$

f_{DATA} —Data output rate.

$$f_{\text{DATA}} = \frac{f_{\text{MOD}}}{64} = \frac{\text{CLK Frequency}}{384}$$

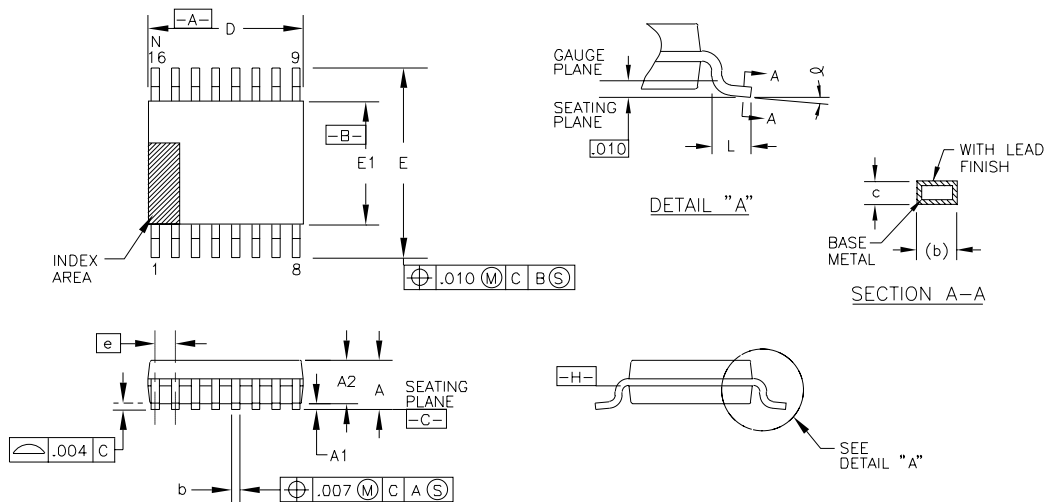
Noise Reduction—for random noise, the ER can be improved with averaging. The result is the reduction in noise by the factor \sqrt{N} , where N is the number of averages, as shown in Table V. This can be used to achieve true 24-bit performance at a lower data rate. To achieve 24 bits of resolution, more than 24 bits must be accumulated. A 36-bit accumulator is required to achieve an ER of 24 bits. The following uses $V_{\text{REF}} = 4.096\text{V}$, with the ADS1253 outputting data at 20kHz, a 4096 point average will take 204.8ms. The benefits of averaging will be degraded if the input signal drifts during that 200ms.

N (Number of Averages)	NOISE REDUCTION FACTOR	ER IN V_{rms}	ER IN BITS rms
1	1	14.6 μV	19.1
2	1.414	10.3 μV	19.6
4	2	7.3 μV	20.1
8	2.82	5.16 μV	20.6
16	4	3.65 μV	21.1
32	5.66	2.58 μV	21.6
64	8	1.83 μV	22.1
128	11.3	1.29 μV	22.6
256	16	0.91 μV	23.1
512	22.6	0.65 μV	23.6
1024	32	0.46 μV	24.1
2048	45.25	0.32 μV	24.6
4096	64	0.23 μV	25.1

TABLE V. Averaging.

PACKAGE DRAWING

Package Number 322 - 16-Lead SSOP, .150 Wide



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
A2	.055	.059	1.40	1.50	
b	.008	.012	0.20	0.30	3.7
c	.007	.010	0.19	0.25	7
D	.188	.197	4.78	5.00	2
E	.228	.244	5.80	6.20	
E1	.149	.157	3.78	4.00	2
e	.025	BASIC	.635	BASIC	
L	.016	.050	0.40	1.27	4
N	16		16		5
α	0°	8°	0°	8°	

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
- D AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT DATUM PLANE $-H-$ MOLD PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .008 INCH (0.20mm) PER SIDE.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13mm) TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION.

- DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN .003 INCH (0.07mm) AT LEAST MATERIAL CONDITION.
- DIMENSION L TO BE DETERMINED AT SEATING PLANE-DATUM "C".
- "N" IS THE NUMBER OF TERMINAL POSITIONS.
- A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSSHATCHED AREA.
- DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .004 AND .010 INCH FROM THE LEAD TIP.

PACKAGE NUMBER: ZZ322 REV.: B
JEDEC NUMBER: MO-137-AB
WITH THE EXCEPTION OF DIM. D, E1

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
ADS1253E	ACTIVE	SSOP	DBQ	16	100
ADS1253E/2K5	ACTIVE	SSOP	DBQ	16	2500

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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