5-Pin μP Reset Circuits with Watchdog Timer and Manual Reset

FEATURES

- Precision Power Supply Monitoring with ± 1.5% Accuracy
- Low Quiescent Current: 3 μA max.
- Low Threshold Voltage Temperature Coefficient: 100 ppm max.
- Guaranteed $\overline{\text{RESET}}$ Valid Dow to V_{CC} = 1 V
- Seven Reset Threshold Options
- Small SOT23-5 Packages
- No External Components
- Power Supply Transient Immunity

APPLICATIONS

- Portable Intelligent Electronics
- Computers and Controllers
- Automotive Electronics
- Critical μP/μC Power Supply Monitoring

DESCRIPTION

The SiP823/SiP824/SiP825 series are μProcessor supervisory circuits in a 5-pin SOT23 package, that combine the functions of power supply and μProcessor monitoring.

If the power supply voltage drops, or has been, below a safe level or the μProcessor shows signs of problematic inactivity, the circuit will generate a reset signal at it's output.

The SiP823 and SiP825 have an input to accommodate manual reset.

Seven pre-programmed reset threshold voltage levels are available as standard options.

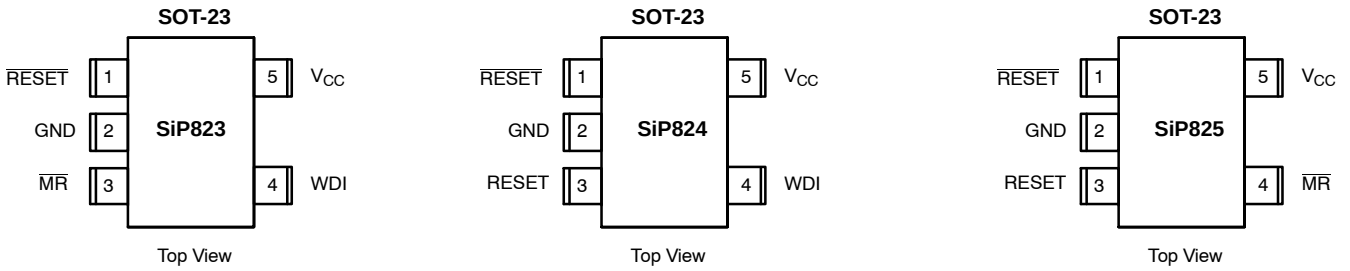
Specially configured options are available upon request, allowing for further customization of reset voltage, reset time-out, and watchdog time-out periods.

The SiP823 has a reset output that is "active low" and the SiP824 and SiP825 have complementary outputs for both "active high" and "active low" resets. Both output drives are push/pull configurations.

Space saving SOT23-5 packages and low quiescent current make this family of products ideally suited for portable battery operated equipment.

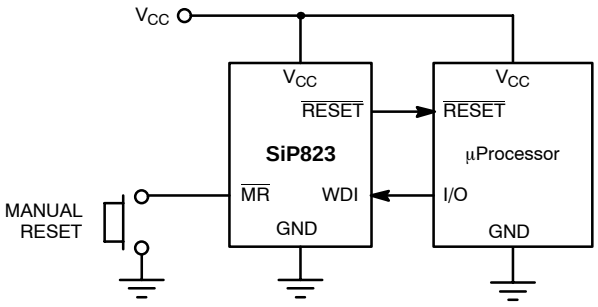
These circuits fully ignore fast negative V_{CC} transients and have valid reset output signals with power supply levels down to 1 V.

PACKAGING AND PIN DEFINITION

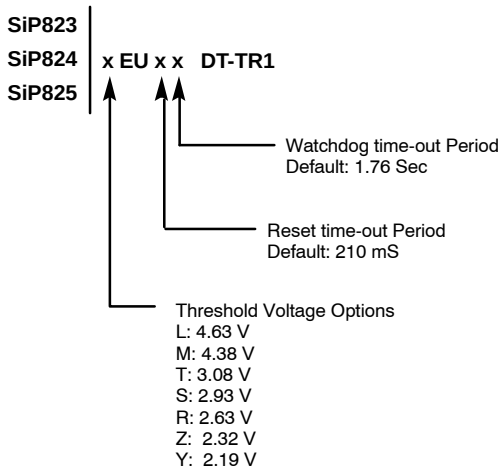


See page 2 for ordering and marking information.

TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION



Please contact your local Vishay Semiconductor Sales Office for information on customization of reset voltage, reset time-out, and watchdog time-out options.

MARKING INFORMATION					
SiP823		SiP824		SiP825	
SiP823LEU	AAxxx	SiP824LEU	AIxxx	SiP825LEU	ARxxx
SiP823MEU	ABxxx	SiP824MEU	AKxxx	SiP825MEU	ASxxx
SiP823TEU	ACxxx	SiP824TEU	ALxxx	SiP825TEU	ATxxx
SiP823SEU	ADxxx	SiP824SEU	AMxxx	SiP825SEU	AVxxx
SiP823REU	AExxx	SiP824REU	ANxxx	SiP825REU	AWxxx
SiP823ZEU	AGxxx	SiP824ZEU	AOxxx	SiP825ZEU	AXxxx
SiP823YEU	AHxxx	SiP824YEU	APxxx	SiP825YEU	AYxxx

Last two characters denote date code.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Supply Voltage	V_{CC}	−0.3 to 6.0	V
All Other Pins	V_{MAX}	−0.3 to (V_{CC} + 0.3)	
Input/Output Current, All Pins	$I_{IN(max)}$	20	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	
Junction Temperature Range	T_J	−40 to 125	
Power Dissipation ($T_A \leq 70°C$) SOT-23 (Derate 4 mW/°C above 70°C)	P_D	310	mW

Notes
a. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified T_A = −40°C to 85°C, Typical Values @ T_A = 25°C	Limits Min[a]	Typ[b]	Max[a]	Unit
Supply Voltage	V_{CC}		1		5.5	V
Supply Current (No Load)	I_{CC}	$V_{CC} = V_{TH}$ + 10%			10.0	µA
		T_A = 25°C			3.0	
RESET Threshold	V_{TH}	T_A = 25°C	V_{TH} −1.5%		V_{TH} 1.5%	V
Threshold Hysteresis	$V_{TH(hys)}$			0.4		$\%V_{TH}$
RESET Threshold Temperature Coefficient				40		PPM/°C
$\overline{RESET}$ Output Voltage	V_{OL}	Sip82_L/M/J: $V_{CC} < V_{TH}$, I_{SINK} = 1.2 mA			0.5	V
		Sip82_R/S/T/Y/Z: $V_{CC} < V_{TH}$, I_{SINK} = 0.5 mA			0.4	
	V_{OH}	$V_{CC} > V_{TH}$, I_{SOURCE} = 0.5 mA	0.8 V_{CC}			
RESET Output Voltage	V_{OL}	Sip82_L/M/J: $V_{CC} > V_{TH}$, I_{SINK} = 1.2 mA			0.5	
		Sip82_R/S/T/Y/Z: $V_{CC} > V_{TH}$, I_{SINK} = 0.5 mA			0.4	
	V_{OH}	$V_{CC} < V_{TH}$, I_{SOURCE} = 0.5 mA	0.8 V_{CC}			
V_{CC} to $\overline{RESET}$ Delay	T_{D1}	$V_{CC} = V_{TH}$ − 100 mV		40		µS
RESET Time-out Period	T_{D2}		140	210	280	mS
Watchdog Input (SiP823/SiP824)						
Watchdog Time-out Period	t_{WD}		1.12	1.76	2.40	S
W_{D1} Pulse Width	t_{WDI}	V_{IL} = 0.4 V, V_{IH} = 0.8 V_{CC}	50			nS
W_{DI} Input Voltage[c]	V_{IL}	$V_{CC} = V_{TH}$ + 20%			0.7	V
	V_{IH}		0.8 V_{CC}			
W_{DI} Input Current	I_{IL}	W_{DI} = 0 V	−15	−8		µA
	I_{IH}	$W_{DI} = V_{CC}$ = 5 V		8	15	
Manual Reset Input (SiP823/SiP825)						
$\overline{MR}$ Pulse Width	t_{MR}		1.0			µS
$\overline{MR}$ Input Voltage	V_{IL}	$V_{CC} = V_{TH}$ + 20%			0.7	V
	V_{IH}		0.8 V_{CC}			
$\overline{MR}$ Noise Immunity (Pulse Width with No RESET)				100		nS
$\overline{MR}$ to RESET Delay	t_{MR}			500		
MR Pull-Up Resistance			80		120	kΩ

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
c. W_{DI} is internally serviced within the watchdog period if W_{DI} is left unconnected.

PIN DESCRIPTION

SiP823	SiP824	SiP825	Name	Description
1	1	1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ is active low. This pin has a push/pull output.
2	2	2	GND	Ground
N/A	3	3	RESET	RESET is active high. This pin has a push/pull output.
3	N/A	4	$\overline{\text{MR}}$	Manual RESET. Active low. Pulling this pin low forces a RESET. After a low to high transition RESET remains asserted for exactly one RESET timed period. This pin is internally pulled high. If this function is unused it can be left open or tied to V_{CC}.
4	4	N/A	W_{DI}	Watchdog Input. Any transition on this pin will RESET the watchdog timer. If this pin remains high or low for longer than the watchdog interval, a RESET is asserted. Float or tristate this pin to disable the watchdog feature.
5	5	5	V_{CC}	Positive power supply. A RESET is asserted after this voltage drops below a predetermined level. After V_{CC} rises above that level, RESET remains asserted until the end of the RESET time-out period.

TIMING DIAGRAMS

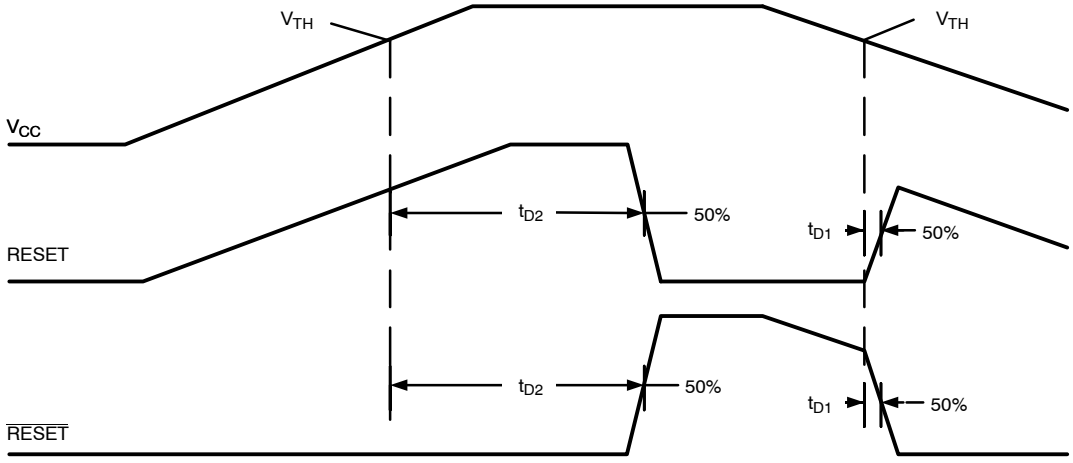


Figure 1. RESET Timing Diagram

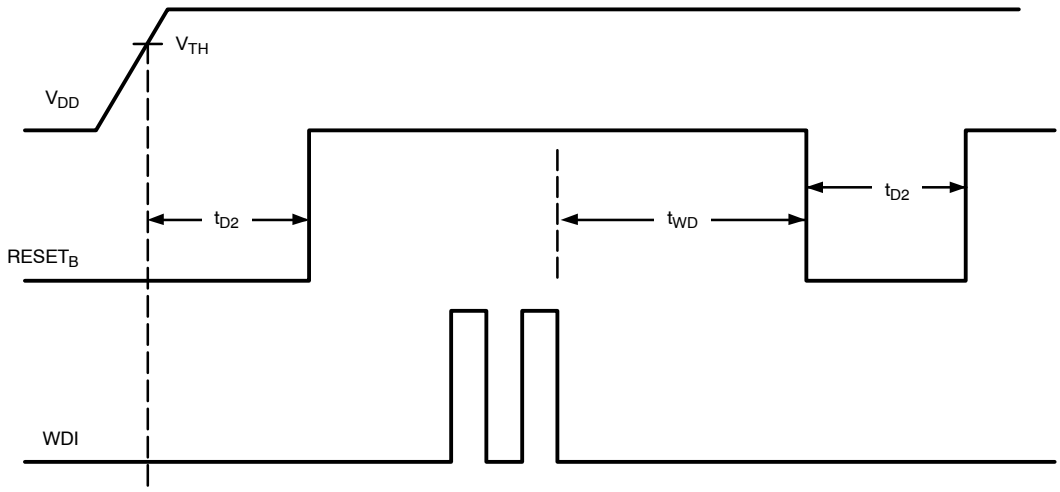


Figure 2. Watchdog Timing Diagram

DETAILED DESCRIPTION

An active signal on a microprocessor (μP) RESET input starts the μP in a know state. The SiP823/SiP824/SiP825 μP supervisory circuits assert a RESET signal to prevent code execution errors during power-up, power-down and brown-out conditions.

The SiP823/SiP824/SiP825 also monitors the μP's health by checking for problematic inactivity at its $W_{DI\,i}$ input.

RESET Output

A RESET will be asserted for the specified RESET time-out period (t_{D2}), if any of three conditions are present:

1) V_{CC} drops below the threshold voltage (V_{TH})
2) The $\overline{MR}$ pin is pulled low
3) The watchdog timer does not detect a transition within the watchdog interval (t_{WD}) and the watchdog input is not left floating.

The RESET output will remain asserted for the specified time-out period (t_{D2}) after:

1) V_{CC} rises above the RESET threshold (V_{TH})
2) $\overline{MR}$ goes high.

Manual RESET Input

μP based products often require a manual RESET capability, which can be activated by manual intervention or external logic circuitry.

A logic low at the $\overline{MR}$ pin of the SiP823/SiP824/SiP825 asserts a RESET signal. RESET remains asserted while $\overline{MR}$ is low and for a period (t_{D2}) after it returns high.

MR has an internal 100-kΩ pull-up resistor, so it can be left floating when not activated. This input can be driven with CMOS logic levels or with open drain devices. The input is internally de-bounced to reject fast input transients.

Watchdog Input (SiP823/SiP824)

The SiP823/SiP824 have a watchdog input (WDI), that monitors the μP's activity. If the μP does not toggle the watchdog input within the watchdog time-out period (t_{WD}), RESET is asserted. The internal RESET timer is cleared by either a RESET pulse or by toggling WDI.

WDI detects pulses as short as 50 nS. While RESET is asserted, the timer remains cleared. As soon as RESET is released the timer starts counting (Figure 2).

The watchdog timer can be disabled by leaving WDI open or by three stating the connected driver. As soon as the WDI input is driven either high or low, the watchdog function resumes with the watchdog timer set to zero.

WDI Input Current

The watchdog input pin (WDI) typically sources or sinks 8 μA when driven high or low.

As a result, the power dissipation at the WDI input is independent of duty cycle. When the WDI pin is left floating or tri-stated, the power supply current is less than 3 μA.

Transient Rejection

The SiP823/SiP824/SiP825 family has good immunity for negative going transients on the V_{CC} line.

The smaller the duration of the transient, the larger the amplitude can be without triggering RESET.

The "Transient Rejection" graph below shows the relation between transient amplitude and allowable transient duration, without triggering RESET.

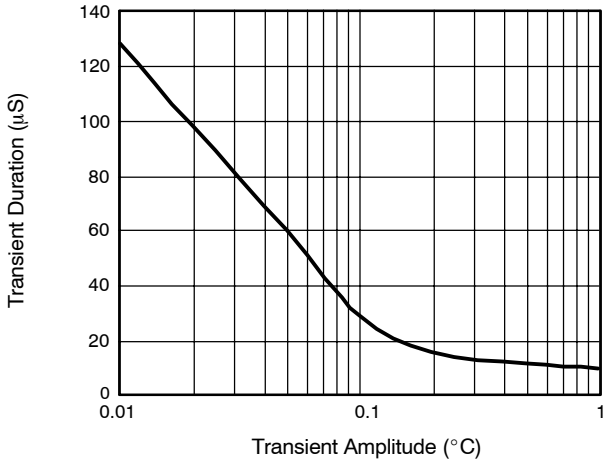
The value on the horizontal scale represents the portion of the amplitude of the transient that is exceeding the V_{TH} level.

RESET Output State at Low V_{DD}

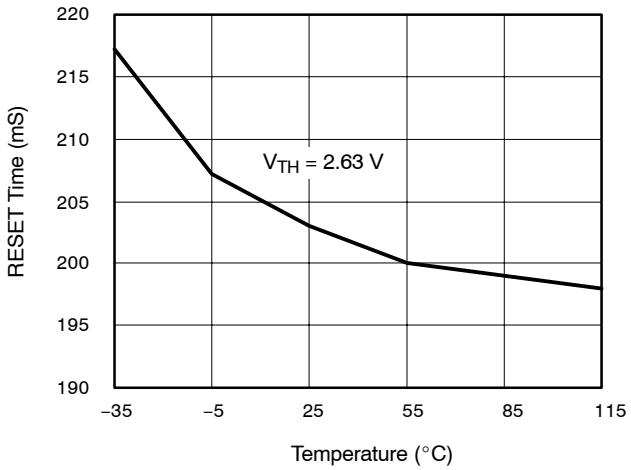
With V_{CC} voltage on the level of MOS transistor thresholds (<1.0 V), the RESET output of the SiP823/SiP824/SiP825 may become undefined. For outputs that are active low ($\overline{RESET}$), a resistor placed between $\overline{RESET}$ and GND on the order of 100 kΩ will ensure that the RESET output stays low when the V_{CC} drops below the MOS transistor threshold. In a like manner, a resistor placed between RESET and V_{CC} will ensure the correct state for active high RESET outputs.

TYPICAL CHARACTERISTICS (T_A = 25°C Unless Otherwise Noted)

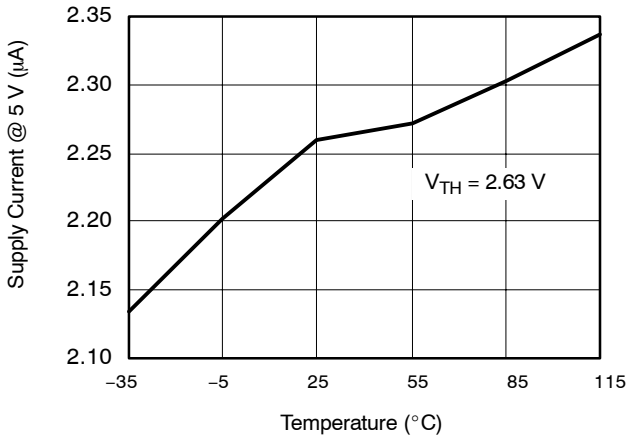
Transient Rejection



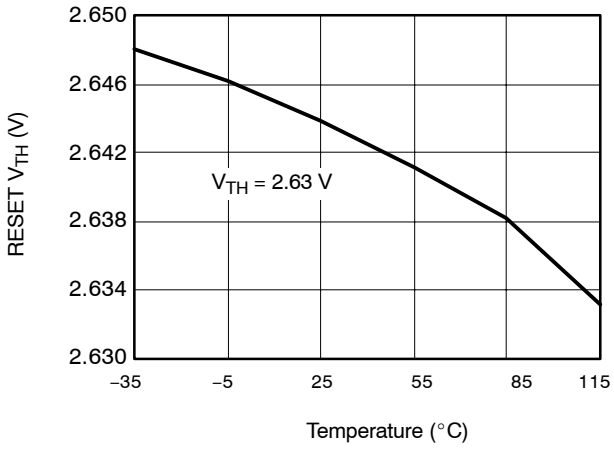
RESET Time (t_{D2}) vs. Temperature



I_{CC} vs. Temperature



RESET V_{TH} vs. Temperature



$\overline{\text{RESET}}$ V_{OL} vs. Temperature