

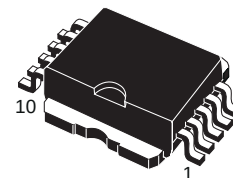
DOUBLE CHANNEL HIGH SIDE SOLID STATE RELAY

TYPE	$R_{DS(on)}$	I_{lim}	V_{CC}
VND600SP	30m Ω	25A	36 V

- DC SHORT CIRCUIT CURRENT: 25 A
- CMOS COMPATIBLE INPUTS
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE AND OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST:
 - LOSS OF GROUND AND LOSS OF V_{CC}
- REVERSE BATTERY PROTECTION (*)

DESCRIPTION

The VND600SP is a monolithic device made using STMicroelectronics VIPower M0-3 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637



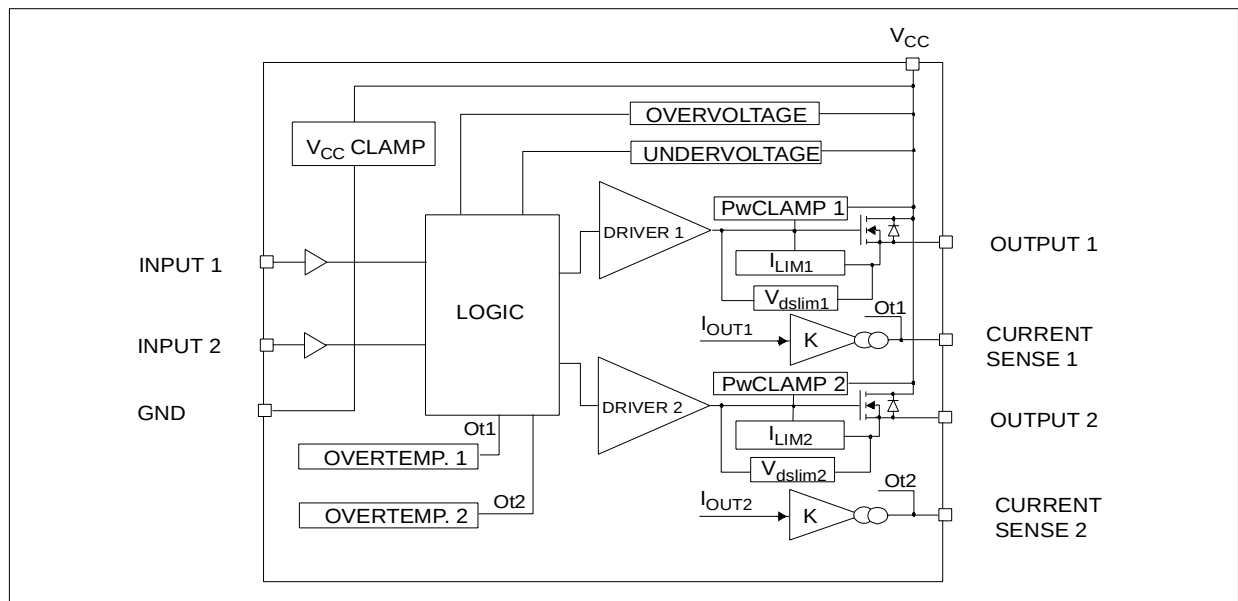
PowerSO-10™

ORDER CODES

PACKAGE	TUBE	T&R
PowerSO-10™	VND600SP	VND600SP13TR

transient compatibility table). This device has two channels in high side configuration; each channel has an analog sense output on which the sensing current is proportional (according to a known ratio) to the corresponding load current. Built-in thermal shut-down and outputs current limitation protect the chip from over temperature and short circuit. Device turns off in case of ground pin disconnection.

BLOCK DIAGRAM



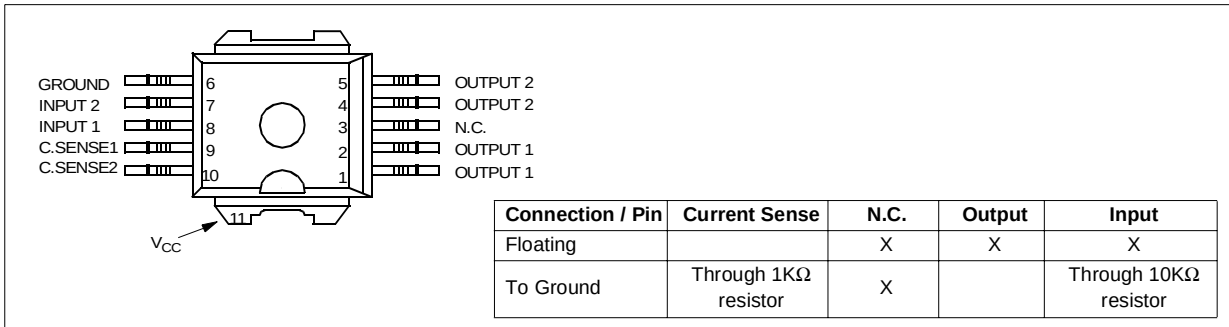
(*) See application schematic at page 8

Rev. 2

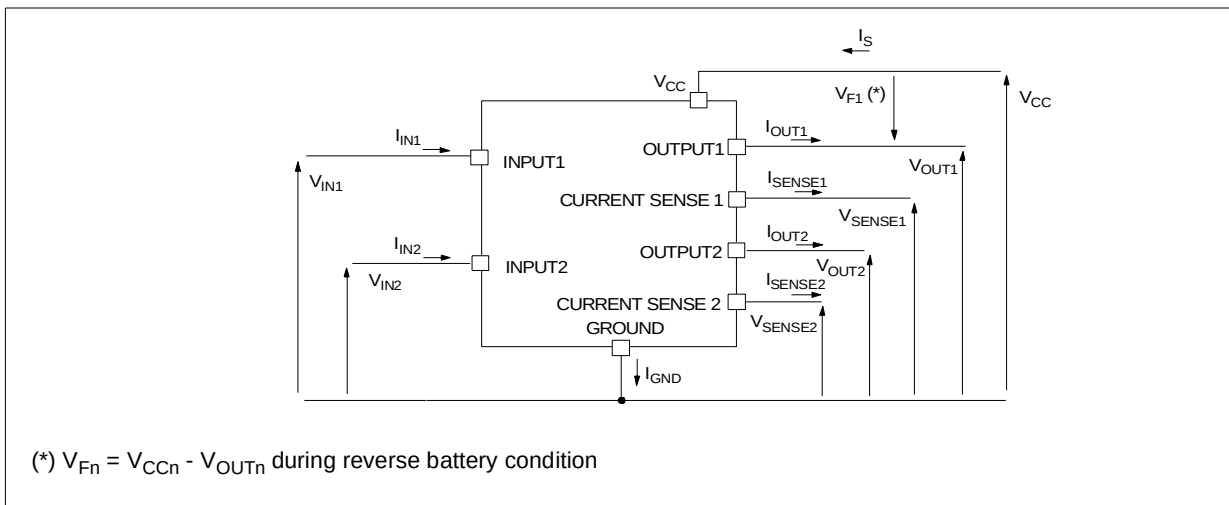
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	Output current	Internally limited	A
I_R	Reverse output current	-21	A
I_{IN}	Input current	+/- 10	mA
V_{CSENSE}	Current sense maximum voltage	-3 +15	V V
V_{ESD}	Electrostatic Discharge (Human Body Model: $R=1.5K\Omega$; $C=100pF$)		
	- INPUT	4000	V
	- CURRENT SENSE	2000	V
	- OUTPUT	5000	V
	- V_{CC}	5000	V
E_{MAX}	Maximum Switching Energy ($L=0.13mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_L=40A$)	145	mJ
P_{tot}	Power dissipation at $T_c=25^\circ C$	96.1	W
T_j	Junction operating temperature	Internally limited	$^\circ C$
T_c	Case operating temperature	-40 to 150	$^\circ C$
T_{STG}	Storage temperature	-55 to 150	$^\circ C$

CONFIGURATION DIAGRAM (TOP VIEW) & SUGGESTED CONNECTIONS FOR UNUSED AND N.C. PINS



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX)	1.3	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (MAX)	51.3 ⁽¹⁾ 37 ⁽²⁾	°C/W

⁽¹⁾ When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35µm thick).

⁽²⁾ When mounted on a standard single-sided FR-4 board with 6 cm² of Cu (at least 35µm thick).

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C; unless otherwise specified)

(Per each channel)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CC} (**)	Operating supply voltage		5.5	13	36	V
V _{USD} (**)	Undervoltage shutdown		3	4	5.5	V
V _{OV} (**)	Overvoltage shutdown		36			V
R _{ON}	On state resistance	I _{OUT} =5A; T _j =25°C I _{OUT} =5A; T _j =150°C I _{OUT} =3A; V _{CC} =6V			30 60 100	mΩ mΩ mΩ
V _{clamp}	Clamp Voltage	I _{CC} =20mA (see note 1)	41	48	55	V
I _S (**)	Supply current	Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V; T _j =25°C On state; V _{IN} =5V; V _{CC} =13V; I _{OUT} =0A; R _{SENSE} =3.9kΩ		12 12	40 25	µA µA
I _{L(off1)}	Off State Output Current	V _{IN} =V _{OUT} =0V	0		50	µA
I _{L(off2)}	Off State Output Current	V _{IN} =0V; V _{OUT} =3.5V	-75		0	µA
I _{L(off3)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =125°C			5	µA
I _{L(off4)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =25°C			3	µA

(**) Per device.

PROTECTIONS (see note 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I _{lim}	DC short circuit current	V _{CC} =13V 5.5V<V _{CC} <36V	25	40	70 70	A A
T _{TSD}	Thermal shut-down temperature		150	175	200	°C
T _R	Thermal reset temperature		135			°C
T _{HYST}	Thermal hysteresis		7	15		°C
V _{demag}	Turn-off output voltage clamp	I _{OUT} =2A; V _{IN} =0V; L=6mH	V _{CC} -41	V _{CC} -48	V _{CC} -55	V
V _{ON}	Output voltage drop limitation	I _{OUT} =0.5A T _j = -40°C...+150°C		50		mV

Note 1: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

VCC - OUTPUT DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _F	Forward on Voltage	-I _{OUT} =2.6A; T _j =150°C			0.6	V

ELECTRICAL CHARACTERISTICS (continued)CURRENT SENSE ($9V \leq V_{CC} \leq 16V$) (See figure 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT1} or $I_{OUT2}=0.5A$; $V_{SENSE}=0.5V$; other channels open; $T_j = -40^\circ C \dots 150^\circ C$	3300	4400	6000	
dK_1/K_1	Current Sense Ratio Drift	I_{OUT1} or $I_{OUT2}=0.5A$; $V_{SENSE}=0.5V$; other channels open; $T_j = -40^\circ C \dots 150^\circ C$	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT1} or $I_{OUT2}=5A$; $V_{SENSE}=4V$; other channels open; $T_j = -40^\circ C$ $T_j = 25^\circ C \dots 150^\circ C$	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current Sense Ratio Drift	I_{OUT1} or $I_{OUT2}=5A$; $V_{SENSE}=4V$; other channels open; $T_j = -40^\circ C \dots 150^\circ C$	-6		+6	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT1} or $I_{OUT2}=15A$; $V_{SENSE}=4V$; other channels open; $T_j = -40^\circ C$ $T_j = 25^\circ C \dots 150^\circ C$	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current Sense Ratio Drift	I_{OUT1} or $I_{OUT2}=15A$; $V_{SENSE}=4V$; other channels open; $T_j = -40^\circ C \dots 150^\circ C$	-6		+6	%
$V_{SENSE1,2}$	Max analog sense output voltage	$V_{CC}=5.5V$; $I_{OUT1,2}=2.5A$; $R_{SENSE}=10k\Omega$ $V_{CC}>8V$, $I_{OUT1,2}=5A$; $R_{SENSE}=10k\Omega$	2 4			V V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	$V_{CC}=13V$; $R_{SENSE}=3.9k\Omega$		5.5		V
$R_{VSENSEH}$	Analog Sense Output Impedance in Overtemperature Condition	$V_{CC}=13V$; $T_j > T_{SD}$; All channels open		400		Ω
t_{DSENSE}	Current sense delay response	to 90% I_{SENSE} (see note 2)			500	μs

LOGIC INPUT (Channels 1,2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	$V_{IN}=1.25V$	1			μA
V_{IH}	Input high level voltage		3.25			V
I_{IH}	High level input current	$V_{IN}=3.25V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN}=1mA$ $I_{IN}=-1mA$	6	6.8 -0.7	8	V V

SWITCHING ($V_{CC}=13V$)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$R_L=2.6\Omega$ (see figure 1)		30		μs
$t_{d(off)}$	Turn-off delay time	$R_L=2.6\Omega$ (see figure 1)		30		μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L=2.6\Omega$ (see figure 1)		See relative diagram		V/ μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L=2.6\Omega$ (see figure 1)		See relative diagram		V/ μs

Note 1: V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

Note 2: current sense signal delay after positive input slope.

TRUTH TABLE (per channel)

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overvoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	$(T_J < T_{TSD})$ 0
	H	L	$(T_J > T_{TSD})$ V_{SENSEH}
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μ s 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μ s 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

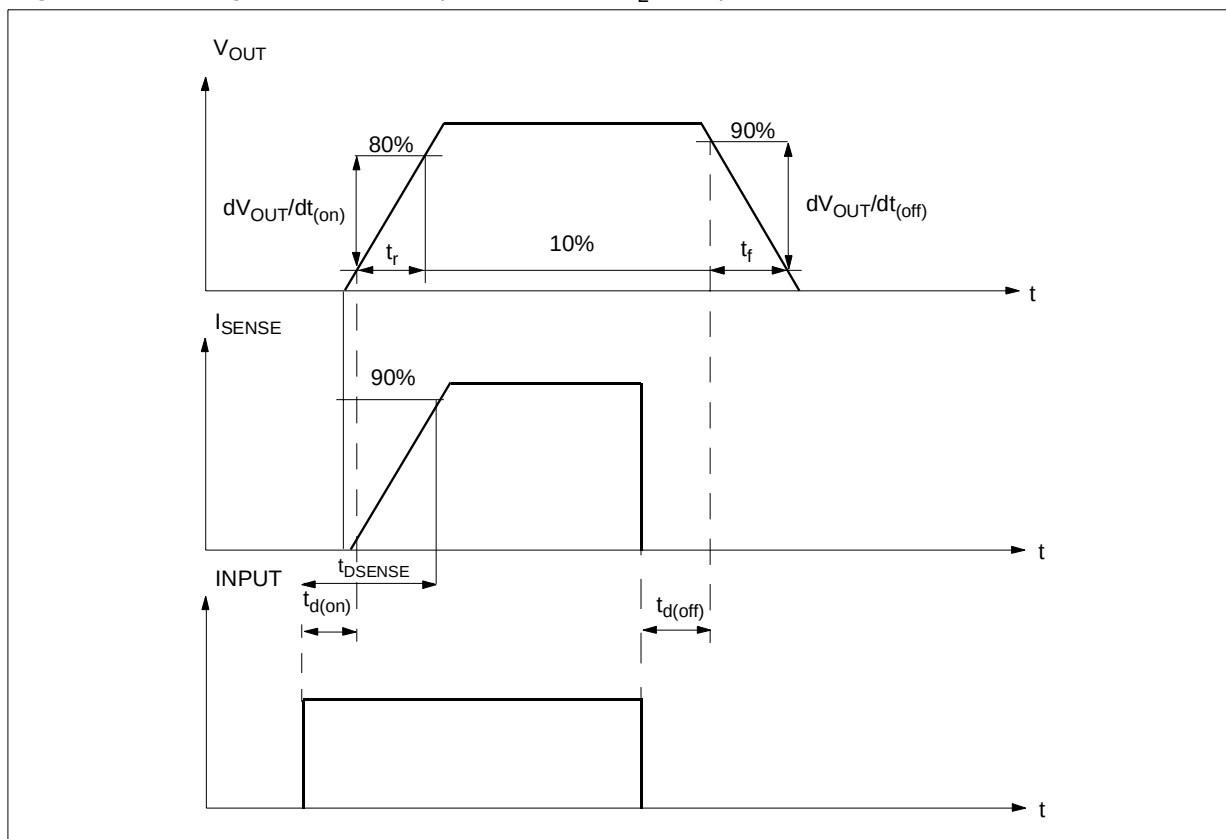
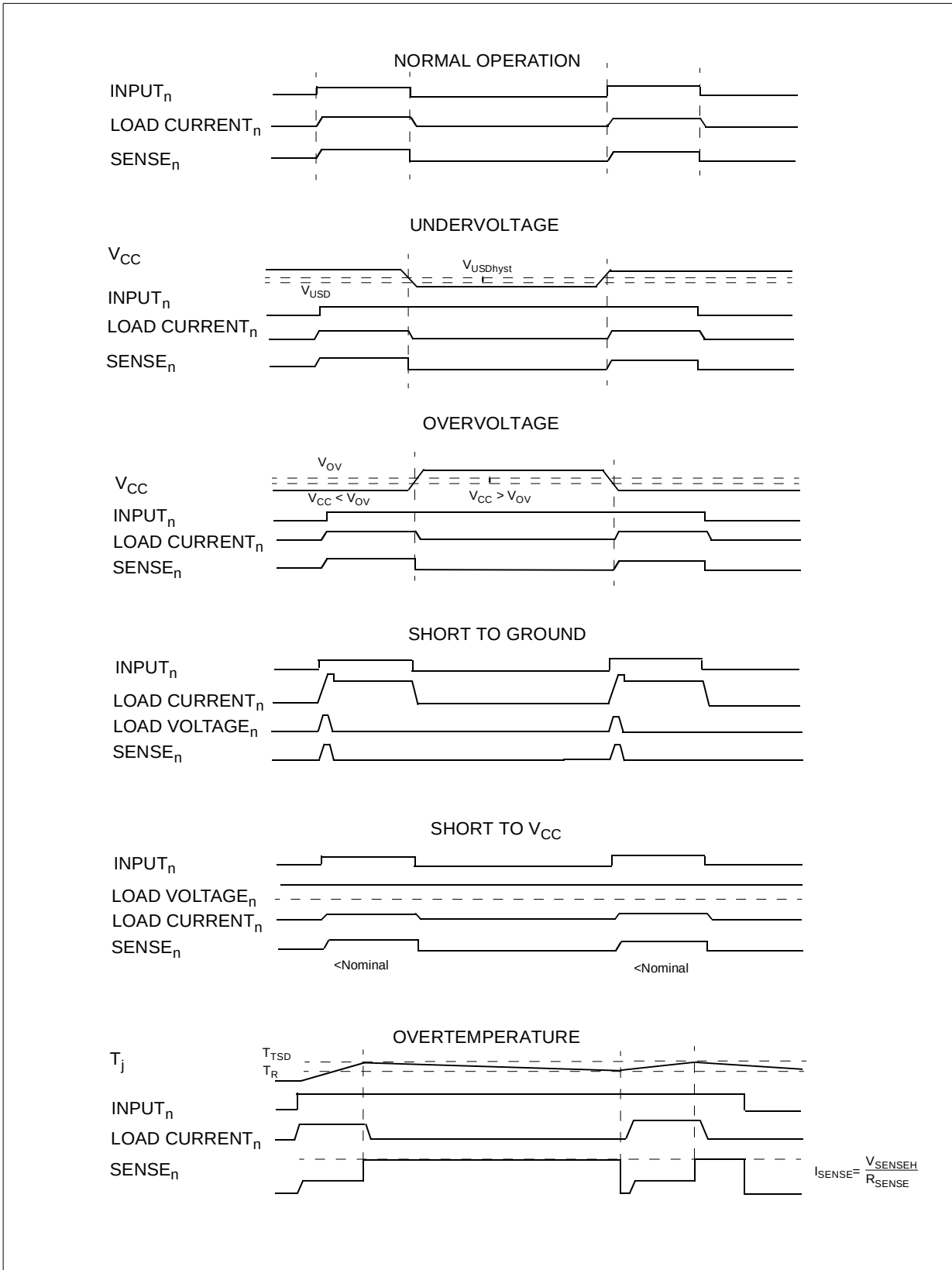
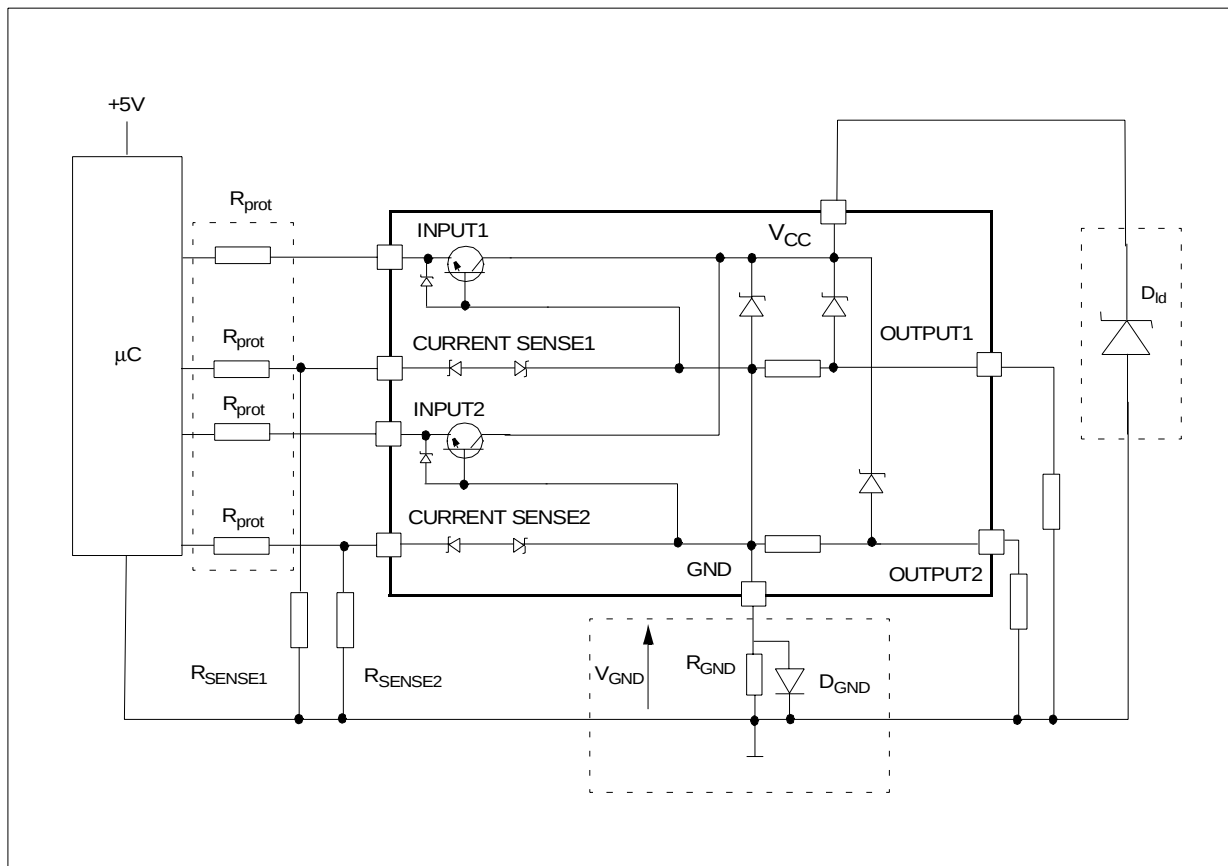
Figure 1: Switching Characteristics (Resistive load $R_L=2.6\Omega$)

Figure 2: Waveforms



APPLICATION SCHEMATIC

**GND PROTECTION NETWORK AGAINST REVERSE BATTERY**

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / I_{S(on)max}$
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND} = 1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600\text{mV}$) in the input thresholds and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

LOAD DUMP PROTECTION

D_{Id} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

μC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

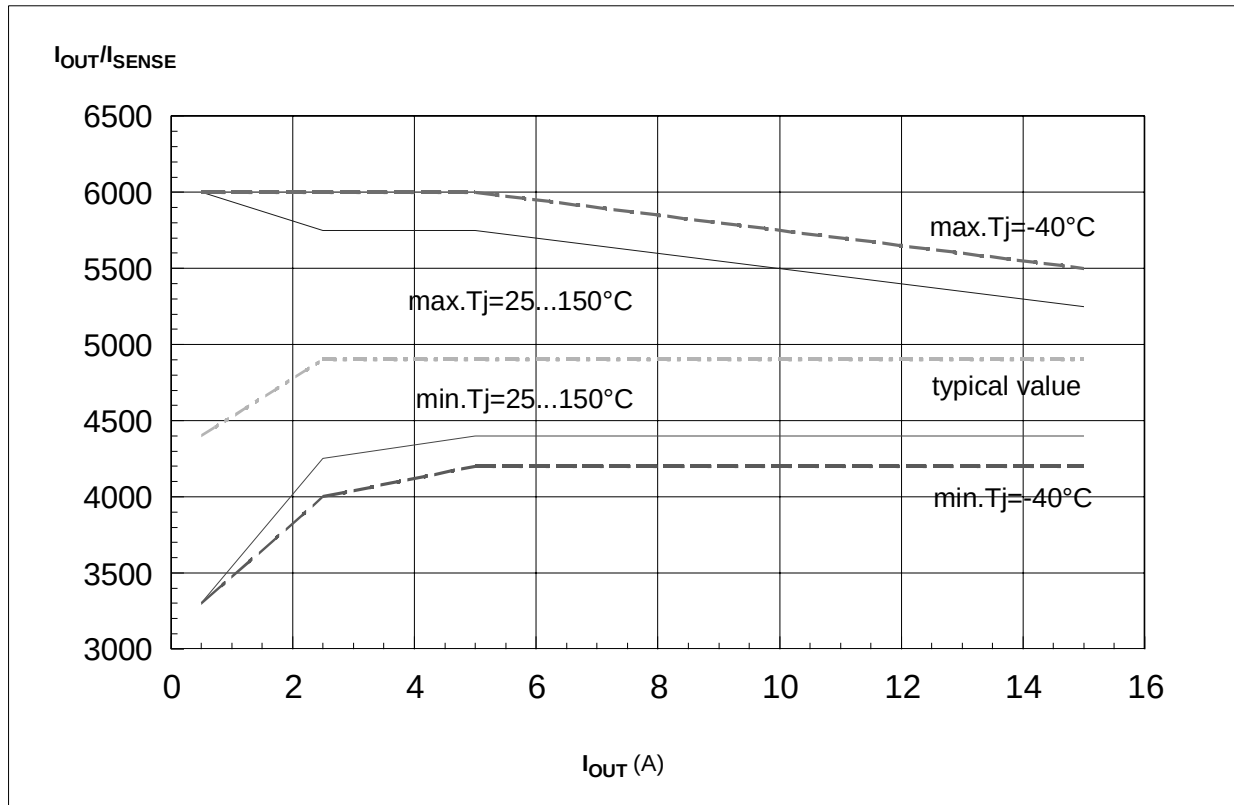
$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

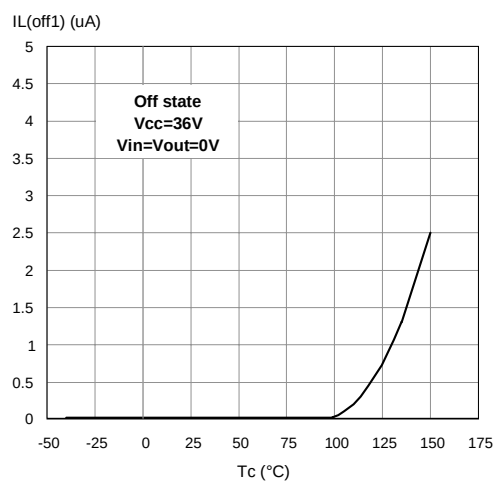
For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$
 $5k\Omega \leq R_{prot} \leq 65k\Omega$.

Recommended R_{prot} value is 10kΩ.

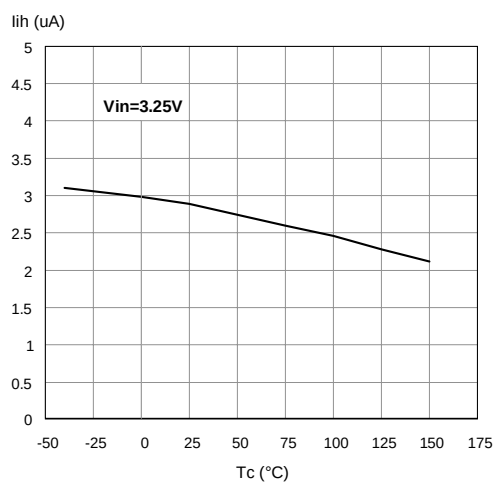
Figure 3: I_{OUT}/I_{SENSE} versus I_{OUT}



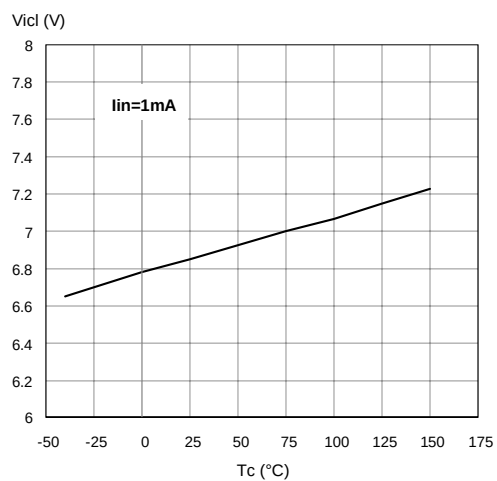
Off State Output Current



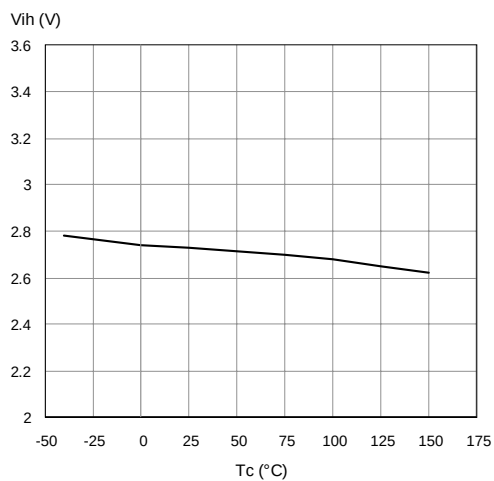
High Level Input Current



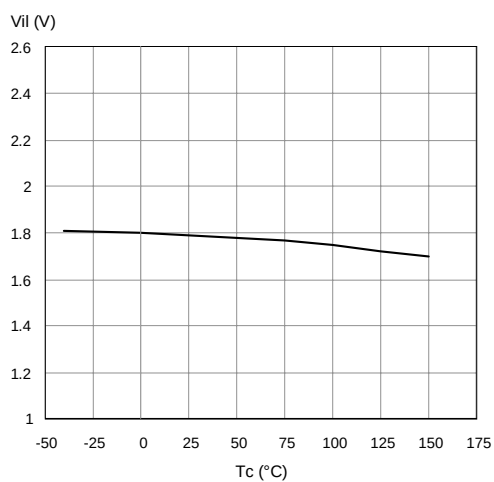
Input Clamp Voltage



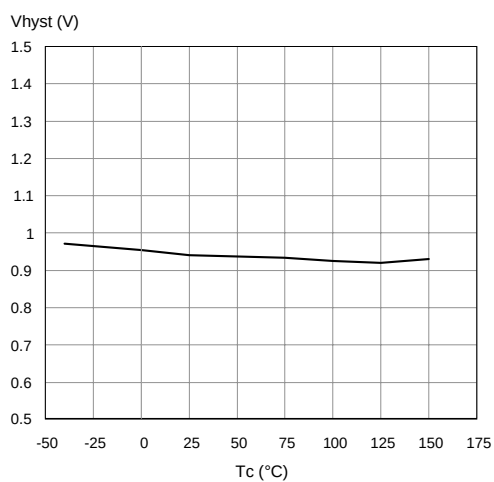
Input High Level



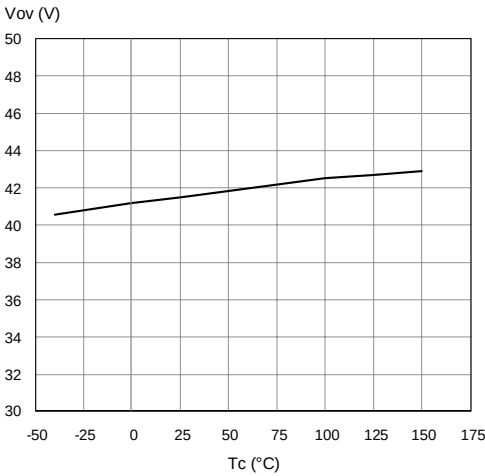
Input Low Level



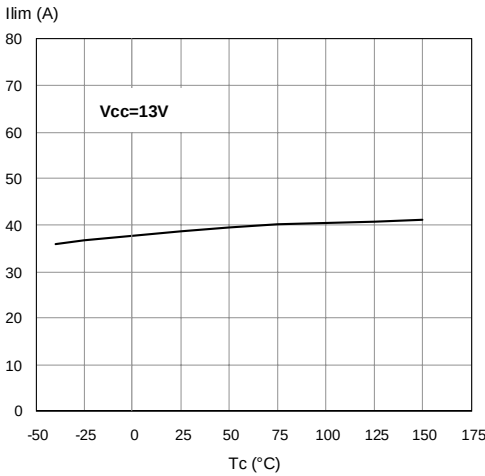
Input Hysteresis Voltage



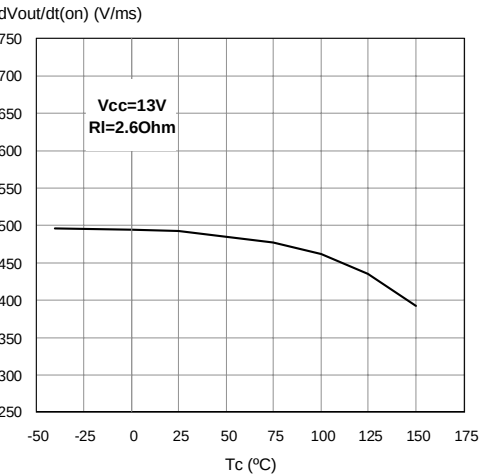
Overvoltage Shutdown



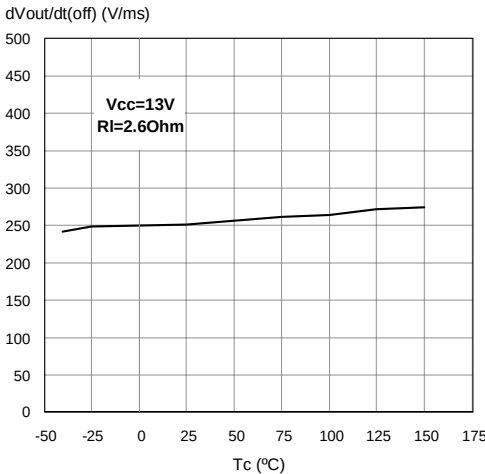
I_{LIM} Vs T_{case}



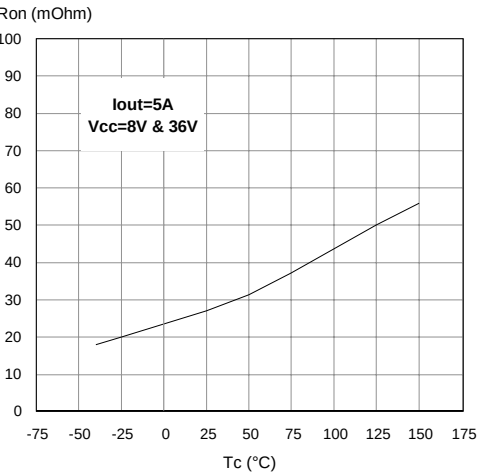
Turn-on Voltage Slope



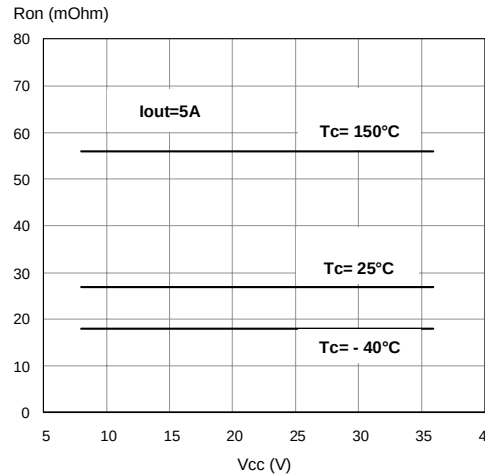
Turn-off Voltage Slope



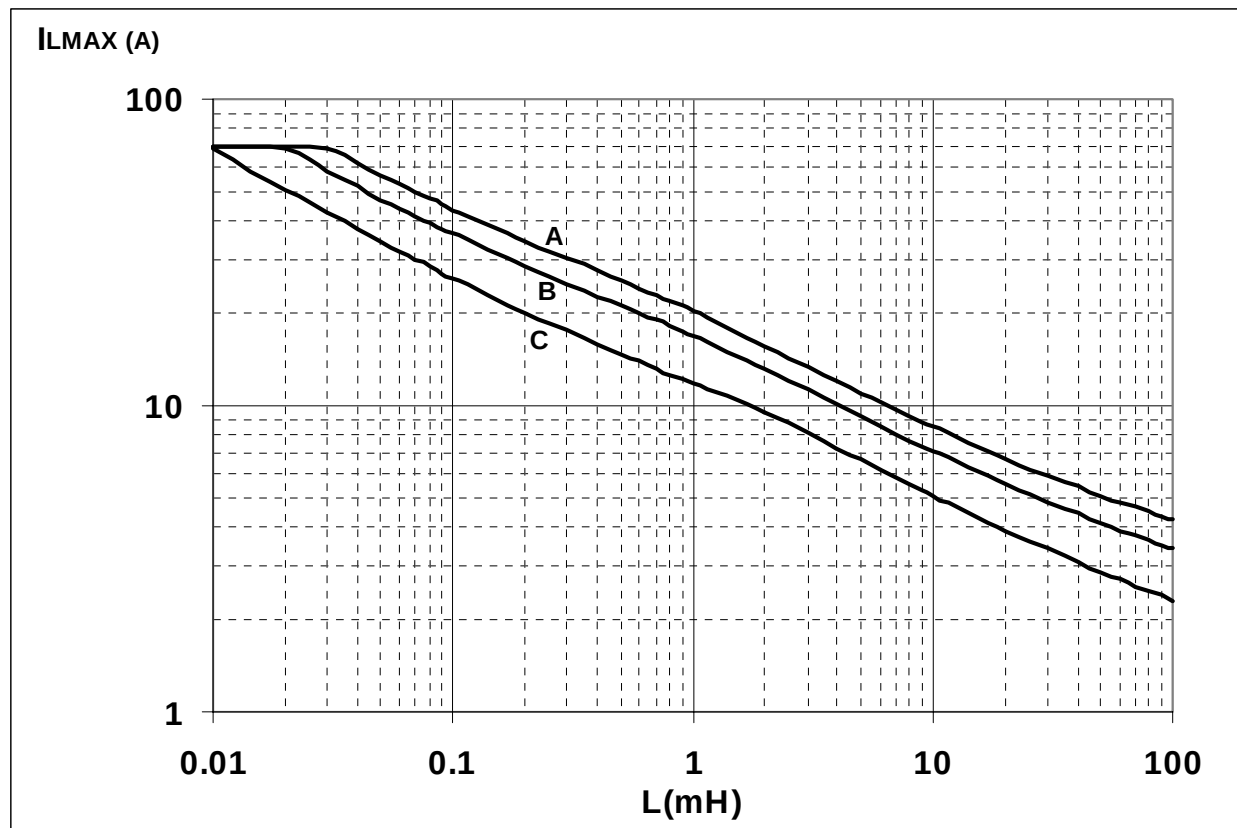
On State Resistance Vs T_{case}



On State Resistance Vs V_{CC}



Maximum turn off current versus load inductance



A = Single Pulse at $T_{jstart}=150^{\circ}\text{C}$

B= Repetitive pulse at $T_{jstart}=100^{\circ}\text{C}$

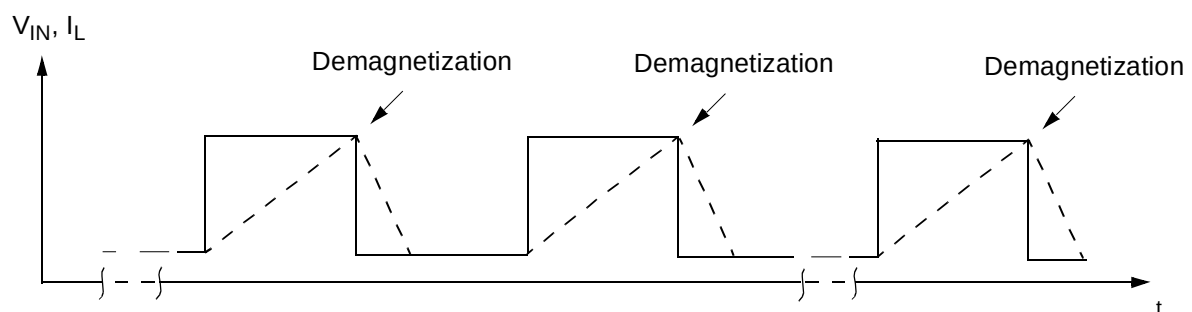
C= Repetitive Pulse at $T_{jstart}=125^{\circ}\text{C}$

Conditions:

$V_{CC}=13.5\text{V}$

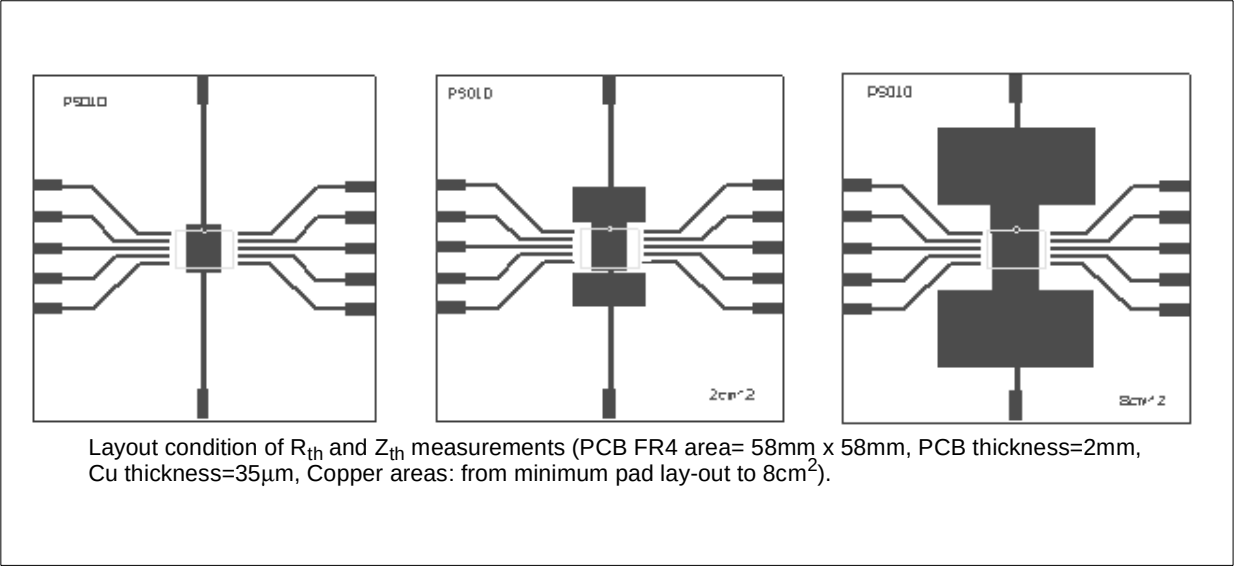
Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

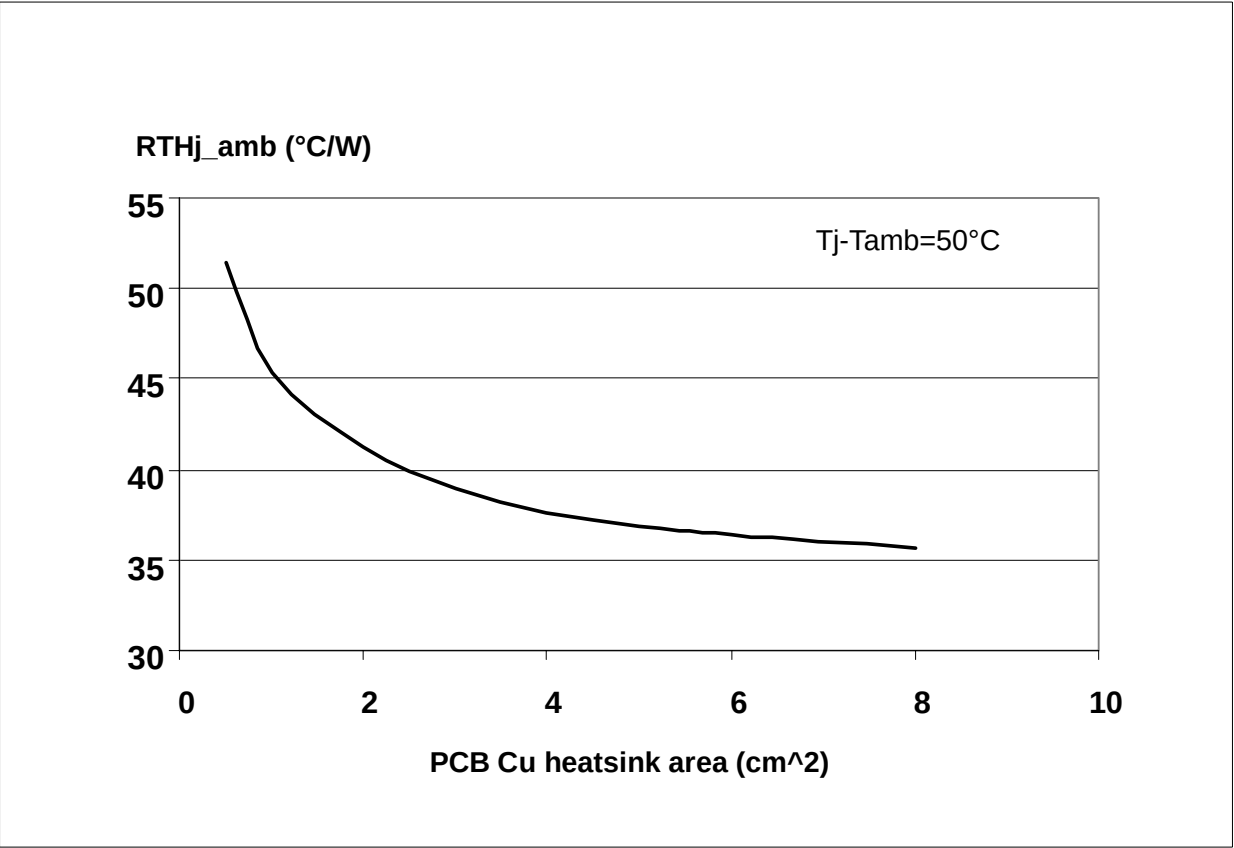


PowerSO-10™ THERMAL DATA

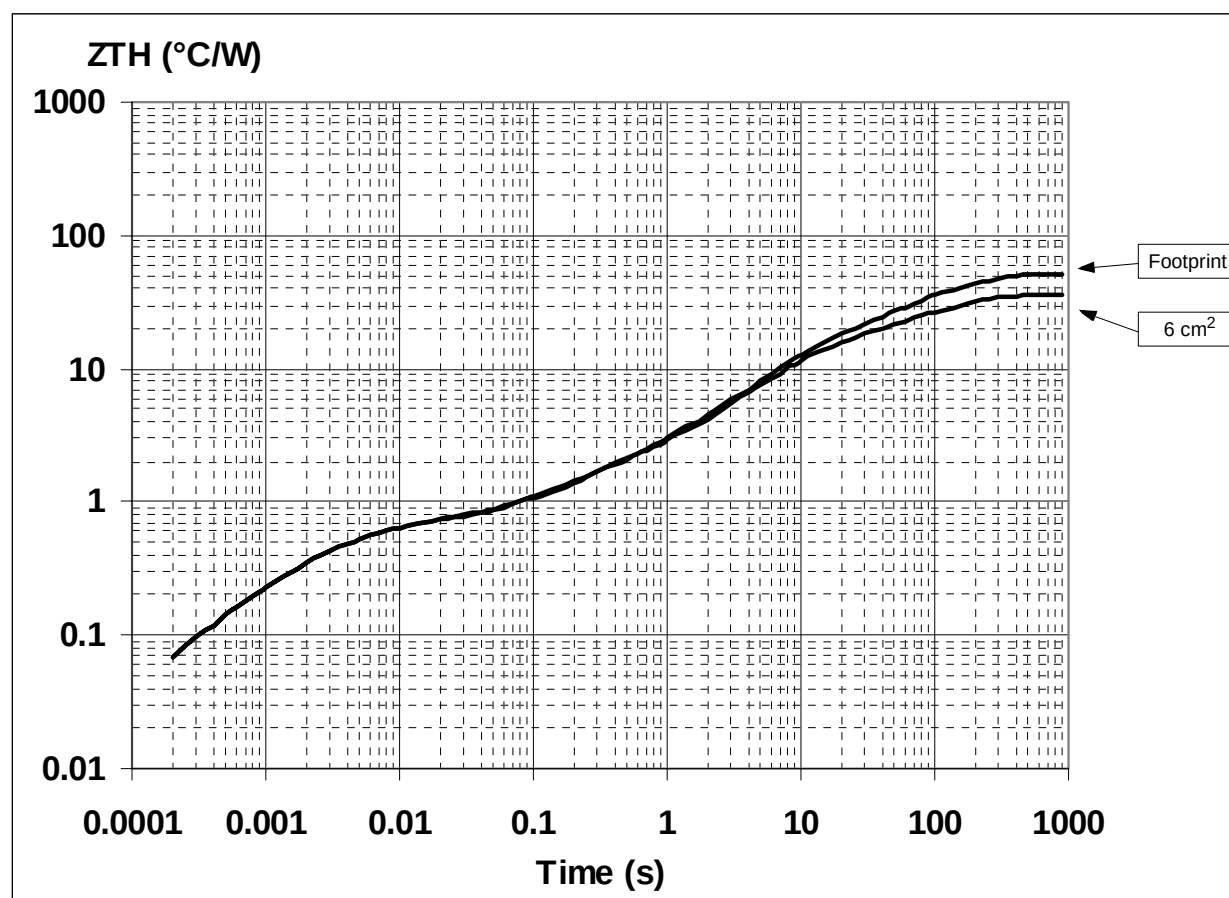
PowerSO-10™ PC Board



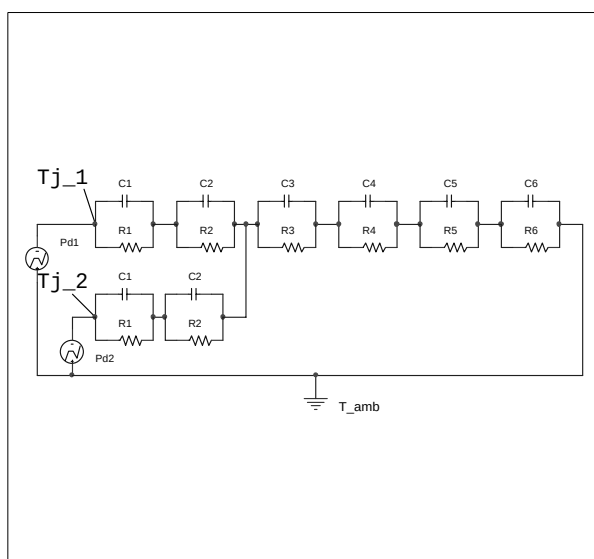
$R_{thj-amb}$ Vs PCB copper area in open box free air condition



PowerSO-10 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a double channel HSD in PowerSO-10



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

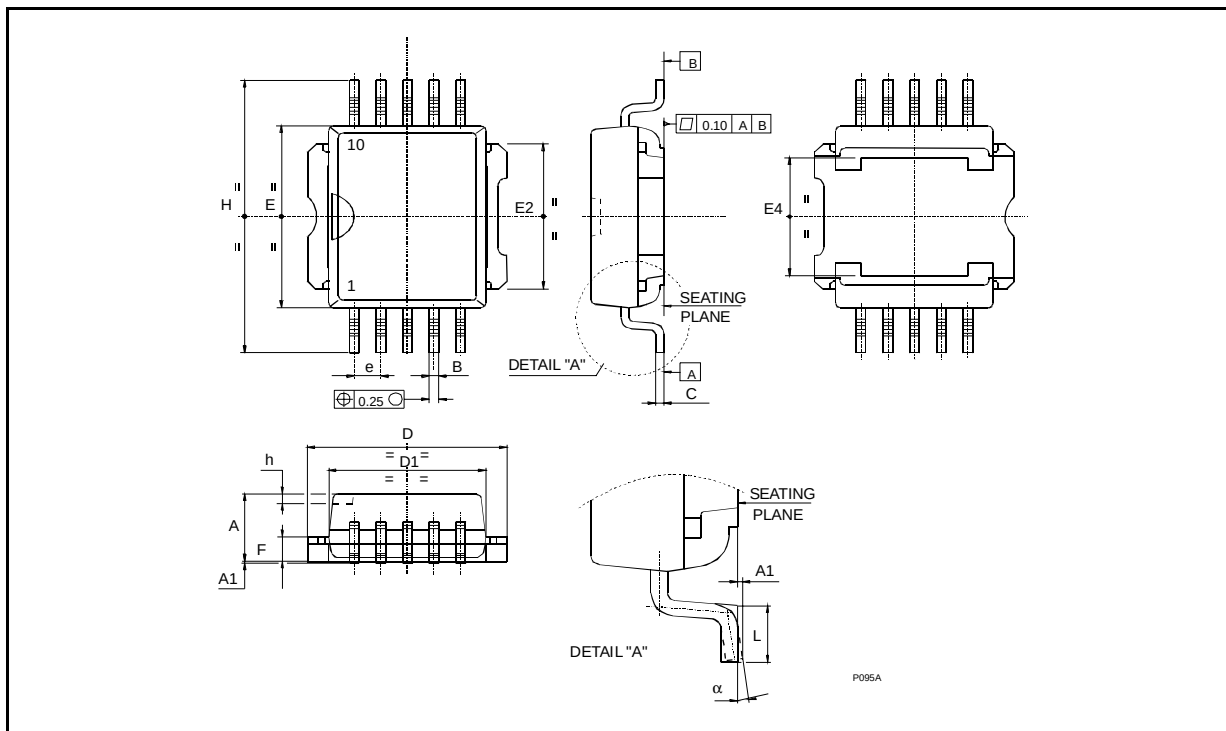
Thermal Parameter

Area/island (cm ²)	Footprint	6
R1 (°C/W)	0.05	
R2 (°C/W)	0.3	
R3 (°C/W)	0.3	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.001	
C2 (W.s/°C)	5.00E-03	
C3 (W.s/°C)	0.02	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

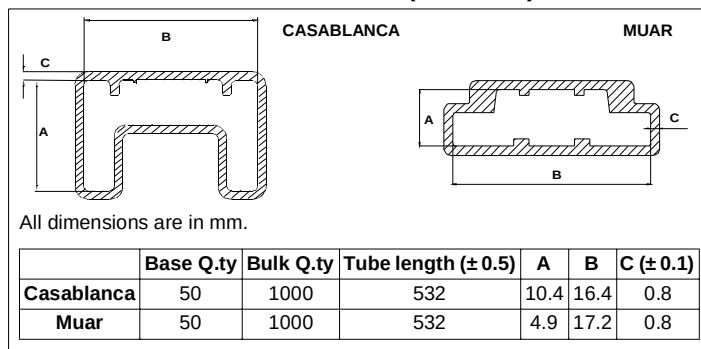
PowerSO-10™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		0.300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0°		8°	0°		8°
α (*)	2°		8°	2°		8°

(*) Muar only POA P013P



TUBE SHIPMENT (no suffix)

**TAPE AND REEL SHIPMENT (suffix "13TR")**

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

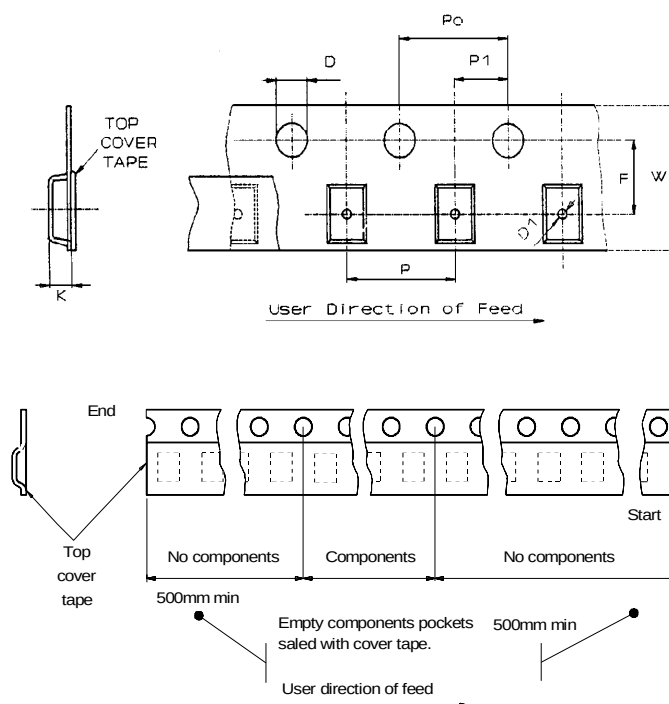
All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



REVISION HISTORY

Date	Revision	Description of Changes
Jul. 2004	1	- Current and voltage convention update (page 2). - "Configuration diagram (top view) & suggested connections for unused and n.c. pins" insertion (page 2). - 6 cm² Cu condition insertion in Thermal Data table (page 3). - V_{CC} - OUTPUT DIODE section update (page 3). - Revision History table insertion (page 17). - Disclaimers update (page 18).
July 2004	2	- Suggested connections for unused and n.c.pins" correction (page 2).

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