MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTD4P06

Designer's Data Sheet

Power Field Effect Transistor

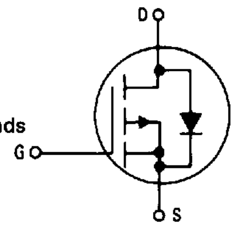
P-Channel Enhancement Mode Silicon Gate DPAK for Surface Mount or Insertion Mount

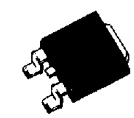
TMOS POWER FET
4 AMPERES
$R_{DS(on)}$ = 0.6 OHM
50 and 60 VOLTS

3

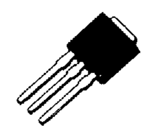
This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ — 0.6 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix





CASE 369A-10
TO-252
MTD4P06



CASE 369-06
TO-251
MTD4P06-1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	4 14	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01	Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$	6.25 100 71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTD4P05 MTD4P06	$V_{(BR)DSS}$	50 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 125°C	I_{DSS}	— —	0.2 1	mAdc

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2 Adc)		$R_{DS(on)}$	—	0.6	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 4 Adc) (I_D = 2 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 2.4 2.4	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2 A)		g_{FS}	0.75	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 12	C_{iss}	—	700	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 10, 14 and 15	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	120	
Turn-Off Delay Time		$t_{d(off)}$	—	80	
Fall Time		t_f	—	70	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 13	Q_g	12 (Typ)	16	nC
Gate-Source Charge		Q_{gs}	7 (Typ)	—	
Gate-Drain Charge		Q_{gd}	5 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.8 (Typ)	5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

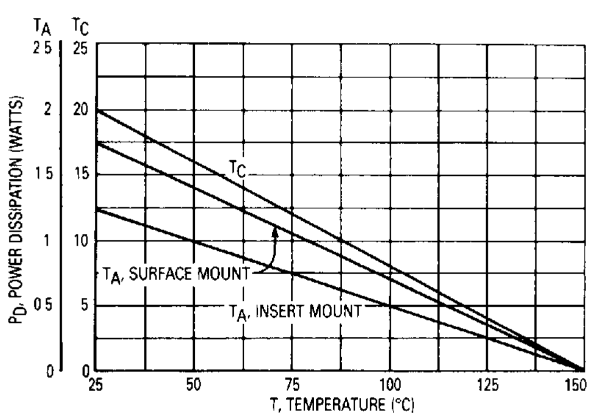


Figure 1. Power Derating

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TYPICAL ELECTRICAL CHARACTERISTICS

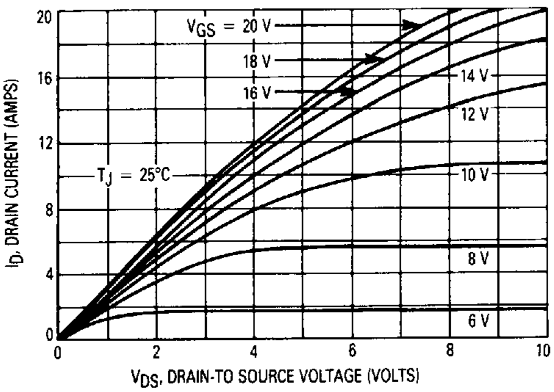

Figure 2. On-Region Characteristics

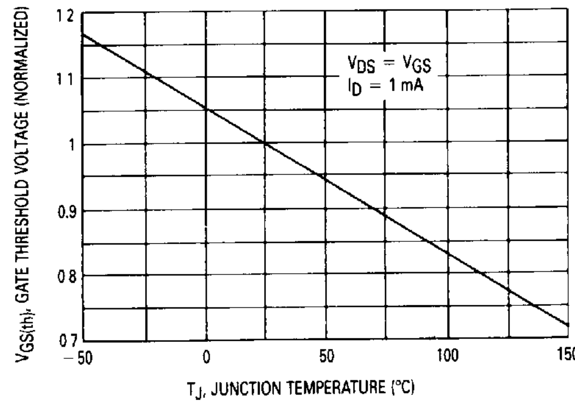

Figure 3. Gate-Threshold Voltage Variation With Temperature

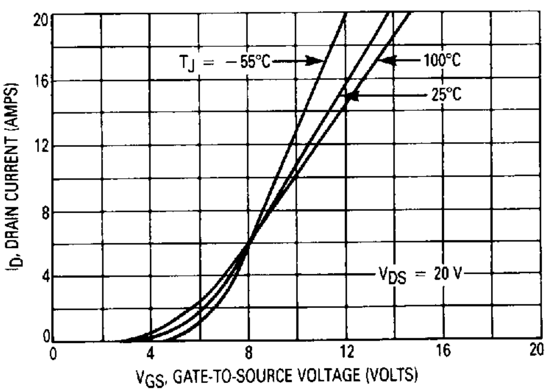

Figure 4. Transfer Characteristics

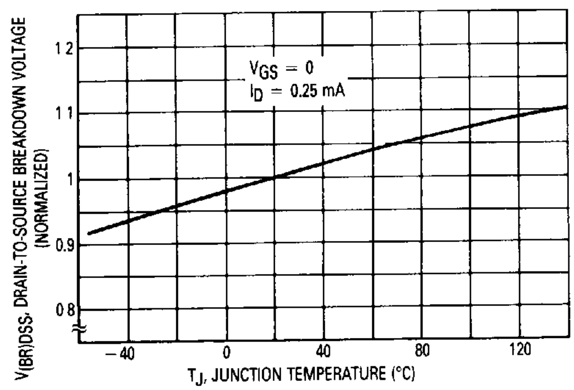

Figure 5. Breakdown Voltage Variation With Temperature

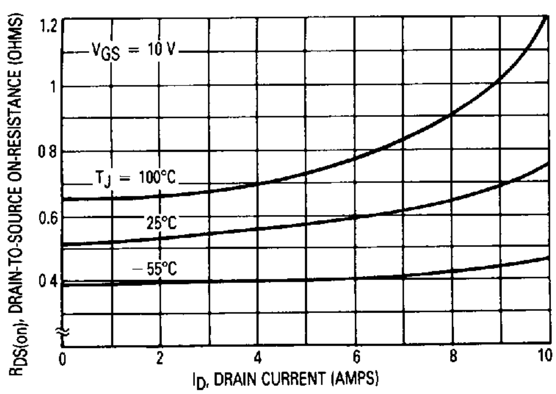

Figure 6. On-Resistance versus Drain Current

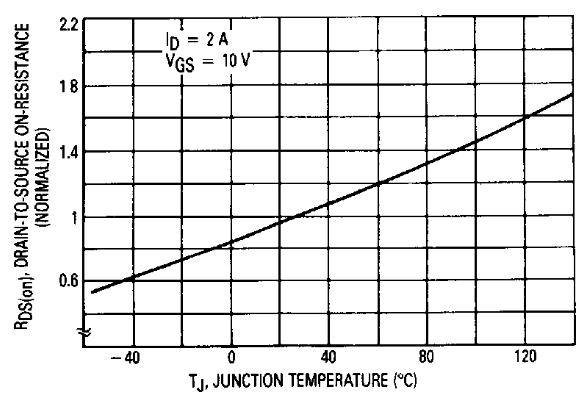

Figure 7. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

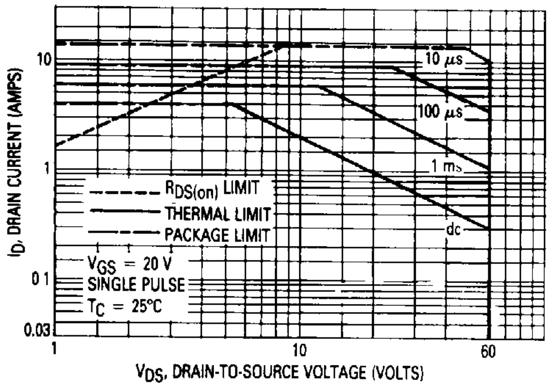

Figure 8. Maximum Rated Forward Bias Safe Operating Area

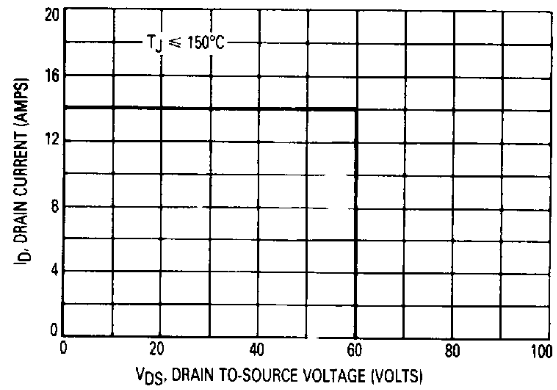

Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

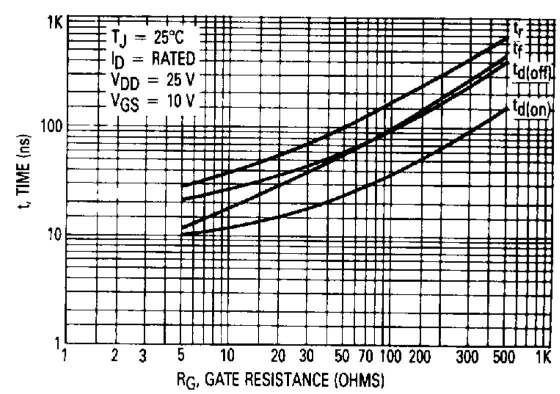

Figure 10. Resistive Switching Time Variation With Gate Resistance

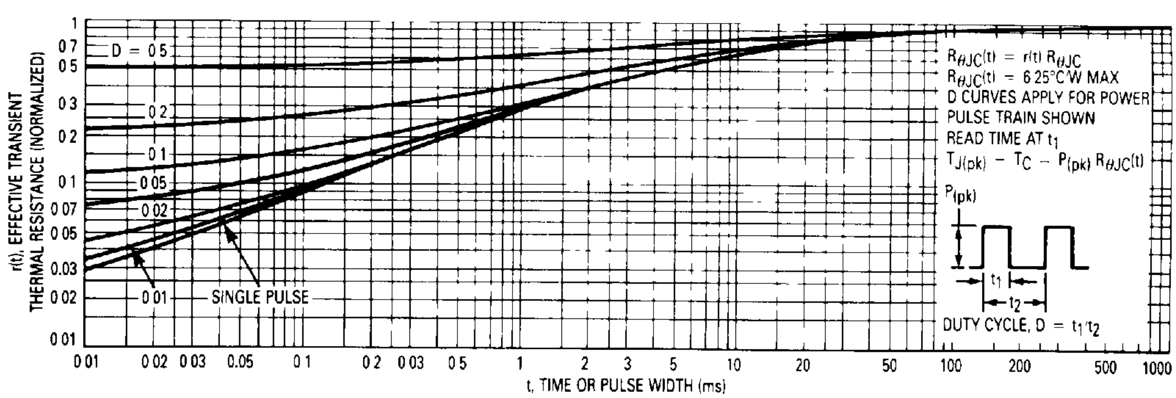

Figure 11. Thermal Response

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TYPICAL CHARACTERISTICS

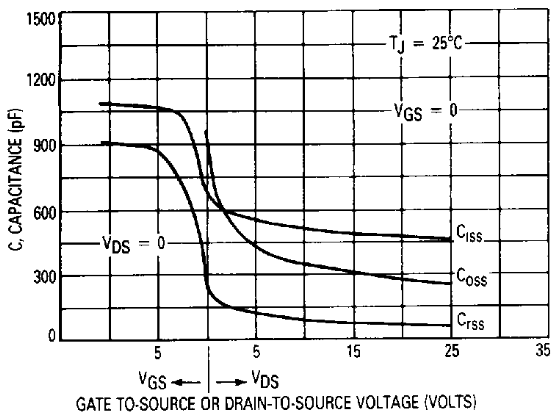

Figure 12. Capacitance Variation

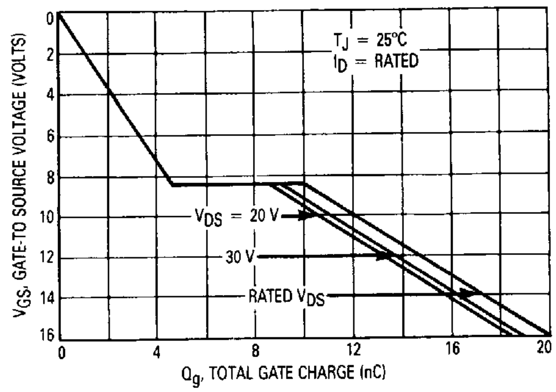

Figure 13. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

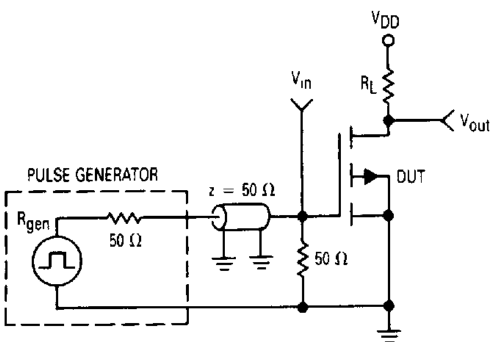

Figure 14. Switching Test Circuit

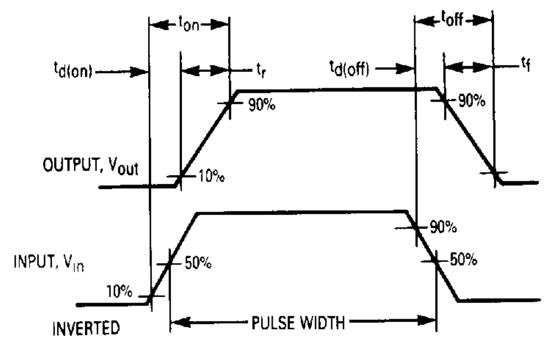

Figure 15. Switching Waveforms