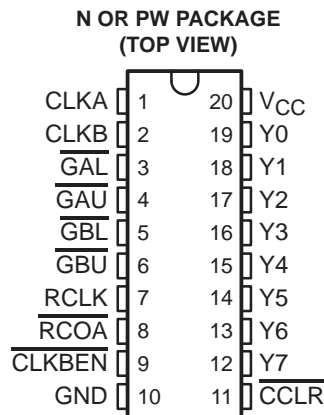


- Can Be Used as Two 16-Bit Counters or a Single 32-Bit Counter
- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 25 ns at 5 V (RCLK to Y)
- Typical V_{OLP} (Output Ground Bounce) <0.7 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >4.4 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



description/ordering information

The SN74LV8154 is a dual 16-bit binary counter with 3-state output registers, designed for 2-V to 5.5-V V_{CC} operation.

This 16-bit counter (A or B) feeds a 16-bit storage register, and each storage register is further divided into an upper byte and lower byte. The \overline{GAL} , \overline{GAU} , \overline{GBL} , \overline{GBU} inputs are used to select the byte that needs to be output at Y0–Y7. CLKA is the clock for A counter, and CLKB is the clock for B counter. RCLK is the clock for the A and B storage registers. All three clock signals are positive-edge triggered.

A 32-bit counter can be realized by connecting CLKA and CLKB together and by connecting \overline{RCOA} to \overline{CLKBEN} .

To ensure the high-impedance state during power up or power down, \overline{GAL} , \overline{GAU} , \overline{GBL} , and \overline{GBU} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74LV8154N	SN74LV8154N
	TSSOP – PW	Tube	SN74LV8154PW	LV8154
		Tape and reel	SN74LV8154PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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SN74LV8154
DUAL 16-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS

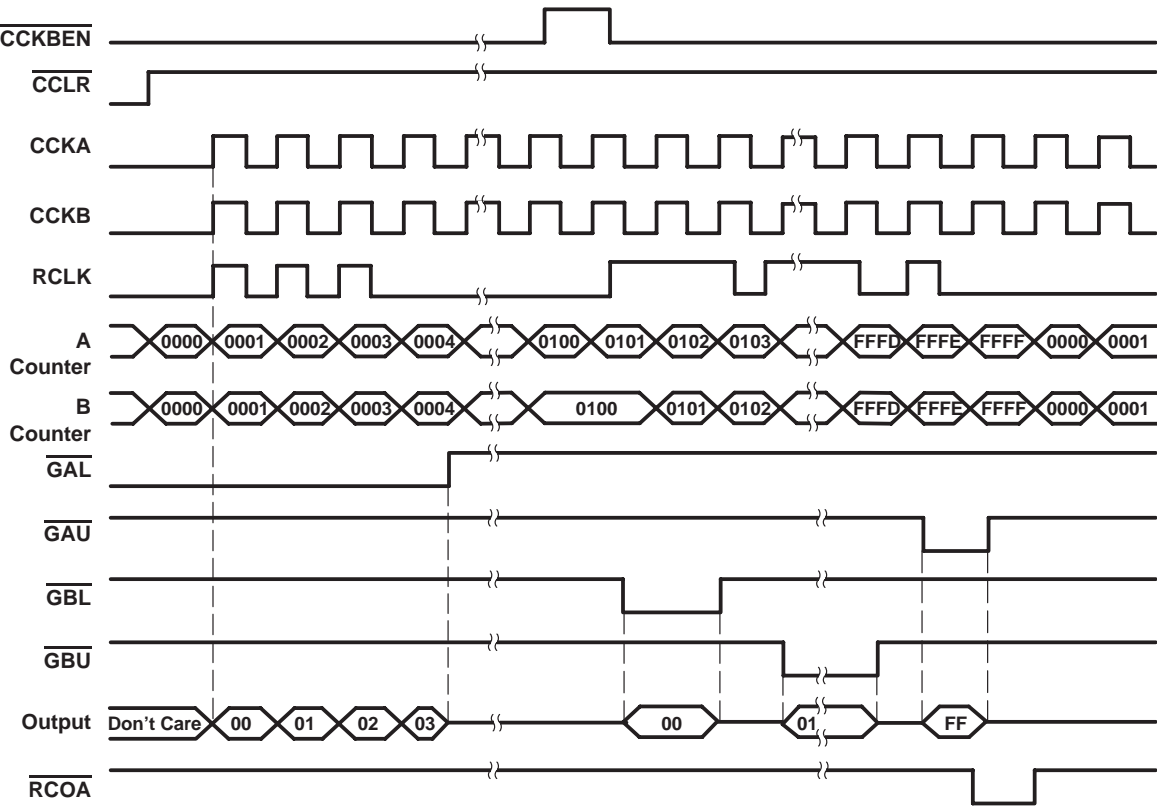
SCLS589 – AUGUST 2004

FUNCTION TABLE
(each buffer)

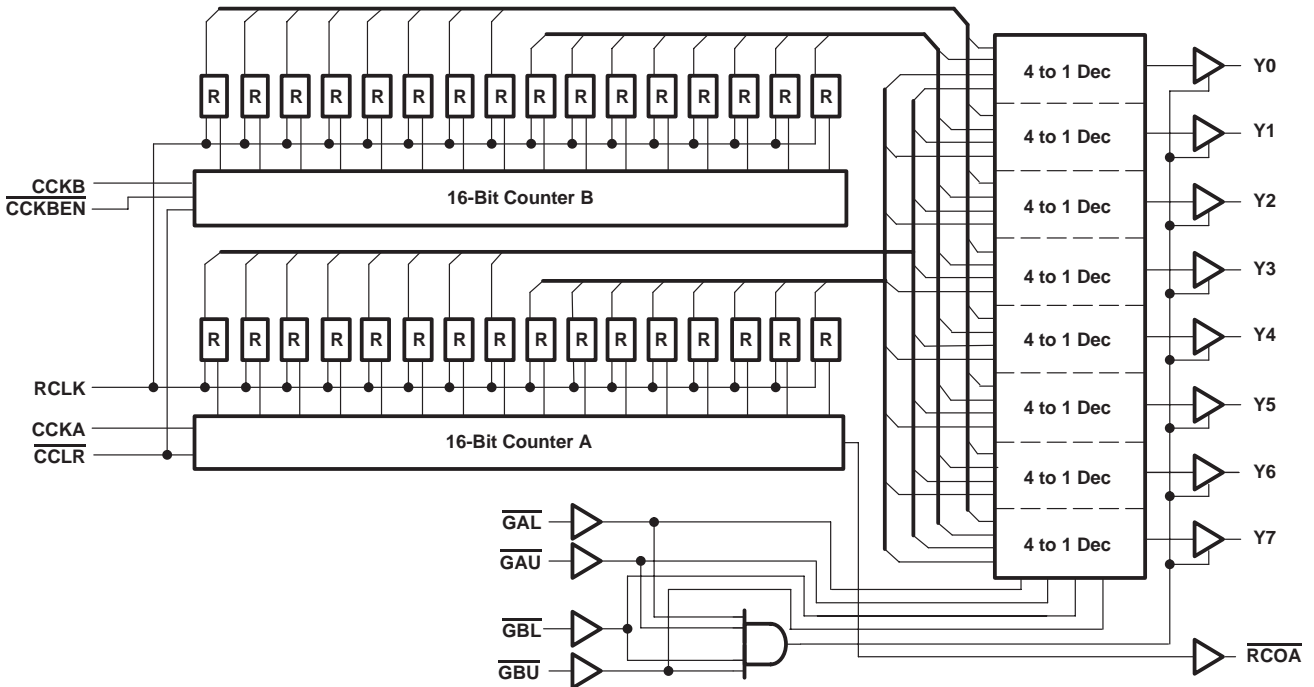
INPUTS				OUTPUT Y _n
$\overline{\text{GAL}}$	$\overline{\text{GAU}}$	$\overline{\text{GBL}}$	$\overline{\text{GBU}}$	
L	H	H	H	Lower byte in A register
H	L	H	H	Upper byte in A register
H	H	L	H	Lower byte in B register
H	H	H	L	Upper byte in B register
H	H	H	H	Z

Combinations of $\overline{\text{GAL}}$, $\overline{\text{GAU}}$, $\overline{\text{GBL}}$, $\overline{\text{GBU}}$, other than those shown above, are prohibited. If more than one input is L at the same time, the output data (Y0–Y7) may be invalid.

timing diagram



block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): N package	69°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LV8154

DUAL 16-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

SCLS589 – AUGUST 2004

recommended operating conditions (see Note 4)

		V _{CC}	MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	2 V	1.5		V
		3 V to 3.6 V	V _{CC} × 0.7		
		4.5 V to 5.5 V	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	2 V		0.5	V
		3 V to 3.6 V		V _{CC} × 0.3	
		4.5 V to 5.5 V		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	Yn outputs	2 V		–50	μA
		3 V to 3.6 V		–6	mA
		4.5 V to 5.5 V		–12	
	$\overline{\text{RCOA}}$	2 V		–50	μA
		3 V to 3.6 V		–6	mA
		4.5 V to 5.5 V		–12	
I _{OL}	Yn outputs	2 V		50	μA
		3 V to 3.6 V		6	mA
		4.5 V to 5.5 V		12	
	$\overline{\text{RCOA}}$	2 V		50	μA
		3 V to 3.6 V		6	mA
		4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	3 V to 3.6 V		100	ns/V
		4.5 V to 5.5 V		20	
T _A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	Y _n	I _{OH} = –50 µA	2 V	1.9			V
		I _{OH} = –6 mA	3 V	2.48			
		I _{OH} = –12 mA	4.5 V	3.8			
	$\overline{\text{RCOA}}$	I _{OH} = –50 µA	2 V	1.9			
		I _{OH} = –6 mA	3 V	2.48			
		I _{OH} = –12 mA	4.5 V	3.8			
V _{OL}	Y _n	I _{OL} = 50 µA	2 V			0.1	V
		I _{OL} = 6 mA	3 V			0.44	
		I _{OL} = 12 mA	4.5 V			0.55	
	$\overline{\text{RCOA}}$	I _{OL} = 50 µA	2 V			0.1	
		I _{OL} = 6 mA	3 V			0.44	
		I _{OL} = 12 mA	4.5 V			0.55	
I _I		V _I = 5.5 V or GND	0 to 5.5 V			±1	µA
I _{OZ}		V _O = V _{CC} or GND	5.5 V			±5	µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V			20	µA
I _{off}		V _I or V _O = 0 to 5.5 V	0			5	µA
C _i		V _I = V _{CC} or GND	5 V		3		pF
C _O		V _O = V _{CC} or GND	5 V		5		pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		MIN	MAX	UNIT
t _w	Pulse duration	CLKA, CLKB, RCLK high or low	10	ns
		$\overline{\text{CCLR}}$ low	22	
t _{su}	Setup time	$\overline{\text{CLKBEN}}$ low before CLKB↑	13	ns
		$\overline{\text{CCLR}}$ high (inactive) before CLKA↑ or CLKB↑	13	
		CLKA↑ or CLKB↑ before RCLK↑	13	
		RCLK↑ before $\overline{\text{GAL}}$ or $\overline{\text{GAU}}$ or $\overline{\text{GBL}}$ or $\overline{\text{GBU}}$ low	13	
		$\overline{\text{GAL}}$ or $\overline{\text{GAU}}$ or $\overline{\text{GBL}}$ or $\overline{\text{GBU}}$ high (inactive) before RCLK↑	13	
t _h	Hold time	$\overline{\text{CLKBEN}}$ low after CLKB↑	0	ns
		CLKA or CLKB after RCLK	0	
t _z [†]	Z-period	$\overline{\text{GAL}}$, $\overline{\text{GAU}}$, $\overline{\text{GBL}}$, $\overline{\text{GBU}}$ all high before one of them switches low	200	ns

[†] t_z condition: C_L = 50 pF, R_L = 1 kΩ

SN74LV8154

DUAL 16-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

SCLS589 – AUGUST 2004

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		MIN	MAX	UNIT
t_w Pulse duration	CLKA, CLKB, RCLK high or low	10		ns
	$\overline{\text{CCLR}}$ low	20		
t_{su} Setup time	$\overline{\text{CLKBEN}}$ low before $\text{CLKB}\uparrow$	10		ns
	$\overline{\text{CCLR}}$ high (inactive) before $\text{CLKA}\uparrow$ or $\text{CLKB}\uparrow$	10		
	$\text{CLKA}\uparrow$ or $\text{CLKB}\uparrow$ before $\text{RCLK}\uparrow$	10		
	$\text{RCLK}\uparrow$ before $\overline{\text{GAL}}$ or $\overline{\text{GAU}}$ or $\overline{\text{GBL}}$ or $\overline{\text{GBU}}$ low	10		
	$\overline{\text{GAL}}$ or $\overline{\text{GAU}}$ or $\overline{\text{GBL}}$ or $\overline{\text{GBU}}$ high (inactive) before $\text{RCLK}\uparrow$	10		
t_h Hold time	$\overline{\text{CLKBEN}}$ low after $\text{CLKB}\uparrow$	0		ns
	CLKA or CLKB after RCLK	0		
t_z^\dagger Z-period	$\overline{\text{GAL}}$, $\overline{\text{GAU}}$, $\overline{\text{GBL}}$, $\overline{\text{GBU}}$ all high before one of them switches low	200		ns

$^\dagger t_z$ condition: $C_L = 50\text{ pF}$, $R_L = 1\text{ k}\Omega$

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f _{MAX}			C _L = 15 pF				40		MHz
			C _L = 50 pF				25		
t _{pd}	RCLK	Y	C _L = 15 pF	22			1	38	ns
	CLKA	RCOA		26			1	44	
t _{PLH}	CCLR	RCOA		18			1	32	ns
t _{en}	GAL, GAU, GBL, GBU	Y		27			1	46	ns
t _{dis}	GAL, GAU, GBL, GBU	Y		12			1	21	ns
t _{pd}	RCLK	Y		C _L = 50 pF	25			1	42
	CLKA	RCOA	28			1	46		
t _{PLH}	CCLR	RCOA	20			1	35	ns	
t _{en}	GAL, GAU, GBL, GBU	Y	30			1	50	ns	
t _{dis}	GAL, GAU, GBL, GBU	Y	14			1	24	ns	



switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f _{MAX}			C _L = 15 pF				40		MHz
			C _L = 50 pF				25		
t _{pd}	RCLK	Y	C _L = 15 pF	14			1	25	ns
	CLKA	RCOA		16			1	27	
t _{PLH}	CCLR	RCOA		12			1	20	ns
t _{en}	GAL, GAU, GBL, GBU	Y		16			1	28	ns
t _{dis}	GAL, GAU, GBL, GBU	Y		8			1	15	ns
t _{pd}	RCLK	Y		C _L = 50 pF	16			1	27
	CLKA	RCOA	17			1	28		
t _{PLH}	CCLR	RCOA	13			1	21	ns	
t _{en}	GAL, GAU, GBL, GBU	Y	18			1	30	ns	
t _{dis}	GAL, GAU, GBL, GBU	Y	9			1	16	ns	

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$

PARAMETER		$T_A = 25^\circ\text{C}$			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}	0.7			V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.75			V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4			V

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = \text{No load}$, $\text{CCLK} = 10\text{ MHz}$, $\text{RCLK} = 1\text{ MHz}$	56	pF

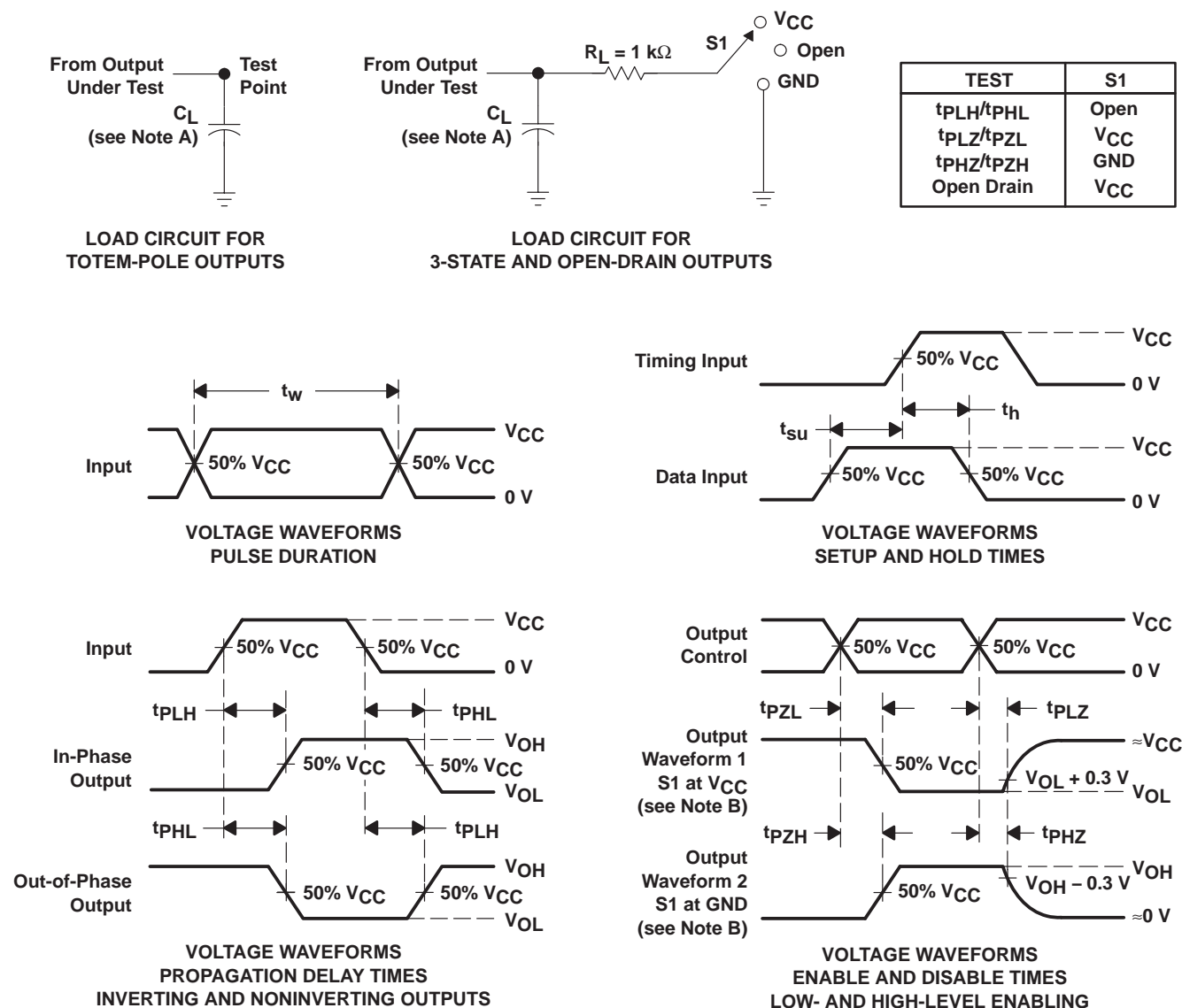
SN74LV8154

DUAL 16-BIT BINARY COUNTERS

WITH 3-STATE OUTPUT REGISTERS

SCLS589 – AUGUST 2004

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



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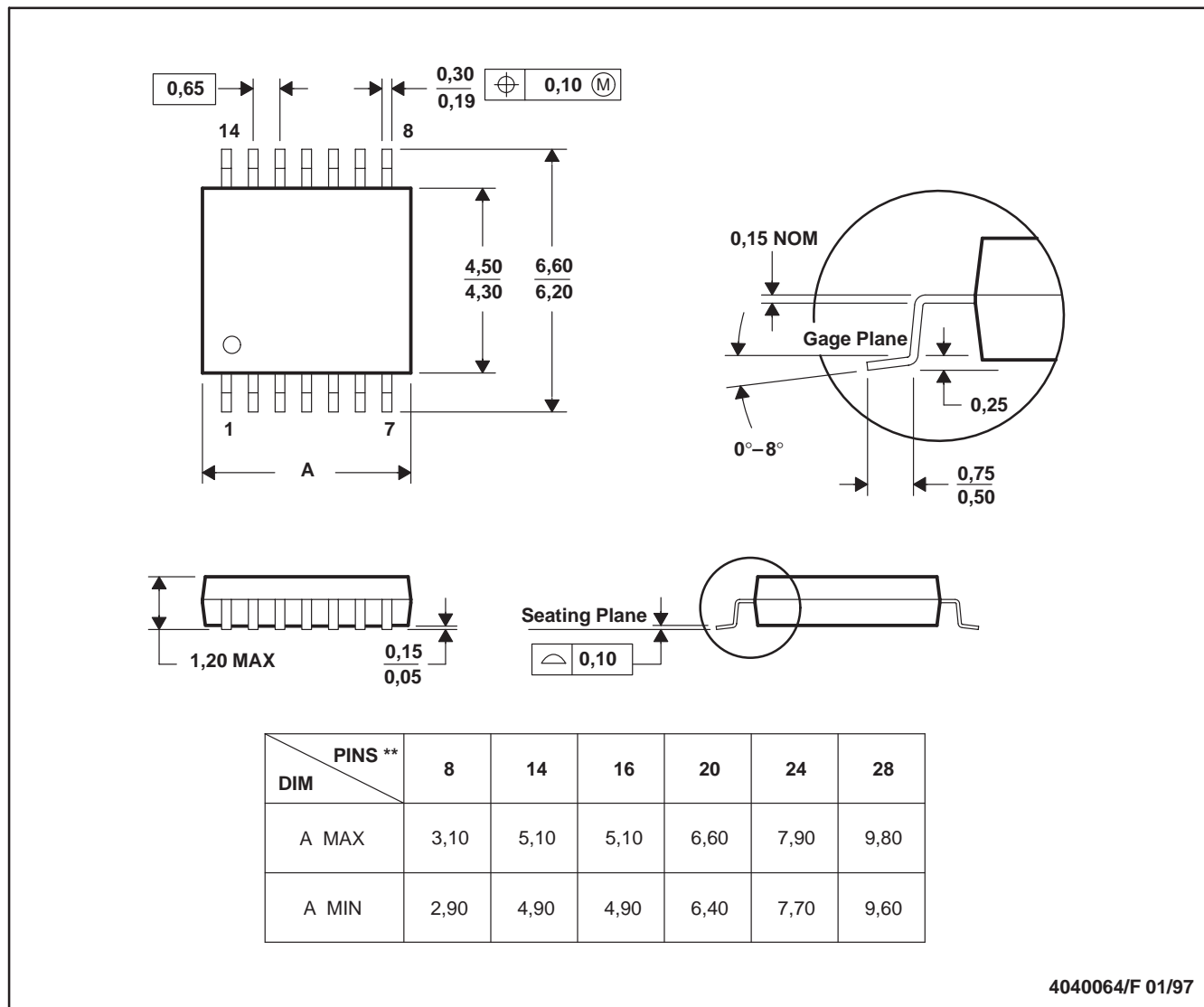
NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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