NEC

MOS INTEGRATED CIRCUIT

μPD78C10A, 78C11A, 78C12A

8-BIT SINGLE-CHIP MICROCOMPUTER (WITH A/D CONVERTER)

DESCRIPTION

The μPD78C11A is a CMOS 8-bit microprocessor which can integrate 16-bit ALU, ROM, RAM, an A/D converter, a multi-function timer/event counter, and a general-purpose serial interface into a single chip, then expand the memory (ROM/RAM) up to 60K bytes externally. The μPD78C10A is a ROM-less product of the μPD78C11A, and can directly address the external memory up to 64k bytes. The μPD78C12A is a product which has more built-in ROM capacity than the μPD78C11A, and its memory (ROM/RAM) can be externally extended up to 56K bytes. The μPD78C10A, μPD78C11A, and μPD78C12A operated at low power consumption, because they have a CMOS construction. Also, they can hold data with low power consumption by using standby function.

On-chip PROM products, μPD78CP14 and μPD78CP18 which are ideal for evaluation or preproduction use during system development, early start-up and short-run multiple-device production of application sets, are available.

FEATURES

- Abundant 159 types of instructions : 87AD series instruction set, multiplication/division instructions, 16-bit operation instructions
- Instruction cycle : 0.8 μs (at 15 MHz operation)
- On-chip ROM : 4096W × 8 (μPD78C11A), 8192W × 8 (μPD78C12A)
  Non (μPD78C10A)
- On-chip RAM : 256W × 8
- High-precision 8-bit A/D converter : 8 analog inputs
- General-purpose serial interface : Asynchronous, synchronous, I/O interface mode
- Multi-function 16-bit timer/event counter
- Two 8-bit timers
- I/O lines : 32 (μPD78C10A), 44 (μPD78C11A, 78C12A)
- Interrupt function (external - 3, internal - 8) : Non-maskable interrupt × 1, maskable interrupt × 10
- Standby function : HALT mode, hardware/software STOP mode
- Zero-cross detection function : (2 inputs)
- On-chip pull-up resistor (port A, B, C: μPD78C11A, 78C12A only) by mask option

Caution The μPD78C10A does not hava a mask option.

Document No. IC-2678C
(O. D. No. IC-7769E)
Date Published February 1995 P
Printed in Japan

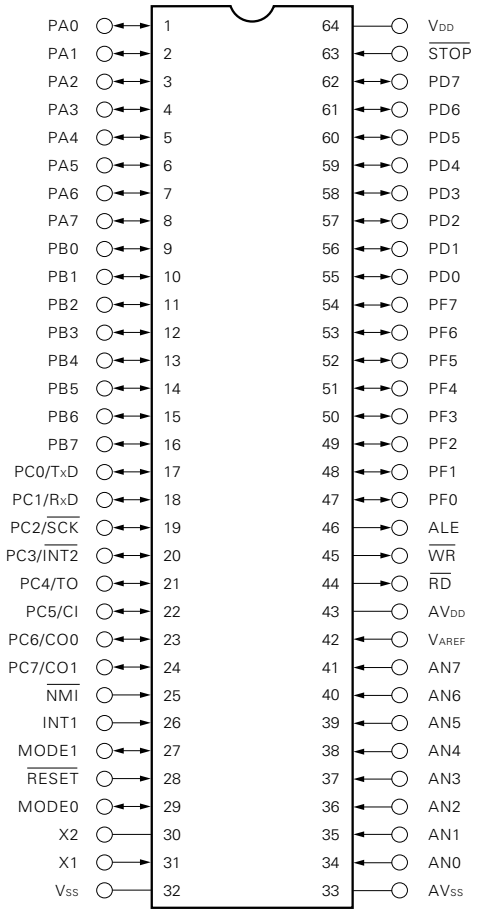
The mark ★ shows major revised points.

ORDERING INFORMATION

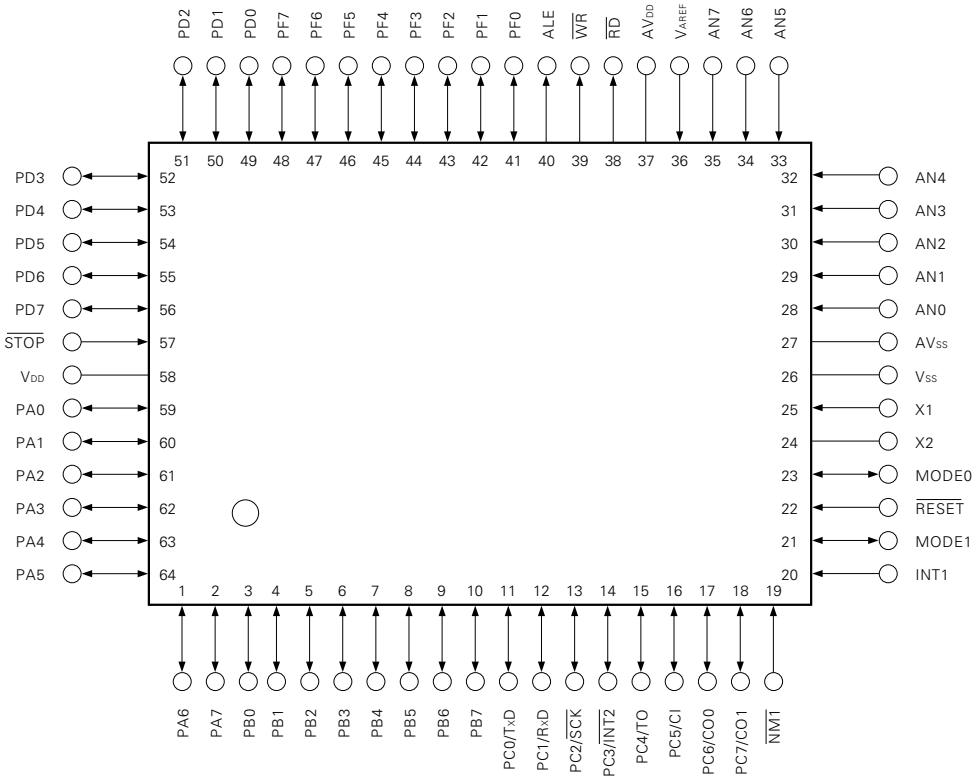
Ordering Code	Package	On-Chip ROM
μPD78C10ACW	64-pin plastic shrink DIP (750 mil)	None
μPD78C10AGF-3BE	64-pin plastic QFP (14 × 20 mm)	None
μPD78C10AGQ-36	64-pin plastic QUIP	None
μPD78C10AL	68-pin plastic QFJ (□ 950 mil)	None
μPD78C11ACW-×××	64-pin plastic shirink DIP (750 mil)	Mask ROM
μPD78C11AGF-×××-3BE	64-pin plastic QFP (14 × 20 mm)	Mask ROM
μPD78C11AGQ-×××-36	64-pin plastic QUIP	Mask ROM
μPD78C11AGQ-×××-37	64-pin plastic QUIP straight	Mask ROM
μPD78C11AL-×××	68-pin plastic QFJ (□ 950 mil)	Mask ROM
μPD78C12ACW-×××	64-pin plastic shrink DIP (750 mil)	Mask ROM
μPD78C12AGF-×××-3BE	64-pin plastic QFP (14 × 20 mm)	Mask ROM
μPD78C12AGQ-×××-36	64-pin plastic QUIP	Mask ROM
μPD78C12AGQ-×××-37	64-pin plastic QUIP straight	Mask ROM
μPD78C12AL-×××	68-pin plastic QFJ (□ 950 mil)	Mask ROM

PIN CONFIGURATION (TOP VIEW)

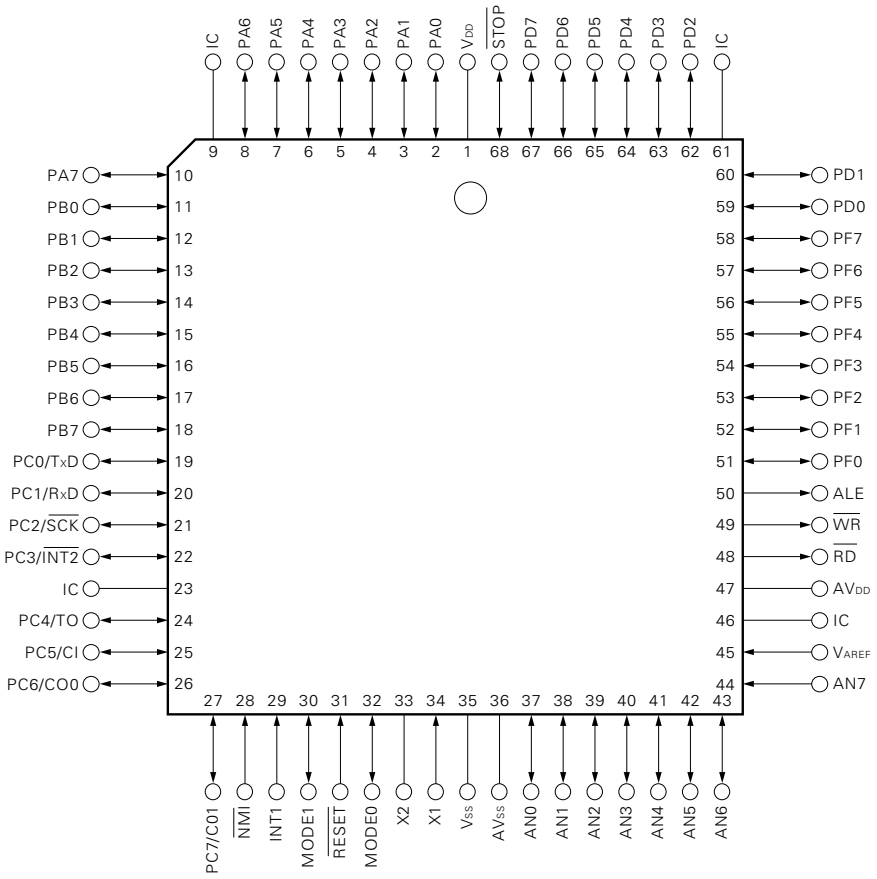
- For μPD78C10ACW, μPD78C10AGQ-36, μPD78C11ACW-xxx, μPD78C11AGQ-xxx-36/37, μPD78C12ACW-xxx, μPD78C12AGQ-xxx-36/37.



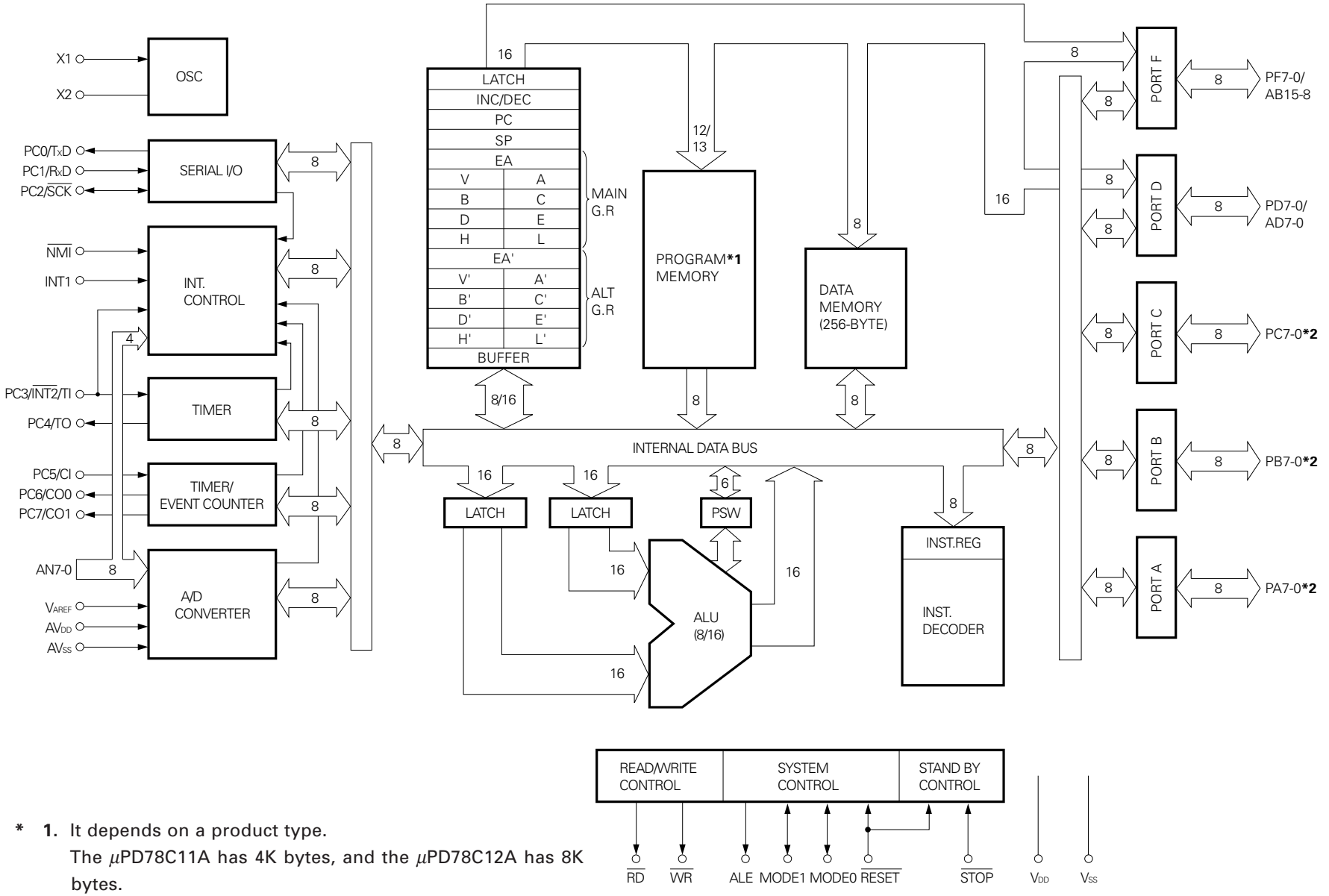
- For μPD78C10AGF-3BE, μPD78C11AGF-xxx-3BE, μPD78C12AGF-xxx-3BE



- For μPD78C10AL, μPD78C11AL-×××, μPD78C12AL-×××



BLOCK DIAGRAM



* **1.** It depends on a product type.
The μPD78C11A has 4K bytes, and the μPD78C12A has 8K bytes.
The μPD78C10A does not incorporate a program memory.

2. An on-chip pull-up resistor is available by mask option (μPD78C11A, 78C12A only).

CONTENTS

1. PIN FUNCTIONS

1.1 LIST OF PIN FUNCTION (1/2)

Pin Name	I/O	Function	
PA7 to PA0 (Port A)	Input/Output	8-bit input-output port, which can specify input/output bit-wise.	
PB7 to PB0 (Port B)	Input/Output	8-bit input-output port, which can specify input/output bit-wise.	
PC0/TxD	Input-output/ Output	Port C 8-bit input-output port, which can specify input/ output bit-wise.	Transmit Data Output pin for serial data.
PC1/RxD	Input-output/ Input		Receive Data Input pin for serial data.
PC2/$\overline{SCK}$	Input-output/ Input-output		Serial Clock Input-output pin for serial clock. It becomes output clock for the internal clock use, and input for the external.
PC3/$\overline{INT2}$/TI	Input-output/ Input/Input		Interrupt Request/Timer Input Maskable interrut input pin of the edge trigger (falling edge), or an external clock input pin for a timer. Also, it can be used as a zero-cross detection pin for AC input.
PC4/TO	Input-output/ Output		Timer Output Square wave defining one cycle of internal clock or timer counter time as half cycle is output.
PC5/CI	Input-output/ Input		Counter Input External pulse input pin to timer/event counter.
PC6/CO0 PC7/CO1	Input-output/ Output		Counter Output 0, 1 Programmable rectangle wave output by timer/event counter.
PD7 to PD0/ AD7 to AD0	Input-output/ Input-output	Port D 8-bit input-output port, which can specify input-output in byte units (μPD78C11A).	Address/Data Bus When external memory is used, it becomes multiplexed address/data bus.
PF7 to PF0/ AB15 to AB8	Input-output/ Output	Port F 8-bit input-output port, which can specify input-output bit-wise.	Address Bus When external memory is used, it becomes address bus.
$\overline{WR}$ (Write Strobe)	Output	Strobe signal which is output for write operation of external memory. It becomes high in any cycle other than the data write machine cycle of external memory. When $\overline{RESET}$ signal is either low or in the hardware STOP mode, this signal becomes output high-impedance.	
$\overline{RD}$ (Read Strobe)	Output	Strobe signal which is output for read operation of external memory. It becomes high in any cycle other than the read machine cycle of external memory. When $\overline{RESET}$ signal is either low or in the hardware STOP mode, this signal becomes output high-impedance.	
ALE (Address Latch Enable)	Output	Strobe signal to latch externally the lower address information which is output to PD7 to PD0 pins to access external memory. When $\overline{RESET}$ signal is either low or in the hardware STOP mode, this signal becomes output high-impedance.	

1.1 LIST OF PIN FUNCTION (2/2)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>MODE0
MODE1
(Mode)</td><td>Input-output</td><td>μPD78C11A and 78C12A sets MODE0 pin to “0” (low level), and MODE1 pin to “1” (high level*)
μPD78C10A allows you to set MODE0, MODE1 pins to select 4K, 16K, or 64K bytes for the size of the memory which is installed externally.
<table>
<tr><th>MODE0</th><th>MODE1</th><th>External Memory</th></tr>
<tr><td>0</td><td>0</td><td>4K bytes</td></tr>
<tr><td>1</td><td>0</td><td>16K bytes</td></tr>
<tr><td>1</td><td>1</td><td>64K bytes</td></tr>
</table>
Also, when each of MODE0 and MODE1 pins is set to “1”*, it is synchronized to ALE to output a control signal.</td></tr>
<tr><td>$\overline{\text{NMI}}$
(Non-Maskable Interrupt)</td><td>Input</td><td>Non-maskable interrupt input pin of the edge trigger (falling edge)</td></tr>
<tr><td>INT1
(Interrupt Request)</td><td>Input</td><td>A maskable interrupt input pin of the edge trigger (rising edge). Also, it can be used as a zero-cross detection pin for AC input.</td></tr>
<tr><td>AN7 to AN0
(Analog Input)</td><td>Input</td><td>8 pins of analog input to A/D converter. AN7 to AN4 can be used as edge detection (falling edge) input.</td></tr>
<tr><td>V_{AREF}
(Reference Voltage)</td><td>Input</td><td>A common pin serving both as a standard voltage input pin for A/D converter and as a control pin for A/D converter operation.</td></tr>
<tr><td>AV_{DD}
(Analog V_{DD})</td><td></td><td>Power supply pin for A/D converter.</td></tr>
<tr><td>AV_{SS}
(Analog V_{SS})</td><td></td><td>GND pin for A/D converter.</td></tr>
<tr><td>X1, X2
(Crystal)</td><td></td><td>Crystal connection pins for system clock oscillation. X1 should be input when a clock is supplied from outside. Input the clock of the reverse phase of X1 to X2.</td></tr>
<tr><td>$\overline{\text{RESET}}$
(Reset)</td><td>Input</td><td>Low-level active system reset input.</td></tr>
<tr><td>$\overline{\text{STOP}}$
(Stop)</td><td></td><td>Control signal input pin in hardware STOP mode. The oscillation stops when a clock is supplied from outside.</td></tr>
<tr><td>V_{DD}</td><td></td><td>Positive power supply pin.</td></tr>
<tr><td>V_{SS}</td><td></td><td>GND pin.</td></tr>
</table>

★

* Pull-up. Pull-up resister R is 4 [kΩ] ≤ R ≤ 0.4 t_{CYC} [kΩ] (t_{CYC} is ns unit).

Remarks The μPD78C11A and μPD78C12A are pull-up resistor incorporation specifiable by mask option at ports A, B and C.

1.2 PIN INPUT/OUTPUT CIRCUITS

Tables 1-1 and 1-2, and figures (1) to (15) show input- output circuits of each pin in a partially simplified form.

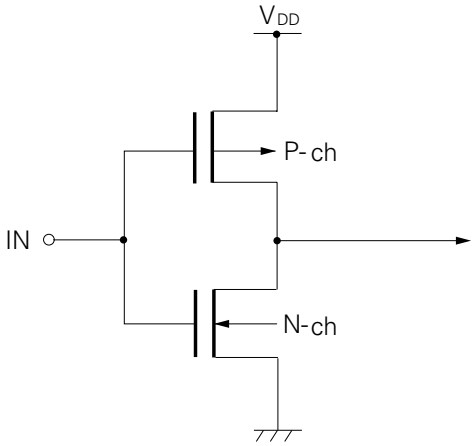
Table 1-1 Pin Type No. (μPD78C10A)

Pin Name	Type No.	Pin Name	Type No.
PA7 to PA0	5	$\overline{\text{RESET}}$	2
PB7 to PB0	5	$\overline{\text{RD}}$	4
PC1 to PC0	5	$\overline{\text{WR}}$	4
PC2/$\overline{\text{SCK}}$	8	ALE	4
PC3/$\overline{\text{INT2}}$	10	$\overline{\text{STOP}}$	2
PC7 to PC4	5	MODE0	11
PD7 to PD0	5	MODE1	11
PF7 to PF0	5	AN3 to AN0	7
$\overline{\text{NMI}}$	5	AN7 to AN4	12
INT1	2	V_{AREF}	13

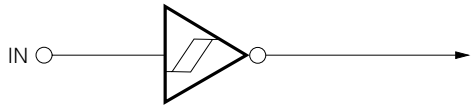
Table 1-2 Pin Type No. (μPD78C11A and 78C12A)

Pin Name	Type No.	Pin Name	Type No.
PA7 to PA0	5-A	$\overline{\text{RESET}}$	2
PB7 to PB0	5-A	$\overline{\text{RD}}$	4
PC1 to PC0	5-A	$\overline{\text{WR}}$	4
PC2/$\overline{\text{SCK}}$	8-A	ALE	4
PC3/$\overline{\text{INT2}}$	10-A	$\overline{\text{STOP}}$	2
PC7 to PC4	5-A	MODE0	11
PD7 to PD0	5	MODE1	11
PF7 to PF0	5	AN3 to AN0	7
$\overline{\text{NMI}}$	2	AN7 to AN4	12
INT1	9	V_{AREF}	13

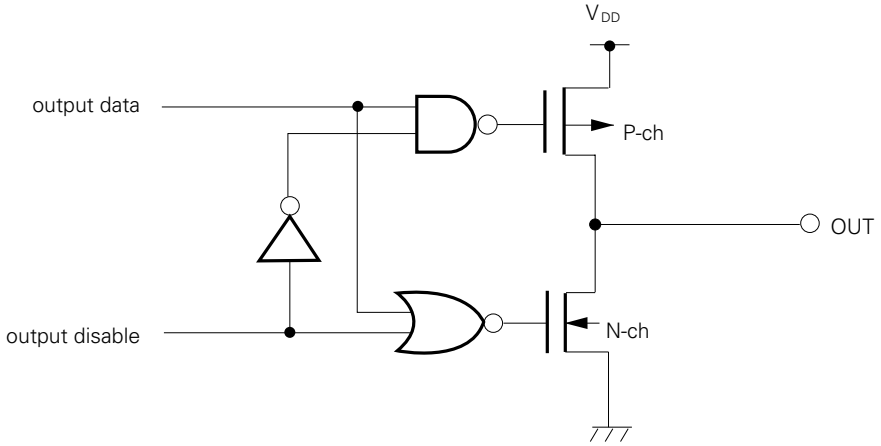
(1) Type 1



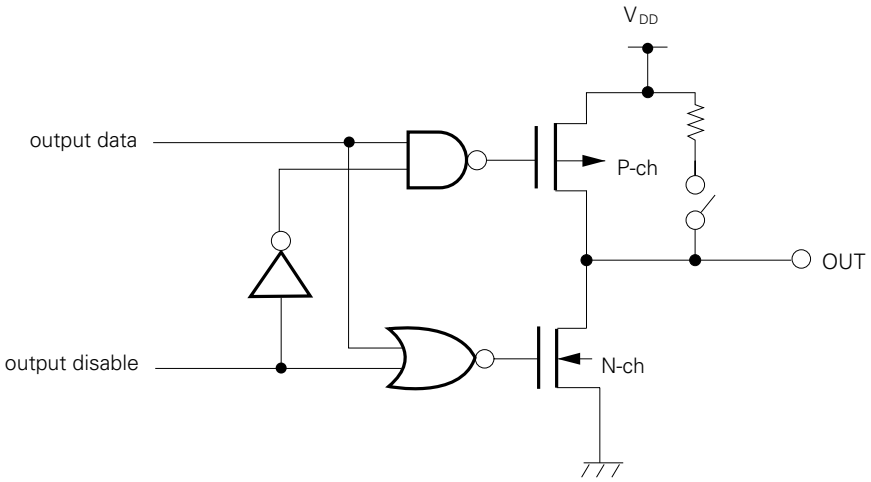
(2) Type 2



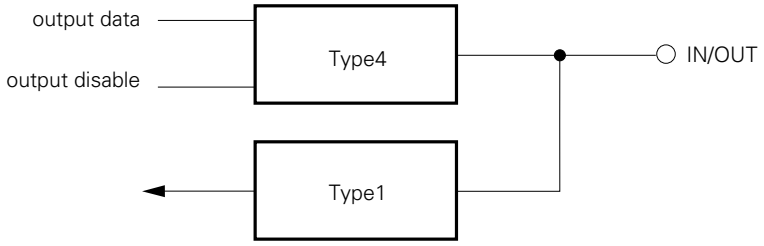
(3) Type 4



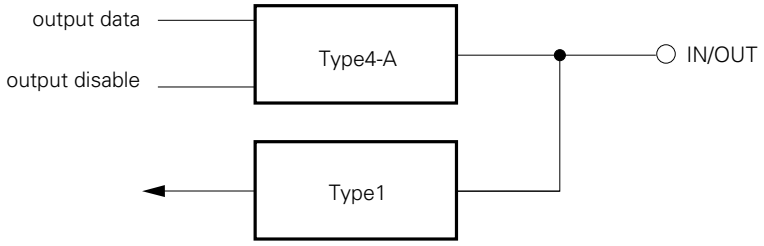
(4) Type 4-A



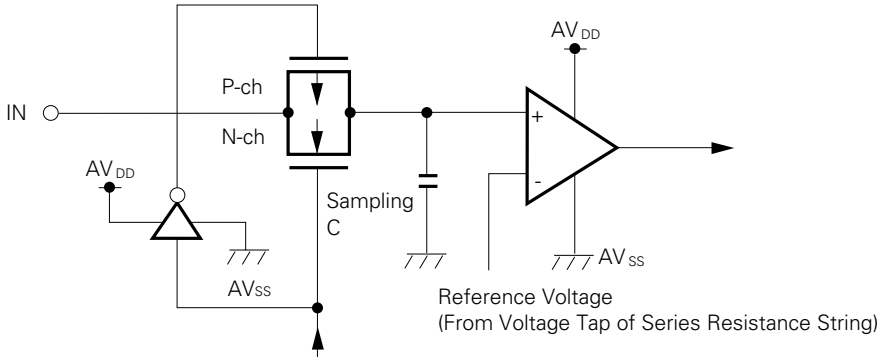
(5) Type 5



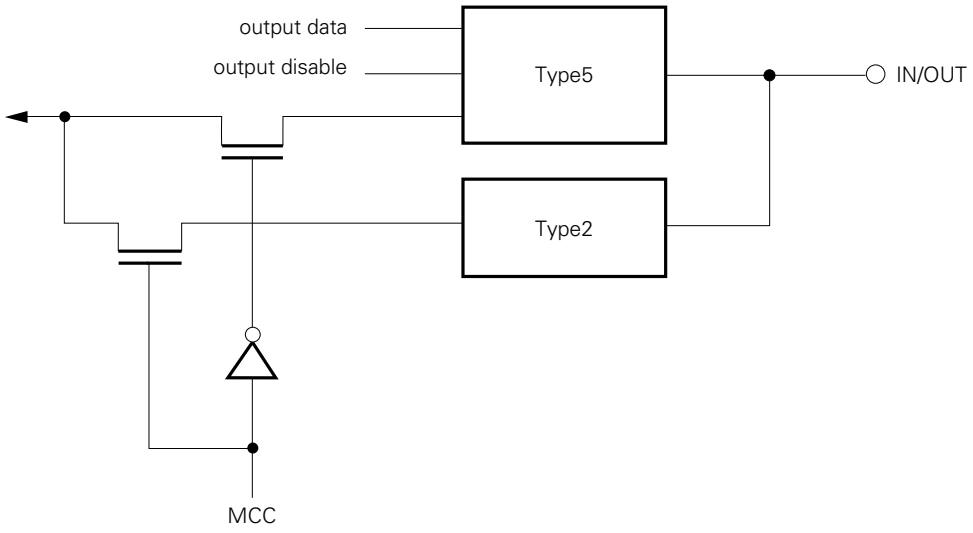
(6) Type 5-A



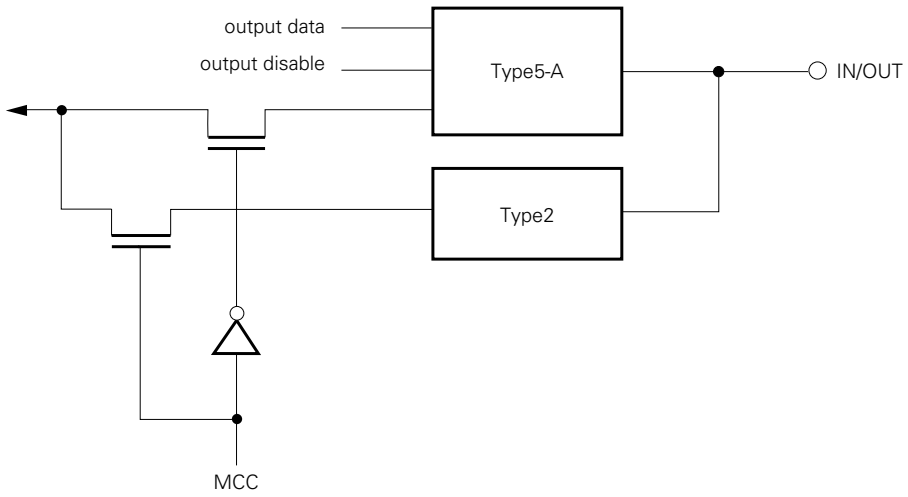
(7) Type 7



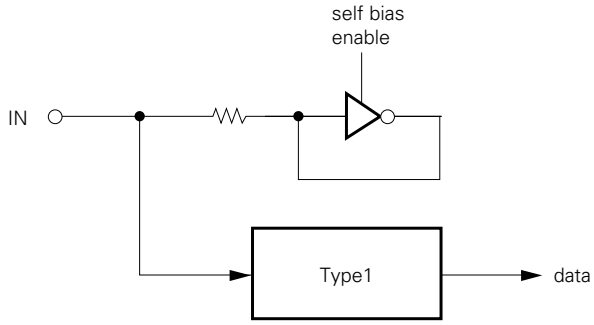
(8) Type 8



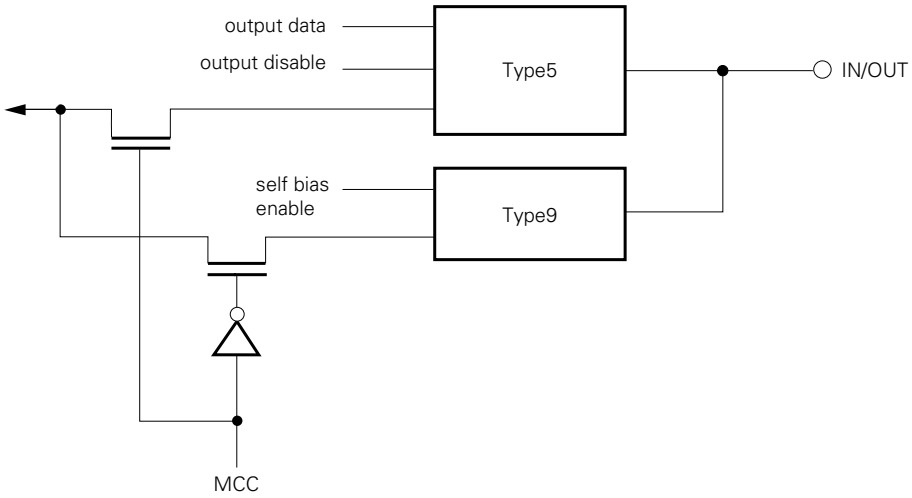
(9) Type 8-A



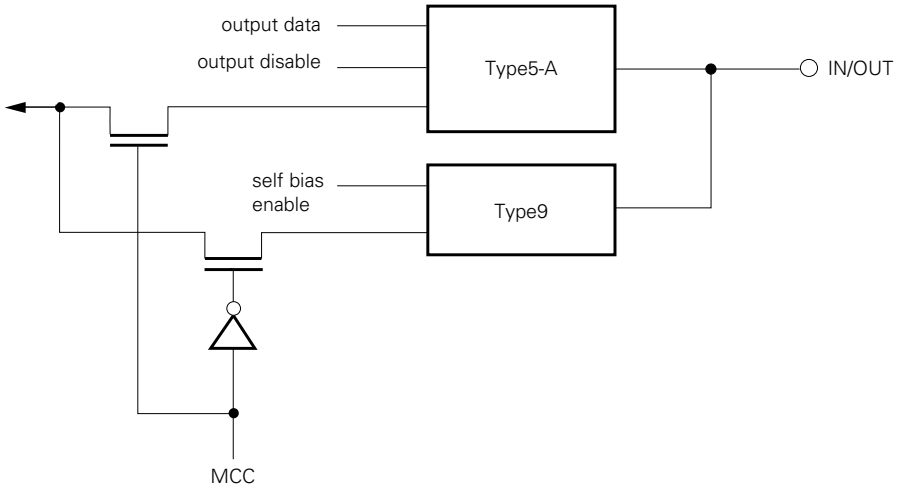
(10) Type 9



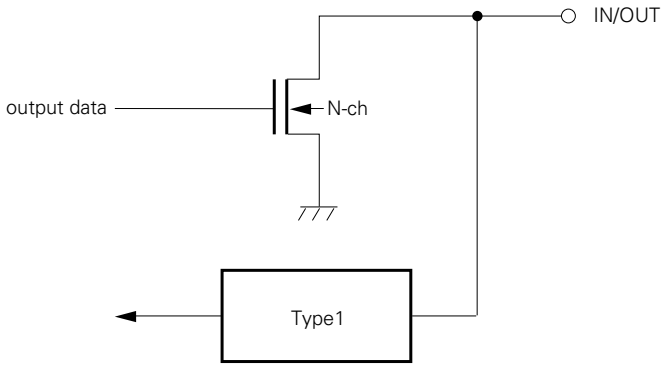
(11) Type 10



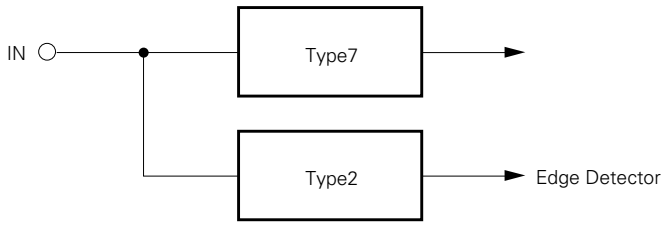
(12) Type 10-A



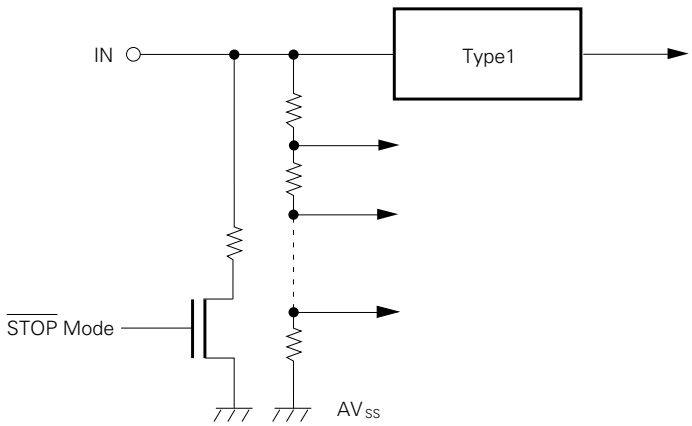
(13) Type 11



(14) Type 12



(15) Type 13



1.3 PIN MASK OPTIONS

μPD78C11A and 78C12A has the following mask options, which can be selected bit-wise according to the application.

Pin Name	Mask Options
PA7 to PA0	① Pull-up resistor incorporated ② Pull-up resistor not incorporated
PB7 to PB0	
PC7 to PC0	

Cautions 1. Zero-cross function can not be operated normally if pull-up resistor is incorporated in PC3.

2. μPD78C10A has no mask option.

1.4 RECOMMENDED CONNECTION OF UNUSED PINS

Pin	Recommended Connection
PA7 to PA0	Connect to V_{SS} or V_{DD} via resistor
PB7 to PB0	
PC7 to PC0	
PD7 to PD0	
PF7 to PF0	
$\overline{RD}$	Leave open
$\overline{WR}$	
ALE	
$\overline{STOP}$	Connect to V_{DD}
INT1, $\overline{NMI}$	Connect to V_{SS} or V_{DD}
AV_{DD}	Connect to V_{DD}
AV_{AREF}	Connect to V_{SS}
AV_{SS}	
AN7 to AN0	Connect to AV_{SS} or AV_{DD}

2. DIFFERENCES BETWEEN μPD78C10A AND μPD78C11A, 78C12A

The difference between the μPD78C10A and μPD78C11A, 78C12A is whether or not there is an on-chip mask programmable ROM. The memory map differs accordingly as described below.

(1) μPD78C10A

Since the μPD78C10A does not have an on-chip ROM, all memory, except the on-chip RAM area (addresses FF00H to FFFFH) can be installed outside. The size of this external memory can be selected from among 4K bytes (0000H to 0FFFH), 16K bytes (0000H to 3FFFH), and 64K bytes (0000H to FEFFH) by MODE0 and MODE1 pin setting as shown in the following table and Fig. 2-1.

Operation Mode	Control Pin		External Memory	On-Chip RAM
	MODE1	MODE0		
4K bytes access	0	0	4K bytes (address 0000H to 0FFFH)	Address FF00H to FFFFH
16K bytes access	0	1	16K bytes (address 0000H to 3FFFH)	Address FF00H to FFFFH
64K bytes access	1	1	64K bytes (address 0000H to FEFFH)	Address FF00H to FFFFH

External memory is accessed by using PD7 to PD0 (multiplexed address/data bus), PF7 to PF0 (address bus), and the $\overline{RD}$, $\overline{WR}$, and ALE signals. When 4K-byte or 16K-byte external memory is accessed PF7 to PF0 not used as address lines can be used as general purpose input/output ports.

The size of external memory can be specified by MODE0 and MODE1 pin setting. Preset each bit of MEMORY MAPPING reisters MM2, MM1, and MM0 to "0".

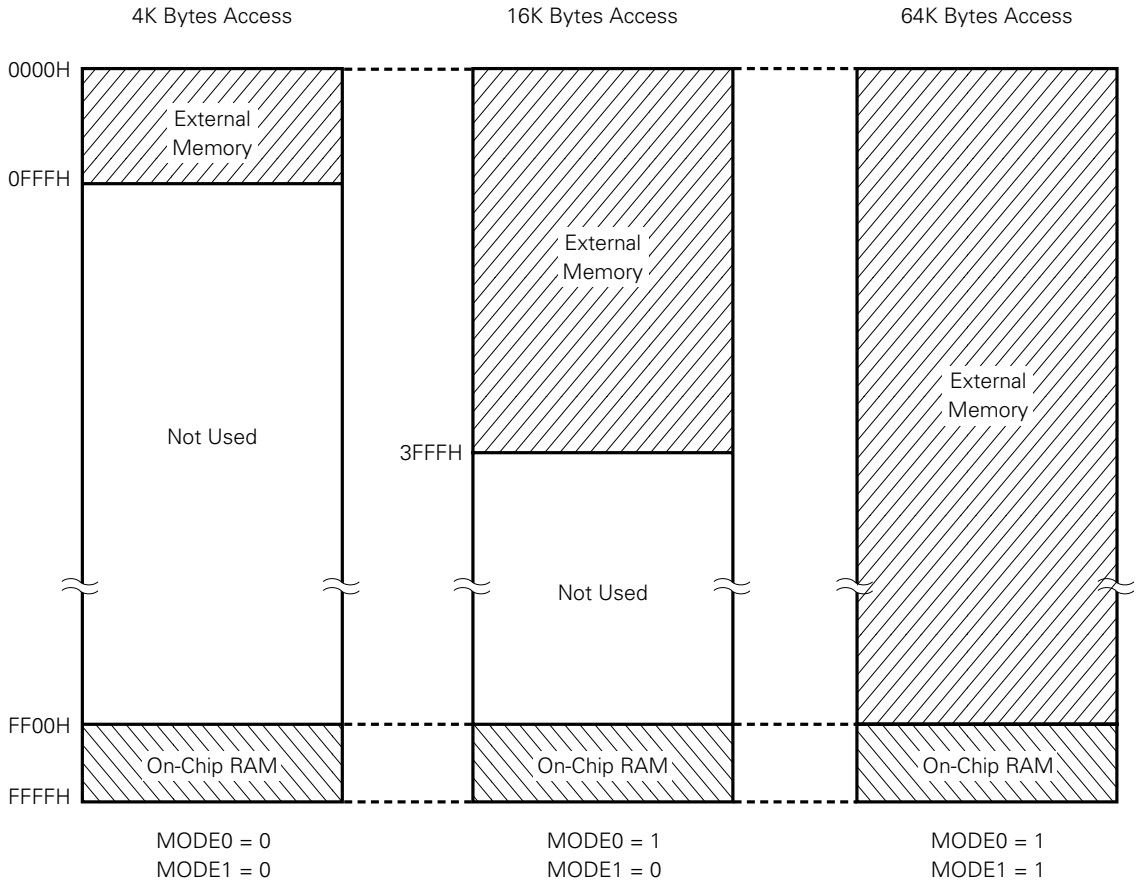
(2) μPD78C11A and 78C12A

The μPD78C11A has an on-chip mask programmable ROM at addresses 0000H to 0FFFH and RAM at addresses FF00H to FFFFH. Externally, memory can be extended up to 60K bytes (addresses 1000H to FEFFH) in steps. The μPD78C12A has an on-chip mask programmable ROM at address 0000H to 1FFFH and RAM at address FF00H to FFFFH. Externally, memory can be extended up to 56K bytes (address 2000H to FEFFH) in steps. The size of the external extension memory can be selected from among no external memory, 256 bytes, 4K bytes, 16K bytes, and 56K/60K bytes* by MEMORY MAPPING register setting. External memory can be accessed by using PD7 to PD0 (multiplexed address/data bus), PF7 to PF0 (address bus), and the $\overline{RD}$, $\overline{WR}$, and ALE signals. Programs and data can be stored in external memory. PF7 to PF0 become address lines corresponding to the size of external memory. The remaining pins can be used as general purpose input/output ports.

PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	External Memory
Port	Port	Port	Port	Port	Port	Port	Port	Maximam 256 bytes
Port	Port	Port	Port	AB11	AB10	AB9	AB8	Maximum 4K bytes
Port	Port	AB13	AB12	AB11	AB10	AB9	AB8	Maximum 16K bytes
AB15	AB14	AB13	AB12	AB11	AB10	AB9	AB8	Maximum 56K/60K bytes*

* μPD78C11A: 60K bytes, μPD78C12A: 56K bytes

Fig. 2-1 μPD78C10A Memory Map



3. RESET OPERATIONS

When $\overline{\text{RESET}}$ Input becomes low, the system reset is activated to create the following status.

- INTERRUPT ENABLE F/F is reset and interrupt is disabled.
- All the interrupt mask registers are set (1) and interrupt is masked.
- An interrupt request flag is reset (0) and hold interrupt is eliminated.
- Each bit of PSW is reset (0).
- 0000H is loaded into the program counter (PC).
- The MODE A, MODE B, MODE C, and MODE F registers are set to FFH and the bits (MM0, 1, and 2) of the MODE CONTROL C and MEMORY MAPPING registers are respectively reset (0), then all the ports (A, B, C, D, and F) become input port (output high-impedance).
- All the test flags but SB flag are reset (0).
- A timer mode register is set to FFH, and TIMER F/F is reset.
- The mode register (ETMM, EOM) of a timer/event counter is reset (0).
- The serial mode high register(SMH) of serial interface is reset (0), while the serial mode low register (SML) is set to 48H.
- The A/D channel mode register of the A/D converter is reset (0).
- $\overline{\text{WR}}$, $\overline{\text{RD}}$, ALE signals become high-impedance.
- The ZC1, ZC2 bits of the zero-cross mode register (ZCM) are set (1).
- The internal timing generator is initialized.
- Data memory and the following register contents are undefined:
  - Stack pointer (SP)
  - Expansion accumulator (EA, EA'), accumulator (A, A')
  - General register (B, C, D, E, H, L, B', C', D', E', H', L')
  - Output latch of each port
  - TIMER REG0, 1 (TM0, TM1)
  - TIMER/EVENT COUNTER REG0, 1 (ETM0, ETM1)
  - RAE bit of MEMORY MAPPING register
  - SB flag of test flag

When $\overline{\text{RESET}}$ input becomes high, the reset status is released. Then, execution of the program is started from 0000H. The contents of various kinds of registers must be initialized or re-initialized in the program, if necessary.

Table 3-1 shows the state of each hardware after reset.

Table 3-2 shows the state of each pin after reset.

Table 3-1 State of Each Hardware after Reset

Hardware				State after Reset
Internal data memory	Power-on reset			Previous contents held.
	Reset input during normal operation	Writing by CPU	Write address data	Undefined
			Address data other than the aboove	Previous contents held.
		Operation other than writing by CPU		
	Reset input in standby mode			
Expansion accumulator (EA, EA')				Undefined
Accumulator (A, A')				
General register (B, C, D, E, H, L, B', C', D', E', H', L')				
Working register vector register (V, V')				
Program counter (PC)				0000H
Stack pointer (SP)				Undefined
Port	Mode register (MA, MB, MC, MF)			FFH
	MCC register			00H
	MM register (bits MM0 to MM2)			0
Output latch of each port				Undefined
Interrupt	INTERRUPT ENABLE F/F			0
	Request flag			0
	Mask register			FFH
Test flag (except SB flag)				0
Standby flag (SB)	Power-on reset			1
	Standby mode			Previous contents held.
	Reset input during normal operation			Contents immediately before $\overline{\text{RESET}}$ input held
Timer	Timer mode register (TMM)			FFH
	Timer F/F			0
	Timer register (TM0, TM1)			Undefined
Timer/event counter	Timer/event counter mode register (ETMM)			00H
	Timer/event counter output mode register (EOM)			
	Timer/event counter register (ETM0, ETM1)			Undefined
	Timer/event counter capture register (ECPT)			
	Timer/event counter (ECNT)			
Serial interface	Serial mode high register (SMH)			00H
	Serial mode low register (SML)			48H
A/D channel mode register (ANM)				00H
MM register (MM3; RAE bit)				Undefined
Zero cross mode register (ZC1, ZC2 bits)				1

Table 3-2 State of Each Pin after Reset

Pin	State after Reset
$\overline{WR}$	High-impedance
$\overline{RD}$	
ALE	
All ports (PA, PB, PC, PD, PF)	

4. INSTRUCTION SET

4.1 IDENTIFIER/DESCRIPTION OF OPERAND

Identifier	Description
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TXB, TM0, TM1, ZCM
sr1	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RXB, CR0, CR1, CR2, CR3
sr2	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM
sr3	ETM0, ETM1
sr4	ECNT, ECPT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D+, H+, D–, H–
rpa1	B, D, H
rpa2	B, D, H, D+, H+, D–, H–, D+byte, H+A, H+B, H+EA, H+byte
rpa3	D, H, D++, H++, D+byte, H+A, H+B, H+EA, H+byte
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	3 bit immediate data
f	CY, HC, Z
irf	NMI*, FT0, FT1, F1, F2, FE0, FE1, FEIN, FAD, FSR, FST, ER, OV, AN4, AN5, AN6, AN7, SB

* NMI can also be described as FNMI.

Remarks

1. sr to sr4 (special register)

PA	:	PORT A	ETMM	:	TIMER/EVENT COUNTER MODE
PB	:	PORT B	EOM	:	TIMER/EVENT COUNTER OUTPUT MODE
PC	:	PORT C	ANM	:	A/D CHANNEL MODE
PD	:	PORT D	CR0 to CR3	:	A/D CONVERSION RESULT 0 to 3
PF	:	PORT F	TXB	:	T_X BUFFER
MA	:	MODE A	RXB	:	R_X BUFFER
MB	:	MODE B	SMH	:	SERIAL MODE High
MC	:	MODE C	SML	:	SERIAL MODE Low
MCC	:	MODE CONTROL C	MKH	:	MASK High
MF	:	MODE F	MKL	:	MASK Low
MM	:	MEMORY MAPPING	ZCM	:	ZERO CROSS MODE
TM0	:	TIMER REG0			
TM1	:	TIMER REG1			
TMM	:	TIMER MODE			
ETM0	:	TIMER/EVENT COUNTER REG0			
ETM1	:	TIMER/EVENT COUNTER REG1			
ECNT	:	TIMER/EVENT COUNTER UPCOUNTER			
ECPT	:	TIMER/EVENT COUNTER CAPTURE			

2. rp to rp3 (register pair)

SP	:	STACK POINTER
B	:	BC
D	:	DE
H	:	HL
V	:	VA
EA	:	EXTENDED ACCUMULATOR

3. rpa to rpa3 (rp addressing)

B	:	(BC)
D	:	(DE)
H	:	(HL)
D+	:	(DE)+
H+	:	(HL)+
D–	:	(DE)–
H–	:	(HL)–
D++	:	(DE)++
H++	:	(HL)++
D + byte	:	(DE + byte)
H + A	:	(HL + A)
H + B	:	(HL + B)
H + EA	:	(HL + EA)
H + byte	:	(HL + byte)

4. f (flag)

CY	:	CARRY
HC	:	HALF CARRY
Z	:	ZERO

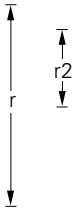
5. irf (interrupt flag)

NMI	:	NMI INPUT
FT0	:	INTFT0
FT1	:	INTFT1
F1	:	INTF1
F2	:	INTF2
FE0	:	INTFE0
FE1	:	INTFE1
FEIN	:	INTFEIN
FAD	:	INTFAD
FSR	:	INTFSR
FST	:	INTFST
ER	:	ERROR
OV	:	OVERFLOW
AN4 to AN7	:	ANALOG INPUT 4 to 7
SB	:	STANDBY

4.2 SYMBOL DESCRIPTION OF OPERATION CODE

r

R_2	R_1	R_0	reg
0	0	0	V
0	0	1	A
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

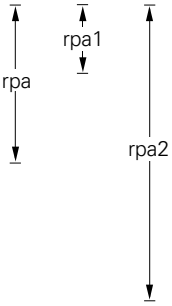


r1

T_2	T_1	T_0	reg
0	0	0	EAH
0	0	1	EAL
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

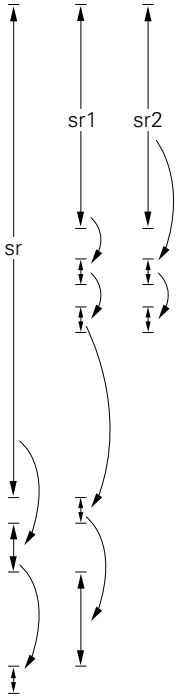
rpa

A_3	A_2	A_1	A_0	addressing
0	0	0	0	———
0	0	0	1	(BC)
0	0	1	0	(DE)
0	0	1	1	(HL)
0	1	0	0	(DE)+
0	1	0	1	(HL)+
0	1	1	0	(DE)-
0	1	1	1	(HL)-
1	0	1	1	(DE + byte)
1	1	0	0	(HL + A)
1	1	0	1	(HL + B)
1	1	1	0	(HL + EA)
1	1	1	1	(HL + byte)



sr

S_5	S_4	S_3	S_2	S_1	S_0	Special-reg
0	0	0	0	0	0	PA
0	0	0	0	0	1	PB
0	0	0	0	1	0	PC
0	0	0	0	1	1	PD
0	0	0	1	0	1	PF
0	0	0	1	1	0	MKH
0	0	0	1	1	1	MKL
0	0	1	0	0	0	ANM
0	0	1	0	0	1	SMH
0	0	1	0	1	0	SML
0	0	1	0	1	1	EOM
0	0	1	1	0	0	ETMM
0	0	1	1	0	1	TMM
0	1	0	0	0	0	MM
0	1	0	0	0	1	MCC
0	1	0	0	1	0	MA
0	1	0	0	1	1	MB
0	1	0	1	0	0	MC
0	1	0	1	1	1	MF
0	1	1	0	0	0	TXB
0	1	1	0	0	1	RXB
0	1	1	0	1	0	TM0
0	1	1	0	1	1	TM1
1	0	0	0	0	0	CR0
1	0	0	0	0	1	CR1
1	0	0	0	1	0	CR2
1	0	0	0	1	1	CR3
1	0	1	0	0	0	ZCM



rpa3

C_3	C_2	C_1	C_0	addressing
0	0	1	0	(DE)
0	0	1	1	(HL)
0	1	0	0	(DE)++
0	1	0	1	(HL)++
1	0	1	1	(DE + byte)
1	1	0	0	(HL + A)
1	1	0	1	(HL + B)
1	1	1	0	(HL + EA)
1	1	1	1	(HL + byte)

irf

I_4	I_3	I_2	I_1	I_0	INTF
0	0	0	0	0	NMI
0	0	0	0	1	FT0
0	0	0	1	0	FT1
0	0	0	1	1	F1
0	0	1	0	0	F2
0	0	1	0	1	FE0
0	0	1	1	0	FE1
0	0	1	1	1	FEIN
0	1	0	0	0	FAD
0	1	0	0	1	FSR
0	1	0	1	0	FST
0	1	0	1	1	ER
0	1	1	0	0	OV
1	0	0	0	0	AN4
1	0	0	0	1	AN5
1	0	0	1	0	AN6
1	0	0	1	1	AN7
1	0	1	0	0	SB

sr3

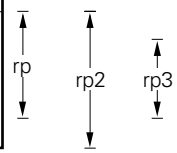
U_0	special-reg
0	ETM0
1	ETM1

sr4

V_0	special-reg
0	ECNT
1	ECPT

rp

P_2	P_1	P_0	reg-pair
0	0	0	SP
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA



rp1

Q_2	Q_1	Q_0	reg-pair
0	0	0	VA
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA

f

F_2	F_1	F_0	flag
0	0	0	——
0	1	0	CY
0	1	1	HC
1	0	0	Z

4.3 INSTRUCTION EXECUTION TIME

1 state shown here is composed of 3 clock cycles. When a clock cycle of 15 MHz is used, the execution time should be 200 ns (= 3 × 1/15 μs). In this case, the 4-state instruction which is the minimum execution time should be execution time of 0.8 μs.

Note 1	Mnemonic		Operand	Operation Code B1	B2	B3	B4	State	Operation	Skip Condition
8-bit data transfer instructions	MOV		r1, A	0 0 0 1 1 T_2 T_1 T_0				4	r1 ← A	
			A, r1	0 0 0 0 1 T_2 T_1 T_0				4	A ← r1	
		*	sr, A	0 1 0 0 1 1 0 1	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	sr ← A	
		*	A, sr1	0 1 0 0 1 1 0 0	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	A ← sr1	
			r, word	0 1 1 1 0 0 0 0	0 1 1 0 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	r ← (word)	
			word, r	0 1 1 1 0 0 0 0	0 1 1 1 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	(word) ← r	
	MVI	*	r, byte	0 1 1 0 1 R_2 R_1 R_0	←Data→			7	r ← byte	
			sr2, byte	0 1 1 0 0 1 0 0	S_3 0 0 0 0 S_2 S_1 S_0	Data		14	sr2 ← byte	
	MVIW	*	wa, byte	0 1 1 1 0 0 0 1	←Offset→	Data		13	(V. wa) ← byte	
	MVIX	*	rpa1, byte	0 1 0 0 1 0 A_1 A_0	←Data→			10	(rpa1) ← byte	
	STAW	*	wa	0 1 1 0 0 0 1 1	←Offset→			10	(V. wa) ← A	
	LDAW	*	wa	0 0 0 0 0 0 0 1	←Offset→			10	A ← (V. wa)	
	STAX	*	rpa2	A_3 0 1 1 1 A_2 A_1 A_0	Data***1***			7/13***3***	(rpa2) ← A	
	LDAX	*	rpa2	A_3 0 1 0 1 A_2 A_1 A_0	Data***1***			7/13***3***	A ← (rpa2)	
	EXX			0 0 0 1 0 0 0 1				4	B ↔ B', C ↔ C', D ↔ D' E ↔ E', H ↔ H', L ↔ L'	
	EXA			0 0 0 1 0 0 0 0				4	V, A ↔ V', A', EA ↔ EA'	
	EXH			0 1 0 1 0 0 0 0				4	H, L ↔ H', L'	
	BLOCK			0 0 1 1 0 0 0 1				13 (C + 1)	$(DE)^+ \leftarrow (HL)^+$, C ← C – 1 End if borrow	
Note 2	DMOV		rp3, EA	1 0 1 1 0 1 P_1 P_0				4	$rp3_L$ ← EAL, $rp3_H$ ← EAH	
			EA, rp3	1 0 1 0 0 1 P_1 P_0				4	EAL ← $rp3_L$, EAH ← $rp3_H$	

Note **1.** Instruction Group

2. 16-bit data transfer instructions

Note 1	Mnemonic	Operand	Operation Code B1	Operation Code B2	Operation Code B3	Operation Code B4	State	Operation	Skip Condition
16-bit data transfer instructions	DMOV	sr3, EA	0 1 0 0 1 0 0 0	1 1 0 1 0 0 1 U_0			14	sr3 ← EA	
		EA, sr4		1 1 0 0 0 0 0 V_0			14	EA ← sr4	
	SBCD	word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 0	Low Adrs	High Adrs	20	(word) ← C, (word + 1) ← B	
	SDED	word		0 0 1 0 1 1 1 0			20	(word) ← E, (word + 1) ← D	
	SHLD	word		0 0 1 1 1 1 1 0			20	(word) ← L, (word + 1) ← H	
	SSPD	word		0 0 0 0 1 1 1 0			20	(word) ← SP_L, (word + 1) ← SP_H	
	STEAX	rpa3	0 1 0 0 1 0 0 0	1 0 0 1 C_3 C_2 C_1 C_0	Data*2		14/20*3	(rpa3) ← EAL, (rpa3 + 1) ← EAH	
	LBCD	word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 1	Low Adrs	High Adrs	20	C ← (word), B ← (word + 1)	
	LDED	word		0 0 1 0 1 1 1 1			20	E ← (word), D ← (word + 1)	
	LHLD	word		0 0 1 1 1 1 1 1			20	L ← (word), H ← (word + 1)	
	LSPD	word		0 0 0 0 1 1 1 1			20	SP_L ← (word), SP_H ← (word + 1)	
	LDEAX	rpa3	0 1 0 0 1 0 0 0	1 0 0 0 C_3 C_2 C_1 C_0	Data*2		14/20*3	EAL ← (rpa3), EAH ← (rpa3 + 1)	
	PUSH	rp1	1 0 1 1 0 Q_2 Q_1 Q_0				13	(SP – 1) ← $rp1_H$, (SP – 2) ← $rp1_L$ SP ← SP – 2	
	POP	rp1	1 0 1 0 0 Q_2 Q_1 Q_0				10	$rp1_L$ ← (SP), $rp1_H$ ← (SP + 1) SP ← SP + 2	
	LXI *	rp2, word	0 P_2 P_1 P_0 0 1 0 0	←Low Byte→	High Byte		10	rp2 ← word	
	TABLE		0 1 0 0 1 0 0 0	1 0 1 0 1 0 0 0			17	C ← (PC + 3 + A) B ← (PC + 3 + A + 1)	
Note 2	ADD	A, r	0 1 1 0 0 0 0 0	1 1 0 0 0 R_2 R_1 R_0			8	A ← A + r	
		r, A		0 1 0 0			8	r ← r + A	
	ADC	A, r		1 1 0 1			8	A ← A + r + CY	
		r, A		0 1 0 1			8	r ← r + A + CY	

Note **1.** Instruction Group

2. 8-bit operation instructions (register)

Note	Mnemonic	Operand	Operation Code B1	Operation Code B2	Operation Code B3	Operation Code B4	State	Operation	Skip Condition
8-bit operation instructions (register)	ADDNC	A, r	0 1 1 0 0 0 0 0	1 0 1 0 0 R_2 R_1 R_0			8	A ← A + r	No Carry
		r, A		0 0 1 0			8	r ← r + A	No Carry
	SUB	A, r		1 1 1 0			8	A ←A – r	
		r, A		0 1 1 0			8	r ← r – A	
	SBB	A, r		1 1 1 1			8	A ← A – r – CY	
		r, A		0 1 1 1			8	r ← r – A – CY	
	SUBNB	A, r		1 0 1 1			8	A ← A – r	No Borrow
		r, A		0 0 1 1			8	r ← r – A	No Borrow
	ANA	A, r		1 0 0 0 1 R_2 R_1 R_0			8	A ← A ∧ r	
		r, A		0 0 0 0			8	r ← r ∧ A	
	ORA	A, r		1 0 0 1			8	A ← A ∨ r	
		r, A		0 0 0 1			8	r ← r ∨ A	
	XRA	A, r		1 0 0 1 0 R_2 R_1 R_0			8	A ← A ⊻ r	
		r, A		0 0 0 1			8	r ← r ⊻ A	
	GTA	A, r		1 0 1 0 1 R_2 R_1 R_0			8	A – r – 1	No Borrow
		r, A		0 0 1 0			8	r – A – 1	No Borrow
	LTA	A, r		1 0 1 1			8	A – r	Borrow
		r, A		0 0 1 1			8	r – A	Borrow
	NEA	A, r		1 1 1 0			8	A – r	No Zero
		r, A		0 1 1 0			8	r – A	No Zero

Note Instruction Group

Note	Mnemonic	Operand	Operation Code B1	Operation Code B2	Operation Code B3	Operation Code B4	State	Operation	Skip Condition
8-bit operation instructions (register)	EQA	A, r	0 1 1 0 0 0 0 0	1 1 1 1 1 R_2 R_1 R_0			8	A – r	Zero
		r, A		0 1 1 1			8	r – A	Zero
	ONA	A, r		1 1 0 0			8	A ∧ r	No Zero
	OFFA	A, r		1 1 0 1			8	A ∧ r	Zero
8-bit operation instructions (memory)	ADDX	rpa	0 1 1 1 0 0 0 0	1 1 0 0 0 A_2 A_1 A_0			11	A ← A + (rpa)	
	ADCX	rpa		1 1 0 1			11	A ← A + (rpa) + CY	
	ADDNCX	rpa		1 0 1 0			11	A ← A + (rpa)	No Carry
	SUBX	rpa		1 1 1 0			11	A ← A – (rpa)	
	SBBX	rpa		1 1 1 1			11	A ← A – (rpa) – CY	
	SUBNBX	rpa		1 0 1 1			11	A ← A – (rpa)	No Borrow
	ANAX	rpa		1 0 0 0 1 A_2 A_1 A_0			11	A ← A ∧ (rpa)	
	ORAX	rpa		1 0 0 1			11	A ← A ∨ (rpa)	
	XRAX	rpa		1 0 0 1 0 A_2 A_1 A_0			11	A ← A ⊻ (rpa)	
	GTAX	rpa		1 0 1 0 1 A_2 A_1 A_0			11	A – (rpa) – 1	No Borrow
	LTAX	rpa		1 0 1 1			11	A – (rpa)	Borrow
	NEAX	rpa		1 1 1 0			11	A – (rpa)	No Zero
	EQAX	rpa		1 1 1 1			11	A – (rpa)	Zero
	ONAX	rpa		1 1 0 0			11	A ∧ (rpa)	No Zero
	OFFAX	rpa		1 1 0 1			11	A ∧ (rpa)	Zero

Note Instruction Group

Note	Mnemonic	Operand	Operation Code B1	Operation Code B2	Operation Code B3	Operation Code B4	State	Operation	Skip Condition
Immediate data operation instructions	ADI *	A, byte	0 1 0 0 0 1 1 0	←Data→			7	A ← A + byte	
		r, byte	0 1 1 1 0 1 0 0	0 1 0 0 0 R_2 R_1 R_0	Data		11	r ← r + byte	
		sr2, byte	0 1 1 0 ↓	S_3 1 0 0 0 S_2 S_1 S_0	↓		20	sr2 ← sr2 + byte	
	ACI *	A, byte	0 1 0 1 0 1 1 0	←Data→			7	A ← A + byte + CY	
		r, byte	0 1 1 1 0 1 0 0	0 1 0 1 0 R_2 R_1 R_0	Data		11	r ← r + byte + CY	
		sr2, byte	0 1 1 0 ↓	S_3 1 0 1 0 S_2 S_1 S_0	↓		20	sr2 ← sr2 + byte + CY	
	ADINC *	A, byte	0 0 1 0 0 1 1 0	←Data→			7	A ← A + byte	No Carry
		r, byte	0 1 1 1 0 1 0 0	0 0 1 0 0 R_2 R_1 R_0	Data		11	r ← r + byte	No Carry
		sr2, byte	0 1 1 0 ↓	S_3 0 1 0 0 S_2 S_1 S_0	↓		20	sr2 ← sr2 + byte	No Carry
	SUI *	A, byte	0 1 1 0 0 1 1 0	←Data→			7	A ← A – byte	
		r, byte	0 1 1 1 0 1 0 0	0 1 1 0 0 R_2 R_1 R_0	Data		11	r ← r – byte	
		sr2, byte	0 1 1 0 ↓	S_3 1 1 0 0 S_2 S_1 S_0	↓		20	sr2 ← sr2 – byte	
	SBI *	A, byte	0 1 1 1 0 1 1 0	←Data→			7	A ← A – byte – CY	
		r, byte	0 1 1 1 0 1 0 0	0 1 1 1 0 R_2 R_1 R_0	Data		11	r ← r – byte – CY	
		sr2, byte	0 1 1 0 ↓	S_3 1 1 1 0 S_2 S_1 S_0	↓		20	sr2 ← sr2 – byte – CY	
	SUINB *	A, byte	0 0 1 1 0 1 1 0	←Data→			7	A ← A – byte	No Borrow
		r, byte	0 1 1 1 0 1 0 0	0 0 1 1 0 R_2 R_1 R_0	Data		11	r ← r – byte	No Borrow
		sr2, byte	0 1 1 0 ↓	S_3 0 1 1 0 S_2 S_1 S_0	↓		20	sr2 ← sr2 – byte	No Borrow
	ANI *	A, byte	0 0 0 0 0 1 1 1	←Data→			7	A ← A ∧ byte	
		r, byte	0 1 1 1 0 1 0 0	0 0 0 0 1 R_2 R_1 R_0	Data		11	r ← r ∧ byte	

Note Instruction Group

Note	Mnemonic	Operand	Operation Code B1	Operation Code B2	Operation Code B3	Operation Code B4	State	Operation	Skip Condition
Immediate data operation instructions	ANI	sr2, byte	0 1 1 0 0 1 0 0	S_3 0 0 0 1 S_2 S_1 S_0	Data		20	sr2 ← sr2 ∧ byte	
	ORI *	A, byte	0 0 0 1 0 1 1 1	←Data→			7	A ← A ∨ byte	
	ORI	r, byte	0 1 1 1 0 1 0 0	0 0 0 1 1 R_2 R_1 R_0	Data		11	r ← r ∨ byte	
	ORI	sr2, byte	0 1 1 0 ↓	S_3 0 0 1 1 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨ byte	
	XRI *	A, byte	0 0 0 1 0 1 1 0	←Data→			7	A ← A ⊻ byte	
	XRI	r, byte	0 1 1 1 0 1 0 0	0 0 0 1 0 R_2 R_1 R_0	Data		11	r ← r ⊻ byte	
	XRI	sr2, byte	0 1 1 0 ↓	S_3 0 0 1 0 S_2 S_1 S_0	↓		20	sr2 ← sr2 ⊻ byte	
	GTI *	A, byte	0 0 1 0 0 1 1 1	←Data→			7	A – byte– 1	No Borrow
	GTI	r, byte	0 1 1 1 0 1 0 0	0 0 1 0 1 R_2 R_1 R_0	Data		11	r – byte – 1	No Borrow
	GTI	sr2, byte	0 1 1 0 ↓	S_3 0 1 0 1 S_2 S_1 S_0	↓		14	sr2 – byte – 1	No Borrow
	LTI *	A, byte	0 0 1 1 0 1 1 1	←Data→			7	A – byte	Borrow
	LTI	r, byte	0 1 1 1 0 1 0 0	0 0 1 1 1 R_2 R_1 R_0	Data		11	r – byte	Borrow
	LTI	sr2, byte	0 1 1 0 ↓	S_3 0 1 1 1 S_2 S_1 S_0	↓		14	sr2 – byte	Borrow
	NEI *	A, byte	0 1 1 0 0 1 1 1	←Data→			7	A – byte	No Zero
	NEI	r, byte	0 1 1 1 0 1 0 0	0 1 1 0 1 R_2 R_1 R_0	Data		11	r – byte	No Zero
	NEI	sr2, byte	0 1 1 0 ↓	S_3 1 1 0 1 S_2 S_1 S_0	↓		14	sr2 – byte	No Zero
	EQI *	A, byte	0 1 1 1 0 1 1 1	←Data→			7	A – byte	Zero
	EQI	r, byte	0 1 1 1 0 1 0 0	0 1 1 1 1 R_2 R_1 R_0	Data		11	r – byte	Zero
	EQI	sr2, byte	0 1 1 0 ↓	S_3 1 1 1 1 S_2 S_1 S_0	↓		14	sr2 – byte	Zero

Note Instruction Group

Note	Mnemonic	Operand	Operation Code B1	Operation Code B2	Operation Code B3	Operation Code B4	State	Operation	Skip Condition
Immediate data operation instructions	ONI *	A, byte	0 1 0 0 0 1 1 1	← Data →			7	A ∧ byte	No Zero
		r, byte	0 1 1 1 0 1 0 0	0 1 0 0 1 R_2 R_1 R_0	Data		11	r ∧ byte	No Zero
		sr2, byte	0 1 1 0 ↓	S_3 1 0 0 1 S_2 S_1 S_0	↓		14	sr2 ∧ byte	No Zero
	OFFI *	A, byte	0 1 0 1 0 1 1 1	← Data →			7	A ∧ byte	Zero
		r, byte	0 1 1 1 0 1 0 0	0 1 0 1 1 R_2 R_1 R_0	Data		11	r ∧ byte	Zero
		sr2, byte	0 1 1 0 ↓	S_3 1 0 1 1 S_2 S_1 S_0	↓		14	sr2 ∧ byte	Zero
Working register operation instructions	ADDW	wa	0 1 1 1 0 1 0 0	1 1 0 0 0 0 0 0	offset		14	A ← A +(V. wa)	
	ADCW	wa	↓ ↓ ↓	1 1 0 1	↓		14	A ← A + (V. wa) + CY	
	ADDNCW	wa	↓ ↓ ↓	1 0 1 0	↓		14	A ← A + (V. wa)	No Carry
	SUBW	wa	↓ ↓ ↓	1 1 1 0	↓		14	A ← A – (V. wa)	
	SBBW	wa	↓ ↓ ↓	1 1 1 1	↓		14	A ← A – (V. wa) – CY	
	SUBNBW	wa	↓ ↓ ↓	1 0 1 1 ↓	↓		14	A ← A – (V. wa)	No Borrow
	ANAW	wa	↓ ↓ ↓	1 0 0 0 1 0 0 0	↓		14	A ← A ∧ (V. wa)	
	ORAW	wa	↓ ↓ ↓	1 0 0 1 ↓	↓		14	A ← A ∨ (V. wa)	
	XRAW	wa	↓ ↓ ↓	1 0 0 1 0 0 0 0	↓		14	A ← A ⊻ (V. wa)	
	GTAW	wa	↓ ↓ ↓	1 0 1 0 1 0 0 0	↓		14	A – (V. wa) – 1	No Borrow
	LTAW	wa	↓ ↓ ↓	1 0 1 1	↓		14	A – (V. wa)	Borrow
	NEAW	wa	↓ ↓ ↓	1 1 1 0	↓		14	A – (V. wa)	No Zero
	EQAW	wa	↓ ↓ ↓	1 1 1 1	↓		14	A – (V. wa)	Zero
	ONAW	wa	↓ ↓ ↓	1 1 0 0 ↓	↓		14	A ∧ (V. wa)	No Zero

Note Instruction Group

Note	Mnemonic	Operand	Operation Code B1	B2	B3	B4	State	Operation	Skip Condition
Working register operation instructions	OFFAW	wa	0 1 1 1 0 1 0 0	1 1 0 1 1 0 0 0	Offset		14	A ∧ (V. wa)	Zero
	ANIW *	wa, byte	0 0 0 0 0 1 0 1	← Offset →	Data		19	(V. wa) ← (V. wa) ∧ byte	
	ORIW *	wa, byte	0 0 0 1				19	(V. wa) ← (V. wa) ∨ byte	
	GTIW *	wa, byte	0 0 1 0				13	(V. wa) – byte – 1	No Borrow
	LTIW *	wa, byte	0 0 1 1				13	(V. wa) – byte	Borrow
	NEIW *	wa, byte	0 1 1 0				13	(V. wa) – byte	No Zero
	EQIW *	wa, byte	0 1 1 1				13	(V. wa) – byte	Zero
	ONIW *	wa, byte	0 1 0 0				13	(V. wa) ∧ byte	No Zero
	OFFIW	wa, byte	0 1 0 1				13	(V. wa) ∧ byte	Zero
16-bit operation instructions	EADD	EA, r2	0 1 1 1 0 0 0 0	0 1 0 0 0 0 R_1 R_0			11	EA ← EA + r2	
	DADD	EA, rp3	0 1 0 0	1 1 0 0 0 1 P_1 P_0			11	EA ← EA + rp3	
	DADC	EA, rp3		1 1 0 1			11	EA ← EA + rp3 +CY	
	DADDNC	EA, rp3		1 0 1 0			11	EA ← EA + rp3	No Carry
	ESUB	EA, r2	0 0 0 0	0 1 1 0 0 0 R_1 R_0			11	EA ← EA – r2	
	DSUB	EA, rp3	0 1 0 0	1 1 1 0 0 1 P_1 P_0			11	EA ← EA – rp3	
	DSBB	EA, rp3		1 1 1 1			11	EA ← EA – rp3 – CY	
	DSUBNB	EA, rp3		1 0 1 1			11	EA ← EA – rp3	No Borrow
	DAN	EA, rp3		1 0 0 0 1 1 P_1 P_0			11	EA ← EA ∧ rp3	
	DOR	EA, rp3		1 0 0 1			11	EA ← EA ∨ rp3	
	DXR	EA, rp3		1 0 0 1 0 1 P_1 P_0			11	EA ← EA ⊻ rp3	

Note Instruction Group

Note 1	Mnemonic	Operand	Operation Code B1	Operation Code B2	Operation Code B3	Operation Code B4	State	Operation	Skip Condition
16-bit operation instructions	DGT	EA, rp3	0 1 1 1 0 1 0 0	1 0 1 0 1 1 P_1 P_0			11	EA – rp3 – 1	No Borrow
	DLT	EA, rp3		1 0 1 1			11	EA – rp3	Borrow
	DNE	EA, rp3		1 1 1 0			11	EA – rp3	No Zero
	DEQ	EA, rp3		1 1 1 1			11	EA – rp3	Zero
	DON	EA, rp3		1 1 0 0			11	EA ∧ rp3	No Zero
	DOFF	EA, rp3		1 1 0 1			11	EA ∧ rp3	Zero
Note 2	MUL	r2	0 1 0 0 1 0 0 0	0 0 1 0 1 1 R_1 R_0			32	EA ← A × r2	
	DIV	r2		0 0 1 1			59	EA ← EA ÷ r2, r2 ← Remainder	
Increment/decrement instructions	INR	r2	0 1 0 0 0 0 R_1 R_0				4	r2 ← r2 + 1	Carry
	INRW *	wa	0 0 1 0 0 0 0 0	← Offset →			16	(V. wa) ← (V. wa) + 1	Carry
	INX	rp	0 0 P_1 P_0 0 0 1 0				7	rp ← rp + 1	
		EA	1 0 1 0 1 0 0 0				7	EA ← EA + 1	
	DCR	r2	0 1 0 1 0 0 R_1 R_0				4	r2 ← r2 – 1	Borrow
	DCRW *	wa	0 0 1 1 0 0 0 0	← Offset →			16	(V. wa) ← (V. wa) – 1	Borrow
	DCX	rp	0 0 P_1 P_0 0 0 1 1				7	rp ← rp – 1	
		EA	1 0 1 0 1 0 0 1				7	EA ← EA – 1	
Note 3	DAA		0 1 1 0 0 0 0 1				4	Decimal Adjust Accumulator	
	STC		0 1 0 0 1 0 0 0	0 0 1 0 1 0 1 1			8	CY ← 1	
	CLC			0 0 1 0 1 0 1 0			8	CY ← 0	
	NEGA			0 0 1 1 1 0 1 0			8	A ← $\overline{A}$ + 1	

Note **1.** Instruction Group
2. Multiplication/division instructions
3. Other operation instructions

Note	Mnemonic	Operand	Operation Code B1	Operation Code B2	Operation Code B3	Operation Code B4	State	Operation	Skip Condition
Rotation/shift instructions	RLD		0 1 0 0 1 0 0 0	0 0 1 1 1 0 0 0			17	Rotate Left Digit	
	RRD			1 0 0 1			17	Rotate Right Digit	
	RLL	r2		0 1 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow CY$, $CY \leftarrow r2_7$	
	RLR	r2		0 0 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow CY$, $CY \leftarrow r2_0$	
	SLL	r2		0 0 1 0 0 1 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	
	SLR	r2		0 0 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	
	SLLC	r2		0 0 0 0 0 1 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	Carry
	SLRC	r2		0 0 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	Carry
	DRLL	EA		1 0 1 1 0 1 0 0			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow CY$, $CY \leftarrow EA_{15}$	
	DRLR	EA		0 0 0 0			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow CY$, $CY \leftarrow EA_0$	
	DSLL	EA		1 0 1 0 0 1 0 0			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow 0$, $CY \leftarrow EA_{15}$	
	DSLR	EA		0 0 0 0			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow 0$, $CY \leftarrow EA_0$	
Jump instructions	JMP *	word	0 1 0 1 0 1 0 0	← Low Adrs →	High Adrs		10	PC ← word	
	JB		0 0 1 0 0 0 0 1				4	$PC_H \leftarrow B$, $PC_L \leftarrow C$	
	JR	word	1 1 ← jdisp 1 →				10	PC ← PC + 1 + jdisp 1	
	JRE *	word	0 1 0 0 1 1 1 ←	jdisp →			10	PC ← PC + 2 + jdisp	
	JEA		0 1 0 0 1 0 0 0	0 0 1 0 1 0 0 0			8	PC ← EA	
Call Instructions	CALL *	word	0 1 0 0 0 0 0 0	← Low Adrs →	High Adrs		16	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$ PC ← word, SP ← SP – 2	
	CALB		0 1 0 0 1 0 0 0	0 0 1 0 1 0 0 1			17	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$ $PC_H \leftarrow B$, $PC_L \leftarrow C$, SP ← SP – 2	
	CALF *	word	0 1 1 1 1 ←	fa →			13	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$ $PC_{15-11} \leftarrow 00001$, $PC_{10-0} \leftarrow fa$, SP ← SP – 2	

Note Instruction Group

Note 1	Mnemonic	Operand	Operation Code B1	B2	B3	B4	State	Operation	Skip Condition
Note 2	CALT	word	1 0 0 ← ta →				16	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$ $PC_L \leftarrow (128+2ta)$, $PC_H \leftarrow (129+2ta)$, $SP \leftarrow SP-2$	
Note 2	SOFTI		0 1 1 1 0 0 1 0				16	$(SP-1) \leftarrow PSW$, $(SP-2) \leftarrow (PC+1)_H$, $(SP-3) \leftarrow (PC+1)_L$, $PC \leftarrow 0060H$, $SP \leftarrow SP-3$	
Return instructions	RET		1 0 1 1 1 0 0 0				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ $SP \leftarrow SP+2$	
Return instructions	RETS		↓ 1 0 0 1				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, $SP \leftarrow SP+2$ $PC \leftarrow PC+n$	Unconditional skip
Return instructions	RETI		0 1 1 0 0 0 1 0				13	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ $PSW \leftarrow (SP+2)$, $SP \leftarrow SP+3$	
Skip instructions	BIT *	bit, wa	0 1 0 1 1 B_2 B_1 B_0	← Offset →			10	Skip if (V. wa) bit = 1	(V. wa)bit = 1
Skip instructions	SK	f	0 1 0 0 1 0 0 0	0 0 0 0 1 F_2 F_1 F_0			8	Skip if f = 1	f = 1
Skip instructions	SKN	f	↓ ↓	0 0 0 1 ↓			8	Skip if f = 0	f = 0
Skip instructions	SKIT	irf	↓ ↓	0 1 0 I_4 I_3 I_2 I_1 I_0			8	Skip if irf = 1, then reset irf	irf = 1
Skip instructions	SKNIT	irf	↓ ↓	0 1 1 I_4 I_3 I_2 I_1 I_0			8	Skip if irf = 0 Reset irf, if irf = 1	irf = 0
CPU control instructions	NOP		0 0 0 0 0 0 0 0				4	No Operation	
CPU control instructions	EI		1 0 1 0 1 0 1 0				4	Enable Interrupt	
CPU control instructions	DI		1 0 1 1 1 0 1 0				4	Disable Interrupt	
CPU control instructions	HLT		0 1 0 0 1 0 0 0	0 0 1 1 1 0 1 1			12	Set Halt Mode	
CPU control instructions	STOP		0 1 0 0 1 0 0 0	1 0 1 1 1 0 1 1			12	Set Stop Mode	

* **1.** Data is B2 if rpa2 = D + byte, H + byte.

2. Data is B3 if rpa3 = D + byte, H + byte.

3. In the State item, a figure is in the right side of slash if rpa2 and rpa3 are D + byte, H + A, H + B, H + EA, H + byte.

Remarks The idle state when each instruction is skipped is different from the execution state as shown below.

1-byte instruction	: 4 states	3-byte instruction (with *)	: 10 states
2-byte instruction (with *)	: 7 states	3-byte instruction	: 11 states
2-byte instruction	: 8 states	4-byte instruction	: 14 states

Note **1.** Instruction Group

2. Call instructions

5. LIST OF MODE REGISTERS

Name of Mode Registers		Read/ Write	Function
MA	MODE A register	W	Specifies bit-wise the input/output of the port A.
MB	MODE B register	W	Specifies bit-wise the input/output of the port B.
MCC	MODE CONTROL C register	W	Specifies bit-wise the port/control mode of the port C.
MC	MODE C register	W	Specifies bit-wise the input/output of the port C which is in port mode.
MM	MEMORY MAPPING register	W	Specifies the port/extension mode of port D and port F.
MF	MODE F register	W	Specifies bit-wise the input/output of the port F which is in port mode.
TMM	Timer mode register	R/W	Specifies operating mode of timer.
ETMM	Timer/event counter mode register	W	Specifies the operating mode of timer/event counter.
EOM	Timer/event counter output mode register	R/W	Control the output level of CO0 and CO1.
SML	Serial mode register	W	Specifies the operating mode of serial interface.
SMH		R/W	
MKL	Interrupt mask register	R/W	Specifies the enable/disable of the interrupt request.
MKH			
ANM	A/D channel mode register	R/W	Specifies the operating mode of A/D converter.
ZCM	Zero-cross mode register	W	Specifies the operation of zero-cross detector circuit.

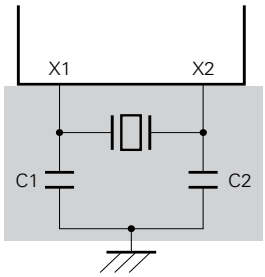
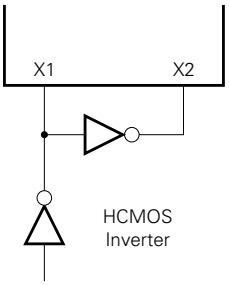
6. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Power supply voltage	V_{DD}		–0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} +0.5	V
	AV_{SS}		–0.5 to +0.5	V
Input voltage	V_I		–0.5 to V_{DD} +0.5	V
Output voltage	V_O		–0.5 to V_{DD} +0.5	V
Output current low	I_{OL}	All output pins	4.0	mA
		Total of all output pins	100	mA
Output current high	I_{OH}	All output pins	–2.0	mA
		Total of all output pins	–50	mA
A/D converter reference input voltage	V_{AREF}		–0.5 to AV_{DD} +0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

★ **Caution Even if one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product.**

OSCILLATOR CHARACTERISTICS **(T_A = –40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} –0.8 V ≤ AV_{DD} ≤ V_{DD}, 3.4 V ≤ V_{AREF} ≤ AV_{DD})**

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
Ceramic*1 or crystal resonator*2		Oscillator frequency (f_{XX})	A/D converter not used	4	15	MHz
			A/D converter used	5.8	15	MHz
External clock		X1 input frequency (f_X)	A/D converter not used	4	15	MHz
			A/D converter used	5.8	15	MHz
		X1 rise time, fall time (t_r, t_f)		0	20	ns
		X1 input high, low level width ($t_{\varnothing H}$, $t_{\varnothing L}$)		20	250	ns

Cautions 1. Place oscillator circuit as close as possible to X1, X2 pins.

2. Ensure that no other signal lines pass through the shadow area.

* **1.** The ceramic oscillators and external capacitance given in the following table are recommended.

MAKER	PRODUCT NAME	RECOMMENDED CONSTANTS	
		C1[pF]	C2[pF]
Murata Mfg. Co., Ltd	CSA7.37MT	30	30
	CST7.37MTW	On-chip	On-chip
	CSA12.0MT	30	30
	CST12.0MTW	On-chip	On-chip
	CSA15.00MX001	15	15
TDK Corp.	FCR8.0MC	On-chip	On-chip
	FCR10.0MC		
	FCR12.0OMC		
	FCR15.0MC		

* **2.** When a crystal oscillator is used, the following external capacitance is recommended.

C1 = C2 = 10 pF

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			10	pF
Output capacitance	C_O				20	pF
Input-output capacitance	C_{IO}				20	pF

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage low	V_{IL1}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to AN7		0		0.8	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to AN7		0		0.2 V_{DD}	V
Input voltage high	V_{1IH}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to AN7, X1, X2		2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to AN7, X1, X2		0.8 V_{DD}		V_{DD}	V
Output voltage low	V_{OL}	I_{OL} = 2.0 mA				0.45	V
Output voltage high	V_{OH}	I_{OH} = –1.0 mA		V_{DD} –1.0			V
		I_{OH} = –100 μA		V_{DD} –0.5			V
Input current	I_I	INT1***1**, TI(PC3)***2**; 0 V ≤ V_I ≤ V_{DD}				±200	μA
Input leakage current	I_{LI}	All except INT1, TI (PC3), 0 V ≤ V_I ≤ V_{DD}				±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
AV_{DD} power supply current	AI_{DD1}	Operating mode f_{XX} = 15 MHz			0.5	1.3	mA
	AI_{DD2}	STOP mode			10	20	μA
V_{DD} power supply current	I_{DD1}	Operating mode f_{XX} = 15 MHz			13	25	mA
	I_{DD2}	HALT mode f_{XX} = 15 MHz			7	13	mA
Data retention voltage	V_{DDDR}	Hardware/software STOP mode		2.5			V
Data retention current	I_{DDDR}	Hardware/software***3**	V_{DDDR} = 2.5 V		1	15	μA
		STOP mode	V_{DDDR} = 5 V ±10%		10	50	μA
Pull-up resistor***4**	R_L	Ports A, B and C	3.5 V ≤ V_{DD} ≤ 5.5 V, V_I = 0 V	17	27	75	kΩ

Caution For a detailed description of the hardware STOP mode, refer to the 87AD Series *m*PD78C18 User's Manual.

* **1.** If self-bias should be generated by ZCM register.

2. If the control mode is set by MCC register, and self-bias should be generated by ZCM register.

3. If self-bias is not generated.

4. μPD78C11A and 78C12A only.

AC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)
Read/write Operation:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
X1 input cycle time	t_{CYC}		66	250	ns
Address setup time (to ALE ↓)	t_{AL}	f_{XX} = 15 MHz, CL = 100 pF	30		ns
Address hold time (from ALE ↓)	t_{LA}		35		ns
$\overline{RD}$ ↓ delay time from address	t_{AR}		100		ns
Address float time from $\overline{RD}$ ↓	t_{AFR}	C_L = 100 pF		20	ns
Data input time from address	t_{AD}	f_{XX} = 15 MHz, C_L = 100 pF		250	ns
Data input time from ALE ↓	t_{LDR}			135	ns
Data input time from $\overline{RD}$ ↓	t_{RD}			120	ns
$\overline{RD}$ ↓ delay time from ALE ↓	t_{LR}		15		ns
Data hold time (from $\overline{RD}$ ↑)	t_{RDH}	C_L = 100 pF	0		ns
ALE ↑ delay time from $\overline{RD}$ ↑	t_{RL}	f_{XX} = 15 MHz, C_L = 100 pF	80		ns
$\overline{RD}$ low level width	t_{RR}	In Data Read f_{XX} = 15 MHz, C_L = 100 pF	215		ns
		In OP Code Fetch f_{XX} = 15 MHz, C_L = 100 pF	415		ns
ALE high level width	t_{LL}	f_{XX} = 15 MHz, C_L = 100 pF	90		ns
$\overline{M1}$ setup time (to ALE ↓)	t_{ML}	f_{XX} = 15 MHz	30		ns
$\overline{M1}$ hold time (from ALE ↓)	t_{LM}		35		ns
$\overline{IO}$/M setup time (to ALE ↓)	t_{IL}		30		ns
$\overline{IO}$/M hold time (from ALE ↓)	t_{LI}		35		ns
$\overline{WR}$ ↓ delay time from address	t_{AW}	f_{XX} = 15 MHz, C_L = 100 pF	100		ns
Data output time from ALE ↓	t_{LDW}			180	ns
Data output time from $\overline{WR}$ ↓	t_{WD}	C_L = 100 pF		100	ns
$\overline{WR}$ ↓ delay time from ALE ↓	t_{LW}	f_{XX} = 15 MHz, C_L = 100 pF	15		ns
Data setup time (to $\overline{WR}$ ↑)	t_{DW}		165		ns
Data hold time (from $\overline{WR}$ ↑)	t_{WDH}		60		ns
ALE ↑ delay time from $\overline{WR}$ ↑	t_{WL}		80		ns
$\overline{WR}$ low level width	t_{WW}		215		ns

Serial Operation :

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{CYK}	$\overline{SCK}$ input	***1**	800		ns
			***2**	400		ns
		$\overline{SCK}$ output		1.6		μs
$\overline{SCK}$ low level width	t_{KKL}	$\overline{SCK}$ input	***1**	335		ns
			***2**	160		ns
		$\overline{SCK}$ output		700		ns
$\overline{SCK}$ high level width	t_{KKH}	$\overline{SCK}$ input	***1**	335		ns
			***2**	160		ns
		$\overline{SCK}$ output		700		ns
RxD setup time (to $\overline{SCK}$ ↑)	t_{RXK}	***1**		80		ns
RxD hold time (from $\overline{SCK}$ ↑)	t_{KRX}	***1**		80		ns
TxD delay time from $\overline{SCK}$ ↓	t_{KTX}	***1**			210	ns

***** **1.** If clock rate is × 1 in asynchronous mode, synchronous mode, or I/O interface mode.

2. If clock rate is × 16 or × 64 in asynchronous mode.

Remarks The numeric values in the table are those when f_{XX} = 15 MHz, C_L = 100 pF.

Zero-Cross Characteristics :

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Zero-cross detection input	V_{ZX}	AC combination 60 Hz sine wave	1	1.8	VAC_{P-P}
Zero-cross accuracy	A_{ZX}			±135	mV
Zero-cross detection input frequency	f_{ZX}		0.05	1	kHz

Other Operation :

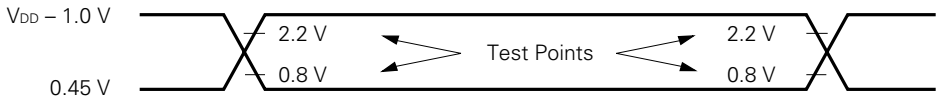
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
TI high, low level width	t_{TIH}, t_{TIL}		6		t_{CYC}
CI high, low level width	t_{CI1H}, t_{CI1L}	Event count mode	6		t_{CYC}
	t_{CI2H},t_{CI2L}	Pulse width test mode	48		t_{CYC}
$\overline{NMI}$ high, low level width	t_{NIH}, t_{NIL}		10		μs
INT1 high, low level width	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ high, low level width	t_{I2H}, t_{I2L}		36		t_{CYC}
AN4 to AN7, low level width	t_{ANH}, t_{ANL}		36		t_{CYC}
$\overline{RESET}$ high, low level width	t_{RSH}, t_{RSL}		10		μs

A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} –0.5 V ≤ AV_{DD} ≤ V_{DD}, 3.4 V ≤ V_{AREF} ≤ AV_{DD})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resolution			8			Bits
Absolute accuracy*		3.4 V ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 170 ns			±0.8%	FSR
		4.0 V ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 170 ns			±0.6%	FSR
		T_A = –10 to +70 °C, 4.0 V ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 170 ns			±0.4%	FSR
Conversion time	t_{CONV}	66 ns ≤ t_{CYC} ≤ 110 ns	576			t_{CYC}
		110 ns ≤ t_{CYC} ≤ 170 ns	432			t_{CYC}
Sampling time	t_{SAMP}	66 ns ≤ t_{CYC} ≤ 110 ns	96			t_{CYC}
		110 ns ≤ t_{CYC} ≤ 170 ns	72			t_{CYC}
Analog input voltage	V_{IAN}	AN0 to AN7 (including unused pins)	–0.3		V_{AREF} +0.3	V
Analog input impedance	R_{AN}			50		MΩ ★
Reference voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} current	I_{AREF1}	Operating mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} power supply current	AI_{DD1}	Operating mode f_{XX} = 15 MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

* Quantization error (±1/2 LSB) is not included.

AC Timing Test Point



t_{CYC}-Dependent AC Characteristics Expression

PARAMETER	EXPRESSION	MIN./MAX.	UNIT
t_{AL}	2T – 100	MIN.	ns
t_{LA}	T – 30	MIN.	ns
t_{AR}	3T – 100	MIN.	ns
t_{AD}	7T – 220	MAX.	ns
t_{LDR}	5T – 200	MAX.	ns
t_{RD}	4T – 150	MAX.	ns
t_{LR}	T – 50	MIN.	ns
t_{RL}	2T – 50	MIN.	ns
t_{RR}	4T – 50 (In data read)	MIN.	ns
	7T – 50 (In OP code fetch)		
t_{LL}	2T – 40	MIN.	ns
t_{ML}	2T – 100	MIN.	ns
t_{LM}	T – 30	MIN.	ns
t_{IL}	2T – 100	MIN.	ns
t_{LI}	T – 30	MIN.	ns
t_{AW}	3T – 100	MIN.	ns
t_{LDW}	T + 110	MAX.	ns
t_{LW}	T – 50	MIN.	ns
t_{DW}	4T – 100	MIN.	ns
t_{WDH}	2T – 70	MIN.	ns
t_{WL}	2T – 50	MIN.	ns
t_{WW}	4T – 50	MIN.	ns
t_{CYK}	12T ($\overline{SCK}$ input)***1**/6T ($\overline{SCK}$ input)***2**	MIN.	ns
	24T ($\overline{SCK}$ output)		
t_{KKL}	5T + 5 ($\overline{SCK}$ input)***1**/2.5T + 5 ($\overline{SCK}$ input)***2**	MIN.	ns
	12T – 100 ($\overline{SCK}$ output)		
t_{KKH}	5T + 5 ($\overline{SCK}$ input)***1**/2.5T + 5 ($\overline{SCK}$ input)***2**	MIN.	ns
	12T – 100 ($\overline{SCK}$ output)		

***** **1.** If clock rate is ×1, in asynchronous mode, synchronous mode, or I/O interface mode.

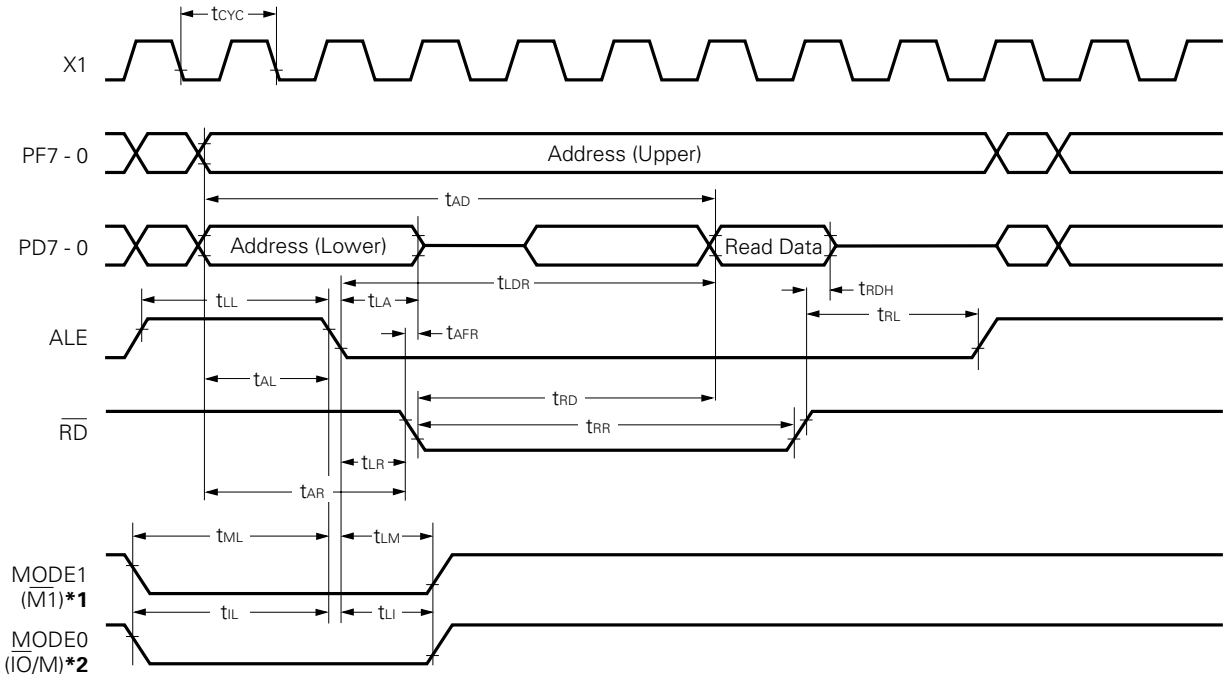
2. If clock rate is 16 × 64, in asynchronous mode.

Cautions 1. T = tCYC = 1/fXX

2. Other items which are not listed in this table are not dependent on oscillator frequency (fXX).

Timing Waveform

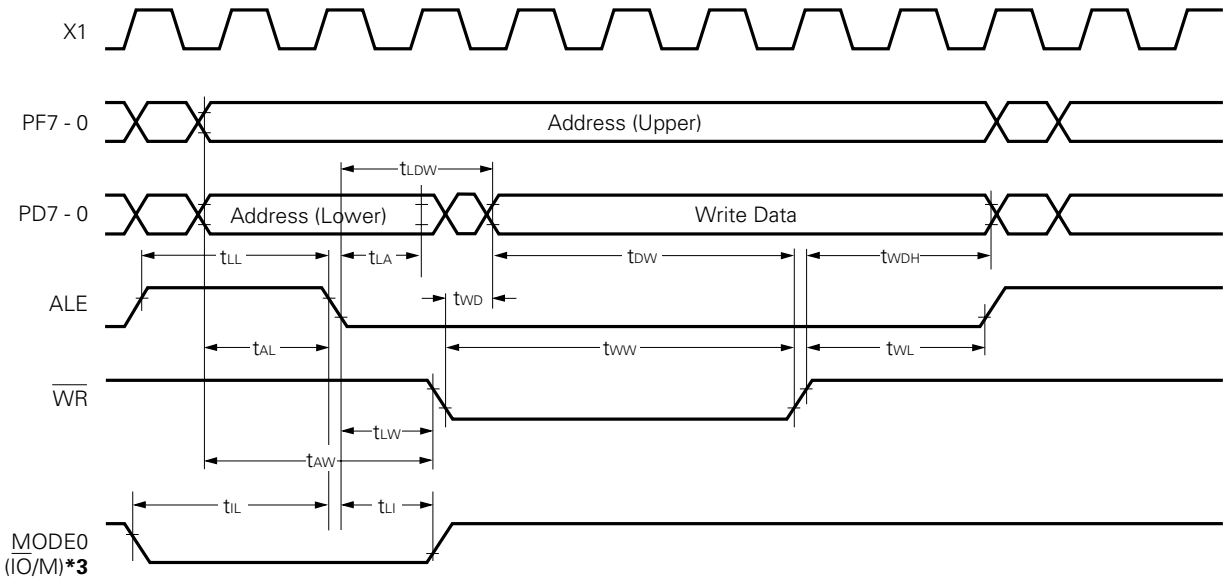
Read operation



* **1.** When MODE1 pin is pulled up, $\overline{M1}$ signal is output to MODE1 pin in the 1st OP code fetch cycle.

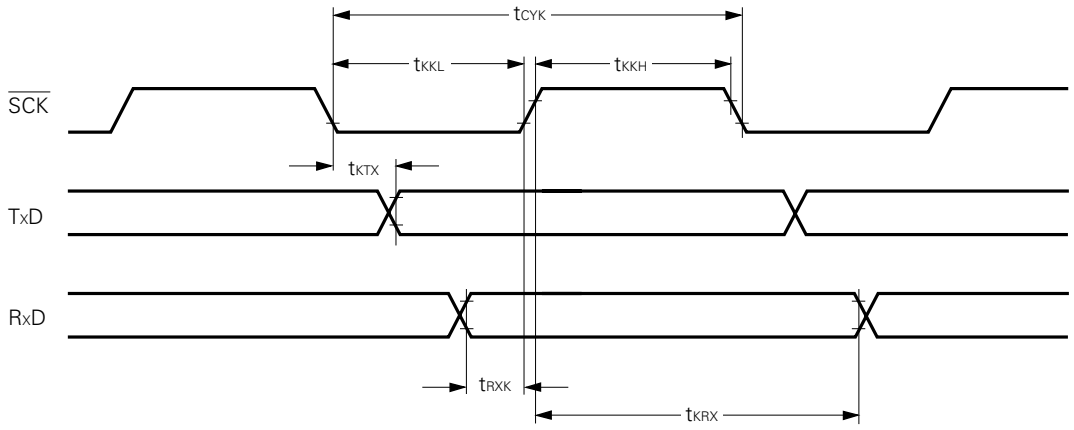
2. When MODE0 pin is pulled up, $\overline{IO}$/M signal is output to MODE0 pin in sr to sr2 register read cycle.

Write operation

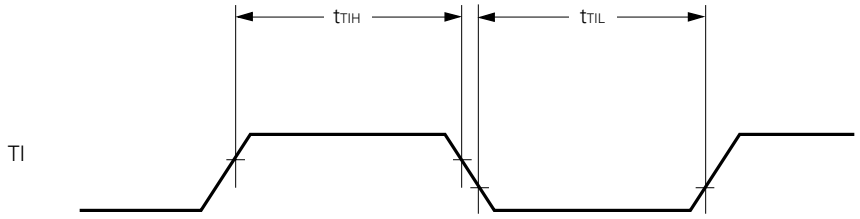


* **3.** When MODE0 pin is pulled up, $\overline{IO}$/M signal is output to MODE0 pin in sr to sr2 register write cycle.

Serial Operation

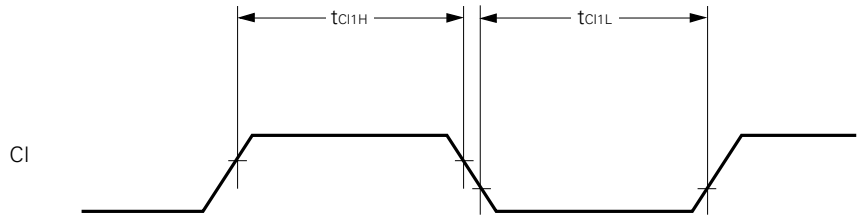


Timer Input Timing

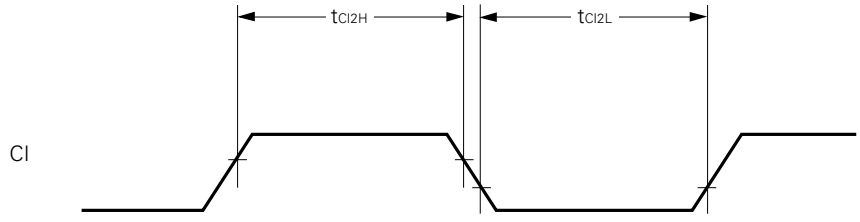


Timer/Event Counter Input Timing

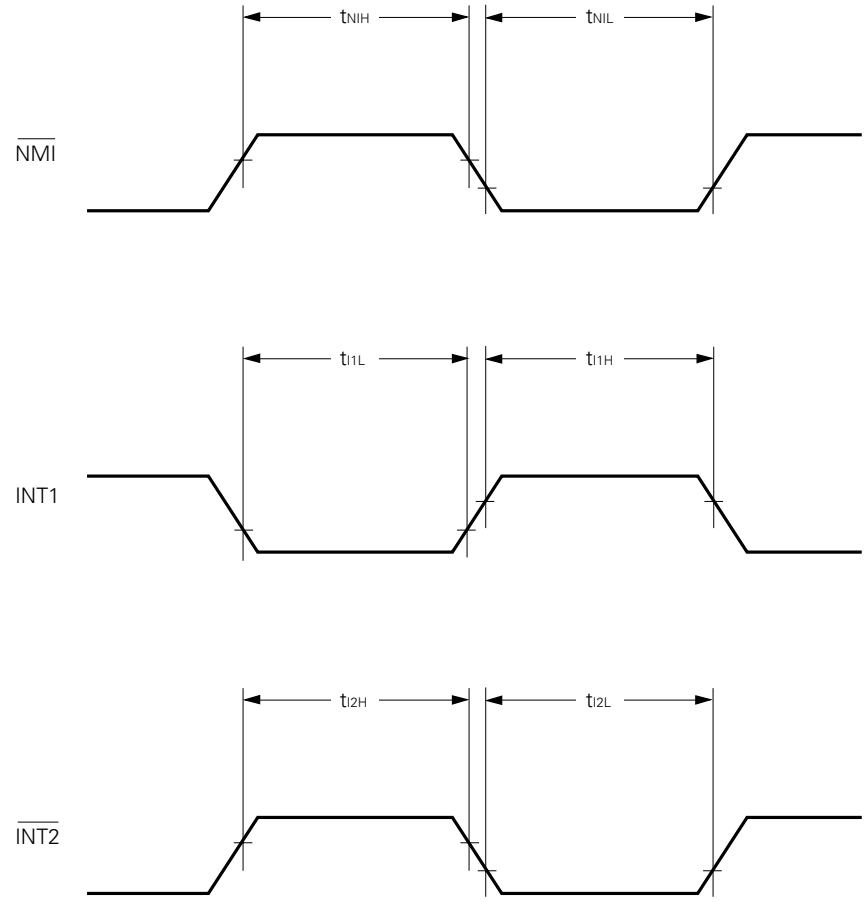
Event Counter Mode



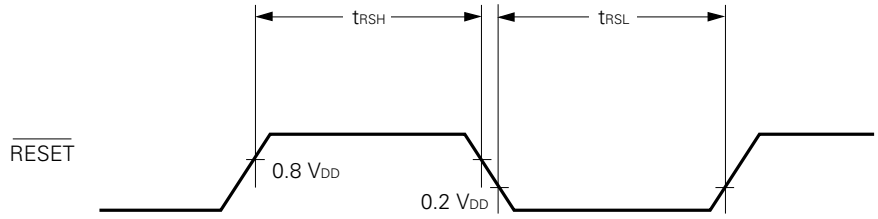
Pulse Width Test Mode



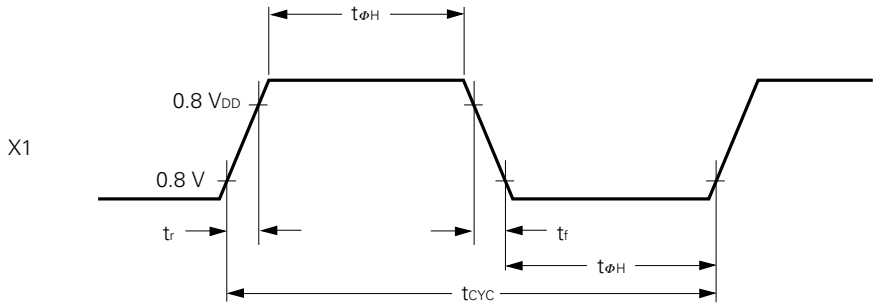
Interrupt Input Timing



Reset Input Timing



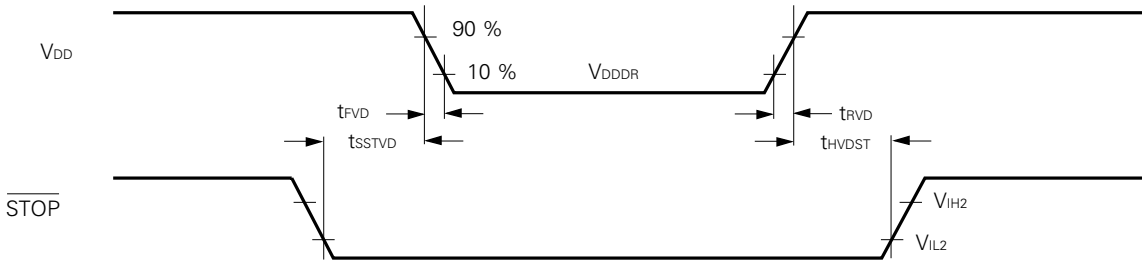
External Clock Timing



DATA MEMORY STOP MODE LOW POWER SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS
(T_A = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention power supply voltage	V_{DDDR}		2.5		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.5 V		1	15	μA
★		V_{DDDR} = 5 V ±10%		10	50	μA
V_{DD} rise/fall time	t_{RVD}, t_{FVD}		200			μs
$\overline{STOP}$ setup time (to V_{DD})	t_{SSTVD}		12T +0.5			μs
$\overline{STOP}$ hold time (from V_{DD})	t_{HVDST}		12T +0.5			μs

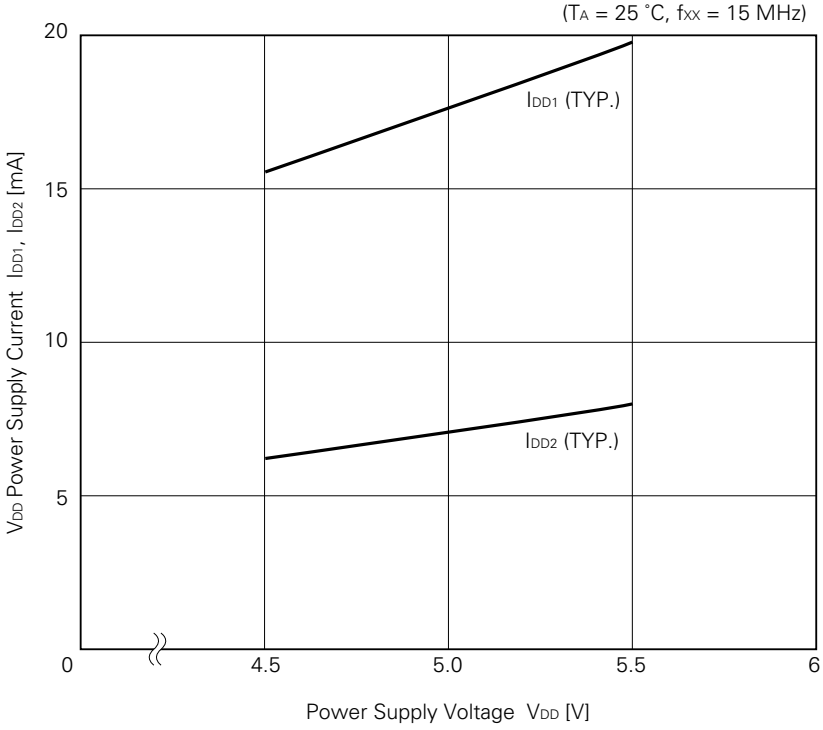
Data Retention Timing



7. CHARACTERISTIC CURVES (REFERENCE VALUES)

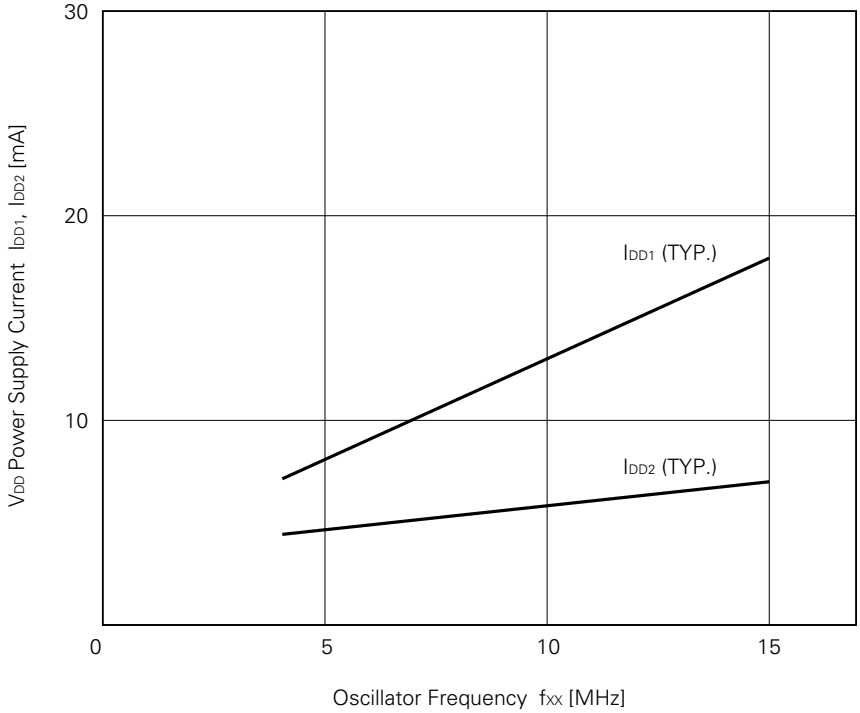
I_{DD1}, I_{DD2} vs V_{DD}

(T_A = 25 °C, f_{XX} = 15 MHz)



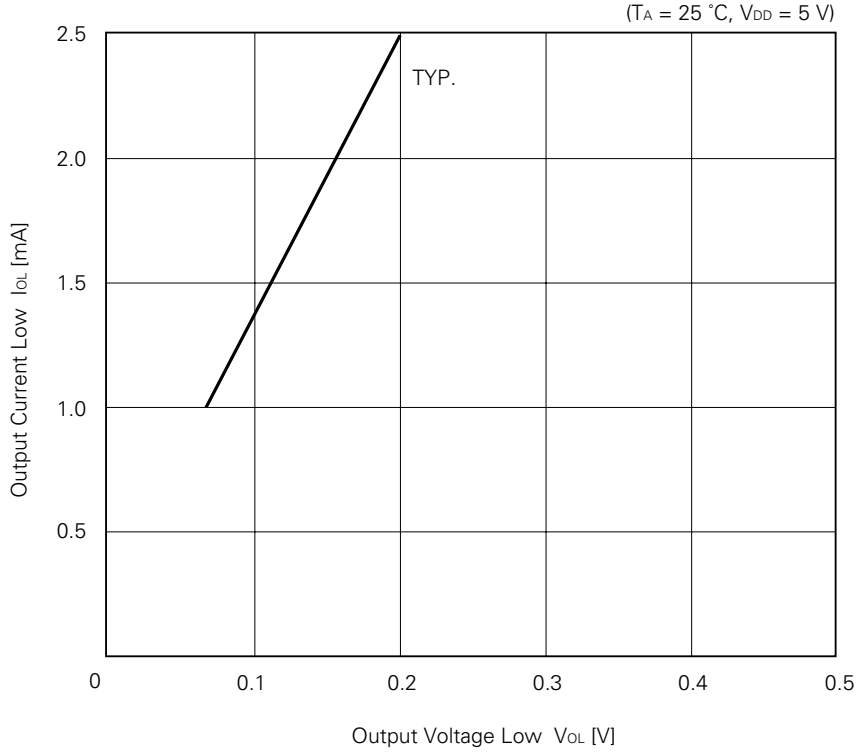
I_{DD1}, I_{DD2} vs f_{XX}

(T_A = 25 °C, V_{DD} = 5 V)



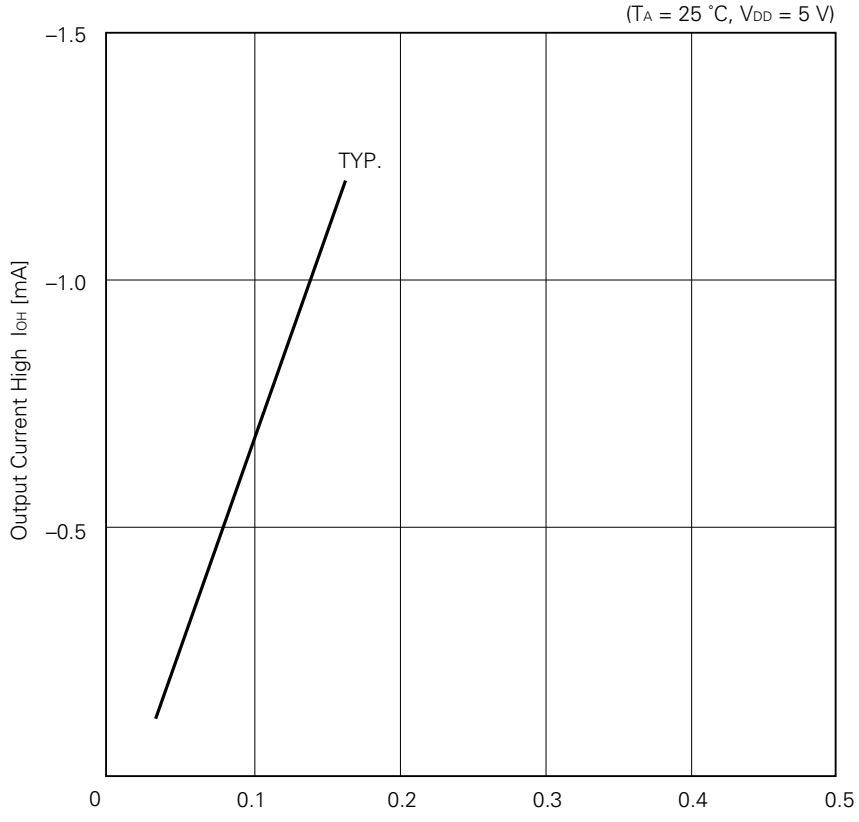
I_{OL} vs V_{OL}

(T_A = 25 °C, V_{DD} = 5 V)

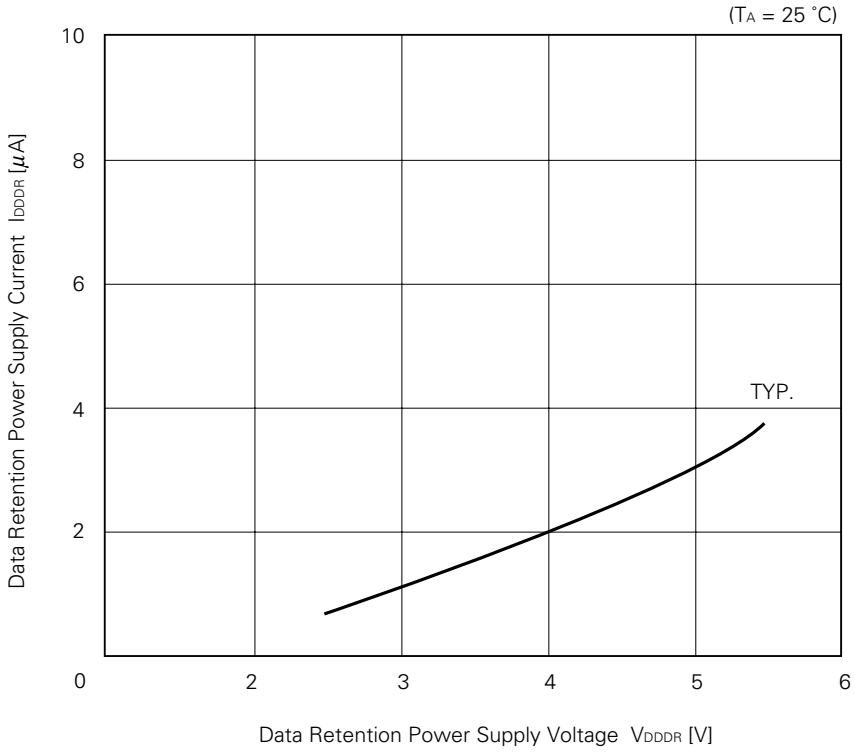


I_{OH} vs V_{OH}

(T_A = 25 °C, V_{DD} = 5 V)



I_{DDDR} vs V_{DDDR}



8. DIFFERENCES IN 87AD SERIES PRODUCTS (1/2)

Item \ Product Name	μPD7810, 7811*1	μPD7810H, 7811H	μPD78C10, 78C11*1
Number of instructions	158 kinds		159 kinds (STOP instruction added)
On-chip ROM	ROM less (μPD7810) 4K × 8 bits (μPD7811)	ROM less (μPD7810H) 4K × 8 bits (μPD7811H)	ROM less (μPD78C10) 4K × 8 bits (μPD78C11)
On-chip RAM	256 × 8 bits		
Nnmber of special registers	27		28 (ZCM register added)
Operating frequency Power supply voltage Operating temperature range	10 to 12 MHz 5 V ±5 % –10 to +70 °C	4 to 10 MHz 5 V ±10 % –40 to +85 °C	4 to 15 MHz 5 V ±10 % –10 to +70 °C	4 to 15 MHz*2 5 V ±10 % –40 to +85 °C
Standby function	Thirty-two bytes of the on-chip RAM 256 bytes of data are held by low power supply voltage (3.2 V)		Three kinds: HALT mode, software STOP mode, and hardware STOP mode. All data of on-chip RAM are held by low power supply voltage (2.5V) in software/ hardware STOP mode.
Number of HALT instruction state	11		12
HALT mode: CPU operation	M3 T2 cycle repeated		Stop
HALT mode: ALE	High level		Low level
Zero crossing detector self-bias control	Self-bias control impossible		Self-bias control possible (by ZCM register specification)
$\overline{NMI}$, $\overline{RESET}$ noise elimination method	By clock sampling		By analog delay
A/D converter operation control	Operation stop impossible		Operation stop possible (V_{AREF} pin operation)
A/D converter absolute accuracy (Unit: FSR)	0.4% (T_A = –10 to +50 °C) 0.6% (T_A = –40 to +85 °C)	0.4% (T_A = –10 to +70 °C)*3	0.4% (T_A = –10 to +70 °C, V_{AREF} = 4.0V to AV_{DD}) 0.6% (T_A = –40 to +85 °C, V_{AREF} = 4.0V to AV_{DD}) 0.8% (T_A = –40 to +85 °C V_{AREF} = 3.4V to AV_{DD})
V_{AREF} voltage range	AV_{CC} to 0.5V to AV_{CC}		3.4 V to AV_{DD}
Analog input voltage range	0V to V_{AREF}		
AI_{CC}/AI_{DD1}	6 mA Typ.		0.5 mA Typ.
AI_{DD2}	—		10 μA Typ.
I_{AREF}/I_{AREF1}	0.5 mA Typ.	2.0 mA Typ.	1.5 mA Typ.
I_{AREF2}	—		0.7 mA Typ.

* **1.** μPD7810, 7811, 78C10 and 78C11 are maintenance products.
2. K, E, P masks apply from 4 MHz to 12 MHz.
3. The μPD7810HG and 7811HG G masks, μPD7810HCW and 7811HCW K masks apply T_A = 0 to +70 °C.

μPD78C10A, 78C11A, 78C12A	μPD78CP14	μPD78CP18
159 kinds (STOP instruction added)		
ROM less (μPD78C10A) 4K × 8 bits (μPD78C11A) 8K × 8 bits (μPD78C12A)	16K × 8 bits (PROM)	32K × 8 bits (PROM)
256 × 8 bits		1024 × 8 bits
28 (ZCM register added)		
4 to 15 MHz 5 V ±10 % –40 to +85 °C	6 to 15 MHz 5 V ±5 % –40 to +85 °C	4 to 15 MHz 5 V ±10 % –40 to +85 °C
Three kinds: Halt mode, software STOP mode, and hardware STOP mode. All data of on-chip RAM are held by low power supply voltage (2.5 V) in software/hardware STOP mode.		
12		
STOP		
Low level		
Self-bias control possible (by ZCM register specification)		
By analog delay		
Operation stop impossible (V_{AREF} pin operation)		
0.4% (T_A = –10 to +70 °C, V_{AREF} = 4.0 V to AV_{DD}) 0.6% (T_A = –40 to +85 °C, V_{AREF} = 4.0 V to AV_{DD}) 0.8% (T_A = –40 to +85 °C, V_{AREF} = 3.4 V to AV_{DD})		
3.4V to AV_{DD}		
–0.3 V to V_{AREF} + 0.3 V	0V to V_{AREF}	–0.3 V to V_{AREF} + 0.3 V
0.5mA Typ.		
10 μA Typ.		
1.5 mA Typ.		
0.7 mA Typ.		

DIFFERENCES IN 87AD SERIES PRODUCTS (2/2)

Item \ Product Name		μPD7810, 7811*1	μPD7810H, 7811H	μPD78C10, 78C11*1
Operation during RESET	$\overline{RD}/\overline{WR}$	High level		High-impedance
	ALE	Output		
	PD/PF*4	Zero is output at the pin specified by the address bus. Other pins are high impedance.		
On-chip pull-up register (Mask option)		Impossible		
Device configuration		NMOS		CMOS
Standby current		3.2 mA (–10 to +70°C) MAX. 3.5 mA (–40 to +85°C) MAX.	3.2 mA MAX.	50 μA MAX. (V_{DD} = 5 V ±10 %)
Current consumption		203.2 mA (–10 to +70°C) MAX. 223.5 mA (–40 to +85°C) MAX.	203.2 mA MAX.	25 mA MAX.
$\overline{SCK}$ (Unit: ns)	Cycle time input	20T	*5	
	Low level width	10T + 80		
	High level width	10T – 80		
Bus timing (Unit: ns)	T_{LDW}	T + 110		
	T_{WD}	100		
	T_{DW}	4T – 100		
Hardware STOP mode restrictions		—		Yes
Asyncronous mode restrictions during external SCK input.		No		Yes
Package		64-pin plastic shrink DIP 64-pin plastic QUIP straight*7 64-pin plastic QUIP		64-pin plastic shrink DIP 64-pin plastic QUIP straight*8 64-pin plastic QUIP 64-pin plastic QFP (14 × 20 mm, 2.05 mm thickness) 64-pin plastic QFP (14 × 20 mm, 2.70 mm thickness) 68-pin plastic QFJ
Pin connection*10		V_{CC} (64-pin), V_{DD} (63-pin)		V_{DD} (64-pin), $\overline{STOP}$ (63-pin)

★

* **1.** μPD7810, 7811, 78C10 and 78C11 are maintenance products.

4. For μPD7810, 7810H, 78C10 and 78C10A.

5.

(Unit : ns)

		For the asyncronous mode with clock rate x1, syncronous mode, and I/O interface mode	For the asyncronous mode with clock rate ×16 and ×64
$\overline{SCK}$	Cycle time input	12T	6T
	Low level width	5T + 5	2.5T + 5
	High level width	5T + 5	2.5T + 5

Remarks T = t_{CYC} = 1/f_{XX}

μPD78C10A, 78C11A, 78C12A	μPD78CP14	μPD78CP18
High-impedance		
Only μPD78C11A, 78C12A possible (ports A, B, C)	Impossible	
CMOS		
50 μA MAX. (V_{DD} = 5 V ±10 %)	1 mA MAX. (V_{DD} = 5 V ±5 %)	50 μA MAX. (V_{DD} = 5 V ±10 %)
25 mA MAX.	32 mA MAX.	35 mA MAX.
***5**		
T + 110		T + 130
110		140
4T – 100		4T – 140
Yes***6**	No	
No		
64-pin plastic shrink DIP 64-pin plastic QUIP straight***9** 64-pin plastic QUIP 64-pin plastic QFP (14 × 20 mm, 2.70 mm thickness) 68-pin plastic QFJ	64-pin plastic shrink DIP 64-pin plastic QUIP 64-pin plastic QFP (14 × 20 mm, 2.70 mm thickness) 68-pin plastic QFJ 64-pin ceramic shrink DIP with window 64-pin ceramic QUIP with window 64-pin ceramic WQFN	64-pin plastic shrink DIP 64-pin plastic QUIP 64-pin plastic QFP (14 × 20 mm, 2.70 mm thickness) 64-pin ceramic shrink DIP with window 64-pin ceramic WQFN
	V_{DD} (64-pin), $\overline{STOP}$ (63-pin)	

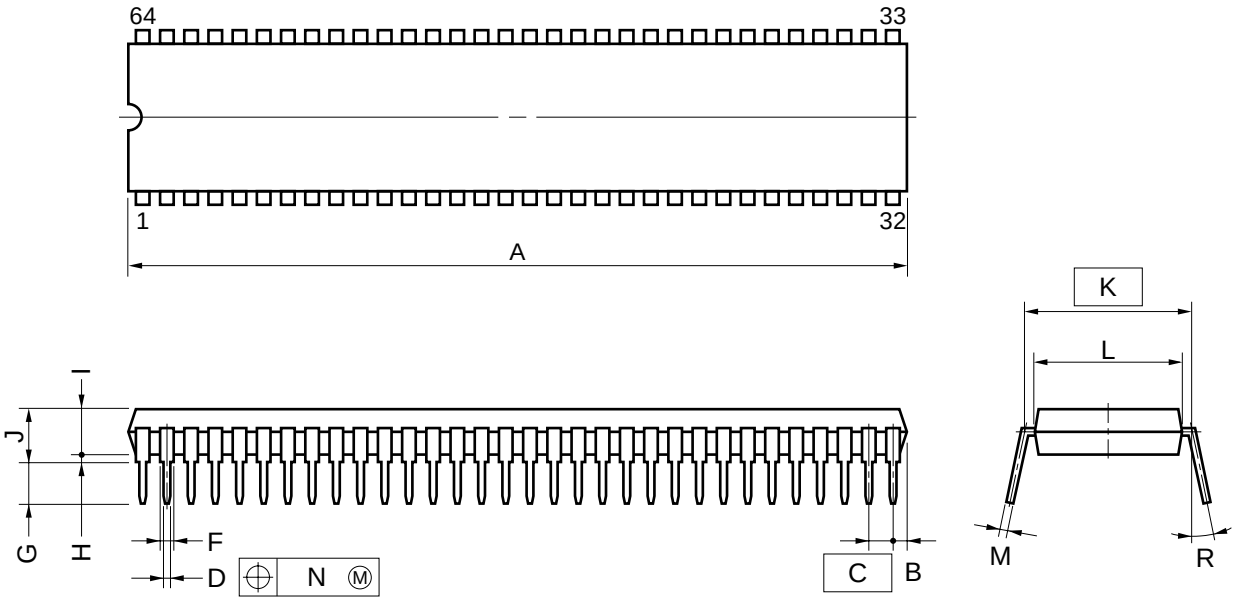
★

* **6.** K mask products only
7. μPD7811, 7811H only
8. μPD78C11, only
9. μPD78C11A, 78C12A only
10. Items in the parentheses are the pin numbers for the 64-pin plastic shrink DIP, 64-pin plastic QUIP straight and 64-pin plastic QUIP.

Caution Since the oscillator characteristics, I/O level, and some internal operation timing are different, be careful when studying direct replacement of the *m*PD78C10A, 78C11A, 78C12A and μPD7810, 7811, 7810H, 7811H, 78C10, 78C11.

9. PACKAGE INFORMATION

64 PIN PLASTIC SHRINK DIP (750 mil)



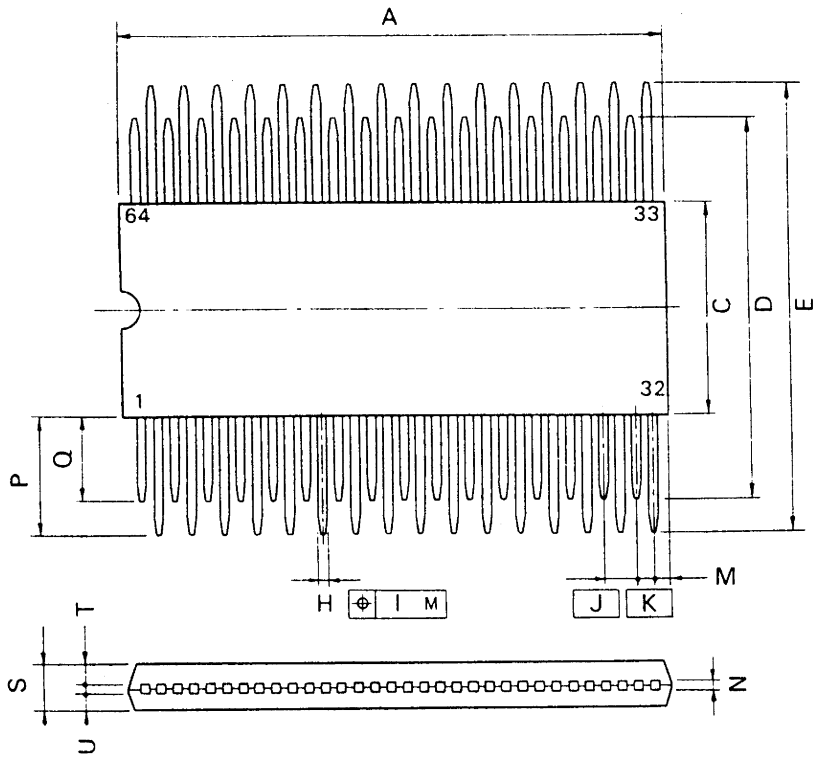
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64PIN PLASTIC QUIP (STRAIGHT)



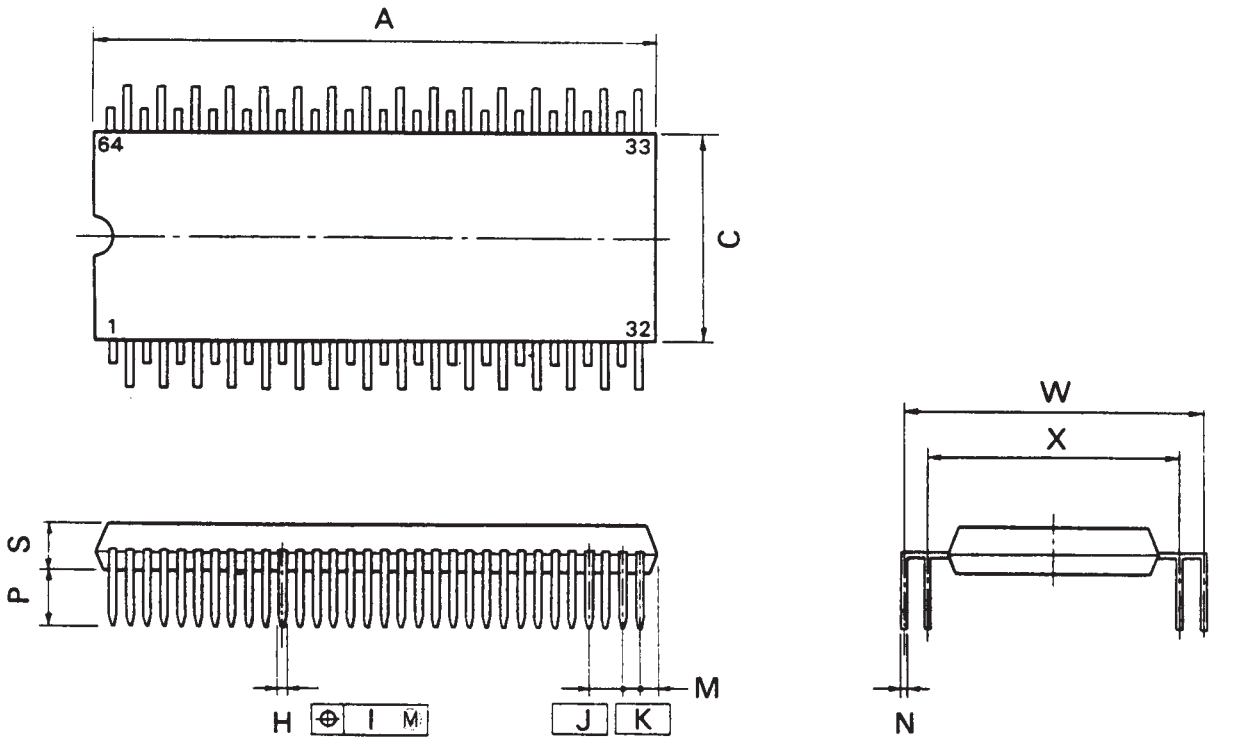
P64GQ-100-37-1

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$41.5^{+0.3}_{-0.2}$	$1.634^{+0.012}_{-0.008}$
C	16.5	0.650
D	$30.0^{\pm0.4}$	$1.181^{\pm0.016}$
E	$35.1^{\pm0.4}$	$1.382^{\pm0.016}$
H	$0.50^{\pm0.10}$	$0.020^{+0.004}_{-0.005}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	$1.1^{+0.25}_{-0.15}$	$0.043^{+0.011}_{-0.006}$
N	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
P	$9.3^{\pm0.2}$	$0.366^{+0.009}_{-0.008}$
Q	$6.75^{\pm0.2}$	$0.266^{+0.008}_{-0.009}$
S	$3.6^{\pm0.1}$	$0.142^{+0.004}_{-0.005}$
T	$1.8^{\pm0.1}$	$0.071^{+0.004}_{-0.005}$
U	$1.55^{\pm0.1}$	$0.061^{\pm0.004}$

64 PIN PLASTIC QUIP



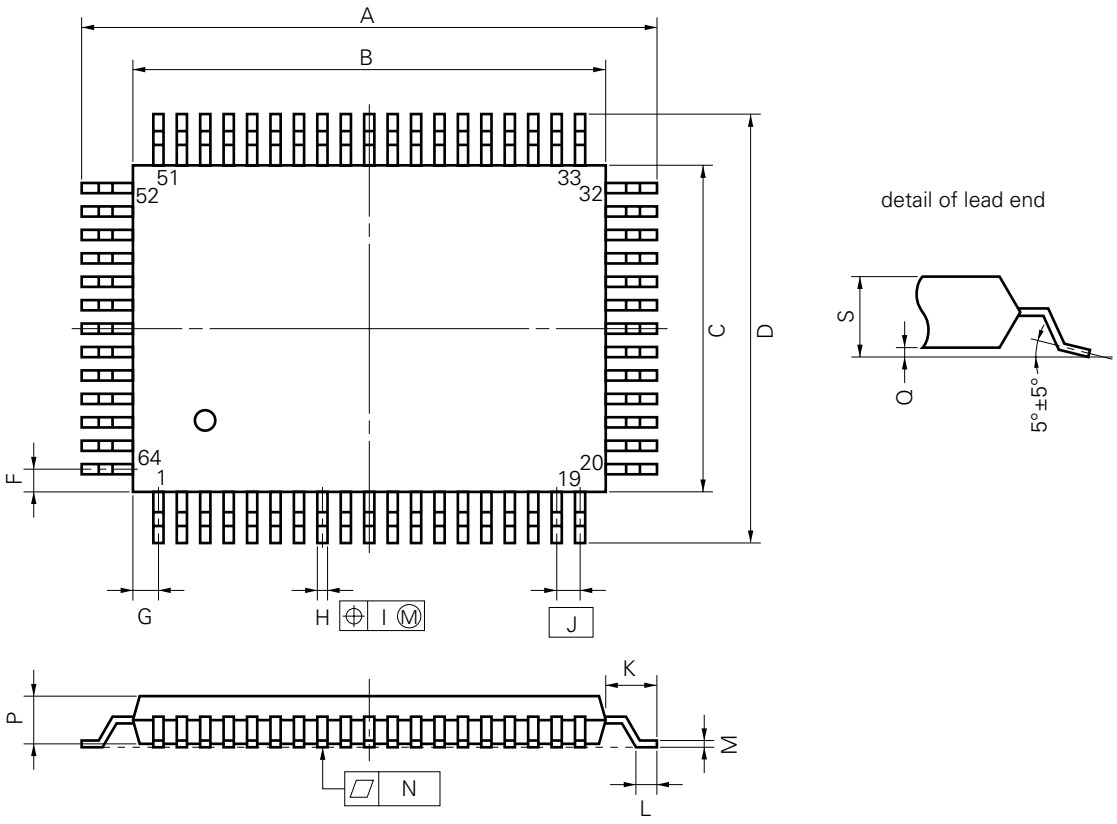
P64GQ-100-36

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$41.5^{+0.3}_{-0.2}$	$1.634^{+0.012}_{-0.008}$
C	16.5	0.650
H	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	$1.1^{+0.25}_{-0.15}$	$0.043^{+0.011}_{-0.006}$
N	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
P	$4.0^{\pm 0.3}$	$0.157^{+0.013}_{-0.012}$
S	$3.6^{\pm 0.1}$	$0.142^{+0.004}_{-0.005}$
W	$24.13^{\pm 1.05}$	$0.950^{\pm 0.042}$
X	$19.05^{\pm 1.05}$	$0.750^{\pm 0.042}$

64PIN PLASTIC QFP (14 × 20) (UNIT: mm)



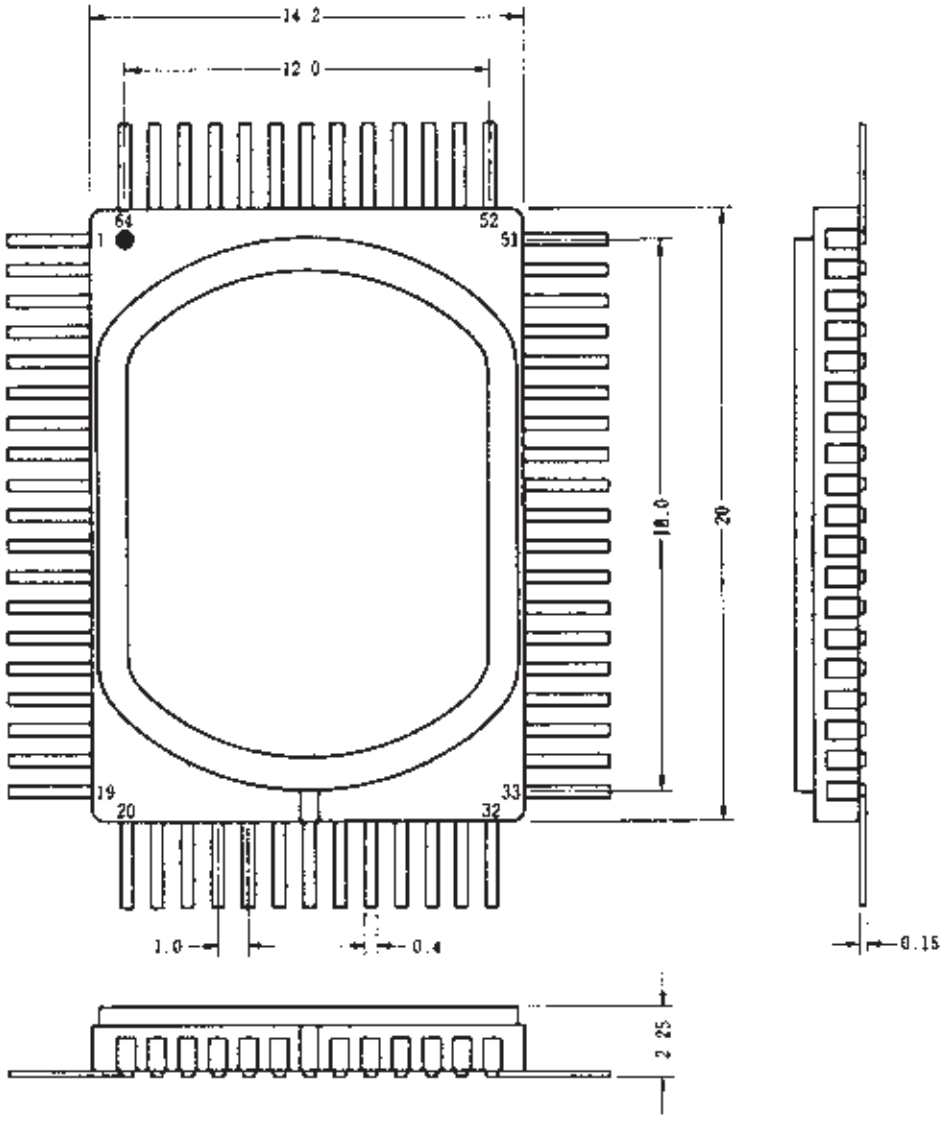
P64GF-100-3B8,3BE,3BR-1

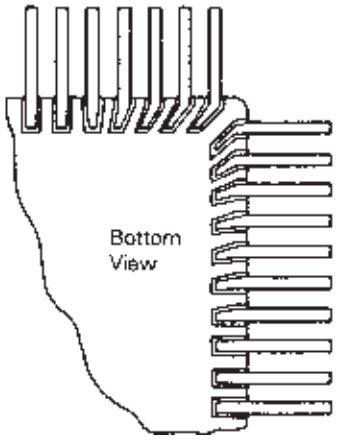
ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ES 64PIN CERAMIC QFP (REFERENCE DRAWING) (UNIT: mm)

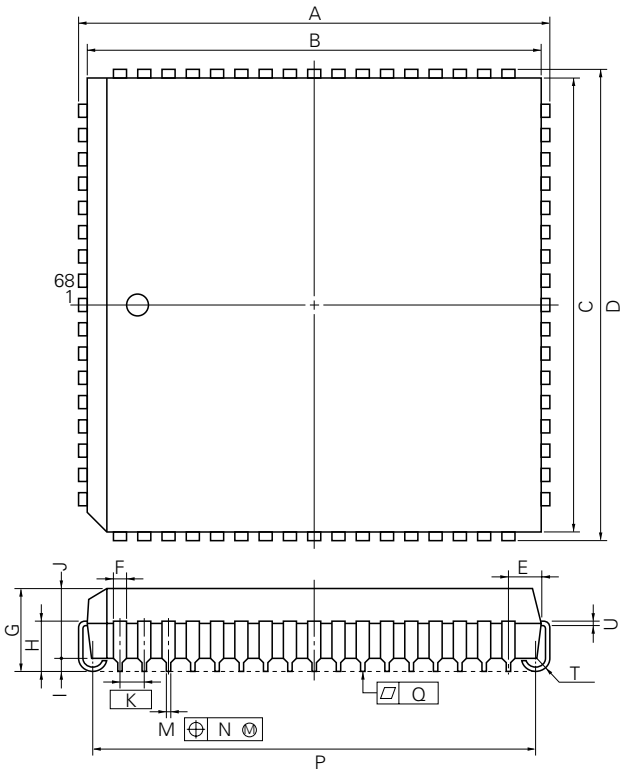




Cautions

1. **The metal cap is connected to pin 26 and is V_{SS} (GND) level.**
2. **The bottom leads are tilted.**
3. **Since cutting of the end of the leads is no process-controlled, the lead length is unspecified.**

68PIN PLASTIC QFJ (□ 950 mil) (UNIT: mm)



P68L-50A1-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20	0.953
C	24.20	0.953
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±1.0	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	23.12±0.20	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

★ 10. RECOMMENDED SOLDERING CONDITIONS

The μPD78C10A, 78C11A, and 78C12A should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (IEI-1207).**

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 10-1 Surface Mounting Type Soldering Conditions

(1) μPD78C10AGF-3BE : 64-pin plastic QFP (14 × 20 mm)
μPD78C11AGF-×××-3BE : 64-pin plastic QFP (14 × 20 mm)
μPD78C12AGF-×××-3BE : 64-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature : 235 °C, Duration : 30 sec. max. (210 °C min.), Number of times : 2 max. <Points to note> (1) Start the second reflow after the device temperature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	IR35-00-2
VPS	Package peak temperature : 215 °C, Duration : 40 sec. max. (200 °C min.), Number of times : 2 max. <Points to note> (1) Start the second reflow after the device temperature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	VP15-00-2
Wave soldering	Solder bath temperature : 260 °C max., Duration : 10 sec. max., Number of times : 1 Pre-heating temperature : 120 °C max. (package surface temperature)	WS60-00-1
Pin part heating	Pin temperature : 300 °C max., Duration: 3 sec. max. (per device side)	———

Caution Do not use two or more soldering methods in combination (except the pin part heating method).

(2) μPD78C10AL : 68-pin plastic QFJ (□ 950 mil)
μPD78C11AL-××× : 68-pin plastic QFJ (□ 950 mil)
μPD78C12AL-××× : 68-pin plastic QFJ (□ 950 mil)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature : 230 °C, Duration : 30 sec. max. (210 °C min.), Number of times : 1	IR30-00-1
VPS	Package peak temperature : 215 °C, Duration : 40 sec. max. (200 °C min.), Number of times : 1	VP15-00-1
Pin part heating	Pin temperature : 300 °C max., Duration : 3 sec. max. (per device side)	———

Caution Do not use two or more soldering methods in combination (except the pin part heating method).

Table 10-2 Inserted Type Soldering Conditions

(1) μPD78C10ACW : 64-pin plastic shrink DIP (750 mil)
μPD78C11ACW-××× : 64-pin plastic shrink DIP (750 mil)
μPD78C12ACW-××× : 64-pin plastic shrink DIP (750 mil)
μPD78C10AGQ-36 : 64-pin plastic QUIP
μPD78C11AGQ-×××-36 : 64-pin plastic QUIP
μPD78C12AGQ-×××-36 : 64-pin plastic QUIP

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260 °C max. Duration: 10 sec. max.
Pin part heating	Pin temperature: 300 °C max. Duration: 3 sec. max. (per pin)

Caution Ensure that the application of wave soldering is limited to the pins and no solder touches the main unit directly.

(2) μPD78C11AGQ-×××-37 : 64-pin plastic QUIP straight
μPD78C12AGQ-×××-37 : 64-pin plastic QUIP straight

Soldering Method	Soldering Conditions
Pin part heating	Pin temperature: 300 °C max. Duration: 3 sec. max. (per pin)

APPENDIX DEVELOPMENT TOOLS ★

The following development tools are available to develop a system which uses 87AD series products.

Language Processor

87AD series relocatable assembler (RA87)	This is a program which converts a program written in mnemonic to an object code that micro-computer execution is possible. Besides, it contains a function to automatically create a symbol/table, and optimize a branch instruction.			
	Host Machine	OS	Supply Medium	Ordering Code (Product Name)
	PC-9800 series	MS-DOS™ Ver. 2.11 to Ver. 5.00A*	3.5-inch 2HD	μS5A13RA87
			5-inch 2HD	μS5A10RA87
	IBM PC/AT™	PC DOS™ (Ver. 3.1)	3.5-inch 2HC	μS7B13RA87
			5-inch 2HC	μS7B10RA87

PROM Write Tools

Hardware	PG-1500	With an provided board and an optional programmer adapter connected, this PROM programmer can manipulate from a stand-alone or host machine to perform programming on single-chip microcomputer which incorporates PROM. It is also capable of programming a typical PROM ranging from 256K to 4M bits.
	PA-78CP14CW/ GF/GQ/KB/L	PROM programmer adapter for μPD78CP14/78CP18. Used by connecting to PG-1500.
	PA-78CP14CW	For μPD78CP14CW, 78CP14DW, 78CP18CW, 78CP18DW
	PA-78CP14GF	For μPD78CP14GF-3BE, 78CP18GF-3BE
	PA-78CP14GQ	For μPD78CP14G-36, 78CP14R, 78CP18GQ-36
	PA-78CP14KB	For μPD78CP14KB, 78CP18KB
	PA-78CP14L	For μPD78CP14L

Software	PG-1500 controller	Connected PG-1500 to a host machine by using serial and parallel interface, to control the PG-1500 on a host machine.		
		Host Machine	OS	Supply Medium	Ordering Code (Product Name)
		PC-9800 series	MS-DOS Ver. 2.11 to Ver. 5.00A*	3.5-inch 2HD	μS5A13PG1500
				5-inch 2HD	μS5A10PG1500
		IBM PC/AT	PC DOS (Ver. 3.1)	5-inch 2HC	μS7B10PG1500

* Ver. 5.00/5.00A has a task swap function, but this function cannot be used with this software.

Remarks Operation of assemblers and the PG-1500 controller are guaranteed only on the host machines and operating systems quoted above.

Debugging tools

An in-circuit emulator (IE-78C11-M) is available as a program debugging tool for 87AD series. The following table shows its system configuration.

<table>
<tr><td rowspan="3">Hardware</td><td>IE-78C11-M</td><td colspan="4">The IE-78C11-M is an in-circuit emulator which works with 87AD series.
Only the IE-78C11-M should be used for a plastic QUIP package, while it should be used with a conversion socket for a plastic shrink DIP package.
It can be connected to a host machine to perform efficient debugging.</td></tr>
<tr><td>EV-9001-64</td><td colspan="4">Conversion sockets for plastic shrink DIP.
Used in combination with the IE-78C11-M.</td></tr>
<tr><td>EV-9200G-64</td><td colspan="4">64-pin LCC socket. Can be used as a substitute for 64-pin plastic QFP products with window in combination with the μPD78CP14KB/78CP18KB.</td></tr>
<tr><td rowspan="4">Software</td><td rowspan="4">IE-78C11-M
control program
(IE controller)</td><td colspan="4">Connects the IE-78C11-M to host machine by using the RS-232-C, then controls the IE-78C11-M on host machine.</td></tr>
<tr><td>Host Machine</td><td>OS</td><td>Supply Medium</td><td>Ordering Code (Product Name)</td></tr>
<tr><td rowspan="2">PC-9800 series</td><td rowspan="2">MS-DOS
[Ver. 2.11 to Ver. 3.30D]</td><td>3.5-inch 2HD</td><td>μS5A13IE78C11</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10IE78C11</td></tr>
<tr><td>IBM PC/AT</td><td>PC DOS
(Ver. 3.1)</td><td>5-inch 2HC</td><td>μS7B10IE78C11</td></tr>
</table>

Remarks Operation of the IE controller is guaranteed only on the host machine and operating systems quoted above.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The export of these products from Japan is regulated by the Japanese government. The export of some or all of these products may be prohibited without governmental license. To export or re-export some or all of these products from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

The customer must judge : the need for license	μPD78C11ACW-xxx, 78C11AGF-xxx-3BE, 78C11AGQ-xxx-36, 78C11AGQ-xxx-37, μPD78C11AL-xxx, 78C12ACW-xxx, 78C12AGF-xxx-3BE, 78C12AGQ-xxx-36, μPD78C12AGQ-xxx-37, 78C12AL-xxx
License not needed :	μPD78C10ACW, 78C10AGF-3BE, 78C10AGQ-36, 78C10AL

M4 94.11