FAIRCHILD
SEMICONDUCTOR™

February 1990
Revised August 2000

100370
Low Power Universal Demultiplexer/Decoder

General Description

The 100370 universal demultiplexer/decoder functions as either a dual 1-of-4 decoder or as a single 1-of-8 decoder, depending on the signal applied to the Mode Control (M) input. In the dual mode, each half has a pair of active-LOW Enable ($\overline{E}$) inputs. Pin assignments for the $\overline{E}$ inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active-LOW enables ($\overline{E}_{1a}$ to $\overline{E}_{1b}$, $\overline{E}_{2a}$ to $\overline{E}_{2b}$). Signals applied to auxiliary inputs H_a, H_b and H_c determine whether the outputs are active HIGH or active LOW. In the dual 1-of-4 mode the Address inputs are A_{0a}, A_{1a} and A_{0b}, A_{1b} with A_{2a} unused (i.e., left open, tied to V_{EE} or with LOW signal applied). In the 1-of-8 mode, the Address inputs are A_{0a}, A_{1a}, A_{2a} with A_{0b} and A_{1b} LOW or OPEN. All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the 100170
- 2000V ESD protection
- Pin/function compatible with 100170
- Voltage compensated operating range = −4.2V to −5.7V

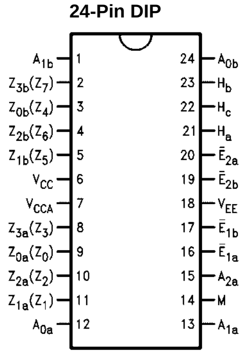
Ordering Code:

Order Number	Package Number	Package Description
100370PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100370QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100370QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (−40°C to +85°C)

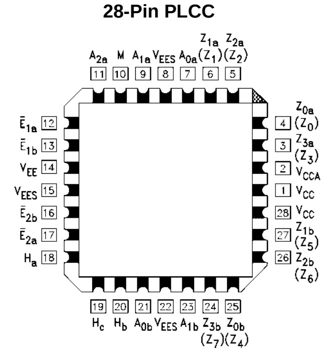
Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagrams

24-Pin DIP

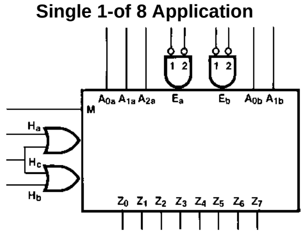


28-Pin PLCC

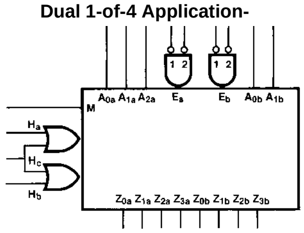


Logic Symbols

Single 1-of 8 Application



Dual 1-of-4 Application-



Pin Descriptions

Pin Names	Description
A_{na}, A_{nb}	Address Inputs
$\overline{E}_{na}$, $\overline{E}_{nb}$	Enable Inputs
M	Mode Control Input
H_a	Z_0–Z_3 ($\overline{Z}_{0a}$–$\overline{Z}_{3a}$) Polarity Select Input
H_b	Z_4–Z_7 ($\overline{Z}_{0b}$–$\overline{Z}_{3b}$) Polarity Select Input
H_c	Common Polarity Select Input
Z_0–Z_7	Single 1-of-8 Data Outputs
Z_{na}, Z_{nb}	Dual 1-of-4 Data Outputs

Truth Tables

Dual 1-of-4 Mode (M = A_{2a} = H_c = LOW)

Inputs				Active HIGH Outputs (H_a and H_b Inputs HIGH)				Active LOW Outputs (H_a and H_b Inputs LOW)			
$\overline{E}_{1a}$ $\overline{E}_{1b}$	$\overline{E}_{2a}$ $\overline{E}_{2b}$	A_{1a} A_{1b}	A_{0a} A_{0b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}
H	X	X	X	L	L	L	L	H	H	H	H
X	H	X	X	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

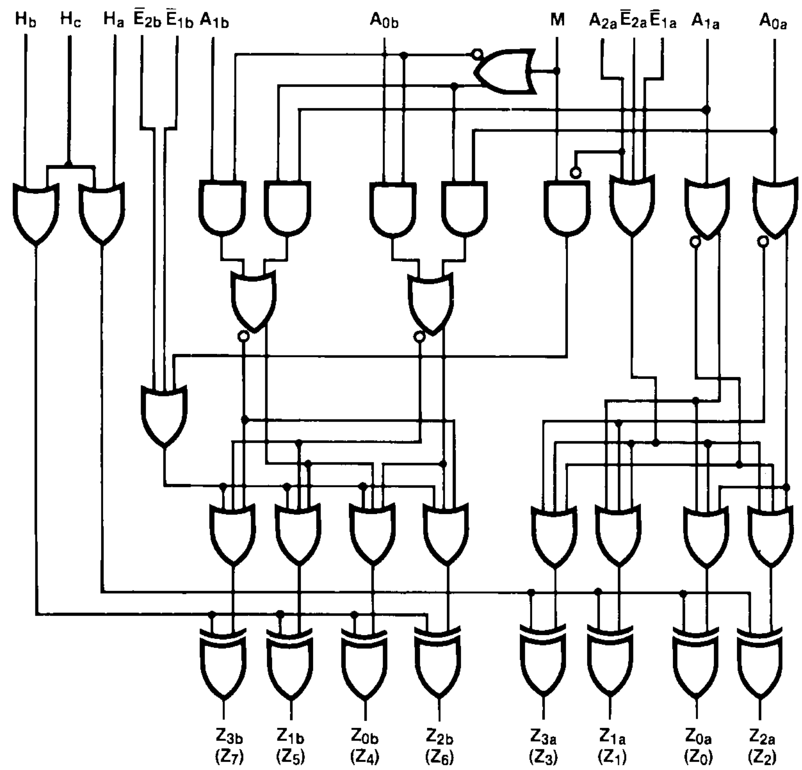
Single 1-of-8 Mode (M = HIGH; A_{0b} = A_{1b} = H_a = H_b = LOW)

Inputs					Active HIGH Outputs (Note 1) (H_c Input HIGH)							
$\overline{E}_1$	$\overline{E}_2$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

H = HIGH Voltage Level L = LOW Voltage Level X = Don't Care $\overline{E}_1 = \overline{E}_{1a}$ and $\overline{E}_{1b}$ wired; $\overline{E}_2 = \overline{E}2_{2a}$ and $\overline{E}_{2b}$ wired

Note 1: for H_c = LOW, output states are complemented

Logic Diagram



(Z_n) for 1-of-4 applications.

Absolute Maximum Ratings (Note 2)

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 3)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

DC Electrical Characteristics (Note 4)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max)	Loading with
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	or V_{IL} (Min)	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min)	Loading with
V_{OLC}	Output LOW Voltage			−1610	mV	or V_{IL} (Max)	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			µA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	µA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−95		−50	mA	Inputs OPEN	

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.75	1.85	0.75	1.85	0.85	2.05	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	0.75	2.20	0.75	2.20	0.75	2.30	ns	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	0.75	2.20	0.75	2.20	0.75	2.20	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.10	2.70	1.10	2.70	1.10	3.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.30	0.40	1.30	0.40	1.30	ns	

Commercial Version (Continued)

PLCC AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.75	1.65	0.75	1.65	0.85	1.85	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	0.75	2.00	0.75	2.00	0.75	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	0.75	2.00	0.75	2.00	0.75	2.00	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.10	2.50	1.10	2.50	1.10	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.20	0.40	1.20	0.40	1.20	ns	

Industrial Version

PLCC DC Electrical Characteristics (Note 5)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -40°C$ to $+85°C$

Symbol	Parameter	$T_C = -40°C$		$T_C = 0°C$ to $+85°C$		Units	Conditions	
		Min	Typ	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	$V_{IN} = V_{IH}$ (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		µA	$V_{IN} = V_{IL}$ (Min)	
I_{IH}	Input HIGH Current		300		240	µA	$V_{IN} = V_{IH}$ (Max)	
I_{EE}	Power Supply Current	−95	−50	−95	−50	mA	Inputs OPEN	

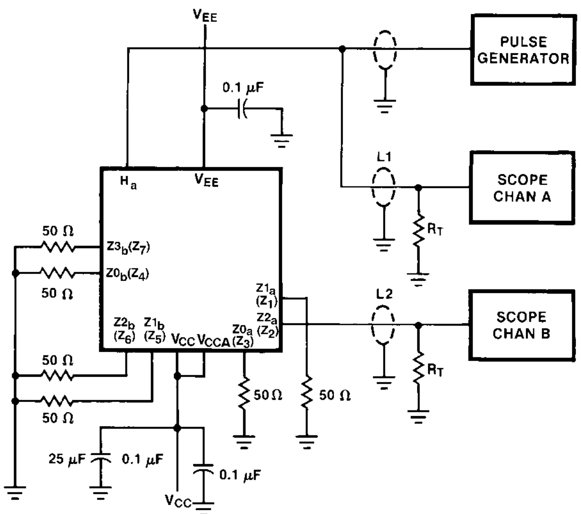
Note 5: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PLCC AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.75	1.65	0.75	1.65	0.85	1.85	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	0.65	2.00	0.75	2.00	0.75	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	0.70	2.00	0.75	2.00	0.75	2.00	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.10	2.50	1.10	2.50	1.10	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.30	0.40	1.20	0.40	1.20	ns	

Test Circuit



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = –2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 µF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms

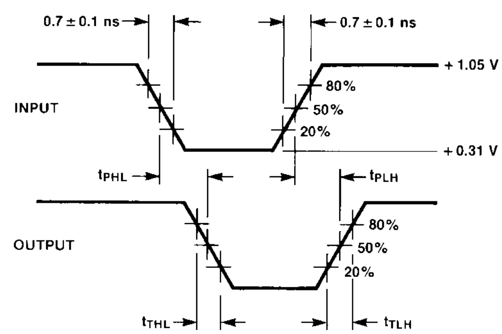
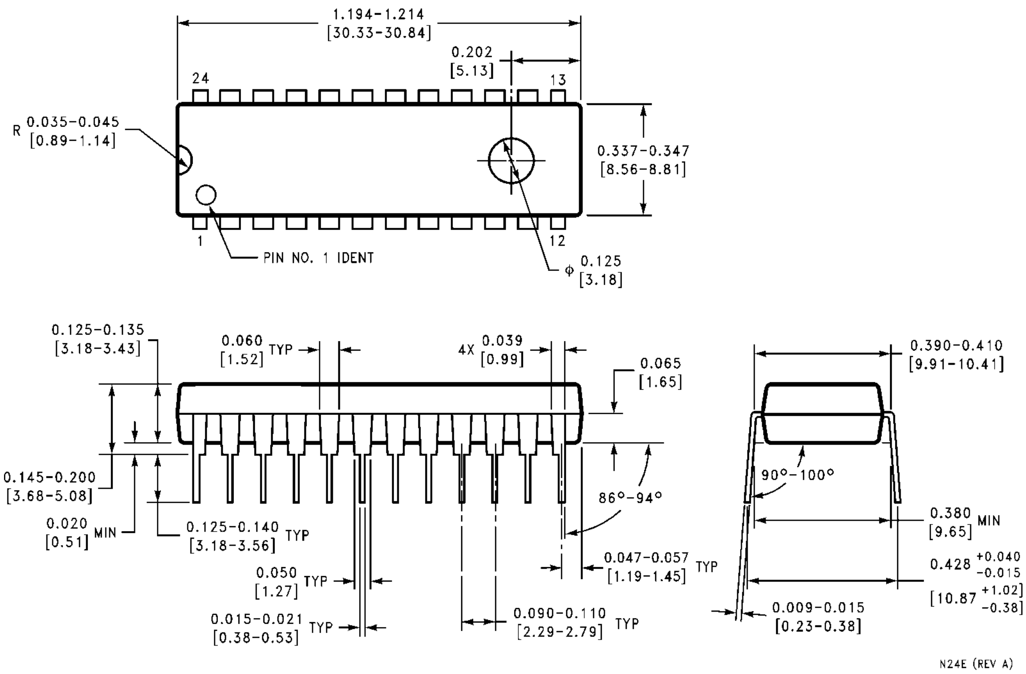


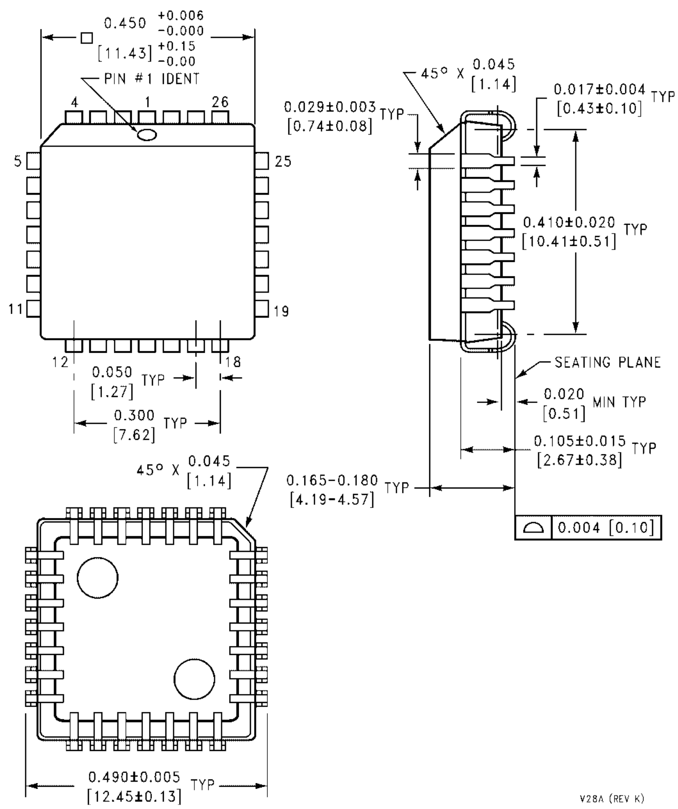
FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A