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This document specifies SPANSION[™] memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a SPANSION[™] product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION[™] memory solutions.





Stacked MCP (Multi-Chip Package) FLASH MEMORY & SRAM cmos

64M (×8/×16) FLASH MEMORY & 8M (×8/×16) STATIC RAM

MB84VD23280FA-70

FEATURES

- Power supply voltage of 2.7 V to 3.1 V
- High performance 70 ns maximum access time (Flash) 70 ns maximum access time (SRAM)
- Operating Temperature -40 °C to +85 °C
- Package 65-ball FBGA

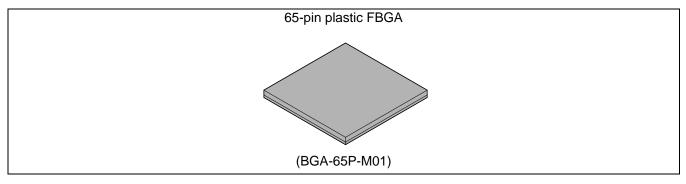
■ PRODUCT LINEUP

(Continued)

	Flash Memory	SRAM
Supply Voltage (V)	$V_{cc}r^* = 3.0 V_{-0.3 V}^{+0.1V}$	$V_{\rm CC}s^* = 3.0 \ V_{-0.3 \ V}^{+0.1 \ V}$
Max Address Access Time (ns)	70	70
Max CE Access Time (ns)	70	70
Max OE Access Time (ns)	30	35

*: Both Vccf and Vccs must be in recommended operation range when either part is being accessed.

PACKAGE





(Continued)

- -FLASH MEMORY
- + 0.16 μm Process Technology
- Simultaneous Read/Write operations (Dual Bank)
- FlexBank^{™*1}

Bank A : 8 Mbit (8 KB \times 8 and 64 KB \times 15)

Bank B : 24 Mbit (64 KB \times 48)

Bank C : 24 Mbit (64 KB \times 48)

Bank D : 8 Mbit (8 KB \times 8 and 64 KB \times 15)

Two virtual Banks are chosen from the combination of four physical banks

Host system can program or erase in one bank, and then read immediately and simultaneously from the other bank with zero latency between read and write operations.

Read-while-erase

Read-while-program

- Single 3.0 V read, program, and erase Minimized system level power requirements
- Minimum 100,000 program/erase cycles
- Sector erase architecture

Sixteen 4 Kword and one hundred twenty-six 32 Kword sectors in word.

Any combination of sectors can be concurrently erased. It also supports full chip erase.

HiddenROM region

256 byte of HiddenROM, accessible through a new "HiddenROM Enable" command sequence Factory serialized and protected to provide a secure electronic serial number (ESN)

• WP/ACC input pin

At VL, allows protection of "outermost" 2×8 Kbytes on both ends of boot sectors, regardless of sector protection/unprotection status

At VIH, allows removal of boot sector protection

At VACC, increases program performance

- Embedded Erase^{™*2} Algorithms Automatically preprograms and erases the chip or any sector
- Embedded Program^{™*2} Algorithms Automatically writes and verifies data at specified address
- Data Polling and Toggle Bit feature for detection of program or erase cycle completion
- Ready/Busy output (RY/BY)

Hardware method for detection of program or erase cycle completion

- Automatic sleep mode When addresses remain stable, the device automatically switches itself to low power mode.
- Low Vccf write inhibit \leq 2.5 V
- **Program Suspend/Resume** Suspends the program operation to allow a read in another byte
- Erase Suspend/Resume Suspends the erase operation to allow a read data and/or program in another sector within the same device
- Please refer to "MBM29DL64DF" data sheet in detailed function

(Continued)

- —SRAM
- Power dissipation
 Operating: 50 mA Max
 Standby: 15 μA Max
- Power down features using CE1s and CE2s
- Data retention supply voltage: 1.5 V to 3.1 V
- CE1s and CE2s Chip Select
- Byte data control: LB (DQ7 to DQ0), UB (DQ15 to DQ8)

*1 : FlexBank[™] is a trademark of Fujitsu Limited, Japan.

*2 : Embedded Erase[™] and Embedded Program[™] are trademarks of Advanced Micro Devices, Inc.

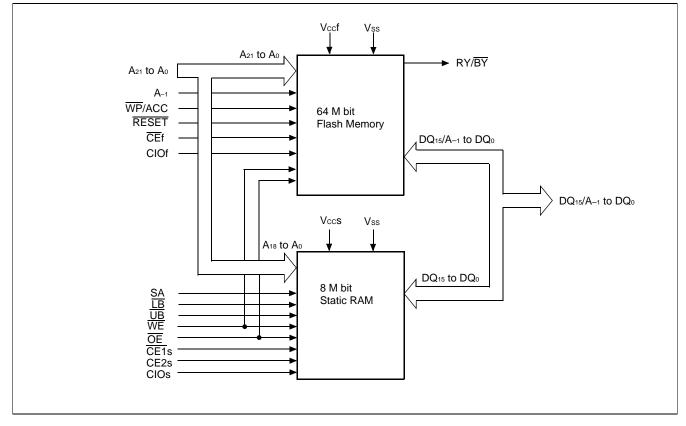
■ PIN ASSIGNMENT

(A10) N.C. (A9) N.C.									1775
	A11 (B7) (B6) (B6) (B5) (WP/ACC	(C9) A15 (C8) A12 (C7) A19 (C6) (C5) (C5) RESET	(D9) A21 (D8) A13 (D7) A9 (D6) A20 (D5) RY/BY	E9 N.C. (E8 A14 (E7) A10	(F9) A16 (F8) SA (F7) DQ6	(G9) CIOf (G8) DQ15/A-1 (G7) DQ13 (G6) DQ4 (G5) DQ3	H9 Vss H8 DQ7 H7 DQ12 H6 Vccs H5 Vccf	DQ14 J7 J6 CIOs J5 DQ11	(K10) N.C. (K9) N.C.
(A2) N.C. (A1) N.C.	(B4) (B3) (B3) (B1) (N.C.	C4 UB C3 A6 C2 A3	(D4) A18 (D3) A5 (D2) A2	(E4) A17 (E3) A4 (E2) A1	(F4) DQ1 (F3) Vss (F2) A0	G4 DQ9 G3 OE G2 CEf	H4 DQ10 H3 DQ0 H2 CE1s	(J4) DQ2 (J3) DQ8	(K2) N.C. (K1) N.C.
N.C.	N.C.			(BGA-6	5P-M01)				N.C.

■ PIN DESCRIPTION

Pin name	Input/ Output	Description
A ₁₈ to A ₀	I	Address Inputs (Common)
A21 to A19, A-1	I	Address Inputs (Flash)
SA	I	Address Input (SRAM)
DQ15 to DQ0	I/O	Data Inputs/Outputs (Common)
CEf	I	Chip Enable (Flash)
CE1s	I	Chip Enable (SRAM)
CE2s	I	Chip Enable (SRAM)
OE	I	Output Enable (Common)
WE	I	Write Enable (Common)
RY/BY	0	Ready/Busy Output (Flash) Open Drain Output
UB	I	Upper Byte Control (SRAM)
LB	I	Lower Byte Control (SRAM)
CIOf	Ι	I/O Configuration (Flash) CIOf = Vccf is Word mode (x16), CIOf = Vss is Byte mode (x8)
CIOs	I	I/O Configuration (SRAM) CIOs = Vccs is Word mode (x16), CIOs = Vss is Byte mode (x8)
RESET	I	Hardware Reset Pin/Sector Protection Unlock (Flash)
WP/ACC	I	Write Protect / Acceleration (Flash)
N.C.	—	No Internal Connection
Vss	Power	Device Ground (Common)
Vccf	Power	Device Power Supply (Flash)
Vccs	Power	Device Power Supply (SRAM)

BLOCK DIAGRAM



■ DEVICE BUS OPERATIONS

User Bus Operations (Flash = Word mode; CIOf = Vccf, SRAM = Word mode; CIOs = Vccs)												
Operation *1,*3	CEf	CE1s	CE2s	OE	WE	SA	LB	UB	DQ7 to DQ0	DQ15 to DQ8	RESET	WP/ ACC *5
Full Standby	Н	Н	Х	х	х	х	х	х	High-Z	High-Z	н	х
		Х	L		~	~	~	~				
	н	L	н	Н	Н	Х	Х	Х	High-Z	High-Z		
Output Disable				Х	Х	Х	Н	H	High-Z	High-Z	H	х
Output Disable	L	Н	Х	н	н	х	х	х	High-Z	High-Z		
	L	Х	L			~	^	~	r lign-z	r ligit-z		
Read from Flash *2	L	Н	Х	-	L Н	х	х	Х	Dout	Dout	Н	х
		Х	L	L		~	~	~	Door	DOOT		
Write to Flash	L	Н	Х	Н	L	х	х	Х	Din	DIN	Н	х
	L	Х	L	• •	Ŀ	~	~	~	Din	Din		
	н						L	L	Dout	Dout		
Read from SRAM		L	Н	L	н	Х	Н	L	High-Z	Dout	н	Х
							L	Т	Dout	High-Z		
							L	L	DIN	Din		
Write to SRAM	Н	L	Н	Х	L	Х	Н	L	High-Z	Din	н	Х
							L	Н	DIN	High-Z		
Temporary Sector Group Unprotec- tion *4	х	х	х	х	х	х	х	х	х	х	Vid	х
Flash Hardware	х	Н	Х	Х	Y	Y	х	х	High-Z	High-Z		х
Reset	^	Х		^	X X		^	^	⊓ig⊓-∠	nigh-z	L	^
Boot Block Sector Write Protection	Х	х	х	Х	х	х	х	Х	х	х	х	L

Legend: $L = V_{IL}$, $H = V_{IH}$, $X = V_{IL}$ or V_{IH} . See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : \overline{WE} can be V_{IL} if \overline{OE} is V_{IL} , \overline{OE} at V_{IH} initiates the write operations.

*3 : Do not apply $\overline{CE}f = V_{IL}$, $\overline{CE1}s = V_{IL}$ and $CE2s = V_{IH}$ at a time.

*4 : Also used for the extended sector group protections.

*5 : Protects of "outermost" 2 x 4 Kwords on both ends of each boot block sector.

User Bus Operations (Flash = Word mode; CIOf = Vccf, SRAM = Byte mode; CIOs = Vss)												
Operation *1,*3	CEf	CE1s	CE2s	ŌĒ	WE	SA	LB	UB	DQ7 to DQ0	DQ15 to DQ8	RESET	WP/ ACC *5
Full Standby	Н	Н	Х	х	х	х	х	х	High-Z	High-Z	Н	Х
		Х	L									
	н	L	Н	Η	Н	Х	Х	Х	High-Z	High-Z		
Output Disable		L		Х	Х	Х	н	н	High-Z	High-Z	Н	Х
Output Disable	L	Н	Х	н	н	х	х	х	High-Z	High-Z		~
	L	Х	L	••	•••	~	~	Λ	riigir Z	riigit Z		
Read from Flash*2	L	Н	Х	L	Н	х	х	х	Dout	Dout	Н	Х
	-	Х	L	-	••	Λ	~		DOOT	DOOT		Λ
Write to Flash	L	Н	Х	Н	L	х	х	х	Din	Din	Н	Х
		Х	L			~	~	^	DIN	Din		~
Read from SRAM	Н	L	Н	L	Н	SA	Х	Х	Dout	High-Z	Н	Х
Write to SRAM	Н	L	Н	Х	L	SA	Х	Х	Din	High-Z	Н	Х
Temporary Sector Group Unprotec- tion*4	х	х	х	х	х	х	х	х	х	х	Vid	х
Flash Hardware	х	Н	Х	х	v	х	х	х	High 7	High-Z	L	Х
Reset	^	Х	L	~	Х	^	^		High-Z	r iigir-z		~
Boot Block Sector Write Protection	Х	Х	х	Х	Х	Х	Х	х	Х	Х	Х	L

User Bus Operations (Flash = Word mode; CIOf = Vccf, SRAM = Byte mode; CIOs = Vss)

Legend: $L = V_{IL}$, $H = V_{IH}$, $X = V_{IL}$ or V_{IH} . See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : \overline{WE} can be V_{IL} if \overline{OE} is V_{IL}, \overline{OE} at V_{IH} initiates the write operations.

*3 : Do not apply $\overline{CE}f = V_{IL}$, $\overline{CE1}s = V_{IL}$ and $CE2s = V_{IH}$ at a time.

*4 : It is also used for the extended sector group protections.

*5 : Protect of "outermost" 2 x 4 Kwords on both ends of each boot block sector.

User bus Operations (Flash = Byte mode, CIOI = Vss, SRAW = Byte mode, CIOS = Vss)													
Operation *1,*3	CEf	CE1s	CE2s	DQ 15 /A -1	OE	WE	SA	LB	UB	DQ⁊ to DQ₀	DQ14 to DQ8	RESET	WP/ ACC *5
Full Standby	н	Н	Х	х	х	х	x	х	х	High-Z	High-Z	Н	х
Full Standby		Х	L		^	^	^	^	^	riigii-z	riigi1-z		^
	н	L	н	Х	Н	Н	Х	Х	Х	High-Z	High-Z	н	
Output Disable		L		Х	Х	Х	Х	Н	Н	High-Z	High-Z		х
Output Disable	L	Н	Х	A_1 H	н	х	х	х	Lligh 7	Lligh 7		^	
	L	Х	L	A -1	п		^	^	^	High-Z	High-Z		
Read from Flash*2	L	Н	Х	A_1	L	н	х	х	х	Dout	Х	Н	х
Read ITOITI Flash -	L	Х	L	A -1	L		^	^	^	DOUT	~		^
Write to Flash	1	Н	Х	Δ.	н	L	х	х	х	Din	Х	Н	х
	L	Х	L	L A_1	11		^	^	^	DIN	~	н	^
Read from SRAM	Н	L	Н	Х	L	Н	SA	Х	Х	Dout	High-Z	Н	Х
Write to SRAM	Н	L	Н	Х	Х	L	SA	Х	Х	Din	High-Z	Н	Х
Temporary Sector Group Unprotection *4	х	х	х	х	Х	x	x	х	х	х	х	Vid	Х
Flash Hardware	х	Н	Х	~	х	х	х	v	х	Lligh 7	Lligh 7	L	Х
Reset	^	Х	L	X	^	^	^	X		High-Z	High-Z	L	^
Boot Block Sector Write Protection	Х	х	Х	X	Х	х	Х	Х	х	Х	Х	Х	L

User Bus Operations (Flash = Byte mode; CIOf = Vss, SRAM = Byte mode; CIOs = Vss)

Legend: $L = V_{IL}$, $H = V_{IH}$, $X = V_{IL}$ or V_{IH} . See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : \overline{WE} can be V_{IL} if \overline{OE} is V_{IL} , \overline{OE} at V_{IH} initiates the write operations.

*3 : Do not apply $\overline{CE}f = V_{IL}$, $\overline{CE1}s = V_{IL}$ and $CE2s = V_{IH}$ at a time.

*4 : It is also used for the extended sector group protections.

*5 : Protect of "outermost" 2 x 8 Kbytes on both ends of each boot block sector.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- Sixteen 4K words, and one hundred twenty-six 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.

3 8KB (4KW) 2 8KB (4KW) 2 8KB (4KW) 3 8KB (4KW) 4 8KB (4KW) 5 8KB (4KW) 5 8KB (4KW) 5 8KB (4KW) 5 8KB (4KW) 6 8KB (4KW) 7 8KB (4KW) 1 64KB (32KW) 0 64KB (32KW) 1 64KB (32KW) 2 64KB (32KW) 3 64KB (32KW) 4 64KB (32KW) 7 64KB (32KW) 1 64KB (32KW) 1 64KB (32KW) 2 64KB	Word Mode 00000h 00100h 00200h 003000h 005000h 006000h 007000h 01000h 018000h 028000h 028000h 028000h 038000h 038000h 058000h 058000h 058000h 058000h 058000h 058000h 088000h	00000h 002000h 004000h 006000h 008000h 00C000h 00C000h 010000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 020000h 100000h 110000h 120000h 120000h 130000h 130000h 140000h 158000h 160000h 170000h 180000h 180000h 180000h	Bank C	SA71 : 64KB (32KW) SA72 : 64KB (32KW) SA73 : 64KB (32KW) SA74 : 64KB (32KW) SA74 : 64KB (32KW) SA74 : 64KB (32KW) SA75 : 64KB (32KW) SA76 : 64KB (32KW) SA77 : 64KB (32KW) SA78 : 64KB (32KW) SA78 : 64KB (32KW) SA78 : 64KB (32KW) SA80 : 64KB (32KW) SA81 : 64KB (32KW) SA81 : 64KB (32KW) SA81 : 64KB (32KW) SA83 : 64KB (32KW) SA85 : 64KB (32KW) SA85 : 64KB (32KW) SA85 : 64KB (32KW) SA87 : 64KB (32KW) SA87 : 64KB (32KW) SA89 : 64KB (32KW) SA91 : 64KB (32KW) SA92 : 64KB (32KW) SA92 : 64KB (32KW) SA93 : 64KB (32KW)	Word Mode 200000h 208000h 218000h 218000h 228000h 238000h 238000h 238000h 258000h 258000h 258000h 258000h 268000h 278000h 278000h 288000h 288000h 288000h 288000h 288000h 288000h 288000h 288000h 28000h 28000h 28000h 20000h 20000h 20000h 20000h 20000h 20000h 20000h 20000h 20000h 20000h 20000h 20000h 20000h 20000h 20000h 20000h 20000h	Byte Modi 400000h 410000h 420000h 430000h 430000h 450000h 450000h 480000h 480000h 480000h 480000h 480000h 480000h 480000h 50000h 510000h 530000h 550000h 580000000000
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2: 8KB (4KW) 3: 64KB (32KW) 0: 64KB (32KW) 0: 64KB (32KW) 1: 64KB (32KW) 2: 64KB (32KW) 3: 64KB (32KW) 3: 64KB (32KW) 3: 64KB (32KW) 3: 64KB (32KW) 0: 64KB (32KW) 20: 64KB (32KW) 21: 64KB (32KW) 22: 64KB (32KW) 23: 64KB (32KW) 24: 64KB (32KW) 25: 64KB (32KW) 26: 64KB (32KW)	003000h 004000h 005000h 007000h 018000h 020000h 028000h 028000h 038000h 038000h 058000h 058000h 058000h 078000h 078000h 088000h 088000h 088000h 088000h 088000h 088000h 088000h 088000h 088000h 088000h 088000h 088000h 088000h 088000h	006000h 008000h 002000h 00E000h 010000h 020000h 020000h 030000h 040000h 050000h 050000h 070000h 050000h 070000h 050000h 050000h 050000h 100000h 120000h 130000h 140000h 158000h 158000h 180000h 180000h	T Bank C	SA73 : 64KB (32KW) SA74 : 64KB (32KW) SA75 : 64KB (32KW) SA76 : 64KB (32KW) SA77 : 64KB (32KW) SA77 : 64KB (32KW) SA78 : 64KB (32KW) SA79 : 64KB (32KW) SA79 : 64KB (32KW) SA79 : 64KB (32KW) SA80 : 64KB (32KW) SA81 : 64KB (32KW) SA81 : 64KB (32KW) SA81 : 64KB (32KW) SA81 : 64KB (32KW) SA84 : 64KB (32KW) SA84 : 64KB (32KW) SA85 : 64KB (32KW) SA86 : 64KB (32KW) SA87 : 64KB (32KW) SA89 : 64KB (32KW) SA90 : 64KB (32KW) SA90 : 64KB (32KW) SA91 : 64KB (32KW) SA92 : 64KB (32KW) SA93 : 64KB (32KW) SA92 : 64KB (32KW) SA93 : 64KB (32KW) SA95 : 64KB (32KW) SA95 : 64KB (32KW) SA97 : 64KB (32KW) SA98 : 64KB (32KW) SA97 : 64KB (32KW) SA98 : 64KB (32KW) SA97 : 64KB (32KW) SA98 : 64KB (32KW) SA97 : 64KB (32KW) >	218000h 220000h 228000h 238000h 240000h 258000h 258000h 268000h 268000h 278000h 278000h 28000h 28000h 28000h 28000h 28000h 28000h 28000h 200000h 200000h 20000000h 200000h 200000	430000h 440000h 460000h 470000h 480000h 480000h 480000h 480000h 420000h 420000h 420000h 510000h 520000h 530000h 530000h 550000h 580000h 580000h 520000h 580000h 520000h 580000h 520000h 580000h 520000h
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20:64KB (32KW) 11:64KB (32KW) 22:64KB (32KW) 23:64KB (32KW) 25:64KB (32KW) 25:64KB (32KW) 26:64KB (32KW) 27:64KB (32KW) 29:64KB (32KW) 29:64KB (32KW) 10:64KB (32KW) 11:64KB (32KW) 12:64KB (32KW) 13:64KB (32KW) 14:64KB (32KW) 14:64KB (32KW) 14:64KB (32KW) 14:64KB (32KW) 14:64KB (32KW) 14:64KB (32KW) 14:64KB (32KW) 14:64KB (32KW) 14:64KB (32KW) 11:64KB (32KW) 14:64KB (32KW) 11:64KB (32KW)	070000h 078000h 080000h 098000h 098000h 0A0000h 0A0000h 0B8000h 0B8000h 0C8000h 0C8000h 0D8000h	0E0000h 0F0000h 100000h 120000h 130000h 130000h 158000h 160000h 170000h 180000h 180000h 1A0000h 180000h	Bank C	SA91 : 64KB (32KW) SA92 : 64KB (32KW) SA93 : 64KB (32KW) SA94 : 64KB (32KW) SA95 : 64KB (32KW) SA95 : 64KB (32KW) SA97 : 64KB (32KW) SA98 : 64KB (32KW) SA98 : 64KB (32KW) SA99 : 64KB (32KW) SA99 : 64KB (32KW) SA91 : 64KB (32KW) SA91 : 64KB (32KW) SA100 : 64KB (32KW) SA101 : 64KB (32KW) SA102 : 64KB (32KW)	2A8000h 2B0000h 2C8000h 2C8000h 2D8000h 2D8000h 2E8000h 2E8000h 2F8000h	550000H 560000H 570000H 580000H 590000H 5A0000H 5B0000H 5C0000H 5D0000H 5E0000H
11:64KB (32KW) 12:64KB (32KW) 13:64KB (32KW) 13:64KB (32KW) 15:64KB (32KW) 16:64KB (32KW) 17:64KB (32KW) 18:64KB (32KW) 10:64KB (32KW) 11:64KB (32KW) 12:64KB (32KW) 13:64KB (32KW) 14:64KB (32KW)	078000h 080000h 098000h 098000h 0A0000h 0A0000h 0B8000h 0C0000h 0C0000h 0D8000h 0D8000h	0F0000h 100000h 120000h 130000h 140000h 158000h 160000h 170000h 180000h 180000h 1A0000h 180000h	Bank C	SA92 : 64KB (32KW) SA93 : 64KB (32KW) SA94 : 64KB (32KW) SA95 : 64KB (32KW) SA96 : 64KB (32KW) SA97 : 64KB (32KW) SA98 : 64KB (32KW) SA98 : 64KB (32KW) SA98 : 64KB (32KW) SA99 : 64KB (32KW) SA100 : 64KB (32KW) SA101 : 64KB (32KW) SA102 : 64KB (32KW)	2B0000h 2B8000h 2C0000h 2C8000h 2D0000h 2D8000h 2E0000h 2E8000h 2F0000h 2F8000h	560000h 570000h 580000h 590000h 5A0000h 5B0000h 5C0000h 5D0000h 5E0000h
22:64KB (32KW) 33:64KB (32KW) 44:64KB (32KW) 45:64KB (32KW) 46:64KB (32KW) 47:64KB (32KW) 48:64KB (32KW) 49:64KB (32KW) 49:64KB (32KW) 40:64KB (32KW) 40:64KB (32KW) 41:64KB (32KW) 41:64KB (32KW)	080000h 088000h 090000h 08000h 08000h 08000h 08000h 0C0000h 0C0000h 0D0000h	10000h 11000h 12000h 13000h 14000h 15800h 16000h 17000h 18000h 18000h 1A000h 1B0000h	Bank C	SA93 : 64KB (32KW) SA94 : 64KB (32KW) SA95 : 64KB (32KW) SA96 : 64KB (32KW) SA97 : 64KB (32KW) SA97 : 64KB (32KW) SA99 : 64KB (32KW) SA100 : 64KB (32KW) SA101 : 64KB (32KW) SA102 : 64KB (32KW)	2B8000h 2C0000h 2D0000h 2D8000h 2E0000h 2E0000h 2E8000h 2F8000h	570000h 580000h 590000h 5A0000h 5B0000h 5C0000h 5D0000h 5E0000h
33 : 64KB (32KW) 44 : 64KB (32KW) 55 : 64KB (32KW) 56 : 64KB (32KW) 77 : 64KB (32KW) 78 : 64KB (32KW) 90 : 64KB (32KW) 90 : 64KB (32KW) 11 : 64KB (32KW) 12 : 64KB (32KW) 13 : 64KB (32KW) 14 : 64KB (32KW)	088000h 090000h 098000h 0A0000h 0B0000h 0B8000h 0C0000h 0C8000h 0D0000h 0D8000h	110000h 120000h 130000h 140000h 158000h 160000h 170000h 180000h 1A0000h 1B0000h	Bank C	SA94 : 64KB (32KW) SA95 : 64KB (32KW) SA96 : 64KB (32KW) SA97 : 64KB (32KW) SA98 : 64KB (32KW) SA99 : 64KB (32KW) SA100 : 64KB (32KW) SA101 : 64KB (32KW) SA102 : 64KB (32KW)	2C0000h 2C8000h 2D0000h 2D8000h 2E0000h 2E8000h 2F0000h 2F8000h	580000h 590000h 5A0000h 5B0000h 5C0000h 5D0000h 5E0000h
14:64KB (32KW) 5:64KB (32KW) 6:64KB (32KW) 17:64KB (32KW) 19:64KB (32KW) 19:64KB (32KW) 10:64KB (32KW) 10:64KB (32KW) 11:64KB (32KW) 13:64KB (32KW) 14:64KB (32KW)	090000h 098000h 0A0000h 0B0000h 0B0000h 0C8000h 0C8000h 0D0000h 0D8000h	120000h 130000h 140000h 158000h 160000h 170000h 180000h 180000h 1A0000h 1B0000h	Bank C	SA95 : 64KB (32KW) SA96 : 64KB (32KW) SA97 : 64KB (32KW) SA98 : 64KB (32KW) SA99 : 64KB (32KW) SA100 : 64KB (32KW) SA101 : 64KB (32KW) SA102 : 64KB (32KW)	2C8000h 2D0000h 2D8000h 2E0000h 2E8000h 2F0000h 2F8000h	590000h 5A0000h 5B0000h 5C0000h 5D0000h 5E0000h
16:64KB (32KW) 17:64KB (32KW) 18:64KB (32KW) 19:64KB (32KW) 10:64KB (32KW) 10:64KB (32KW) 11:64KB (32KW) 12:64KB (32KW) 13:64KB (32KW) 14:64KB (32KW) 15:64KB (32KW) 16:64KB (32KW) 17:64KB (32KW) 17:64KB (32KW) 17:64KB (32KW) 17:64KB (32KW)	098000h 0A0000h 0B0000h 0B0000h 0C0000h 0C0000h 0C8000h 0D0000h 0D8000h	130000h 140000h 158000h 160000h 170000h 180000h 180000h 1A0000h 1B0000h	Bank C	SA97 : 64KB (32KW) SA98 : 64KB (32KW) SA99 : 64KB (32KW) SA100 : 64KB (32KW) SA101 : 64KB (32KW) SA102 : 64KB (32KW)	2D0000h 2D8000h 2E0000h 2E8000h 2F0000h 2F8000h	5A0000h 5B0000h 5C0000h 5D0000h 5E0000h
27 : 64KB (32KW) 28 : 64KB (32KW) 29 : 64KB (32KW) 30 : 64KB (32KW) 11 : 64KB (32KW) 22 : 64KB (32KW) 23 : 64KB (32KW) 24 : 64KB (32KW)	0A0000h 0A8000h 0B0000h 0B8000h 0C0000h 0C8000h 0D0000h 0D8000h	140000h 158000h 160000h 170000h 180000h 190000h 1A0000h 1B0000h	Bank C	SA98 : 64KB (32KW) SA99 : 64KB (32KW) SA100 : 64KB (32KW) SA101 : 64KB (32KW) SA102 : 64KB (32KW)	2D8000h 2E0000h 2E8000h 2F0000h 2F8000h	5B0000h 5C0000h 5D0000h 5E0000h
28 : 64KB (32KW) 29 : 64KB (32KW) 30 : 64KB (32KW) 31 : 64KB (32KW) 32 : 64KB (32KW) 33 : 64KB (32KW) 34 : 64KB (32KW)	0A8000h 0B0000h 0B8000h 0C0000h 0C8000h 0D0000h 0D8000h	158000h 160000h 170000h 180000h 190000h 1A0000h 1B0000h	Bank C	 SA99 : 64KB (32KW) SA100 : 64KB (32KW) SA101 : 64KB (32KW) SA102 : 64KB (32KW) 	2E0000h 2E8000h 2F0000h 2F8000h	5D0000h 5E0000h
29 : 64KB (32KW) 30 : 64KB (32KW) 31 : 64KB (32KW) 32 : 64KB (32KW) 33 : 64KB (32KW) 34 : 64KB (32KW)	0B8000h 0C0000h 0C8000h 0D0000h 0D8000h	170000h 180000h 190000h 1A0000h 1B0000h		SA100 : 64KB (32KW) SA101 : 64KB (32KW) SA102 : 64KB (32KW)	2F0000h 2F8000h	5E0000h
80:64KB (32KW) 31:64KB (32KW) 32:64KB (32KW) 33:64KB (32KW) 34:64KB (32KW)	0C0000h 0C8000h 0D0000h 0D8000h	180000h 190000h 1A0000h 1B0000h		SA101 : 64KB (32KW) SA102 : 64KB (32KW)	2F8000h	
31 : 64KB (32KW) 32 : 64KB (32KW) 33 : 64KB (32KW) 34 : 64KB (32KW)	0C8000h 0D0000h 0D8000h	190000h 1A0000h 1B0000h		SA102 : 64KB (32KW)		5F0000h
32 : 64KB (32KW) 33 : 64KB (32KW) 34 : 64KB (32KW)	0D0000h 0D8000h	1A0000h 1B0000h			300000n	
34 : 64KB (32KW)	0D8000h	1B0000h			308000h	600000h 610000h
				SA104 : 64KB (32KW)	310000h	620000h
		1C0000h		SA105 : 64KB (32KW)	318000h	630000ł
35:64KB (32KW)	0E8000h	1D0000h		SA106 : 64KB (32KW)	320000h	640000h
8 <u>6 : 64KB (32KW)</u> 87 : 64KB (32KW)	0F0000h	1E0000h		SA107 : 64KB (32KW)	328000h	650000h
38 : 64KB (32KW)	0F8000h	1F0000h		SA108 : 64KB (32KW) SA109 : 64KB (32KW)	330000h	660000ł
39 : 64KB (32KW)	100000h	200000h		SA109 : 64KB (32KW) SA110 : 64KB (32KW)	338000h	670000h
0 : 64KB (32KW)	108000h	210000h		SA111 : 64KB (32KW)	340000h	680000h
1 : 64KB (32KW)	110000h 118000h	220000h 230000h		SA112 : 64KB (32KW)	348000h 350000h	690000h 6A0000h
2 : 64KB (32KW)	120000h	240000h		SA113 : 64KB (32KW)	358000h	6B0000h
<u>13 : 64KB (32KW)</u>	128000h	250000h		SA114 : 64KB (32KW)	360000h	6C0000h
4 : 64KB (32KW)	130000h	260000h		SA115 : 64KB (32KW)	368000h	6D0000h
1 <u>5 : 64KB (32KW)</u> 16 : 64KB (32KW)	138000h	270000h	\perp	SA116 : 64KB (32KW) SA117 : 64KB (32KW)	370000h	6E0000ł
7 : 64KB (32KW)	140000h	280000h		SA118 : 64KB (32KW)	378000h	6F0000ł
8 : 64KB (32KW)	148000h	290000h		SA119 : 64KB (32KW)	380000h	700000ł
9 : 64KB (32KW)	150000h	2A0000h	T	SA120 : 64KB (32KW)	388000h 390000h	710000ł 720000ł
<u>50 : 64KB (32KW)</u>	158000h 160000h	2B0000h 2C0000h		SA121 : 64KB (32KW)	398000h	730000
51 : 64KB (32KW)	168000h	2D0000h		SA122 : 64KB (32KW)	3A0000h	740000
52 : 64KB (32KW) 53 : 64KB (32KW)	170000h	2E0000h		SA123 : 64KB (32KW) SA124 : 64KB (32KW)	3A8000h	750000ł
54 : 64KB (32KW)	178000h	2F0000h		SA125 : 64KB (32KW)	3B0000h	760000ł
55 : 64KB (32KW)	180000h	300000h		SA126 : 64KB (32KW)	3B8000h	770000ł
6 : 64KB (32KW)	188000h	310000h	Bank D		3C0000h	780000h
57 : 64KB (32KW)	190000h	320000h	Dalik L	SA128 : 64KB (32KW)	3C8000h 3D0000h	790000h 7A0000h
58 : 64KB (32KW)				SA129 : 64KB (32KW)		7B0000
			1			7C0000
	1B0000h	360000h		SA131 : 64KB (32KW)	3E8000h	7D0000ł
	1B8000h	370000h			3F0000h	7E0000ł
	1C0000h	380000h				7F0000ł
64 : 64KB (32KW)	1C8000h	390000h		SA135 : 8KB (4KW)		7F2000h
65 : 64KB (32KW)				SA136 : 8KB (4KW)		7F4000h
6 : 64KB (32KW)				SA137: 8KB (4KW)		7F6000h 7F8000h
				SA138: 8KB (4KW)		7FA000h
						7FC000l
	1F8000h	3F0000h	V		3FF000h	7FE000ł
	1FFFFFh	3FFFFFh	I		3FFFFFh	7FFFFF
<u>69 : 64KB (32KW)</u> 70 : 64KB (32KW)						
		Seator A	rohitooturo			
		Sector A	ichitecture			
	9:64KB (32KW) 0:64KB (32KW) 1:64KB (32KW) 3:64KB (32KW) 5:64KB (32KW) 6:64KB (32KW) 6:64KB (32KW) 6:64KB (32KW) 7:64KB (32KW) 9:64KB (32KW)	9:64KB (32KW) 1A8000h 0:64KB (32KW) 1A8000h 1:64KB (32KW) 1B8000h 2:64KB (32KW) 1B8000h 3:64KB (32KW) 1C8000h 4:64KB (32KW) 1C8000h 5:64KB (32KW) 1C8000h 6:64KB (32KW) 1C8000h 6:64KB (32KW) 1D8000h 7:64KB (32KW) 1D8000h 8:64KB (32KW) 1E8000h 9:64KB (32KW) 1F8000h	0: 0+ND (32KW) 1A0000h 340000h 0: 64KB (32KW) 1A8000h 350000h 1: 64KB (32KW) 1A8000h 360000h 1: 64KB (32KW) 1B8000h 360000h 1: 64KB (32KW) 1C000h 380000h 1: 64KB (32KW) 1C000h 380000h 1: 64KB (32KW) 1C000h 380000h 1: 64KB (32KW) 1D0000h 3A0000h 1: 64KB (32KW) 1D8000h 3B0000h 1: 64KB (32KW) 1D8000h 3B0000h 1: 64KB (32KW) 1E8000h 3D0000h 1: 64KB (32KW) 1E8000h 3D0000h 1: 64KB (32KW) 1F8000h 3E0000h 1: 64KB (32KW) 1F8000h 3F0000h 1: 64KB (32KW) 1F8000h 3F0000h 1: 64KB (32KW) 1F8000h 3F0000h 1: 64KB (32KW) 1FFFFFh 3FFFFFh	0. 04ND (32KW) 1A0000h 340000h 9: 64KB (32KW) 1A8000h 350000h 0: 64KB (32KW) 1A8000h 36000h 1: 64KB (32KW) 1B8000h 36000h 2: 64KB (32KW) 1C0000h 380000h 3: 64KB (32KW) 1C0000h 380000h 4: 64KB (32KW) 1C0000h 380000h 5: 64KB (32KW) 1C8000h 390000h 6: 64KB (32KW) 1D8000h 360000h 6: 64KB (32KW) 1D8000h 30000h 6: 64KB (32KW) 1E0000h 3C0000h 8: 64KB (32KW) 1E8000h 3D0000h 9: 64KB (32KW) 1F8000h 3E0000h 9: 64KB (32KW) 1F8000h 3F0000h 0: 64KB (32KW) 1F8000h 3F0000h 0: 64KB (32KW) 1F8000h 3F0000h 0: 64KB (32KW) 1FFFFFh 3FFFFFFh	O: 04ND (32KW) 1A0000h 340000h SA129: 04ND (32KW) 9: 64KB (32KW) 1A8000h 350000h SA130: 64KB (32KW) 1: 64KB (32KW) 1B8000h 360000h SA131: 64KB (32KW) 1: 64KB (32KW) 1B8000h 360000h SA131: 64KB (32KW) 2: 64KB (32KW) 1B8000h 36000h SA131: 64KB (32KW) 3: 64KB (32KW) 1C0000h 380000h SA131: 64KB (32KW) 3: 64KB (32KW) 1C0000h 380000h SA134: 8KB (4KW) 5: 64KB (32KW) 1D0000h 390000h SA135: 8KB (4KW) 6: 64KB (32KW) 1D0000h 360000h SA136: 8KB (4KW) 7: 64KB (32KW) 1D0000h 3C0000h SA136: 8KB (4KW) 7: 64KB (32KW) 1E0000h 3C0000h SA138: 8KB (4KW) 7: 64KB (32KW) 1F8000h 3D0000h SA139: 8KB (4KW) 9: 64KB (32KW) 1F8000h 3F0000h SA140: 8KB (4KW)	0: 04HD (32KW) 1A0000h 340000h SA122: 04KD (32KW) 3D8000h 0: 64KB (32KW) 1A8000h 350000h SA130: 64KB (32KW) 3D8000h 1: 64KB (32KW) 1B8000h 360000h SA131: 64KB (32KW) 3E8000h 1: 64KB (32KW) 1B8000h 370000h SA132: 64KB (32KW) 3F8000h 2: 64KB (32KW) 1C0000h 380000h SA133: 64KB (32KW) 3F8000h 3: 64KB (32KW) 1C0000h 380000h SA133: 64KB (32KW) 3F8000h 3: 64KB (32KW) 1C0000h 30000h SA135: 8KB (4KW) 3F8000h 5: 64KB (32KW) 1D8000h 3A0000h SA136: 8KB (4KW) 3F8000h 5: 64KB (32KW) 1D8000h 3C0000h SA137: 8KB (4KW) 3F8000h 5: 64KB (32KW) 1B8000h 3D0000h SA137: 8KB (4KW) 3F2000h 5: 64KB (32KW) 1E8000h 3D0000h SA138: 8KB (4KW) 3F2000h 5: 64KB (32KW) 1E8000h 3D0000h SA139: 8KB (4KW) 3F2000h 5: 64KB (32KW) 1E8000h 3D0000h SA139: 8KB (4KW) 3F2000h 5: 64KB (32KW) 1F8000h 3

Bank		Bank 1	Bank 2					
Splits	Volume	Combination	Volume	Combination				
1	8 Mbit	Bank A	56 Mbit	Remainder (Bank B, C, D)				
2	24 Mbit	Bank B	40 Mbit	Remainder (Bank A, C, D)				
3	24 Mbit	Bank C	40 Mbit	Remainder (Bank A, B, D)				
4	8 Mbit	Bank D	56 Mbit	Remainder (Bank A, B, C)				

FlexBank[™] Architecture

Example of Virtual Banks Combination

Bank		Ba	nk 1		Ba	ank 2
Splits	Volume	Combination	Sector Size	Volume	Combination	Sector Size
					Bank B	
			8×8 Kbyte/4 Kword		+	8×8 Kbyte/4 Kword
1	8 Mbit	Bank A	+	56 Mbit	Bank C	+
			15×64 Kbyte/32 Kword		+	111 $ imes$ 64 Kbyte/32 Kword
					Bank D	
		Bank A	16 × 8 Kbyte/4 Kword		Bank B	
2	16 Mbit	+	+	48 Mbit	+	96×64 Kbyte/32 Kword
		Bank D	30×64 Kbyte/32 Kword		Bank C	
					Bank A	
					+	16×8 Kbyte/4 Kword
3	24 Mbit	Bank B	48×64 Kbyte/32 Kword	40 Mbit	Bank C	+
					+	78×64 Kbyte/32 Kword
					Bank D	
		Bank A	8 × 8 Kbyte/4 Kword		Bank C	8 × 8 Kbyte/4 Kword
4	32 Mbit	+	+	32 Mbit	+	+
		Bank B	63×64 Kbyte/32 Kword		Bank D	63×64 Kbyte/32 Kword

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out (they would output the sequence flag once they were selected.) Meanwhile the system would get to read from either Bank C or Bank D.

Simultaneous Operation

Case	Bank 1 Status	Bank 2 Status				
1	Read mode	Read mode				
2	Read mode	Autoselect mode				
3	Read mode	Program mode				
4	Read mode	Erase mode *				
5	Autoselect mode	Read mode				
6	Program mode	Read mode				
7	Erase mode *	Read mode				

*: By writing erase suspend command on the bank address of sector being erased, the erase operation gets suspended so that it enables reading from or programming the remaining sectors.

Note: Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. Actually, the Bank consists of 4 banks, Bank A, Bank B, Bank C and Bank D. Bank Address (BA) meant to specify each of the Banks.

		1				-	ector		C33 I	abies	•		_
					Se	ctor /	Addre	ess				Address	s Range
Bank	Sector	Ban	k Add	lress								Dute Mede	Word Modo
		A 21	A ₂₀	A 19	A 18	A 17	A 16	A 15	A 14	A 13	A ₁₂	Byte Mode	Word Mode
	SA0	0	0	0	0	0	0	0	0	0	0	000000h to 001FFFh	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	0	1	002000h to 003FFFh	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	0	1	0	004000h to 005FFFh	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	0	1	1	006000h to 007FFFh	003000h to 003FFFh
	SA4	0	0	0	0	0	0	0	1	0	0	008000h to 009FFFh	004000h to 004FFFh
	SA5	0	0	0	0	0	0	0	1	0	1	00A000h to 00BFFFh	005000h to 005FFFh
	SA6	0	0	0	0	0	0	0	1	1	0	00C000h to 00DFFFh	006000h to 006FFFh
	SA7	0	0	0	0	0	0	0	1	1	1	00E000h to 00FFFFh	007000h to 007FFFh
	SA8	0	0	0	0	0	0	1	Х	Х	Х	010000h to 01FFFFh	008000h to 00FFFFh
	SA9	0	0	0	0	0	1	0	Х	Х	Х	020000h to 02FFFFh	010000h to 017FFFh
	SA10	0	0	0	0	0	1	1	Х	Х	Х	030000h to 03FFFFh	018000h to 01FFFFh
Bank A	SA11	0	0	0	0	1	0	0	Х	Х	Х	040000h to 04FFFFh	020000h to 027FFFh
	SA12	0	0	0	0	1	0	1	Х	Х	Х	050000h to 05FFFFh	028000h to 02FFFFh
	SA13	0	0	0	0	1	1	0	Х	Х	Х	060000h to 06FFFFh	030000h to 037FFFh
	SA14	0	0	0	0	1	1	1	Х	Х	Х	070000h to 07FFFFh	038000h to 03FFFFh
	SA15	0	0	0	1	0	0	0	Х	Х	Х	080000h to 08FFFFh	040000h to 047FFFh
	SA16	0	0	0	1	0	0	1	Х	Х	Х	090000h to 09FFFFh	048000h to 04FFFFh
	SA17	0	0	0	1	0	1	0	Х	Х	Х	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA18	0	0	0	1	0	1	1	Х	Х	Х	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA19	0	0	0	1	1	0	0	Х	Х	Х	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA20	0	0	0	1	1	0	1	Х	Х	Х	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA21	0	0	0	1	1	1	0	Х	Х	Х	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA22	0	0	0	1	1	1	1	Х	Х	Х	0F0000h to 0FFFFFh	078000h to 07FFFFh
					•				•	•	•	•	(Continued)

Sector Address Tables

(Continued)

					Se	ctor /	Addre	ess				Addres	s Range
Bank	Sector	Ban	k Add	lress								Byte Mode	Word Mode
		A 21	A 20	A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12		
	SA23	0	0	1	0	0	0	0	Х	Х	Х	100000h to 10FFFFh	080000h to 087FFFh
	SA24	0	0	1	0	0	0	1	Х	Х	Х	110000h to 11FFFFh	088000h to 08FFFFh
	SA25	0	0	1	0	0	1	0	Х	Х	Х	120000h to 12FFFFh	090000h to 097FFFh
	SA26	0	0	1	0	0	1	1	Х	Х	Х	130000h to 13FFFFh	098000h to 09FFFFh
	SA27	0	0	1	0	1	0	0	Х	Х	Х	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA28	0	0	1	0	1	0	1	Х	Х	Х	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA29	0	0	1	0	1	1	0	Х	Х	Х	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA30	0	0	1	0	1	1	1	Х	Х	Х	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA31	0	0	1	1	0	0	0	Х	Х	Х	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA32	0	0	1	1	0	0	1	Х	Х	Х	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA33	0	0	1	1	0	1	0	Х	Х	Х	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA34	0	0	1	1	0	1	1	Х	Х	Х	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA35	0	0	1	1	1	0	0	Х	Х	Х	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA36	0	0	1	1	1	0	1	Х	Х	Х	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA37	0	0	1	1	1	1	0	Х	Х	Х	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA38	0	0	1	1	1	1	1	Х	Х	Х	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh
	SA39	0	1	0	0	0	0	0	Х	Х	Х	200000h to 20FFFFh	100000h to 107FFFh
	SA40	0	1	0	0	0	0	1	Х	Х	Х	210000h to 21FFFFh	108000h to 10FFFFh
	SA41	0	1	0	0	0	1	0	Х	Х	Х	220000h to 22FFFFh	110000h to 117FFFh
	SA42	0	1	0	0	0	1	1	Х	Х	Х	230000h to 23FFFFh	118000h to 11FFFFh
	SA43	0	1	0	0	1	0	0	Х	Х	Х	240000h to 24FFFFh	120000h to 127FFFh
	SA44	0	1	0	0	1	0	1	Х	Х	Х	250000h to 25FFFFh	128000h to 12FFFFh
	SA45	0	1	0	0	1	1	0	Х	Х	Х	260000h to 26FFFFh	130000h to 137FFFh
	SA46	0	1	0	0	1	1	1	Х	Х	Х	270000h to 27FFFFh	138000h to 13FFFFh
Bank B	SA47	0	1	0	1	0	0	0	Х	Х	Х	280000h to 28FFFFh	140000h to 147FFFh
	SA48	0	1	0	1	0	0	1	Х	Х	Х	290000h to 29FFFFh	148000h to 14FFFFh
	SA49	0	1	0	1	0	1	0	Х	Х	Х	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA50	0	1	0	1	0	1	1	Х	Х	Х	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA51	0	1	0	1	1	0	0	Х	Х	Х	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA52	0	1	0	1	1	0	1	Х	Х	Х	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA53	0	1	0	1	1	1	0	Х	Х	Х	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA54	0	1	0	1	1	1	1	X	X	X	2F0000h to 2FFFFh	178000h to 17FFFFh
	SA55	0	1	1	0	0	0	0	Х	Х	Х	300000h to 30FFFFh	180000h to 187FFFh
	SA56	0	1	1	0	0	0	1	Х	Х	Х	310000h to 31FFFFh	188000h to 18FFFFh
	SA57	0	1	1	0	0	1	0	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA58	0	1	1	0	0	1	1	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA59	0	1	1	0	1	0	0	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA60	0	1	1	0	1	0	1	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA61	0	1	1	0	1	1	0	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA62	0	1	1	0	1	1	1	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA63	0	1	1	1	0	0	0	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA64	0	1	1	1	0	0	1	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFh
	SA65	0	1	1	1	0	1	0	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA65	0	1	1	1	0	1	1	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA60 SA67	0	1	1	1	1	0	0	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA67	0	1	1	1	1	0	1	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA69	0	1	1	1	1	1	0	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
	SA09 SA70	0	1	1	1	1	1	1	X	X	X	3F0000h to 3FFFFFh	1F8000h to 1FFFFh
	5410	0	1		I	1	1	'	^	^	^		(Continued

(Continued)

Bank					Se	ctor /	Addre	ess				Address	s Range
Bank	Sector	Banl	k Add	ress								Byte Mode	Word Mode
		A 21	A 20	A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12	Byte wode	
	SA71	1	0	0	0	0	0	0	Х	Х	Х	400000h to 40FFFFh	200000h to 207FFFh
	SA72	1	0	0	0	0	0	1	Х	Х	Х	410000h to 41FFFFh	208000h to 20FFFFh
	SA73	1	0	0	0	0	1	0	Х	Х	Х	420000h to 42FFFFh	210000h to 217FFFh
	SA74	1	0	0	0	0	1	1	Х	Х	Х	430000h to 43FFFFh	218000h to 21FFFF
	SA75	1	0	0	0	1	0	0	Х	Х	Х	440000h to 44FFFFh	220000h to 227FFF
	SA76	1	0	0	0	1	0	1	Х	Х	Х	450000h to 45FFFFh	228000h to 22FFFF
	SA77	1	0	0	0	1	1	0	Х	Х	Х	460000h to 46FFFFh	230000h to 237FFFI
	SA78	1	0	0	0	1	1	1	Х	Х	Х	470000h to 47FFFFh	238000h to 23FFFF
	SA79	1	0	0	1	0	0	0	Х	Х	Х	480000h to 48FFFFh	240000h to 247FFF
	SA80	1	0	0	1	0	0	1	Х	Х	Х	490000h to 49FFFFh	248000h to 24FFFF
	SA81	1	0	0	1	0	1	0	Х	Х	Х	4A0000h to 4AFFFFh	250000h to 257FFFI
	SA82	1	0	0	1	0	1	1	Х	Х	Х	4B0000h to 4BFFFFh	258000h to 25FFFFh
	SA83	1	0	0	1	1	0	0	Х	Х	Х	4C0000h to 4CFFFFh	260000h to 267FFF
	SA84	1	0	0	1	1	0	1	Х	Х	Х	4D0000h to 4DFFFFh	268000h to 26FFFF
	SA85	1	0	0	1	1	1	0	Х	Х	Х	4E0000h to 4EFFFFh	270000h to 277FFF
	SA86	1	0	0	1	1	1	1	Х	Х	Х	4F0000h to 4FFFFh	278000h to 27FFFF
	SA87	1	0	1	0	0	0	0	Х	Х	Х	500000h to 50FFFFh	280000h to 287FFF
	SA88	1	0	1	0	0	0	1	Х	Х	Х	510000h to 51FFFFh	288000h to 28FFFF
	SA89	1	0	1	0	0	1	0	Х	Х	Х	520000h to 52FFFFh	290000h to 297FFF
	SA90	1	0	1	0	0	1	1	X	X	X	530000h to 53FFFFh	298000h to 29FFFF
	SA91	1	0	1	0	1	0	0	X	X	X	540000h to 54FFFFh	2A0000h to 2A7FFF
	SA92	1	0	1	0	1	0	1	X	X	X	550000h to 55FFFFh	2A8000h to 2AFFFF
	SA93	1	0	1	0	1	1	0	X	X	X	560000h to 56FFFFh	2B0000h to 2B7FFF
	SA94	1	0	1	0	1	1	1	X	X	X	570000h to 57FFFFh	2B8000h to 2BFFFF
Bank C	SA95	1	0	1	1	0	0	0	X	X	X	580000h to 58FFFFh	2C0000h to 2C7FFF
	SA96	1	0	1	1	0	0	1	X	X	X	590000h to 59FFFFh	2C8000h to 2CFFFF
	SA97	1	0	1	1	0	1	0	X	X	X	5A0000h to 5AFFFFh	2D0000h to 2D7FFF
	SA98	1	0	1	1	0	1	1	X	X	X	5B0000h to 5BFFFFh	2D8000h to 2DFFFF
	SA99	1	0	1	1	1	0	0	X	X	X	5C0000h to 5CFFFFh	2E0000h to 2E7FFF
	SA100	1	0	1	1	1	0	1	X	X	X	5D0000h to 5DFFFFh	2E8000h to 2EFFFF
	SA101	1	0	1	1	1	1	0	X	X	X	5E0000h to 5EFFFFh	2F0000h to 2F7FFFI
	SA102	1	0	1	1	1	1	1	X	X	X	5F0000h to 5FFFFh	2F8000h to 2FFFFF
	SA103	1	1	0	0	0	0	0	X	X	X	600000h to 60FFFFh	300000h to 307FFF
	SA104	1	1	0	0	0	0	1	X	X	X	610000h to 61FFFFh	308000h to 30FFFF
	SA105	1	1	0	0	0	1	0	X	X	X	620000h to 62FFFFh	310000h to 317FFF
	SA105	1	1	0	0	0	1	1	X	X	X	630000h to 63FFFFh	318000h to 31FFFF
	SA107	1	1	0	0	1	0	0	X	X	X	640000h to 64FFFFh	320000h to 327FFFI
	SA108	1	1	0	0	1	0	1	X	X	X	650000h to 65FFFFh	328000h to 32FFFF
	SA109	1	1	0	0	1	1	0	X	X	X	660000h to 66FFFFh	330000h to 337FFF
	SA110	1	1	0	0	1	1	1	X	X	X	670000h to 67FFFh	338000h to 33FFFFI
	SA111	1	1	0	1	0	0	0	X	X	X	680000h to 68FFFFh	340000h to 347FFF
	SA112	1	1	0	1	0	0	1	X	X	X	690000h to 69FFFFh	348000h to 34FFFF
	SA113	1	1	0	1	0	1	0	X	X	X	6A0000h to 6AFFFFh	350000h to 357FFF
	SA114	1	1	0	1	0	1	1	X	X	X	6B0000h to 6BFFFFh	358000h to 35FFFF
	SA115	1	1	0	1	1	0	0	X	X	X	6C0000h to 6CFFFh	360000h to 367FFF
	SA116	1	1	0	1	1	0	1	X	X	X	6D0000h to 6DFFFFh	368000h to 36FFFF
	SA117	1	1	0	1	1	1	0	X	X	X	6E0000h to 6EFFFFh	370000h to 377FFFI
	0,111	1	1	0	1	1	1	1	X	X	X	6F0000h to 6FFFFh	378000h to 37FFFF

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					Se	ctor /	Addre	ess				Address	s Range
Bank	Sector	Banl	k Add	ress								Dute Made	Mand Made
		A 21	A 20	A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12	Byte Mode	Word Mode
	SA119	1	1	1	0	0	0	0	Х	Х	Х	700000h to 70FFFFh	380000h to 387FFFh
	SA120	1	1	1	0	0	0	1	Х	Х	Х	710000h to 71FFFFh	388000h to 38FFFFh
	SA121	1	1	1	0	0	1	0	Х	Х	Х	720000h to 72FFFFh	390000h to 397FFFh
	SA122	1	1	1	0	0	1	1	Х	Х	Х	730000h to 73FFFFh	398000h to 39FFFFh
	SA123	1	1	1	0	1	0	0	Х	Х	Х	740000h to 74FFFFh	3A0000h to 3A7FFFh
	SA124	1	1	1	0	1	0	1	Х	Х	Х	750000h to 75FFFFh	3A8000h to 3AFFFFh
	SA125	1	1	1	0	1	1	0	Х	Х	Х	760000h to 76FFFFh	3B0000h to 3B7FFFh
	SA126	1	1	1	0	1	1	1	Х	Х	Х	770000h to 77FFFFh	3B8000h to 3BFFFFh
	SA127	1	1	1	1	0	0	0	Х	Х	Х	780000h to 78FFFFh	3C0000h to 3C7FFFh
F	SA128	1	1	1	1	0	0	1	Х	Х	Х	790000h to 79FFFFh	3C8000h to 3CFFFFh
	SA129	1	1	1	1	0	1	0	Х	Х	Х	7A0000h to 7AFFFFh	3D0000h to 3D7FFFh
Bank D	SA130	1	1	1	1	0	1	1	Х	Х	Х	7B0000h to 7BFFFFh	3D8000h to 3DFFFFh
	SA131	1	1	1	1	1	0	0	Х	Х	Х	7C0000h to 7CFFFFh	3E0000h to 3E7FFFh
	SA132	1	1	1	1	1	0	1	Х	Х	Х	7D0000h to 7DFFFFh	3E8000h to 3EFFFFh
	SA133	1	1	1	1	1	1	0	Х	Х	Х	7E0000h to 7EFFFFh	3F0000h to 3F7FFFh
	SA134	1	1	1	1	1	1	1	0	0	0	7F0000h to 7F1FFFh	3F8000h to 3F8FFFh
	SA135	1	1	1	1	1	1	1	0	0	1	7F2000h to 7F3FFFh	3F9000h to 3F9FFFh
	SA136	1	1	1	1	1	1	1	0	1	0	7F4000h to 7F5FFFh	3FA000h to 3FAFFFh
	SA137	1	1	1	1	1	1	1	0	1	1	7F6000h to 7F7FFFh	3FB000h to 3FBFFFh
	SA138	1	1	1	1	1	1	1	1	0	0	7F8000h to 7F9FFFh	3FC000h to 3FCFFFh
	SA139	1	1	1	1	1	1	1	1	0	1	7FA000h to 7FBFFFh	3FD000h to 3FDFFFh
	SA140	1	1	1	1	1	1	1	1	1	0	7FC000h to 7FDFFFh	3FE000h to 3FEFFFh
	SA141	1	1	1	1	1	1	1	1	1	1	7FE000h to 7FFFFFh	3FF000h to 3FFFFFh

Sector Group	A 21	A 20	A 19	A18	A17	A16	A15	A 14	A 13	A 12	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	1	0	SA1
SGA3	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	1	0	0	SA3
SGA5	0	0	0	0	0	0	0	1	0	1	SA5
SGA5 SGA6	0	0	0	0	0	0	0	1	1	0	SA5 SA6
	0	0	0	0	0	0	-			-	SA0
SGA7	0	0	0	0	0	-	0	1	1	1	547
0040	0	0	~		0	0	1	Ň	X	X	
SGA8	0	0	0	0	0	1	0	Х	Х	X	SA8 to SA10
SGA9	0	0	0	0	1	0	1	V	V	V	SA11 to SA14
	-	0	0	0	1	X	X	X	X	X	
SGA10	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	0	1	0	0	X	Х	X	X	X	SA23 to SA26
SGA13	0	0	1	0	1	Х	Х	Х	Х	Х	SA27 to SA30
SGA14	0	0	1	1	0	Х	Х	Х	Х	Х	SA31 to SA34
SGA15	0	0	1	1	1	Х	Х	Х	Х	Х	SA35 to SA38
SGA16	0	1	0	0	0	Х	Х	Х	Х	Х	SA39 to SA42
SGA17	0	1	0	0	1	Х	Х	Х	Х	Х	SA43 to SA46
SGA18	0	1	0	1	0	Х	Х	Х	Х	Х	SA47 to SA50
SGA19	0	1	0	1	1	Х	Х	Х	Х	Х	SA51 to SA54
SGA20	0	1	1	0	0	Х	Х	Х	Х	Х	SA55 to SA58
SGA21	0	1	1	0	1	Х	Х	Х	Х	Х	SA59 to SA62
SGA22	0	1	1	1	0	Х	Х	Х	Х	Х	SA63 to SA66
SGA23	0	1	1	1	1	Х	Х	Х	Х	Х	SA67 to SA70
SGA24	1	0	0	0	0	Х	Х	Х	Х	Х	SA71 to SA74
SGA25	1	0	0	0	1	Х	Х	Х	Х	Х	SA75 to SA78
SGA26	1	0	0	1	0	Х	Х	Х	Х	Х	SA79 to SA82
SGA27	1	0	0	1	1	Х	Х	Х	Х	Х	SA83 to SA86
SGA28	1	0	1	0	0	Х	Х	Х	х	Х	SA87 to SA90
SGA29	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA30	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA31	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA32	1	1	0	0	0	X	X	X	X	X	SA103 to SA106
SGA33	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA34	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA35	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA35 SGA36	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA30 SGA37	1	1	1	0	1		X				SA123 to SA122
			1	-		X		X	X	X	
SGA38	1	1	1	1	0	X	X	Х	Х	Х	SA127 to SA130
00400						0	0				0.4.04 / 0.4.00
SGA39	1	1	1	1	1	0	1	Х	Х	Х	SA131 to SA133
						1	0				
SGA40	1	1	1	1	1	1	1	0	0	0	SA134
SGA41	1	1	1	1	1	1	1	0	0	1	SA135
SGA42	1	1	1	1	1	1	1	0	1	0	SA136
SGA43	1	1	1	1	1	1	1	0	1	1	SA137
SGA44	1	1	1	1	1	1	1	1	0	0	SA138
SGA45	1	1	1	1	1	1	1	1	0	1	SA139
SGA46	1	1	1	1	1	1	1	1	1	0	SA140
SGA47	1	1	1	1	1	1	1	1	1	1	SA141

Sector Group Addresses

Туре	A21 to A12	A ₆	A3	A 2	A 1	Ao	Code (HEX)
Manufacture's Code	BA	L	L	L	L	L	04h
Device Code	BA	L	L	L	L	Н	227Eh
Extended Device	BA	L	Н	Н	Н	L	2202h
Code *2	BA	L	Н	Н	Н	Н	2201h
Sector Group Protec- tion	Sector Group Addresses	L	L	L	Н	L	01h*1

Flash Memory Autoselect Codes

Legend: $L = V_{IL}$, $H = V_{IH}$. See DC Characteristics for voltage levels.

*1 : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*2 : A read cycle at address (BA) 01h outputs device code. When 227Eh was output, this indicates that there will require two additional codes, called Extended Device Codes. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh.

		_					mmand		Fourth	Bus			•	_
Comma Sequen		Bus Write Cycles	First Write (Secono Write (Cycle	Third Write (Cycle	Read/ Cyc	Write	Fifth Write	Cycle	Sixth Write	Cycle
		Req'd	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	Word Byte	1	XXXh	F0h	_	—	—	—	—	—	_	—	_	_
Read/Reset	Word Byte	3	555h AAAh	AAh	2AAh 555h	55h	555h AAAh	F0h	RA	RD		_		_
	Word		555h		2AAh		(BA) 555h							
Autoselect	Byte	3	AAAh	AAh	555h	55h	(BA) AAAh	90h	_	_	—	_	—	_
Program	Word Byte	4	555h AAAh	AAh	2AAh 555h	55h	555h AAAh	A0h	PA	PD	_	_	_	_
Program Sus	pend	1	BA	B0h	_	—	_	—	—	—	_	_	_	—
Program Res	ume	1	BA	30h	_	—	_	—	—	—	_	_	_	—
Chip Erase	Word Byte	6	555h AAAh	AAh	2AAh 555h	55h	555h AAAh	80h	555h AAAh	AAh	2AAh 555h	55h	555h AAAh	10h
Sector Erase	Word Byte	6	555h AAAh	AAh	2AAh 555h	55h	555h AAAh	80h	555h AAAh	AAh	2AAh 555h	55h	SA	30h
Erase Suspe		1	BA	B0h				_		_				_
Erase Resum		1	BA	30h							_		_	_
Extended Sector Group Protection *2	Word Byte	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD		_		
Set to Fast Mode	Word Byte	3	555h AAAh	AAh	2AAh 555h	55h	555h AAAh	20h	_					_
Fast Program *1	Word Byte	2	XXXh XXXh	A0h	PA	PD		_		_				
Reset from Fast Mode *1	Word Byte	2	BABA	90h	XXXh XXXh	*4 F0h	_							_
Over	Word	4	(BA) 55h	006										
Query	Byte	1	(BA) AAh	98h	_		_	_		_	_	_	_	_
HiddenROM Entry	Word Byte	3	555h AAAh	AAh	2AAh 555h	55h	555h AAAh	88h	_	_		_		_
HiddenROM Program * ³	Word Byte	4	555h AAAh	AAh	2AAh 555h	55h	555h AAAh	A0h	(HRA) PA	PD		_		_
HiddenROM	Word	4	555h	۸ ۸ հ	2AAh	E E L	(HRBA) 555h	005	VVVL	005				
Exit *3	Byte	4	AAAh	AAh	555h	55h	(HRBA) AAAh	90h	XXXh	00h				

Flash Memory Command Definitions

(Continued)

*1: This command is valid while Fast Mode.

*2: This command is valid while $\overline{\text{RESET}} = V_{\text{ID.}}$

- *3: This command is valid while HiddenROM mode.
- *4: The data "00h" is also acceptable.
- Notes : Address bits A₂₁ to A₁₁ = X = "H" or "L" for all address commands except or Program Address (PA), Sector Address (SA), and Bank Address (BA), and Sector Group Address (SPA).
 - Bus operations are defined.
 - RA = Address of the memory location to be read
 - PA = Address of the memory location to be programmed

Addresses are latched on the falling edge of the write pulse.

- SA = Address of the sector to be erased. The combination of A₂₁, A₂₀, A₁₉, A₁₈, A₁₇, A₁₆, A₁₅, A₁₄, A₁₃, and
- A12 will uniquely select any sector.
 - $BA = Bank Address (A_{21}, A_{20}, A_{19})$
- RD = Data read from location RA during read operation.
 - PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
- SPA = Sector group address to be protected. Set sector group address and (A₆, A₃, A₂, A₁, A₀) = (0, 0, 0, 1, 0).

SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.

• HRA = Address of the HiddenROM area Word Mode : 000000h to 00007Fh

Byte Mode : 000000h to 0000FFh

- HRBA = Bank Address of the HiddenROM area (A₂₁ = A₂₀ = A₁₉ = VIL)
- The system should generate the following address patterns: Word Mode: 555h or 2AAh to addresses A₁₀ to A₀
 - Byte Mode: AAAh or 555h to addresses A10 to A0, and A-1
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rat	ing	Unit
Falameter	Symbol	Min	Max	Onit
Storage Temperature	Tstg	-55	+125	°C
Ambient Temperature with Power Applied	Та	-40	+85	°C
Voltage with Respect to Ground All pins	Vin, Vout	-0.3	Vccf +0.3	V
except RESET, WP/ACC *1	VIN, VOUT	-0.3	Vccs +0.3	V
Vccf/Vccs Supply *1	Vccf, Vcc s	-0.3	+3.3	V
RESET *2	Vin	-0.5	+ 13.0	V
WP/ACC *3	Vin	-0.5	+10.5	V

*1 Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, input or I/O pins may undershoot Vss to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is Vccf + 0.3 V or Vccs + 0.3 V. During voltage transitions, input or I/O pins may overshoot to Vccf + 2.0 V or Vccs + 2.0 V for periods of up to 20 ns.

- *2: Minimum DC input voltage on RESET pin is –0.5 V. During voltage transitions, RESET pins may undershoot Vss to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (VIN-Vccf or Vccs) does not exceed +9.0 V. Maximum DC input voltage on RESET pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.
- *3: Minimum DC input voltage on WP/ACC pin is –0.5 V. During voltage transitions, WP/ACC pin may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on WP/ACC pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when Vccf is applied.
- WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit	
Farameter	Symbol	Min	Max	Unit
Ambient Temperature	Та	-40	+85	°C
Vccf/Vccs Supply Voltages	Vccf, Vccs	+2.7	+3.1	V

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Co	nditions			Value		Unit
Farameter	Symbol		nations		Min	Тур	Max	Unit
Input Leakage Current	lu	VIN = Vss to Vccf, V	/cc s		-1.0	_	+1.0	μΑ
Output Leakage Current	Ilo	Vout = Vss to Vccf,	Vccs		-1.0	—	+1.0	μΑ
RESET Inputs Leakage Current	Ілт	Vccf = Vccf Max, V RESET = 12.5 V	′ccs = Vccs Max,		_	_	35	μA
Acc Input Leakage Current	LIA	Vccf = Vccf Max, V WP/ACC = Vacc M			_	20	mA	
			tcycle = 5 MHz	Byte	_	_	16	m۸
Flash Vcc Active Current	lf	<u>CE</u> f = Vı∟,	tcycle = 5 MHz	Word	_	_	18	– mA
(Read) *1	lcc₁f	OE = VIH	tcycle = 1 MHz	Byte	_	_	4	
			tcycle = 1 MHz	Word	_	_	4	mA
Flash Vcc Active Current*2	Icc ₂ f	$\overline{CE}f = V_{IL}, \overline{OE} = V_{I}$	н		_	_	30	mA
Flash Vcc Active Current				Byte	_	_	46	
(Read-While-Program) *5	lcc3f	$\overline{CE}f = V_{IL}, \overline{OE} = V_{I}$	Н	Word	_	_	48	mA
Flash Vcc Active Current				Byte	_	_	46	
(Read-While-Erase) *5	lcc₄f	$\overline{CE}f = V_{IL}, \overline{OE} = V_{I}$	Н	Word	_	_	48	mA
Flash Vcc Active Current (Erase-Suspend-Program)	lcc5f	$\overline{CE}f = V_{IL}, \overline{OE} = V_{I}$	1	_	_	30	mA	
SRAM Vcc Active Current	Icc1S	$\label{eq:Vccs} \begin{split} \frac{V_{ccs} = V_{ccs} \; Max,}{CE1s = V_{IL},} \\ CE2s = V_{IH} \end{split}$	tcycle = 10 MHz	_	_	50	mA	
		<u>CE1</u> s = 0.2 V,	tcycle = 10 MHz		_	_	50	mA
SRAM Vcc Active Current	Icc2S	CE2s = Vccs – 0.2 V	tcycle = 1 MHz		—	_	10	mA
Flash Vcc Standby Current	Isb1f	Vccf = Vccf Max, C RESET = Vccf ± 0 WP/ACC = Vccf ± 0	.3 V,	/	_	1	5	μA
Flash Vcc Standby Current (RESET)	Isb2f	Vccf = Vccf Max, F WP/ACC = Vccf±		3 V,	_	1	5	μΑ
Flash Vcc Current (Automatic Sleep Mode) *3	lsвзf	$\frac{V_{ccf} = V_{ccf} Max, \overline{C}}{\overline{RESET} = V_{ccf} \pm 0}$ $\frac{WP}{ACC} = V_{ccf} \pm 0$ $V_{IN} = V_{ccf} \pm 0.3 V C$.3 V, 0.3 V,			1	5	μA
SRAM Vcc Standby Current	Isb1 S	CE1s ≥ Vccs – 0.2	2 V, CE2s <u>></u> Vccs	– 0.2 V	_	_	15	μΑ
SRAM Vcc Standby Current	Isb2 S	CE2s <u><</u> 0.2V			_	_	15	μA

(Continued)

Parameter	Symbol	Conditions			Value		Unit
Farameter	Symbol	Conditions		Min	Тур	Max 0.5 Vcc+0.3 *6 12.5 9.5 0.45 0.4 2.5	Unit
Input Low Level	VIL	—		-0.3	_	0.5	V
Input High Level	Vін	_		2.4			V
Voltage for Sector Protection, and Temporary Sector Unpro- tection (RESET) *4	Vid	_		11.5	12	12.5	V
Voltage for Program Acceleration (WP/ACC) *4	VACC	_		8.5	9.0	9.5	V
Output Low Voltage Level	Vol	Vccf = Vccf Min, Io∟= 4.0 mA	Flash	_	_	0.45	V
Oulput Low Voltage Level	VOL	Vccs = Vccs Min, Io∟= 1.0 mA	SRAM	_	_	0.4	V
Output High Voltage Level	Vон	Vccf = Vccf Min, Iон= –0.1 mA	Flash	0.85× Vccf	_	_	V
		Vccs = Vccs Min, Iон= –0.5 mA	SRAM	2.2	_	_	V
Flash Low Vccf Lock-Out Voltage	Vlko	_		2.3	2.4	2.5	V

*1: The Icc current listed includes both the DC operating current and the frequency dependent component.

*2: Icc active while Embedded Algorithm (program or erase) is in progress.

*3: Automatic sleep mode enables the low power mode when address remains stable for 150 ns.

*4: Applicable for only Vccf applying.

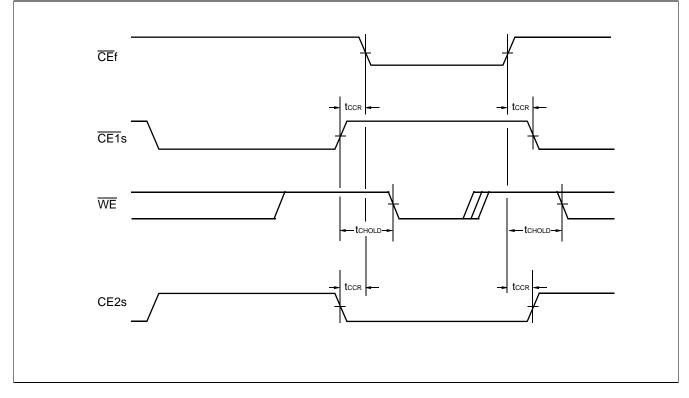
*5: Embedded Alogorithm (program or erase) is in progress. (@5 MHz)

*6: Vcc indicates lower of Vccf or Vccs.

2. AC Characteristics • CE Timing

Parameter	Syn	nbol	Condition	Va	Unit	
Farameter	JEDEC	Standard	Condition	Min	Max	Onit
CE Recover Time	_	tccr	—	0	—	ns
CE Hold Time	_	t CHOLD	—	3	—	ns

• Timing Diagram for alternating SRAM to Flash

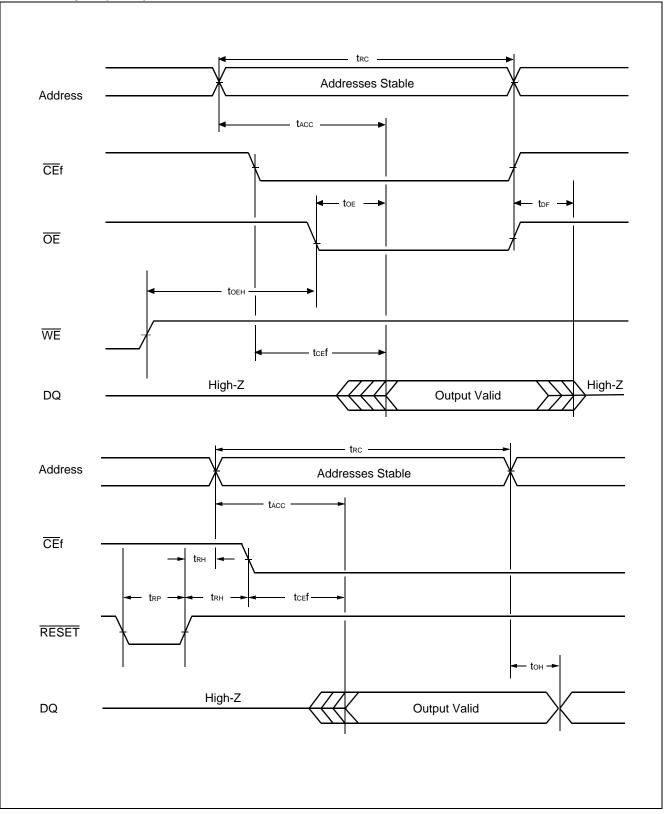


Parameter	Syn	nbol	Condition	Val	ue*	Unit
Farameter	JEDEC	Standard	Condition	Min	Max	Unit
Read Cycle Time	tavav	t RC	_	70	—	ns
Address to Output Delay	t avqv	tacc	$\frac{\overline{CE}f}{\overline{OE}} = V_{IL}$	—	70	ns
Chip Enable to Output Delay	t elqv	tc⊧f	OE = VIL	_	70	ns
Output Enable to Output Delay	t GLQV	toe	—	—	30	ns
Chip Enable to Output High-Z	t ehqz	tdf	—	—	25	ns
Output Enable to Output High-Z	t _{GHQZ}	tdf	—	—	25	ns
Output Hold Time From Addresses, CEf or OE, Whichever Occurs First	taxqx	tон	_	0	_	ns
RESET Pin Low to Read Mode	—	t READY	—	—	20	μs

• Read Only Operations Characteristics (Flash)

*: Test Conditions– Output Load:1 TTL gate and 30 pF Input rise and fall times: 5 ns Input pulse levels: 0.0 V to Vccf Timing measurement reference level Input: 0.5×Vccf Output: 0.5×Vccf

• Read Cycle (Flash)



• Write/Erase/Program Operations

Write/Erase/Program Operations		Symbol		Value				
Parameter			JEDEC	Standard	Min	Тур	Max	Unit
Write Cycle Time			t avav	twc	70			ns
Address Setup Time			t avwl	tas	0			ns
Address Setup Time to OE Low During Toggle Bit Polling			taso	12			ns	
Address Hold Time			t wLAX	tан	45			ns
Address Hold Time from CE or OE High During Toggle Bit Polling			tант	0			ns	
Data Setup Time			t dvwh	tos	30			ns
Data Hold Time		t whdx	tон	0			ns	
Output Enable Hold Time	Read			tоен	0			ns
	Toggle and Data Polling				10			ns
CE High During Toggle Bit Polling			t CEPH	20			ns	
OE High During Toggle Bit Polling				toeph	20			ns
Read Recover Time Before Write			t GHWL	t GHWL	0			ns
Read Recover Time Before Write			t GHEL	t GHEL	0	—		ns
CE Setup Time			t elwl	tcs	0			ns
WE Setup Time		twlel	tws	0			ns	
CE Hold Time		twhen	tсн	0			ns	
WE Hold Time		t ehwh	twн	0			ns	
Write Pulse Width		t wlwh	twp	35		—	ns	
CE Pulse Width		t eleh	tcp	35	—		ns	
Write Pulse Width High		t whwL	twpн	25			ns	
CE Pulse Width High		t ehel	tсрн	25			ns	
Programming Operation		Byte	t	twnwn1		4		μs
	peration	Word	twhwh1	LVVHVVHI		6	_	μs
Sector Erase Operation *1		t wHwH2	t wHwH2		0.5	—	S	
Vcc Setup Time				tvcs	50	—		μs
Rise Time to V _{ID} *2				tvidr	500		—	ns
Rise Time to V _{ACC} *3				t vaccr	500			ns
Voltage Transition Time *2				tvlht	4			μs
Write Pulse Wic	Write Pulse Width *2			twpp	100			μs

(Continued)

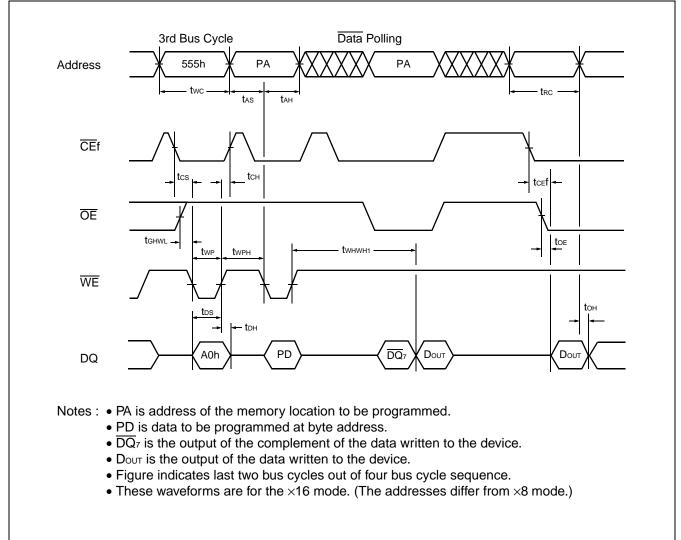
Peromotor	Symbol		Value			l Init
Parameter	JEDEC	Standard	Min	Тур	Max	Unit
OE Setup Time to WE Active *2		toesp	4			μs
CE Setup Time to WE Active *2		tcsp	4		_	μs
Recover Time from RY/BY		trв	0			ns
RESET Pulse Width		t RP	500		_	ns
RESET High Level Period Before Read	—	tкн	200		_	ns
BYTE Switching Low to Output High-Z		t FLQZ			30	ns
BYTE Switching High to Output Active		t fhqv			70	ns
Program/Erase Valid to RY/BY Delay		t BUSY			90	ns
Delay Time from Embedded Output Enable		t eoe	_	_	70	ns
Erase Time-out Time	—	tтоw	50		_	μs
Erase Suspend Transition Time		t spd			20	μs

*1: This does not include preprogramming time.

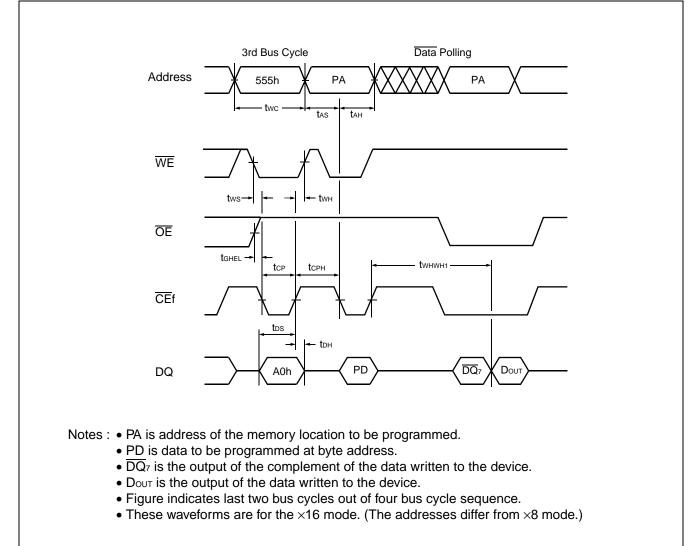
*2: This timing is for Sector Group Protection operation.

*3: This timing is for Accelerated Program operation.

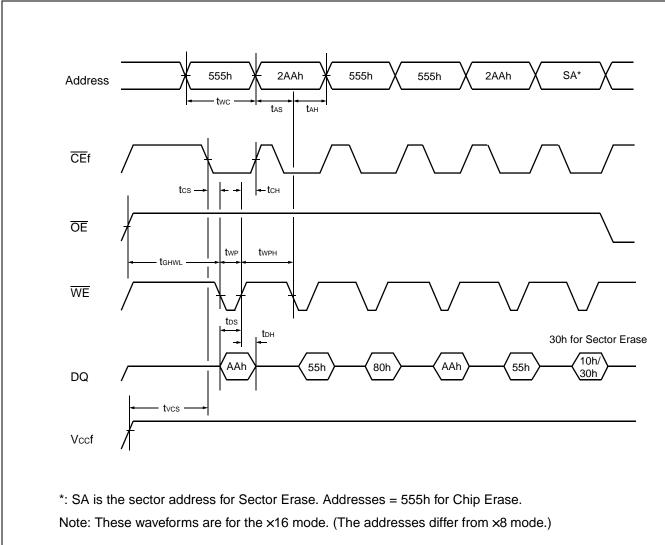
• Write Cycle (WE control) (Flash)

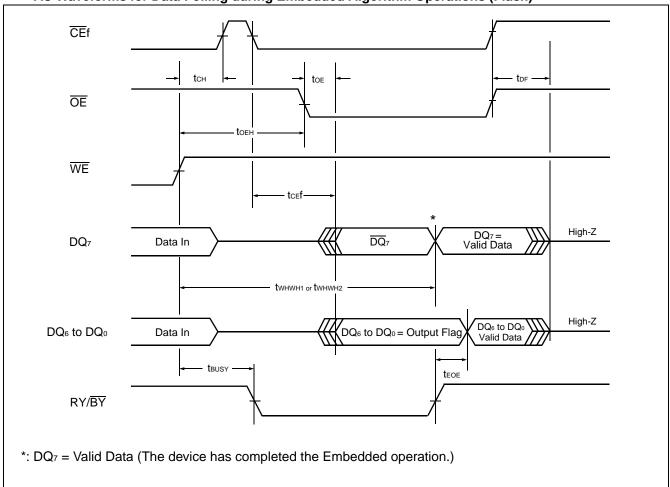


• Write Cycle (CEf control) (Flash)

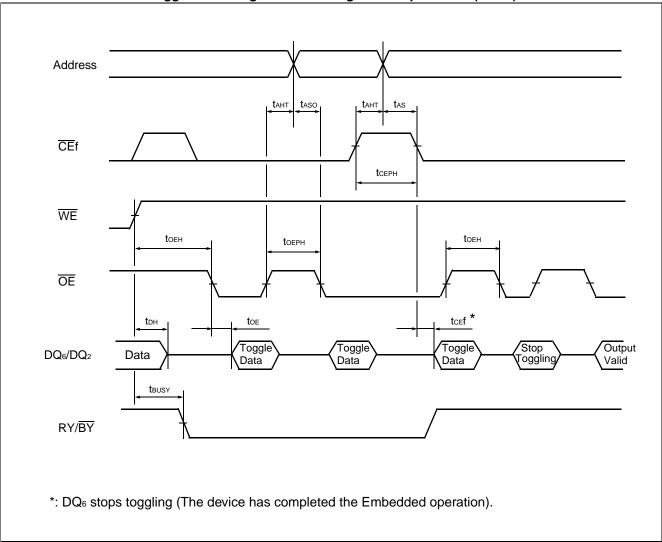




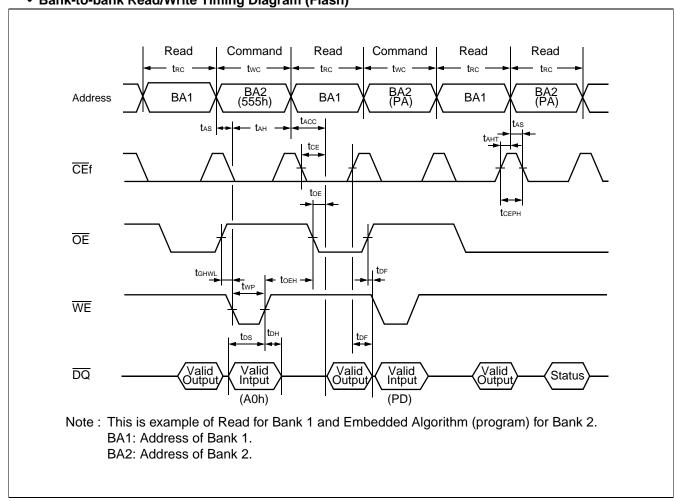




• AC Waveforms for Data Polling during Embedded Algorithm Operations (Flash)

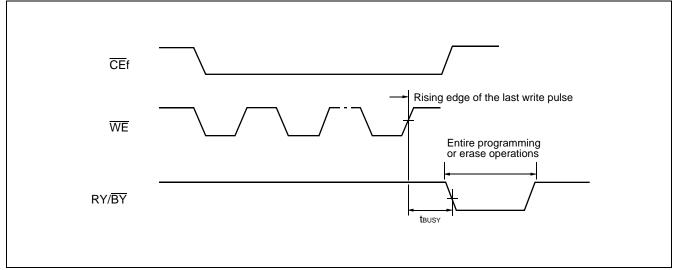


• AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)

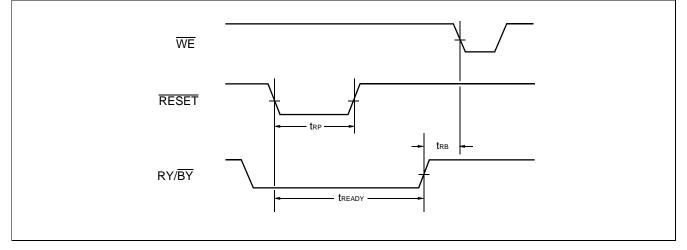


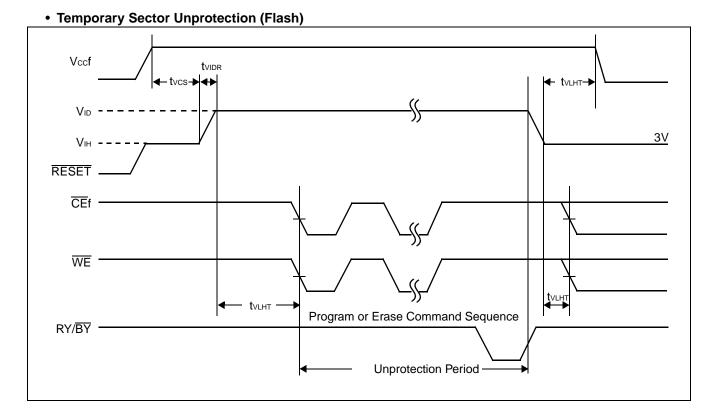
• Bank-to-bank Read/Write Timing Diagram (Flash)

• RY/BY Timing Diagram during Write/Erase Operations (Flash)

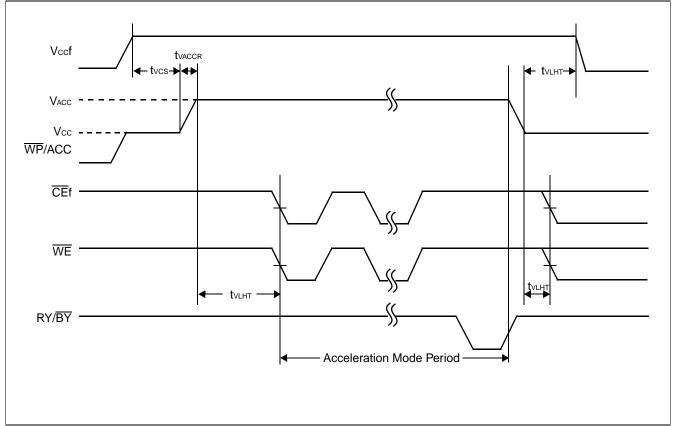


• RESET, RY/BY Timing Diagram (Flash)

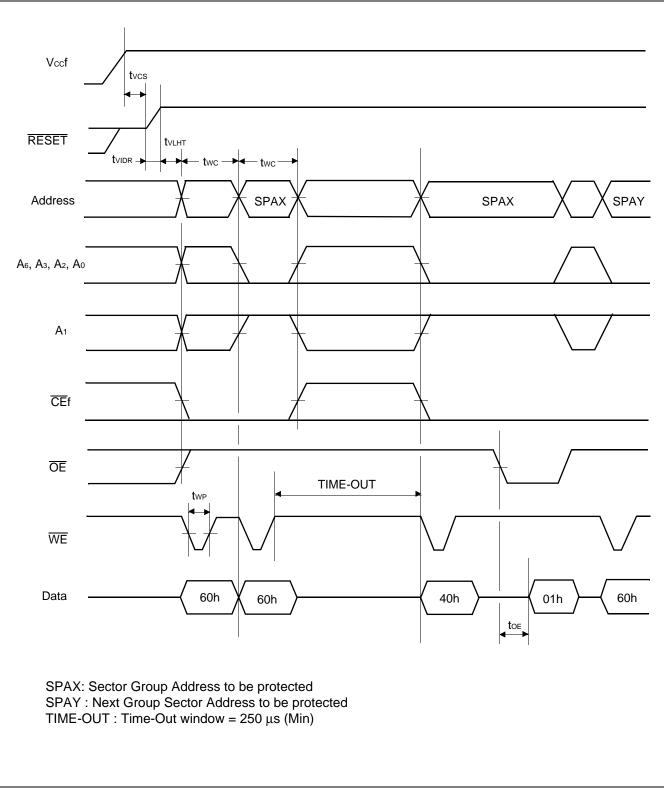




• Acceleration Mode Timing Diagram (Flash)



• Extended Sector Group Protection (Flash)



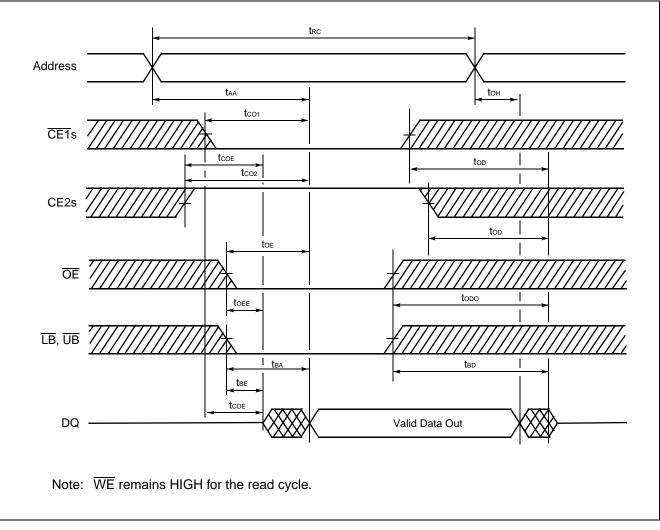
■ 8M SRAM CHARACTERISTICS for MCP

• Read Cycle (SRAM)

Parameter	Symbol	Va	Unit	
Falametei	Symbol	Min	Max	Unit
Read Cycle Time	t RC	70	—	ns
Address Access Time	t AA	—	70	ns
Chip Enable (CE1s) Access Time	tco1	—	70	ns
Chip Enable (CE2s) Access Time	tco2	—	70	ns
Output Enable Access Time	t OE	—	35	ns
LB, UB to Output Valid	tва	—	70	ns
Chip Enable (CE1s Low and CE2s High) to Output Active	t COE	5	—	ns
Output Enable Low to Output Active	toee	0	—	ns
LB, UB Enable Low to Output Active	tве	0	—	ns
Chip Enable (CE1s High or CE2s Low) to Output High-Z	tod	—	25	ns
Output Enable High to Output High-Z	todo	—	25	ns
LB, UB Output Enable to Output High-Z	t BD	—	25	ns
Output Data Hold Time	tон	10	—	ns

Note: Test Conditions-Output Load:1 TTL gate and 30 pF

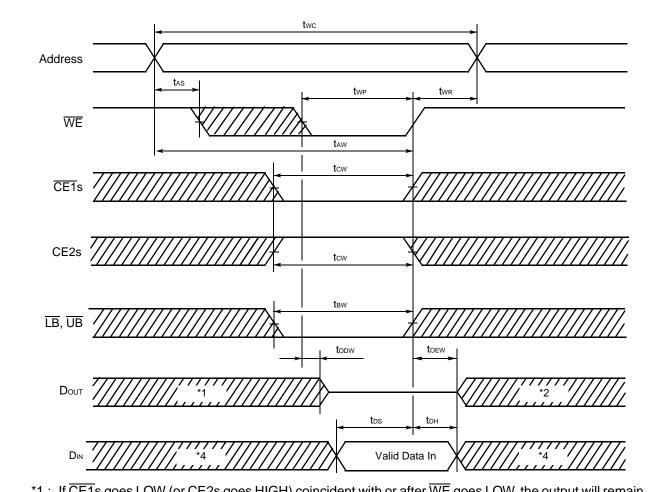
Input rise and fall times: 5 ns Input pulse levels: 0.0 V or 3.0 V Timing measurement reference level Input: $0.5 \times Vccs$ Output: $0.5 \times Vccs$ • Read Cycle (SRAM)



• Write Cycle (SRAM)

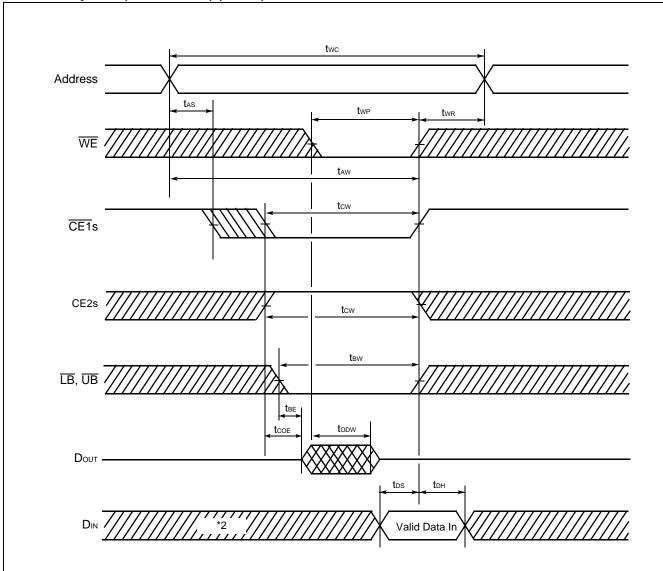
Parameter	Symbol	Va	Unit	
Falametei	Symbol	Min	Max	Unit
Write Cycle Time	twc	70	—	ns
Write Pulse Width	twp	50	—	ns
Chip Enable to End of Write	tcw	55	—	ns
Address valid to End of Write	taw	55	—	ns
LB, UB to End of Write	tвw	55	—	ns
Address Setup Time	tas	0	—	ns
Write Recovery Time	twr	0	—	ns
WE Low to Output High-Z	todw	—	25	ns
WE High to Output Active	toew	0	—	ns
Data Setup Time	tos	30	—	ns
Data Hold Time	tрн	0		ns

• Write Cycle *3 (WE control) (SRAM)



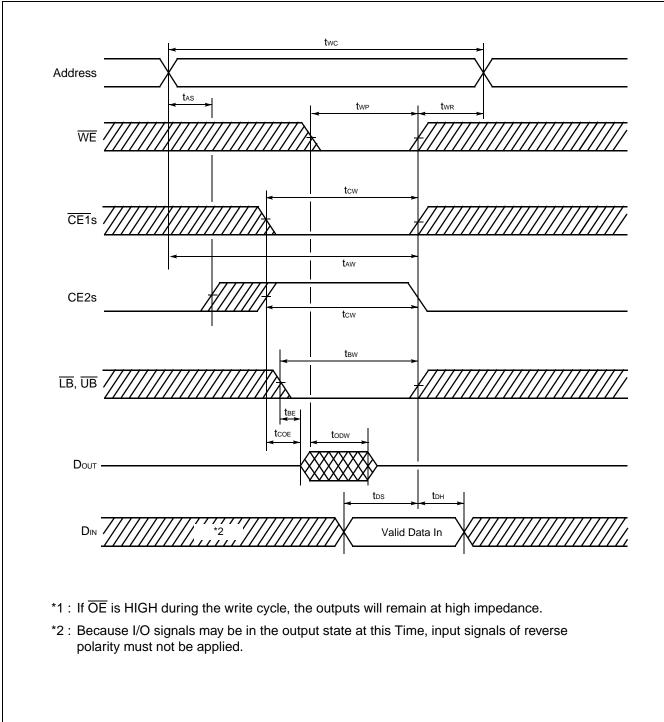
- *1 : If CE1s goes LOW (or CE2s goes HIGH) coincident with or after WE goes LOW, the output will remain at high impedance.
- *2 : If CE1s goes HIGH (or CE2s goes LOW) coincident with or before WE goes HIGH, the output will remain at high impedance.
- *3 : If OE is HIGH during the write cycle, the outputs will remain at high impedance.
- *4 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

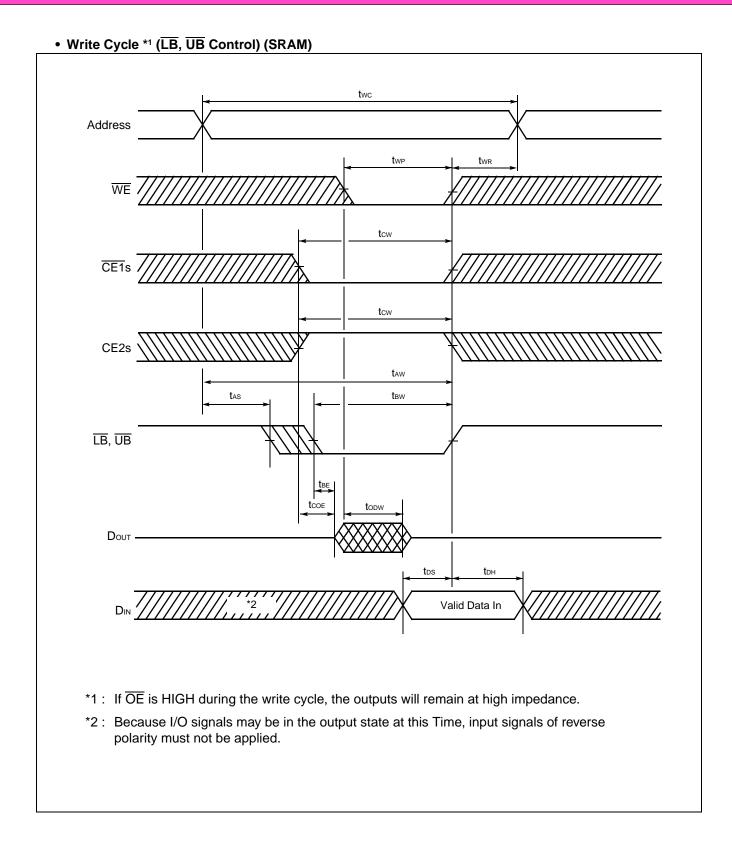
Write Cycle *1 (CE1s control) (SRAM)



- *1 : If $\overline{\text{OE}}$ is HIGH during the write cycle, the outputs will remain at high impedance.
- *2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

• Write Cycle *1 (CE2s Control) (SRAM)





■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

Parameter	Value			Unit	Remarks	
Farameter	Min	Тур	Max	Onit	Rellidiks	
Sector Erase Time	_	0.5	2	S	Excludes programming time prior to erasure	
Word Programming Time		6	100	μs	Excludes system-level overhead	
Byte Programming Time	_	4	80	μs	Excludes system-level overhead	
Chip Programming Time	_	25.2	95	S	Excludes system-level overhead	
Erase/Program Cycle	100,000	_	_	cycle		

Note : Typical Erase conditions $T_A = +25^{\circ}C$, VCCf_1 & VCCf_2 = 2.9 V Typical Program conditions $T_A = +25^{\circ}C$, VCCf_1 & VCCf_2 = 2.9 V D

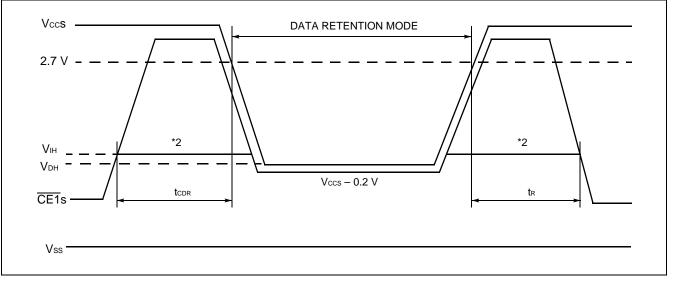
Data= Checker

■ DATA RETENTION CHARACTERISTICS (SRAM)

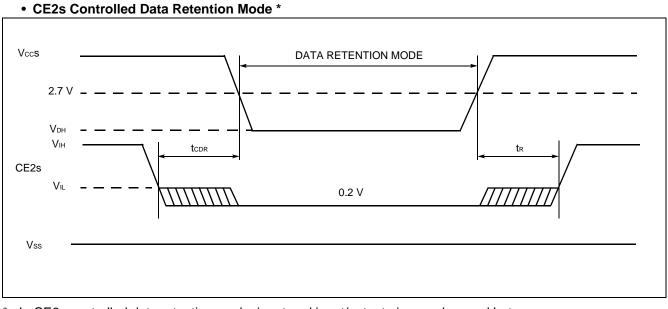
Parameter		Symbol	Value			Unit
		Symbol	Min	Тур	Max	Onit
Data Retention Supply Voltage		Vdh	1.5	_	3.1	V
Standby Current	V _{DH} = 3.0 V	DDS2	—	—	15	μA
Chip Deselect to Data Retention Mode Time		t cdr	0	_	—	ns
Recovery Time		t _R	t RC			ns

Note : tRC: Read cycle time

• CE1s Controlled Data Retention Mode *1



- *1 : In CE1s controlled data retention mode, input level of CE2s should be fixed Vccs to Vccs–0.2 V or Vss to 0.2 V during data retention mode. Other input and input/output pins can be used between –0.3 V to Vccs+0.3 V.
- *2 : When CE1s is operating at the VIH Min level, the standby current is given by IsB1s during the transition of Vccs from Vccs Max to VIH Min level.



 *: In CE2s controlled data retention mode, input and input/output pins can be used between -0.3 V to Vccs+0.3V.

■ PIN CAPACITANCE

Parameter	Symbol	Test Setup	Val	Unit	
	Symbol	Test Setup	Тур	Max	Unit
Input Capacitance	CIN	V _{IN} = 0	11	14	pF
Output Capacitance	Соит	Vout = 0	12	16	pF
Control Pin Capacitance	CIN2	V _{IN} = 0	14	16	pF
WP/ACC Pin Capacitance	Сімз	V _{IN} = 0	21.5	26	pF

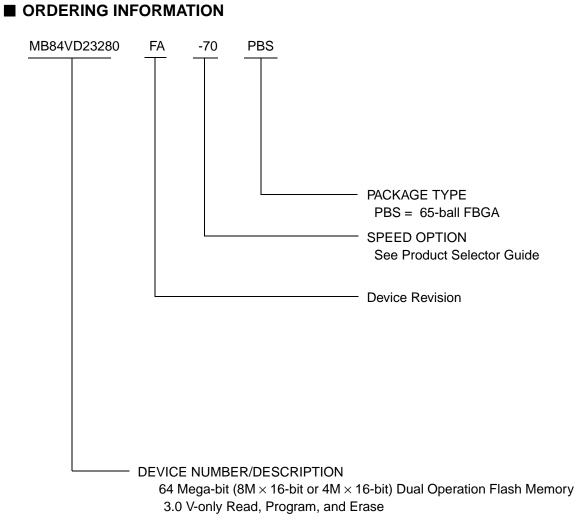
Note: Test conditions Ta = $+25^{\circ}$ C, f = 1.0 MHz

HANDLING OF PACKAGE

Please handle this package carefully since the sides of packages are right angle.

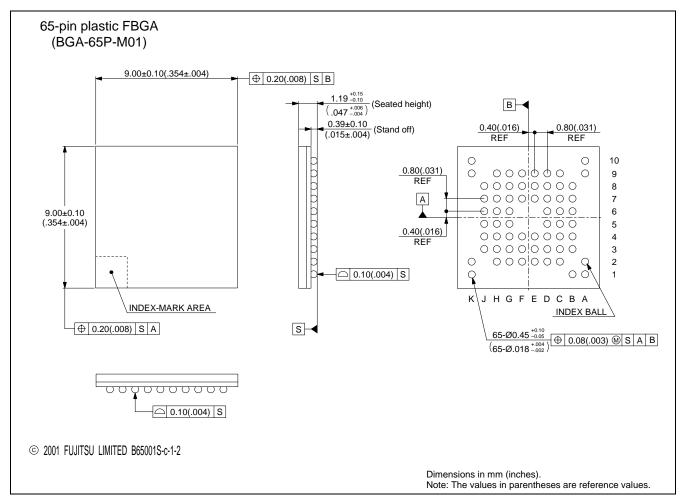
■ CAUTION

- (1) The high voltage (V_{ID}) can not apply to address pins and control pins except RESET. Therefore, it can not use autoselect and sector protect function by applying the high voltage (V_{ID}) to specific pins.
- (2) For the sector protection, since the high voltage (V_{ID}) can be applied to the RESET, it can be protected the sector useing "Extended sector protect" command.



8 Mega-bit(1M \times 8-bit or 512K \times 16-bit) SRAM

■ PACKAGE DIMENSION



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