SPANSION™ MCP

Data Sheet

September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.

AMD

FUJITSU

FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-50221-2E

Stacked MCP (Multi-Chip Package) FLASH MEMORY & SRAM

CMOS

64M (×8/×16) FLASH MEMORY & 8M (×8/×16) STATIC RAM

MB84VD23280FA-70

■ FEATURES

- **Power supply voltage of 2.7 V to 3.1 V**
- **High performance**
  70 ns maximum access time (Flash)
  70 ns maximum access time (SRAM)
- **Operating Temperature**
  –40 °C to +85 °C
- **Package 65-ball FBGA**

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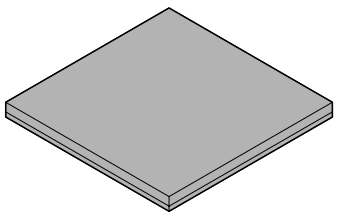
■ PRODUCT LINEUP

	Flash Memory	SRAM
Supply Voltage (V)	V_{CCf}* = 3.0 V $^{+0.1V}_{-0.3\ V}$	V_{CCS}* = 3.0 V $^{+0.1V}_{-0.3\ V}$
Max Address Access Time (ns)	70	70
Max $\overline{CE}$ Access Time (ns)	70	70
Max $\overline{OE}$ Access Time (ns)	30	35

*: Both V_{CCf} and V_{CCS} must be in recommended operation range when either part is being accessed.

■ PACKAGE

65-pin plastic FBGA



(BGA-65P-M01)

FUJITSU

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—FLASH MEMORY

- **0.16 µm Process Technology**
- **Simultaneous Read/Write operations** (**Dual Bank**)
- **FlexBank™*1**
  Bank A : 8 Mbit (8 KB × 8 and 64 KB × 15)
  Bank B : 24 Mbit (64 KB × 48)
  Bank C : 24 Mbit (64 KB × 48)
  Bank D : 8 Mbit (8 KB × 8 and 64 KB × 15)
  Two virtual Banks are chosen from the combination of four physical banks
  Host system can program or erase in one bank, and then read immediately and simultaneously from the other bank with zero latency between read and write operations.
  Read-while-erase
  Read-while-program
- **Single 3.0 V read**, **program**, **and erase**
  Minimized system level power requirements
- **Minimum 100,000 program/erase cycles**
- **Sector erase architecture**
  Sixteen 4 Kword and one hundred twenty-six 32 Kword sectors in word.
  Any combination of sectors can be concurrently erased. It also supports full chip erase.
- **HiddenROM region**
  256 byte of HiddenROM, accessible through a new “HiddenROM Enable” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}$/ACC input pin**
  At V_{IL}, allows protection of “outermost” 2 × 8 Kbytes on both ends of boot sectors, regardless of sector protection/unprotection status
  At V_{IH}, allows removal of boot sector protection
  At V_{ACC}, increases program performance
- **Embedded Erase™*2 Algorithms**
  Automatically preprograms and erases the chip or any sector
- **Embedded Program™*2 Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output** (**RY/$\overline{\text{BY}}$**)
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, the device automatically switches itself to low power mode.
- **Low V_{CC}f write inhibit ≤ 2.5 V**
- **Program Suspend/Resume**
  Suspends the program operation to allow a read in another byte
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Please refer to “MBM29DL64DF” data sheet in detailed function**

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—SRAM

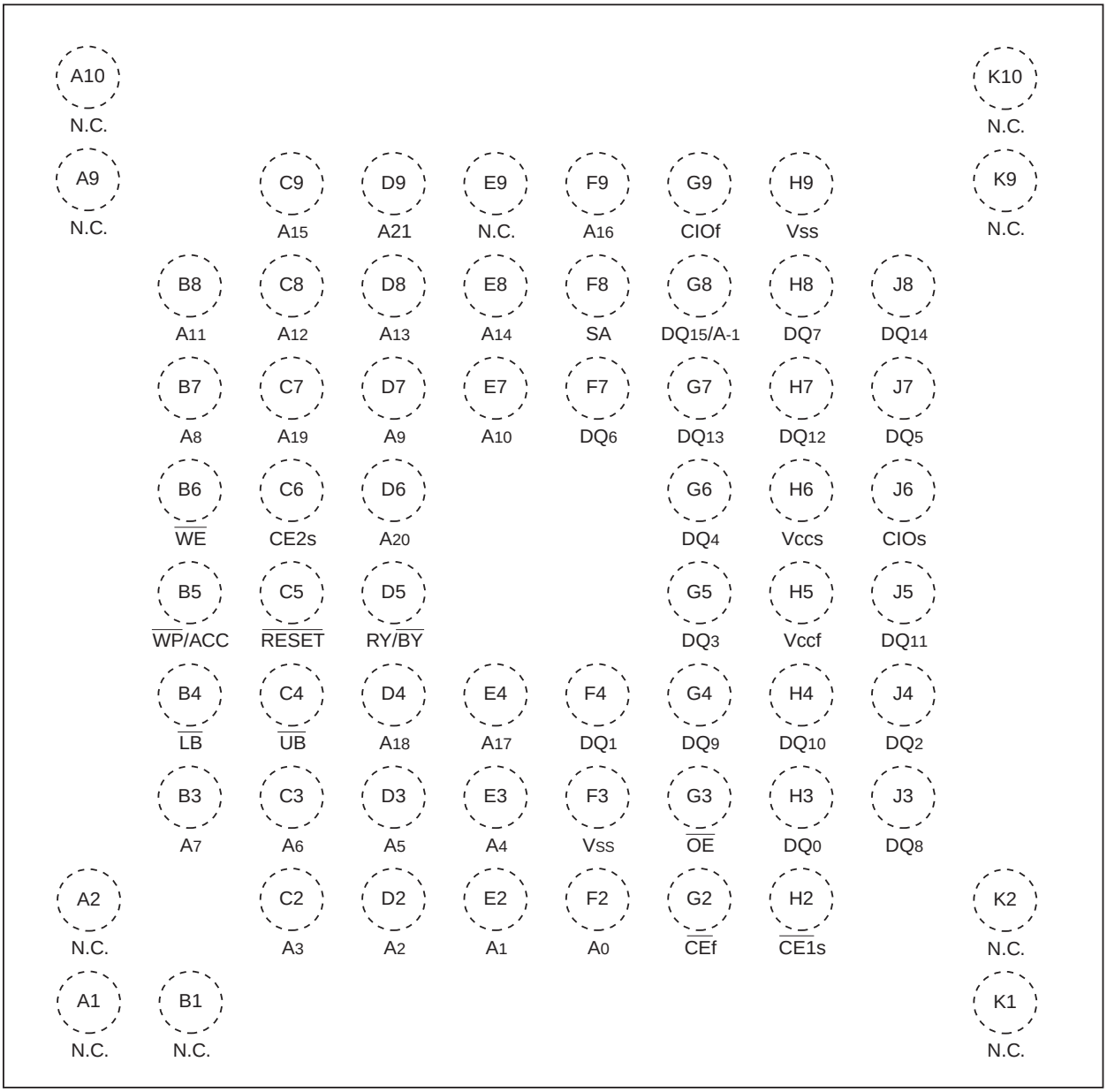
- **Power dissipation**
  Operating: 50 mA Max
  Standby: 15 μA Max
- **Power down features using $\overline{\text{CE1}}$s and CE2s**
- **Data retention supply voltage: 1.5 V to 3.1 V**
- **$\overline{\text{CE1}}$s and CE2s Chip Select**
- **Byte data control: $\overline{\text{LB}}$ (DQ_7 to DQ_0), $\overline{\text{UB}}$ (DQ_{15} to DQ_8)**

*1 : FlexBank™ is a trademark of Fujitsu Limited, Japan.

*2 : Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENT

(Top View)
Marking side

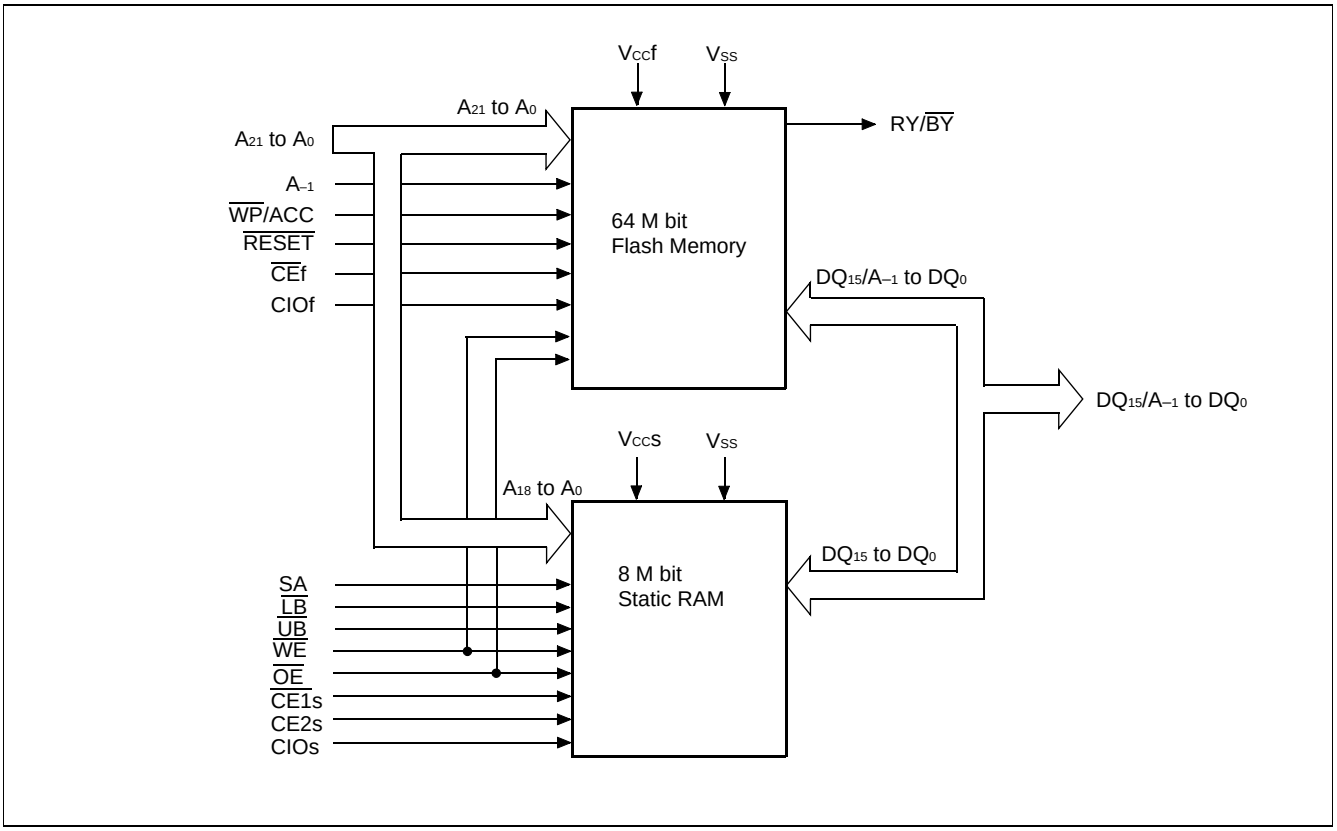


(BGA-65P-M01)

■ PIN DESCRIPTION

Pin name	Input/ Output	Description
A_{18} to A_0	I	Address Inputs (Common)
A_{21} to A_{19}, A_{-1}	I	Address Inputs (Flash)
SA	I	Address Input (SRAM)
DQ_{15} to DQ_0	I/O	Data Inputs/Outputs (Common)
$\overline{CE}$f	I	Chip Enable (Flash)
$\overline{CE1}$s	I	Chip Enable (SRAM)
CE2s	I	Chip Enable (SRAM)
$\overline{OE}$	I	Output Enable (Common)
$\overline{WE}$	I	Write Enable (Common)
RY/$\overline{BY}$	O	Ready/Busy Output (Flash) Open Drain Output
$\overline{UB}$	I	Upper Byte Control (SRAM)
$\overline{LB}$	I	Lower Byte Control (SRAM)
CIOf	I	I/O Configuration (Flash) CIOf = V_{CC}f is Word mode (×16), CIOf = V_{SS} is Byte mode (×8)
CIOs	I	I/O Configuration (SRAM) CIOs = V_{CC}s is Word mode (×16), CIOs = V_{SS} is Byte mode (×8)
$\overline{RESET}$	I	Hardware Reset Pin/Sector Protection Unlock (Flash)
$\overline{WP}$/ACC	I	Write Protect / Acceleration (Flash)
N.C.	—	No Internal Connection
V_{SS}	Power	Device Ground (Common)
V_{CC}f	Power	Device Power Supply (Flash)
V_{CC}s	Power	Device Power Supply (SRAM)

■ BLOCK DIAGRAM



■ DEVICE BUS OPERATIONS

User Bus Operations (Flash = Word mode; CIOf = V_{CC}f, SRAM = Word mode; CIOs = V_{CC}s)

Operation *1,*3	$\overline{CE}$f	$\overline{CE1}$s	CE2s	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	DQ_7 to DQ_0	DQ_{15} to DQ_8	$\overline{RESET}$	$\overline{WP}$/ACC *5
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L									
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
				X	X	X	H	H	High-Z	High-Z		
	L	H	X	H	H	X	X	X	High-Z	High-Z		
		X	L									
Read from Flash *2	L	H	X	L	H	X	X	X	D_{OUT}	D_{OUT}	H	X
		X	L									
Write to Flash	L	H	X	H	L	X	X	X	D_{IN}	D_{IN}	H	X
		X	L									
Read from SRAM	H	L	H	L	H	X	L	L	D_{OUT}	D_{OUT}	H	X
							H	L	High-Z	D_{OUT}		
							L	H	D_{OUT}	High-Z		
Write to SRAM	H	L	H	X	L	X	L	L	D_{IN}	D_{IN}	H	X
							H	L	High-Z	D_{IN}		
							L	H	D_{IN}	High-Z		
Temporary Sector Group Unprotection *4	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L									
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*3 : Do not apply $\overline{CE}$f = V_{IL}, $\overline{CE1}$s = V_{IL} and CE2s = V_{IH} at a time.

*4 : Also used for the extended sector group protections.

*5 : Protects of “outermost” 2 x 4 Kwords on both ends of each boot block sector.

User Bus Operations (Flash = Word mode; ClOf = V_{CC}f, SRAM = Byte mode; ClOs = V_{SS})

Operation *1,*3	$\overline{CE}$f	$\overline{CE1}$s	CE2s	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	DQ_7 to DQ_0	DQ_{15} to DQ_8	$\overline{RESET}$	$\overline{WP}$/ ACC *5
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L									
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
				X	X	X	H	H	High-Z	High-Z		
	L	H	X	H	H	X	X	X	High-Z	High-Z		
		X	L									
Read from Flash*2	L	H	X	L	H	X	X	X	D_{OUT}	D_{OUT}	H	X
		X	L									
Write to Flash	L	H	X	H	L	X	X	X	D_{IN}	D_{IN}	H	X
		X	L									
Read from SRAM	H	L	H	L	H	SA	X	X	D_{OUT}	High-Z	H	X
Write to SRAM	H	L	H	X	L	SA	X	X	D_{IN}	High-Z	H	X
Temporary Sector Group Unprotection*4	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L									
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*3 : Do not apply $\overline{CE}$f = V_{IL}, $\overline{CE1}$s = V_{IL} and CE2s = V_{IH} at a time.

*4 : It is also used for the extended sector group protections.

*5 : Protect of “outermost” 2 x 4 Kwords on both ends of each boot block sector.

User Bus Operations (Flash = Byte mode; CIOf = V_{SS}, SRAM = Byte mode; CIOs = V_{SS})

Operation *1,*3	$\overline{CE}$f	$\overline{CE1}$s	CE2s	DQ_{15}/A_{-1}	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	DQ_7 to DQ_0	DQ_{14} to DQ_8	$\overline{RESET}$	$\overline{WP}$/ACC *5
Full Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L										
Output Disable	H	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
				X	X	X	X	H	H	High-Z	High-Z		
	L	H	X	A_{-1}	H	H	X	X	X	High-Z	High-Z		
		X	L										
Read from Flash*2	L	H	X	A_{-1}	L	H	X	X	X	D_{OUT}	X	H	X
		X	L										
Write to Flash	L	H	X	A_{-1}	H	L	X	X	X	D_{IN}	X	H	X
		X	L										
Read from SRAM	H	L	H	X	L	H	SA	X	X	D_{OUT}	High-Z	H	X
Write to SRAM	H	L	H	X	X	L	SA	X	X	D_{IN}	High-Z	H	X
Temporary Sector Group Unprotection *4	X	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L										
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

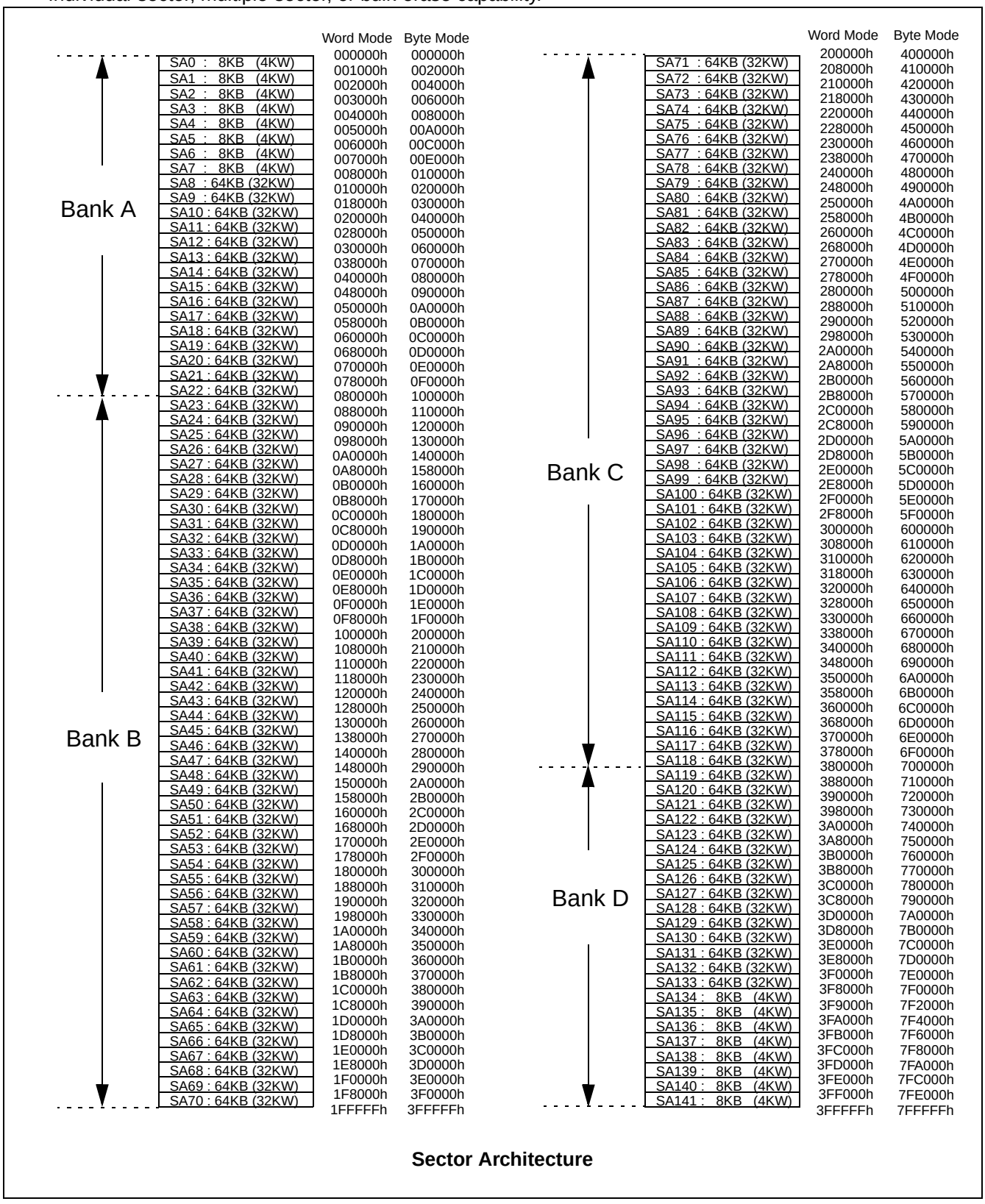
*3 : Do not apply $\overline{CE}$f = V_{IL}, $\overline{CE1}$s = V_{IL} and CE2s = V_{IH} at a time.

*4 : It is also used for the extended sector group protections.

*5 : Protect of “outermost” 2 x 8 Kbytes on both ends of each boot block sector.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- Sixteen 4K words, and one hundred twenty-six 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



Sector Architecture

FlexBank™ Architecture

Bank Splits	Bank 1		Bank 2	
	Volume	Combination	Volume	Combination
1	8 Mbit	Bank A	56 Mbit	Remainder (Bank B, C, D)
2	24 Mbit	Bank B	40 Mbit	Remainder (Bank A, C, D)
3	24 Mbit	Bank C	40 Mbit	Remainder (Bank A, B, D)
4	8 Mbit	Bank D	56 Mbit	Remainder (Bank A, B, C)

Example of Virtual Banks Combination

Bank Splits	Bank 1			Bank 2		
	Volume	Combination	Sector Size	Volume	Combination	Sector Size
1	8 Mbit	Bank A	8 × 8 Kbyte/4 Kword + 15 × 64 Kbyte/32 Kword	56 Mbit	Bank B + Bank C + Bank D	8 × 8 Kbyte/4 Kword + 111 × 64 Kbyte/32 Kword
2	16 Mbit	Bank A + Bank D	16 × 8 Kbyte/4 Kword + 30 × 64 Kbyte/32 Kword	48 Mbit	Bank B + Bank C	96 × 64 Kbyte/32 Kword
3	24 Mbit	Bank B	48 × 64 Kbyte/32 Kword	40 Mbit	Bank A + Bank C + Bank D	16 × 8 Kbyte/4 Kword + 78 × 64 Kbyte/32 Kword
4	32 Mbit	Bank A + Bank B	8 × 8 Kbyte/4 Kword + 63 × 64 Kbyte/32 Kword	32 Mbit	Bank C + Bank D	8 × 8 Kbyte/4 Kword + 63 × 64 Kbyte/32 Kword

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out (they would output the sequence flag once they were selected.) Meanwhile the system would get to read from either Bank C or Bank D.

Simultaneous Operation

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode *
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode *	Read mode

* : By writing erase suspend command on the bank address of sector being erased, the erase operation gets suspended so that it enables reading from or programming the remaining sectors.

Note: Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. Actually, the Bank consists of 4 banks, Bank A, Bank B, Bank C and Bank D. Bank Address (BA) meant to specify each of the Banks.

Sector Address Tables

Bank	Sector	Sector Address										Address Range	
		Bank Address										Byte Mode	Word Mode
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank A	SA0	0	0	0	0	0	0	0	0	0	0	000000h to 001FFFh	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	0	1	002000h to 003FFFh	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	0	1	0	004000h to 005FFFh	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	0	1	1	006000h to 007FFFh	003000h to 003FFFh
	SA4	0	0	0	0	0	0	0	1	0	0	008000h to 009FFFh	004000h to 004FFFh
	SA5	0	0	0	0	0	0	0	1	0	1	00A000h to 00BFFFh	005000h to 005FFFh
	SA6	0	0	0	0	0	0	0	1	1	0	00C000h to 00DFFFh	006000h to 006FFFh
	SA7	0	0	0	0	0	0	0	1	1	1	00E000h to 00FFFFh	007000h to 007FFFh
	SA8	0	0	0	0	0	0	1	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA9	0	0	0	0	0	1	0	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA10	0	0	0	0	0	1	1	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA11	0	0	0	0	1	0	0	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA12	0	0	0	0	1	0	1	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA13	0	0	0	0	1	1	0	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA14	0	0	0	0	1	1	1	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA15	0	0	0	1	0	0	0	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA16	0	0	0	1	0	0	1	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA17	0	0	0	1	0	1	0	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA18	0	0	0	1	0	1	1	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA19	0	0	0	1	1	0	0	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA20	0	0	0	1	1	0	1	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA21	0	0	0	1	1	1	0	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA22	0	0	0	1	1	1	1	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh

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Bank	Sector	Sector Address										Address Range	
		Bank Address										Byte Mode	Word Mode
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank B	SA23	0	0	1	0	0	0	0	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA24	0	0	1	0	0	0	1	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA25	0	0	1	0	0	1	0	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA26	0	0	1	0	0	1	1	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA27	0	0	1	0	1	0	0	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA28	0	0	1	0	1	0	1	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA29	0	0	1	0	1	1	0	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA30	0	0	1	0	1	1	1	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA31	0	0	1	1	0	0	0	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA32	0	0	1	1	0	0	1	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA33	0	0	1	1	0	1	0	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA34	0	0	1	1	0	1	1	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA35	0	0	1	1	1	0	0	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA36	0	0	1	1	1	0	1	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA37	0	0	1	1	1	1	0	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA38	0	0	1	1	1	1	1	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh
	SA39	0	1	0	0	0	0	0	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA40	0	1	0	0	0	0	1	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA41	0	1	0	0	0	1	0	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA42	0	1	0	0	0	1	1	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA43	0	1	0	0	1	0	0	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA44	0	1	0	0	1	0	1	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA45	0	1	0	0	1	1	0	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA46	0	1	0	0	1	1	1	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA47	0	1	0	1	0	0	0	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA48	0	1	0	1	0	0	1	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA49	0	1	0	1	0	1	0	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA50	0	1	0	1	0	1	1	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA51	0	1	0	1	1	0	0	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA52	0	1	0	1	1	0	1	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA53	0	1	0	1	1	1	0	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA54	0	1	0	1	1	1	1	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
	SA55	0	1	1	0	0	0	0	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA56	0	1	1	0	0	0	1	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA57	0	1	1	0	0	1	0	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA58	0	1	1	0	0	1	1	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA59	0	1	1	0	1	0	0	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA60	0	1	1	0	1	0	1	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA61	0	1	1	0	1	1	0	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA62	0	1	1	0	1	1	1	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA63	0	1	1	1	0	0	0	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA64	0	1	1	1	0	0	1	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA65	0	1	1	1	0	1	0	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA66	0	1	1	1	0	1	1	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA67	0	1	1	1	1	0	0	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA68	0	1	1	1	1	0	1	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA69	0	1	1	1	1	1	0	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
	SA70	0	1	1	1	1	1	1	X	X	X	3F0000h to 3FFFFFh	1F8000h to 1FFFFFh

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Bank	Sector	Sector Address										Address Range	
		Bank Address										Byte Mode	Word Mode
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank C	SA71	1	0	0	0	0	0	0	X	X	X	400000h to 40FFFFh	200000h to 207FFFh
	SA72	1	0	0	0	0	0	1	X	X	X	410000h to 41FFFFh	208000h to 20FFFFh
	SA73	1	0	0	0	0	1	0	X	X	X	420000h to 42FFFFh	210000h to 217FFFh
	SA74	1	0	0	0	0	1	1	X	X	X	430000h to 43FFFFh	218000h to 21FFFFh
	SA75	1	0	0	0	1	0	0	X	X	X	440000h to 44FFFFh	220000h to 227FFFh
	SA76	1	0	0	0	1	0	1	X	X	X	450000h to 45FFFFh	228000h to 22FFFFh
	SA77	1	0	0	0	1	1	0	X	X	X	460000h to 46FFFFh	230000h to 237FFFh
	SA78	1	0	0	0	1	1	1	X	X	X	470000h to 47FFFFh	238000h to 23FFFFh
	SA79	1	0	0	1	0	0	0	X	X	X	480000h to 48FFFFh	240000h to 247FFFh
	SA80	1	0	0	1	0	0	1	X	X	X	490000h to 49FFFFh	248000h to 24FFFFh
	SA81	1	0	0	1	0	1	0	X	X	X	4A0000h to 4AFFFFh	250000h to 257FFFh
	SA82	1	0	0	1	0	1	1	X	X	X	4B0000h to 4BFFFFh	258000h to 25FFFFh
	SA83	1	0	0	1	1	0	0	X	X	X	4C0000h to 4CFFFFh	260000h to 267FFFh
	SA84	1	0	0	1	1	0	1	X	X	X	4D0000h to 4DFFFFh	268000h to 26FFFFh
	SA85	1	0	0	1	1	1	0	X	X	X	4E0000h to 4EFFFFh	270000h to 277FFFh
	SA86	1	0	0	1	1	1	1	X	X	X	4F0000h to 4FFFFFh	278000h to 27FFFFh
	SA87	1	0	1	0	0	0	0	X	X	X	500000h to 50FFFFh	280000h to 287FFFh
	SA88	1	0	1	0	0	0	1	X	X	X	510000h to 51FFFFh	288000h to 28FFFFh
	SA89	1	0	1	0	0	1	0	X	X	X	520000h to 52FFFFh	290000h to 297FFFh
	SA90	1	0	1	0	0	1	1	X	X	X	530000h to 53FFFFh	298000h to 29FFFFh
	SA91	1	0	1	0	1	0	0	X	X	X	540000h to 54FFFFh	2A0000h to 2A7FFFh
	SA92	1	0	1	0	1	0	1	X	X	X	550000h to 55FFFFh	2A8000h to 2AFFFFh
	SA93	1	0	1	0	1	1	0	X	X	X	560000h to 56FFFFh	2B0000h to 2B7FFFh
	SA94	1	0	1	0	1	1	1	X	X	X	570000h to 57FFFFh	2B8000h to 2BFFFFh
	SA95	1	0	1	1	0	0	0	X	X	X	580000h to 58FFFFh	2C0000h to 2C7FFFh
	SA96	1	0	1	1	0	0	1	X	X	X	590000h to 59FFFFh	2C8000h to 2CFFFFh
	SA97	1	0	1	1	0	1	0	X	X	X	5A0000h to 5AFFFFh	2D0000h to 2D7FFFh
	SA98	1	0	1	1	0	1	1	X	X	X	5B0000h to 5BFFFFh	2D8000h to 2DFFFFh
	SA99	1	0	1	1	1	0	0	X	X	X	5C0000h to 5CFFFFh	2E0000h to 2E7FFFh
	SA100	1	0	1	1	1	0	1	X	X	X	5D0000h to 5DFFFFh	2E8000h to 2EFFFFh
	SA101	1	0	1	1	1	1	0	X	X	X	5E0000h to 5EFFFFh	2F0000h to 2F7FFFh
	SA102	1	0	1	1	1	1	1	X	X	X	5F0000h to 5FFFFFh	2F8000h to 2FFFFFh
	SA103	1	1	0	0	0	0	0	X	X	X	600000h to 60FFFFh	300000h to 307FFFh
	SA104	1	1	0	0	0	0	1	X	X	X	610000h to 61FFFFh	308000h to 30FFFFh
	SA105	1	1	0	0	0	1	0	X	X	X	620000h to 62FFFFh	310000h to 317FFFh
	SA106	1	1	0	0	0	1	1	X	X	X	630000h to 63FFFFh	318000h to 31FFFFh
	SA107	1	1	0	0	1	0	0	X	X	X	640000h to 64FFFFh	320000h to 327FFFh
	SA108	1	1	0	0	1	0	1	X	X	X	650000h to 65FFFFh	328000h to 32FFFFh
	SA109	1	1	0	0	1	1	0	X	X	X	660000h to 66FFFFh	330000h to 337FFFh
	SA110	1	1	0	0	1	1	1	X	X	X	670000h to 67FFFFh	338000h to 33FFFFh
	SA111	1	1	0	1	0	0	0	X	X	X	680000h to 68FFFFh	340000h to 347FFFh
	SA112	1	1	0	1	0	0	1	X	X	X	690000h to 69FFFFh	348000h to 34FFFFh
	SA113	1	1	0	1	0	1	0	X	X	X	6A0000h to 6AFFFFh	350000h to 357FFFh
	SA114	1	1	0	1	0	1	1	X	X	X	6B0000h to 6BFFFFh	358000h to 35FFFFh
	SA115	1	1	0	1	1	0	0	X	X	X	6C0000h to 6CFFFFh	360000h to 367FFFh
	SA116	1	1	0	1	1	0	1	X	X	X	6D0000h to 6DFFFFh	368000h to 36FFFFh
	SA117	1	1	0	1	1	1	0	X	X	X	6E0000h to 6EFFFFh	370000h to 377FFFh
	SA118	1	1	0	1	1	1	1	X	X	X	6F0000h to 6FFFFFh	378000h to 37FFFFh

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Bank	Sector	Sector Address										Address Range	
		Bank Address										Byte Mode	Word Mode
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank D	SA119	1	1	1	0	0	0	0	X	X	X	700000h to 70FFFFh	380000h to 387FFFh
	SA120	1	1	1	0	0	0	1	X	X	X	710000h to 71FFFFh	388000h to 38FFFFh
	SA121	1	1	1	0	0	1	0	X	X	X	720000h to 72FFFFh	390000h to 397FFFh
	SA122	1	1	1	0	0	1	1	X	X	X	730000h to 73FFFFh	398000h to 39FFFFh
	SA123	1	1	1	0	1	0	0	X	X	X	740000h to 74FFFFh	3A0000h to 3A7FFFh
	SA124	1	1	1	0	1	0	1	X	X	X	750000h to 75FFFFh	3A8000h to 3AFFFFh
	SA125	1	1	1	0	1	1	0	X	X	X	760000h to 76FFFFh	3B0000h to 3B7FFFh
	SA126	1	1	1	0	1	1	1	X	X	X	770000h to 77FFFFh	3B8000h to 3BFFFFh
	SA127	1	1	1	1	0	0	0	X	X	X	780000h to 78FFFFh	3C0000h to 3C7FFFh
	SA128	1	1	1	1	0	0	1	X	X	X	790000h to 79FFFFh	3C8000h to 3CFFFFh
	SA129	1	1	1	1	0	1	0	X	X	X	7A0000h to 7AFFFFh	3D0000h to 3D7FFFh
	SA130	1	1	1	1	0	1	1	X	X	X	7B0000h to 7BFFFFh	3D8000h to 3DFFFFh
	SA131	1	1	1	1	1	0	0	X	X	X	7C0000h to 7CFFFFh	3E0000h to 3E7FFFh
	SA132	1	1	1	1	1	0	1	X	X	X	7D0000h to 7DFFFFh	3E8000h to 3EFFFFh
	SA133	1	1	1	1	1	1	0	X	X	X	7E0000h to 7EFFFFh	3F0000h to 3F7FFFh
	SA134	1	1	1	1	1	1	1	0	0	0	7F0000h to 7F1FFFh	3F8000h to 3F8FFFh
	SA135	1	1	1	1	1	1	1	0	0	1	7F2000h to 7F3FFFh	3F9000h to 3F9FFFh
	SA136	1	1	1	1	1	1	1	0	1	0	7F4000h to 7F5FFFh	3FA000h to 3FAFFFh
	SA137	1	1	1	1	1	1	1	0	1	1	7F6000h to 7F7FFFh	3FB000h to 3FBFFFh
	SA138	1	1	1	1	1	1	1	1	0	0	7F8000h to 7F9FFFh	3FC000h to 3FCFFFh
	SA139	1	1	1	1	1	1	1	1	0	1	7FA000h to 7FBFFFh	3FD000h to 3FDFFFh
	SA140	1	1	1	1	1	1	1	1	1	0	7FC000h to 7FDFFFh	3FE000h to 3FEFFFh
	SA141	1	1	1	1	1	1	1	1	1	1	7FE000h to 7FFFFFh	3FF000h to 3FFFFFh

Sector Group Addresses

Sector Group	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	0	1	X	X	X	SA8 to SA10
						1	0				
						0	1				
SGA9	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA24	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA25	1	0	0	0	1	X	X	X	X	X	SA75 to SA78
SGA26	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA27	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA28	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA29	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA30	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA31	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA32	1	1	0	0	0	X	X	X	X	X	SA103 to SA106
SGA33	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA34	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA35	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA36	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA37	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA38	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA39	1	1	1	1	1	0	0	X	X	X	SA131 to SA133
						0	1				
						1	0				
SGA40	1	1	1	1	1	1	1	0	0	0	SA134
SGA41	1	1	1	1	1	1	1	0	0	1	SA135
SGA42	1	1	1	1	1	1	1	0	1	0	SA136
SGA43	1	1	1	1	1	1	1	0	1	1	SA137
SGA44	1	1	1	1	1	1	1	1	0	0	SA138
SGA45	1	1	1	1	1	1	1	1	0	1	SA139
SGA46	1	1	1	1	1	1	1	1	1	0	SA140
SGA47	1	1	1	1	1	1	1	1	1	1	SA141

Flash Memory Autoselect Codes

Type	A_{21} to A_{12}	A_6	A_3	A_2	A_1	A_0	Code (HEX)
Manufacture's Code	BA	L	L	L	L	L	04h
Device Code	BA	L	L	L	L	H	227Eh
Extended Device Code *2	BA	L	H	H	H	L	2202h
	BA	L	H	H	H	H	2201h
Sector Group Protection	Sector Group Addresses	L	L	L	H	L	01h*1

Legend: L = V_{IL}, H = V_{IH}. See DC Characteristics for voltage levels.

*1 : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*2 : A read cycle at address (BA) 01h outputs device code. When 227Eh was output, this indicates that there will require two additional codes, called Extended Device Codes. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh.

Flash Memory Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	Word	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
	Byte													
Read/Reset	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Autoselect	Word	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
	Byte		AAAh		555h		(BA) AAAh							
Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Program Suspend		1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Program Resume		1	BA	30h	—	—	—	—	—	—	—	—	—	—
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Erase Suspend		1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume		1	BA	30h	—	—	—	—	—	—	—	—	—	—
Extended Sector Group Protection *2	Word	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD	—	—	—	—
	Byte													
Set to Fast Mode	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Fast Program *1	Word	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
	Byte		XXXh											
Reset from Fast Mode *1	Word	2	BA	90h	XXXh	*4 F0h	—	—	—	—	—	—	—	—
	Byte		BA		XXXh									
Query	Word	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—
	Byte		(BA) AAh											
HiddenROM Entry	Word	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
HiddenROM Program *3	Word	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
HiddenROM Exit *3	Word	4	555h	AAh	2AAh	55h	(HRBA) 555h	90h	XXXh	00h	—	—	—	—
	Byte		AAAh		555h		(HRBA) AAAh							

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*1: This command is valid while Fast Mode.

*2: This command is valid while $\overline{\text{RESET}}$ = V_{ID}.

*3: This command is valid while HiddenROM mode.

*4: The data “00h” is also acceptable.

Notes :
- Address bits A_{21} to A_{11} = X = “H” or “L” for all address commands except or Program Address (PA), Sector Address (SA), and Bank Address (BA), and Sector Group Address (SPA).
- Bus operations are defined.
- RA = Address of the memory location to be read
  PA = Address of the memory location to be programmed

Addresses are latched on the falling edge of the write pulse.

SA = Address of the sector to be erased. The combination of A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.

BA = Bank Address (A_{21}, A_{20}, A_{19})

- RD = Data read from location RA during read operation.
  PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
- SPA = Sector group address to be protected. Set sector group address and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0).

SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.

- HRA = Address of the HiddenROM area Word Mode : 000000h to 00007Fh
  Byte Mode : 000000h to 0000FFh
- HRBA = Bank Address of the HiddenROM area (A_{21} = A_{20} = A_{19} = V_{IL})
- The system should generate the following address patterns:
  Word Mode: 555h or 2AAh to addresses A_{10} to A_0
  Byte Mode: AAAh or 555h to addresses A_{10} to A_0, and A_{-1}
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	Ta	–40	+85	°C
Voltage with Respect to Ground All pins except $\overline{RESET}$,$\overline{WP}$/ACC *1	V_{IN}, V_{OUT}	–0.3	$V_{CC}f$ +0.3	V
			$V_{CC}s$ +0.3	V
$V_{CC}f$/$V_{CC}s$ Supply *1	$V_{CC}f$, $V_{CC}s$	–0.3	+3.3	V
$\overline{RESET}$ *2	V_{IN}	–0.5	+ 13.0	V
$\overline{WP}$/ACC *3	V_{IN}	–0.5	+10.5	V

*1 Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is $V_{CC}f$ + 0.3 V or $V_{CC}s$ + 0.3 V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}f$ + 2.0 V or $V_{CC}s$ + 2.0 V for periods of up to 20 ns.

*2: Minimum DC input voltage on $\overline{RESET}$ pin is –0.5 V. During voltage transitions, $\overline{RESET}$ pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}-$V_{CC}f$ or $V_{CC}s$) does not exceed +9.0 V. Maximum DC input voltage on $\overline{RESET}$ pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

*3: Minimum DC input voltage on $\overline{WP}$/ACC pin is –0.5 V. During voltage transitions, $\overline{WP}$/ACC pin may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{WP}$/ACC pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when $V_{CC}f$ is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Ambient Temperature	Ta	–40	+85	°C
$V_{CC}f$/$V_{CC}s$ Supply Voltages	$V_{CC}f$, $V_{CC}s$	+2.7	+3.1	V

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Conditions			Value			Unit
					Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CCf}, V_{CCS}			–1.0	—	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CCf}, V_{CCS}			–1.0	—	+1.0	µA
$\overline{RESET}$ Inputs Leakage Current	I_{LIT}	V_{CCf} = V_{CCf} Max, V_{CCS} = V_{CCS} Max, $\overline{RESET}$ = 12.5 V			—	—	35	µA
A_{CC} Input Leakage Current	I_{LIA}	V_{CCf} = V_{CCf} Max, V_{CCS} = V_{CCS} Max, $\overline{WP}$/ACC = V_{ACC} Max			—	—	20	mA
Flash V_{CC} Active Current (Read) *1	I_{CC1f}	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}	t_{CYCLE} = 5 MHz	Byte	—	—	16	mA
			t_{CYCLE} = 5 MHz	Word	—	—	18	
			t_{CYCLE} = 1 MHz	Byte	—	—	4	mA
			t_{CYCLE} = 1 MHz	Word	—	—	4	
Flash V_{CC} Active Current*2	I_{CC2f}	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}			—	—	30	mA
Flash V_{CC} Active Current (Read-While-Program) *5	I_{CC3f}	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		Byte	—	—	46	mA
				Word	—	—	48	
Flash V_{CC} Active Current (Read-While-Erase) *5	I_{CC4f}	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		Byte	—	—	46	mA
				Word	—	—	48	
Flash V_{CC} Active Current (Erase-Suspend-Program)	I_{CC5f}	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}			—	—	30	mA
SRAM V_{CC} Active Current	I_{CC1S}	V_{CCS} = V_{CCS} Max, $\overline{CE1}s$ = V_{IL}, CE2s = V_{IH}	t_{CYCLE} = 10 MHz		—	—	50	mA
SRAM V_{CC} Active Current	I_{CC2S}	$\overline{CE1}s$ = 0.2 V, CE2s = V_{CCS} – 0.2 V	t_{CYCLE} = 10 MHz		—	—	50	mA
			t_{CYCLE} = 1 MHz		—	—	10	mA
Flash V_{CC} Standby Current	I_{SB1f}	V_{CCf} = V_{CCf} Max, $\overline{CE}f$ = V_{CCf} ± 0.3 V, $\overline{RESET}$ = V_{CCf} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V			—	1	5	µA
Flash V_{CC} Standby Current ($\overline{RESET}$)	I_{SB2f}	V_{CCf} = V_{CCf} Max, $\overline{RESET}$ = V_{SS} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V			—	1	5	µA
Flash V_{CC} Current (Automatic Sleep Mode) *3	I_{SB3f}	V_{CCf} = V_{CCf} Max, $\overline{CE}f$ = V_{SS} ± 0.3 V, $\overline{RESET}$ = V_{CCf} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V, V_{IN} = V_{CCf}± 0.3 V or V_{SS} ± 0.3 V			—	1	5	µA
SRAM V_{CC} Standby Current	I_{SB1S}	$\overline{CE1}s \geq V_{CCS}$ – 0.2 V, CE2s ≥ V_{CCS} – 0.2 V			—	—	15	µA
SRAM V_{CC} Standby Current	I_{SB2S}	CE2s ≤ 0.2V			—	—	15	µA

(Continued)

(Continued)

Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Input Low Level	V_{IL}	—		–0.3	—	0.5	V
Input High Level	V_{IH}	—		2.4	—	V_{CC}+0.3 *6	V
Voltage for Sector Protection, and Temporary Sector Unprotection ($\overline{RESET}$) *4	V_{ID}	—		11.5	12	12.5	V
Voltage for Program Acceleration ($\overline{WP}$/ACC) *4	V_{ACC}	—		8.5	9.0	9.5	V
Output Low Voltage Level	V_{OL}	$V_{CC}f = V_{CC}f$ Min, I_{OL}= 4.0 mA	Flash	—	—	0.45	V
		$V_{CC}s = V_{CC}s$ Min, I_{OL}= 1.0 mA	SRAM	—	—	0.4	V
Output High Voltage Level	V_{OH}	$V_{CC}f = V_{CC}f$ Min, I_{OH}= –0.1 mA	Flash	0.85× $V_{CC}f$	—	—	V
		$V_{CC}s = V_{CC}s$ Min, I_{OH}= –0.5 mA	SRAM	2.2	—	—	V
Flash Low $V_{CC}f$ Lock-Out Voltage	V_{LKO}	—		2.3	2.4	2.5	V

*1: The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2: I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3: Automatic sleep mode enables the low power mode when address remains stable for 150 ns.

*4: Applicable for only $V_{CC}f$ applying.

*5: Embedded Alogorithm (program or erase) is in progress. (@5 MHz)

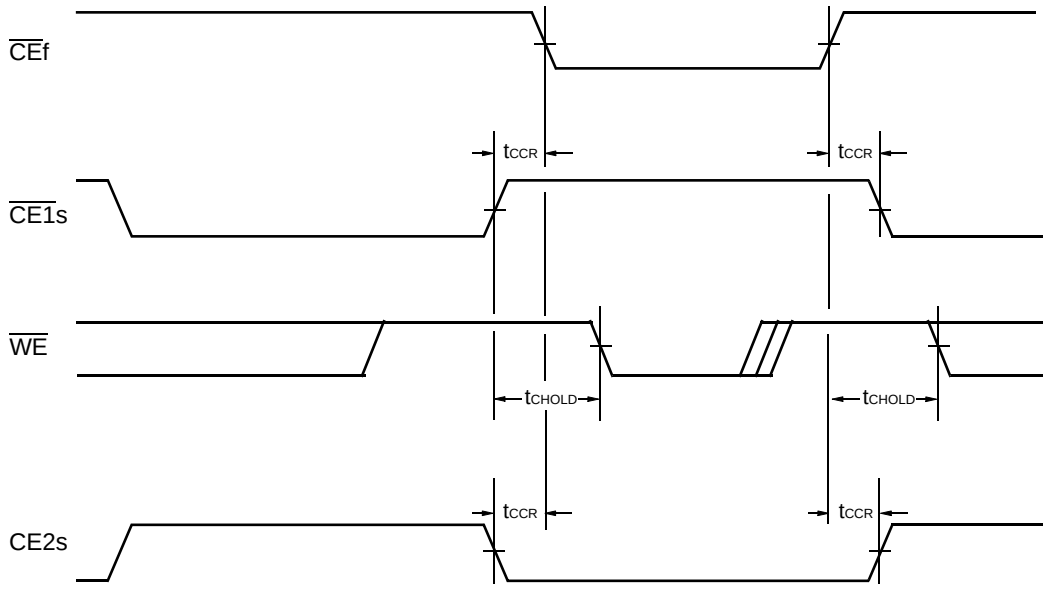
*6: V_{CC} indicates lower of $V_{CC}f$ or $V_{CC}s$.

2. AC Characteristics

- **$\overline{CE}$ Timing**

Parameter	Symbol		Condition	Value		Unit
	JEDEC	Standard		Min	Max	
$\overline{CE}$ Recover Time	—	t_{CCR}	—	0	—	ns
$\overline{CE}$ Hold Time	—	t_{CHOLD}	—	3	—	ns

- **Timing Diagram for alternating SRAM to Flash**

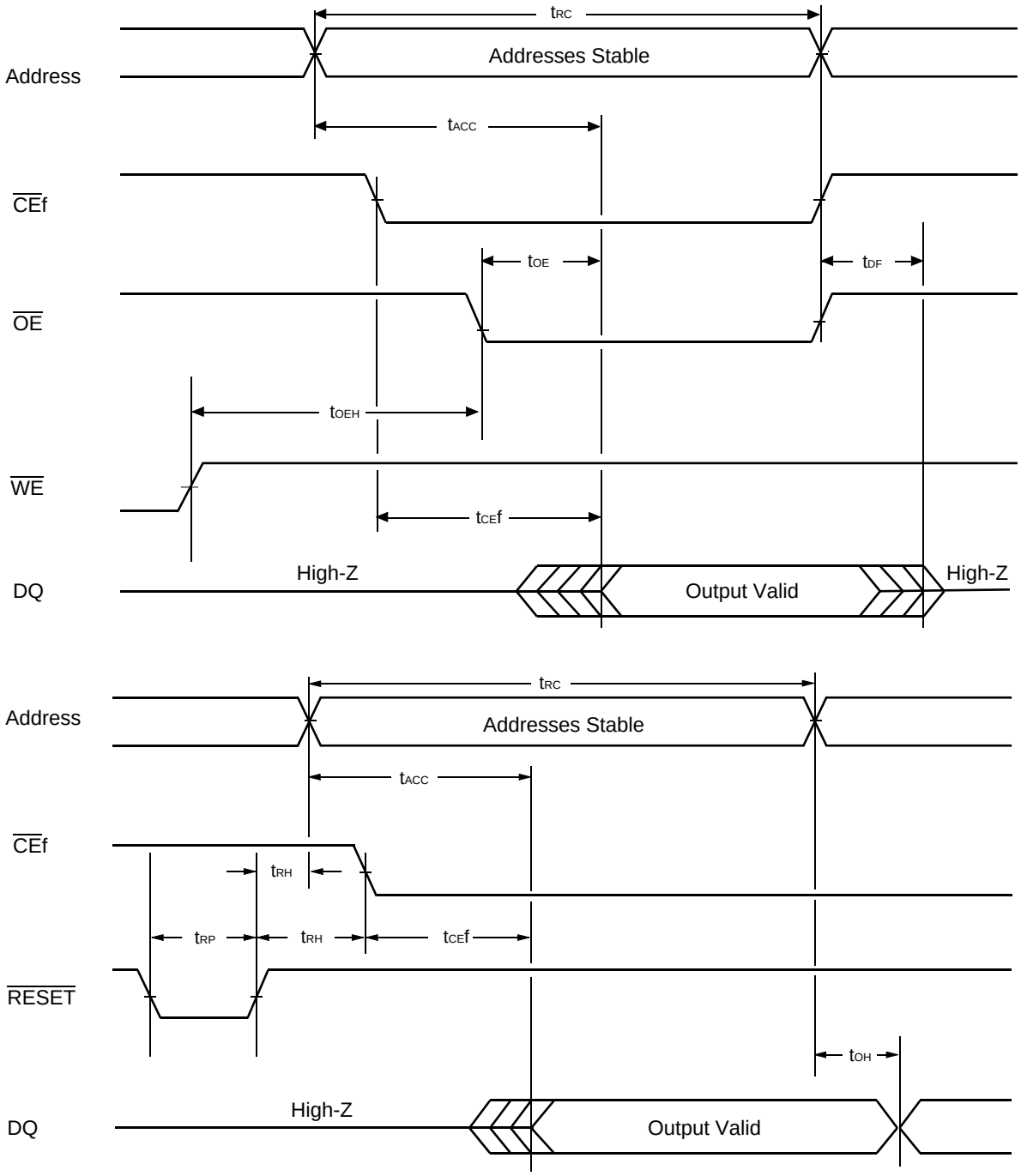


- **Read Only Operations Characteristics (Flash)**

Parameter	Symbol		Condition	Value*		Unit
	JEDEC	Standard		Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	70	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	70	ns
Chip Enable to Output Delay	t_{ELQV}	$t_{CE}f$	$\overline{OE} = V_{IL}$	—	70	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	30	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	25	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	25	ns
Output Hold Time From Addresses, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t_{READY}	—	—	20	µs

*: Test Conditions– Output Load:1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to $V_{CC}f$
Timing measurement reference level
Input: $0.5 \times V_{CC}f$
Output: $0.5 \times V_{CC}f$

- **Read Cycle (Flash)**



• **Write/Erase/Program Operations**

Parameter		Symbol		Value			Unit
		JEDEC	Standard	Min	Typ	Max	
Write Cycle Time		t_{AVAV}	t_{WC}	70	—	—	ns
Address Setup Time		t_{AVWL}	t_{AS}	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling		—	t_{ASO}	12	—	—	ns
Address Hold Time		t_{WLAX}	t_{AH}	45	—	—	ns
Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling		—	t_{AHT}	0	—	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	30	—	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	—	ns
Output Enable Hold Time	Read	—	t_{OEH}	0	—	—	ns
	Toggle and $\overline{Data}$ Polling			10	—	—	ns
$\overline{CE}$ High During Toggle Bit Polling		—	t_{CEPH}	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling		—	t_{OEPH}	20	—	—	ns
Read Recover Time Before Write		t_{GHWL}	t_{GHWL}	0	—	—	ns
Read Recover Time Before Write		t_{GHEL}	t_{GHEL}	0	—	—	ns
$\overline{CE}$ Setup Time		t_{ELWL}	t_{CS}	0	—	—	ns
$\overline{WE}$ Setup Time		t_{WLEL}	t_{WS}	0	—	—	ns
$\overline{CE}$ Hold Time		t_{WHEH}	t_{CH}	0	—	—	ns
$\overline{WE}$ Hold Time		t_{EHWH}	t_{WH}	0	—	—	ns
Write Pulse Width		t_{WLWH}	t_{WP}	35	—	—	ns
$\overline{CE}$ Pulse Width		t_{ELEH}	t_{CP}	35	—	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	25	—	—	ns
$\overline{CE}$ Pulse Width High		t_{EHEL}	t_{CPH}	25	—	—	ns
Programming Operation	Byte	t_{WHWH1}	t_{WHWH1}	—	4	—	µs
	Word			—	6	—	µs
Sector Erase Operation *1		t_{WHWH2}	t_{WHWH2}	—	0.5	—	s
V_{CC} Setup Time		—	t_{VCS}	50	—	—	µs
Rise Time to V_{ID} *2		—	t_{VIDR}	500	—	—	ns
Rise Time to V_{ACC} *3		—	t_{VACCR}	500	—	—	ns
Voltage Transition Time *2		—	t_{VLHT}	4	—	—	µs
Write Pulse Width *2		—	t_{WPP}	100	—	—	µs

(Continued)

(Continued)

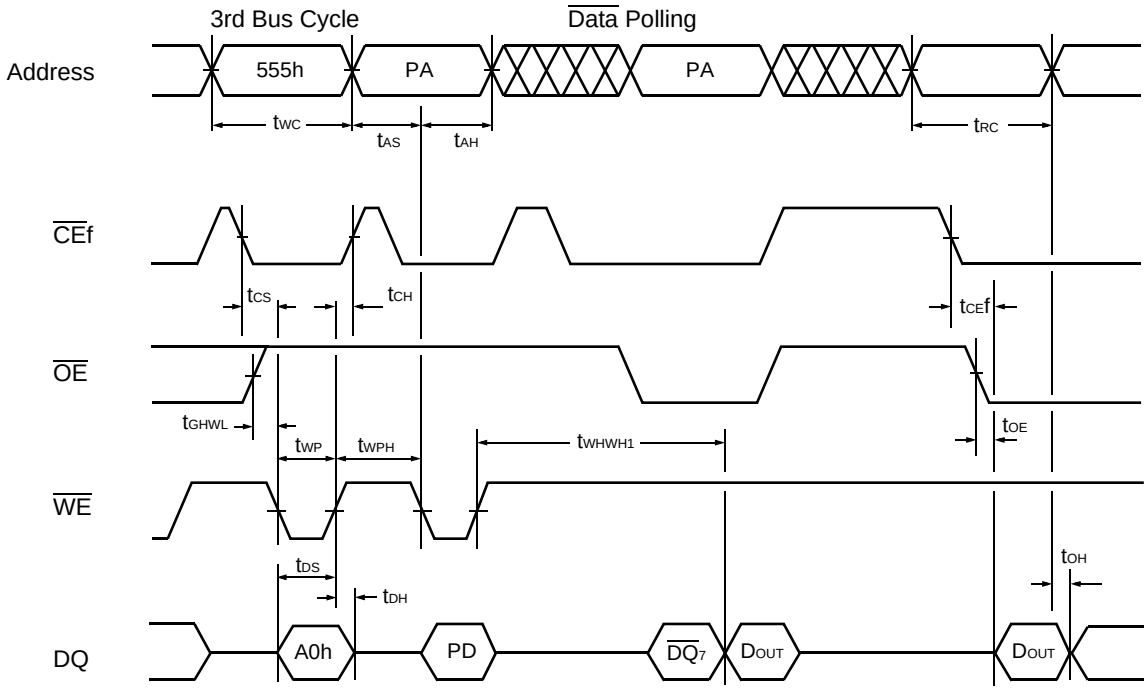
Parameter	Symbol		Value			Unit
	JEDEC	Standard	Min	Typ	Max	
$\overline{OE}$ Setup Time to $\overline{WE}$ Active *2	—	t_{OESP}	4	—	—	µs
$\overline{CE}$ Setup Time to $\overline{WE}$ Active *2	—	t_{CSP}	4	—	—	µs
Recover Time from RY/$\overline{BY}$	—	t_{RB}	0	—	—	ns
$\overline{RESET}$ Pulse Width	—	t_{RP}	500	—	—	ns
$\overline{RESET}$ High Level Period Before Read	—	t_{RH}	200	—	—	ns
$\overline{BYTE}$ Switching Low to Output High-Z	—	t_{FLQZ}	—	—	30	ns
$\overline{BYTE}$ Switching High to Output Active	—	t_{FHQV}	—	—	70	ns
Program/Erase Valid to RY/$\overline{BY}$ Delay	—	t_{BUSY}	—	—	90	ns
Delay Time from Embedded Output Enable	—	t_{EOE}	—	—	70	ns
Erase Time-out Time	—	t_{TOW}	50		—	µs
Erase Suspend Transition Time	—	t_{SPD}	—	—	20	µs

*1: This does not include preprogramming time.

*2: This timing is for Sector Group Protection operation.

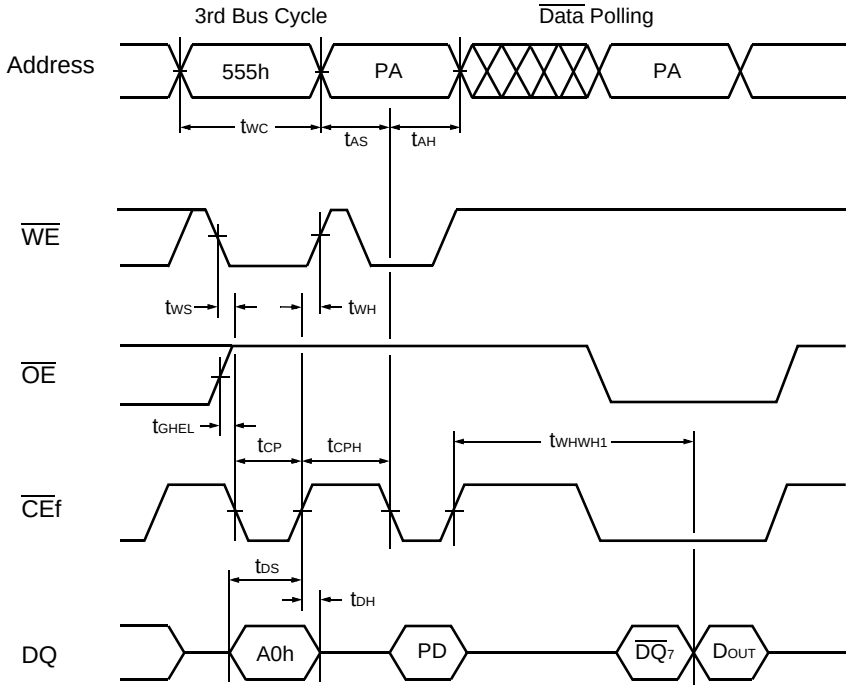
*3: This timing is for Accelerated Program operation.

• **Write Cycle ($\overline{WE}$ control) (Flash)**



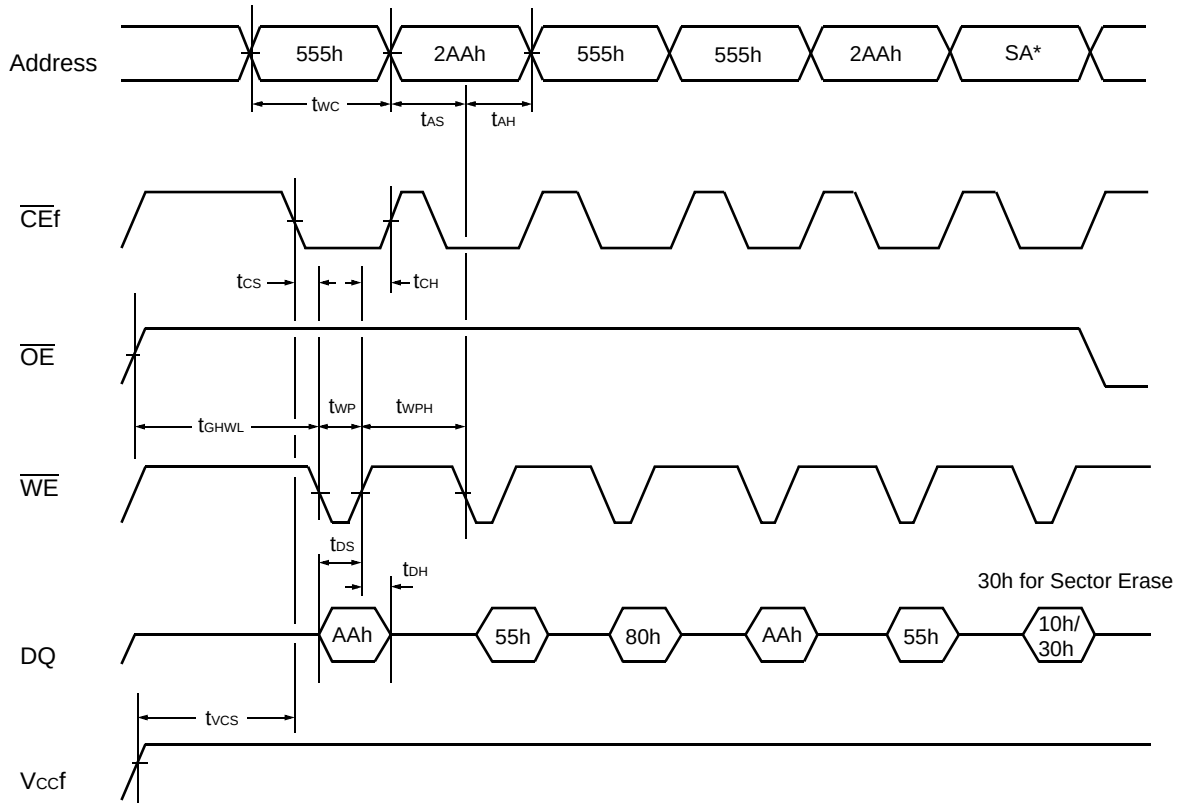
Notes :
- PA is address of the memory location to be programmed.
- PD is data to be programmed at byte address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

- **Write Cycle ($\overline{CE}$f control) (Flash)**



Notes :
- PA is address of the memory location to be programmed.
- PD is data to be programmed at byte address.
- $\overline{DQ}_7$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

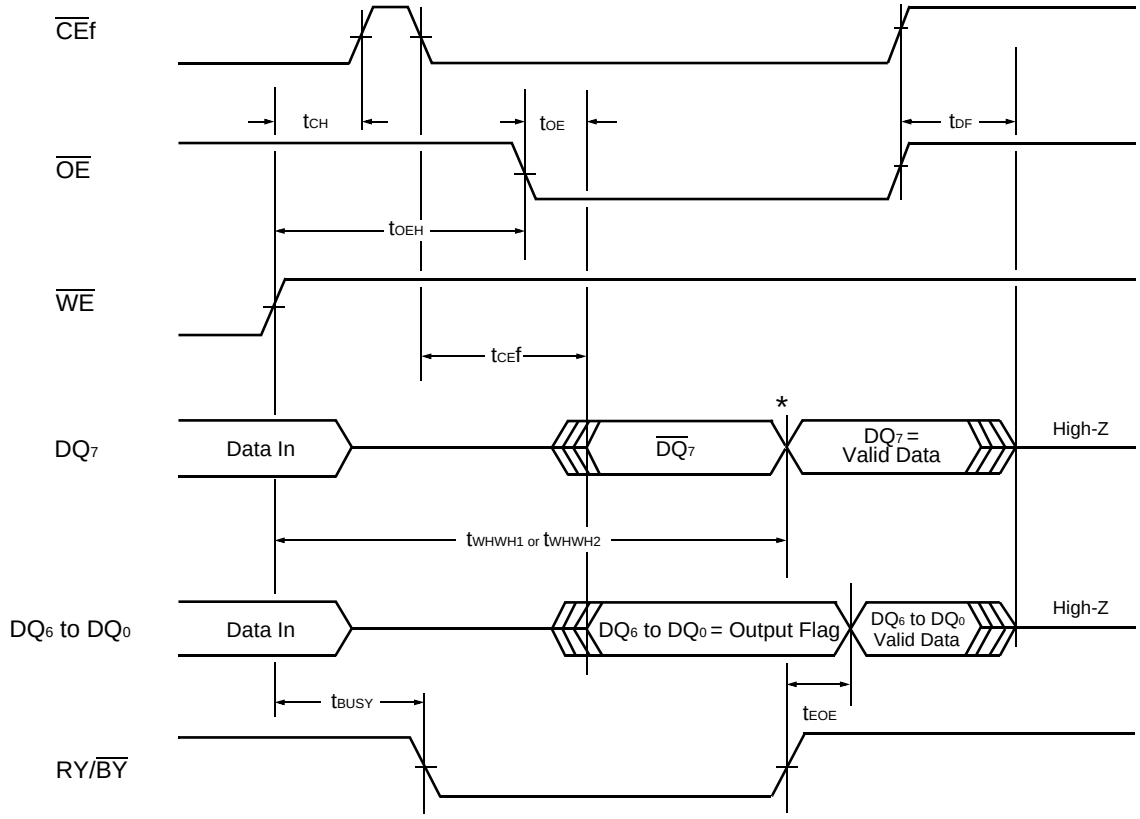
- **AC Waveforms Chip/Sector Erase Operations (Flash)**



*: SA is the sector address for Sector Erase. Addresses = 555h for Chip Erase.

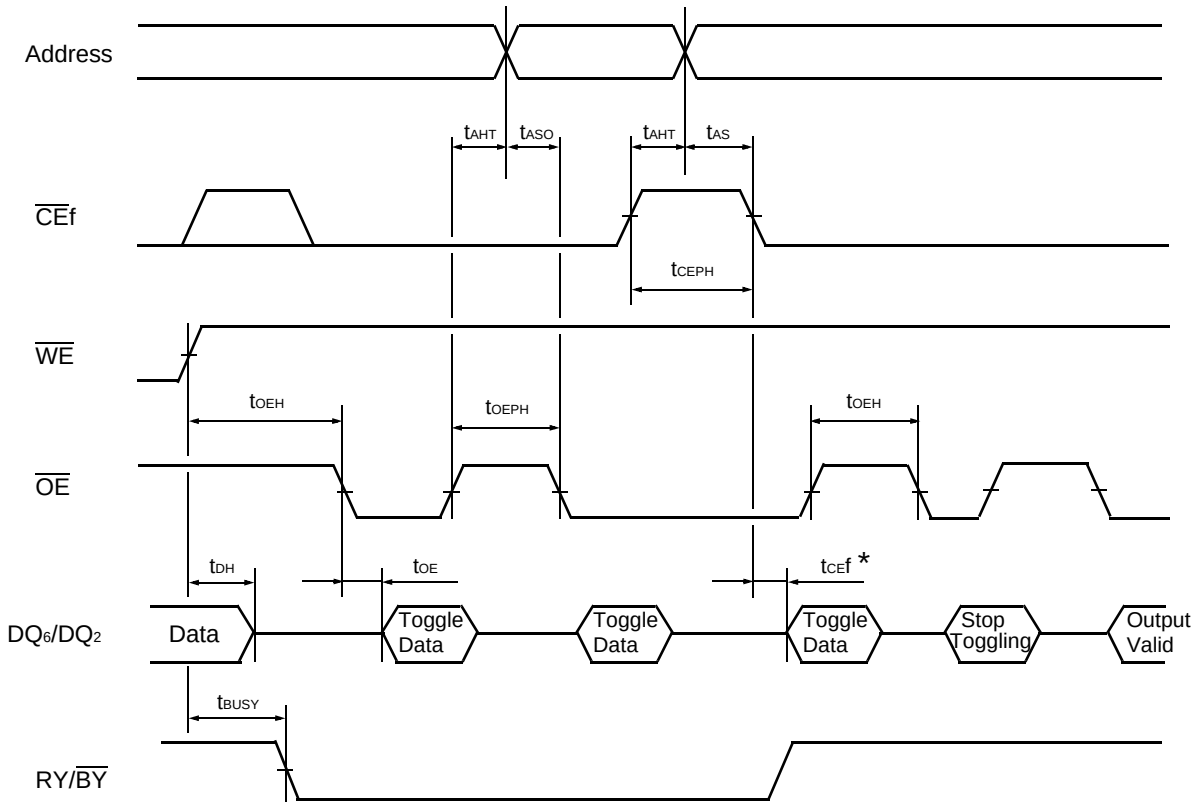
Note: These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

- **AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations (Flash)**



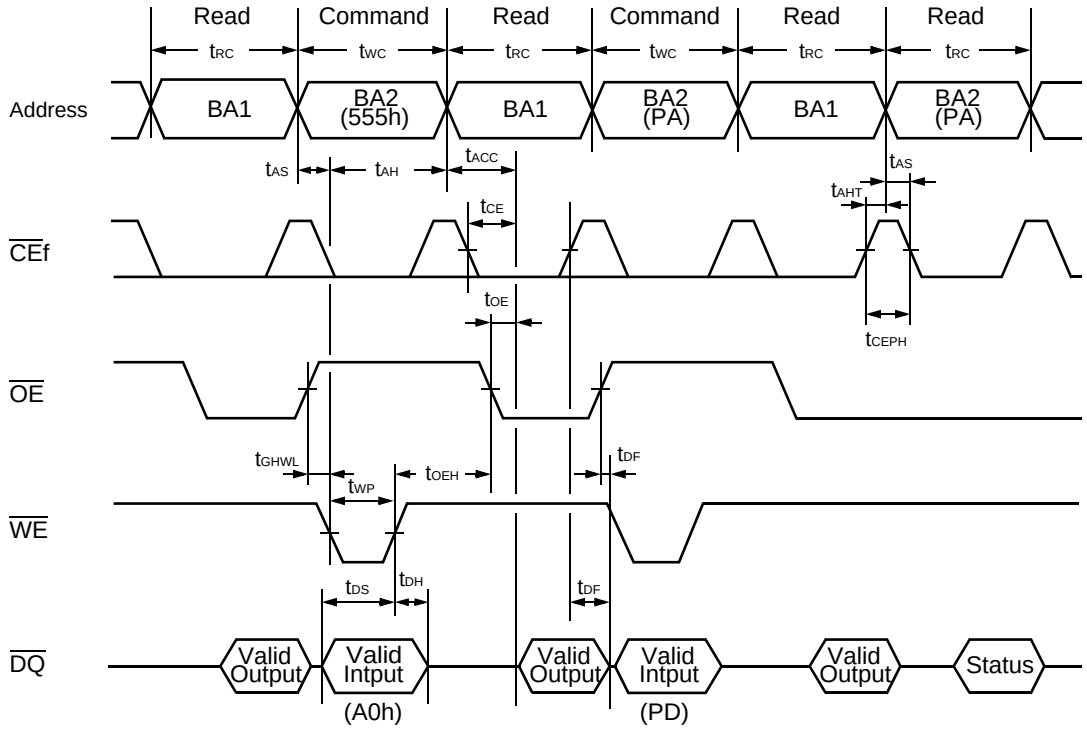
*: DQ_7 = Valid Data (The device has completed the Embedded operation.)

- **AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)**



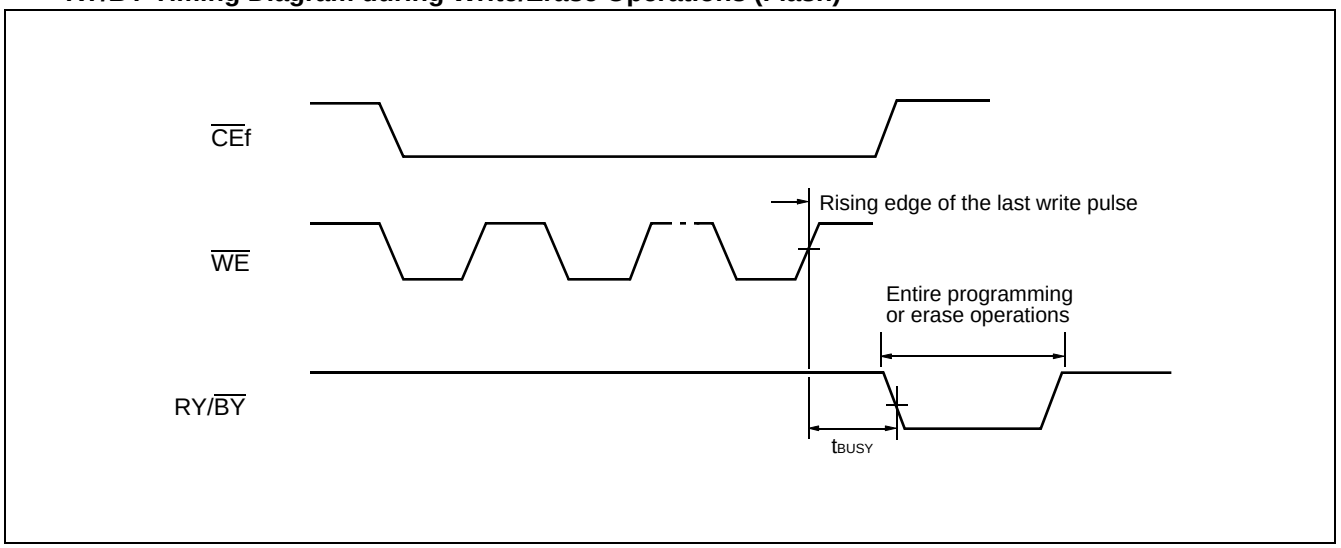
*: DQ_6 stops toggling (The device has completed the Embedded operation).

- **Bank-to-bank Read/Write Timing Diagram (Flash)**

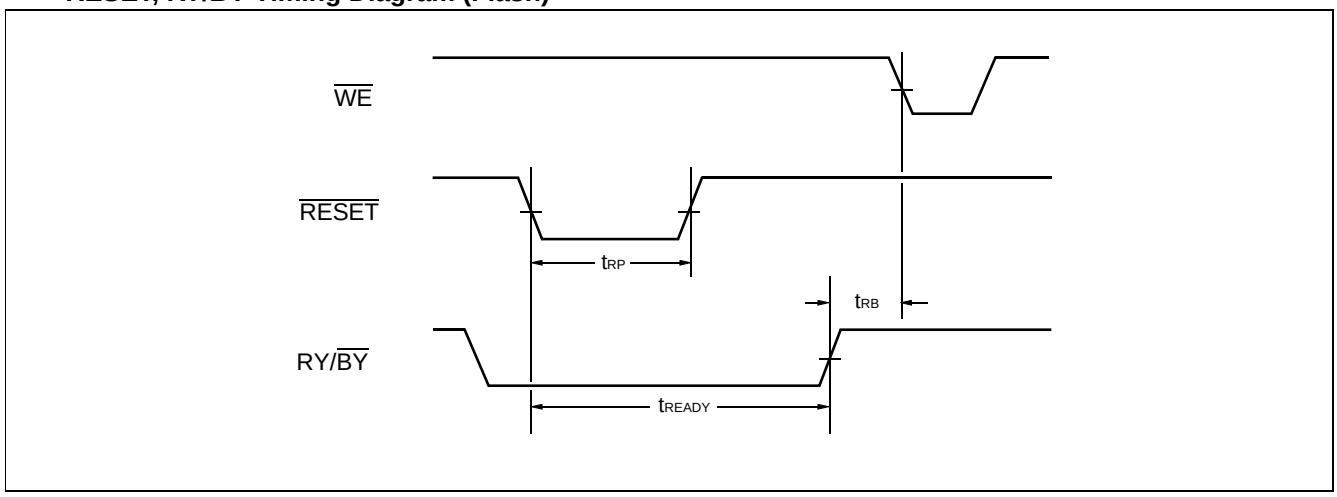


Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1: Address of Bank 1.
BA2: Address of Bank 2.

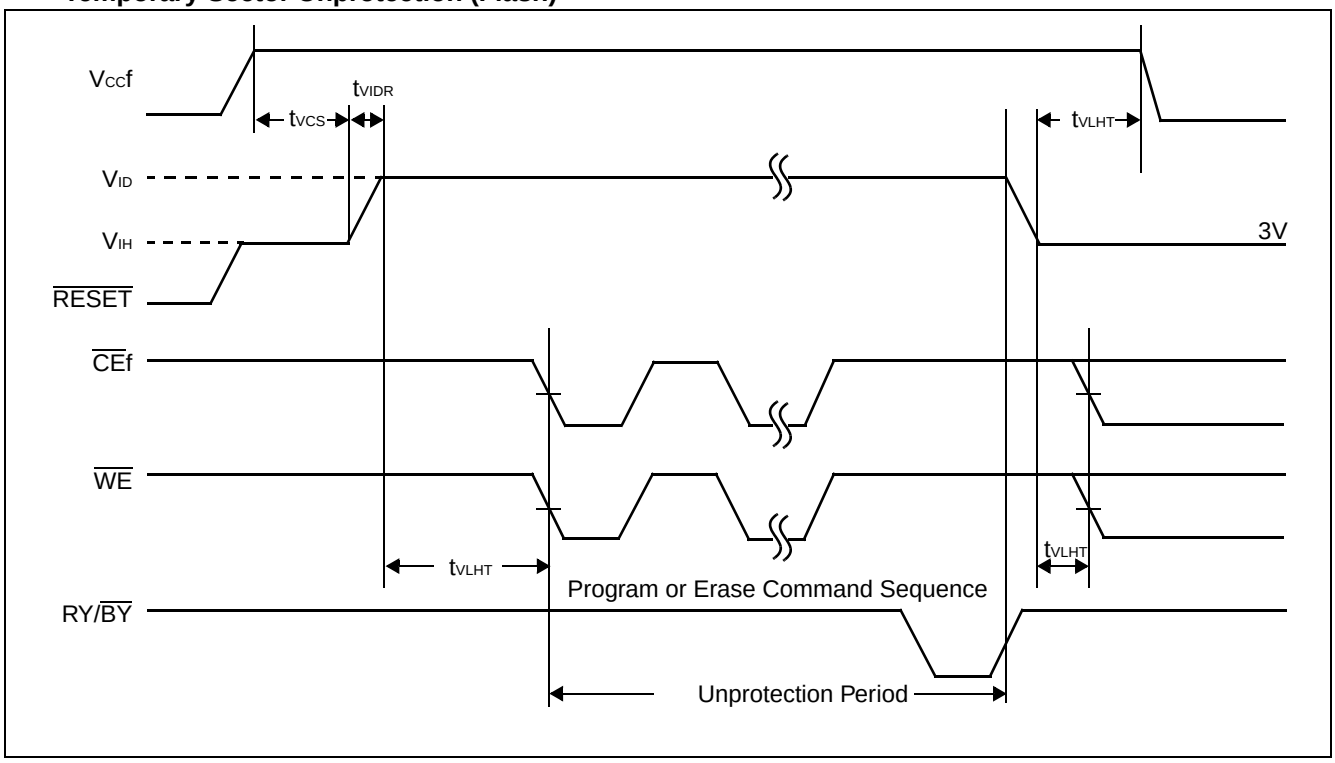
- **RY/$\overline{BY}$ Timing Diagram during Write/Erase Operations (Flash)**



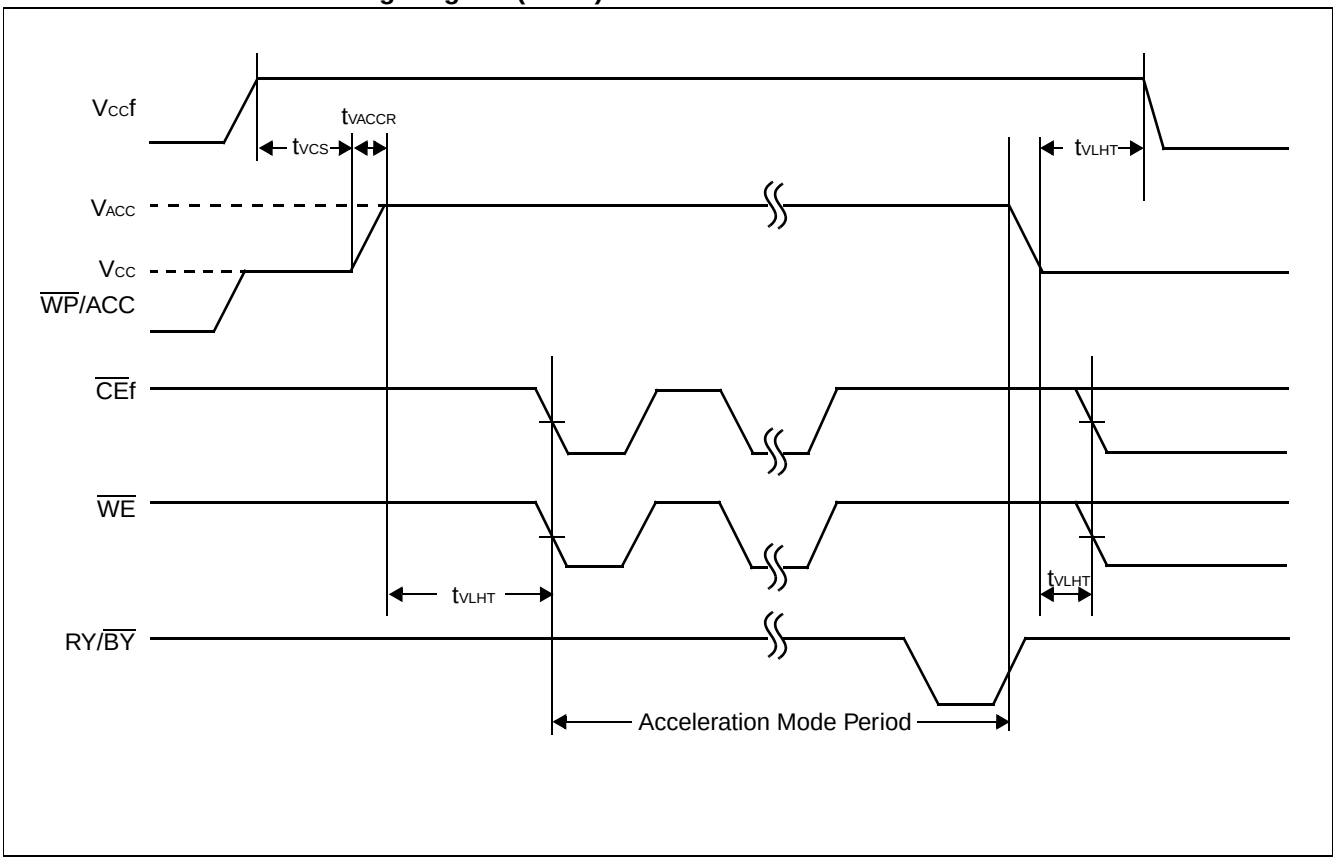
- **$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram (Flash)**



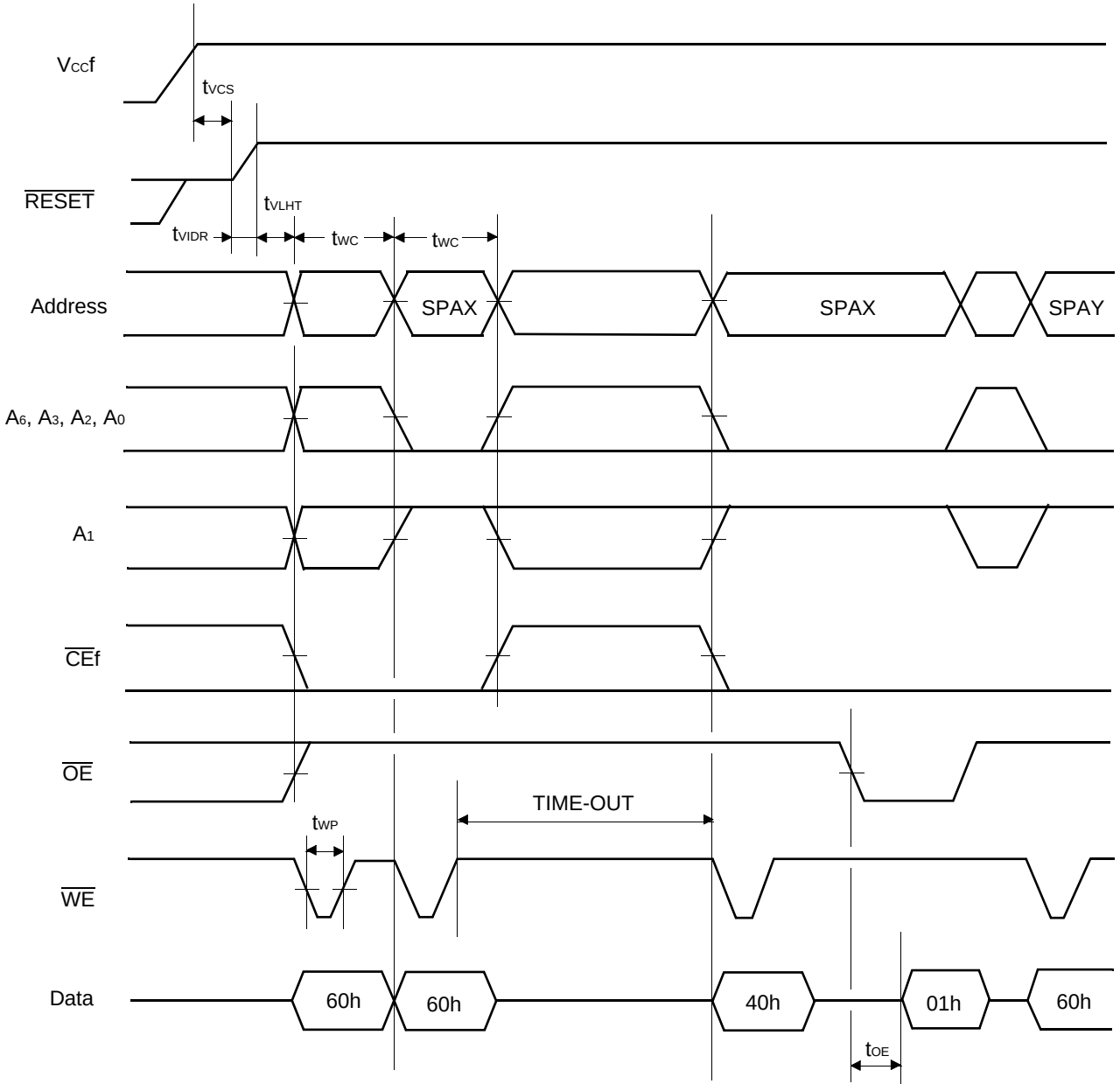
- **Temporary Sector Unprotection (Flash)**



- **Acceleration Mode Timing Diagram (Flash)**



- **Extended Sector Group Protection (Flash)**



SPAX: Sector Group Address to be protected
SPAY : Next Group Sector Address to be protected
TIME-OUT : Time-Out window = 250 μs (Min)

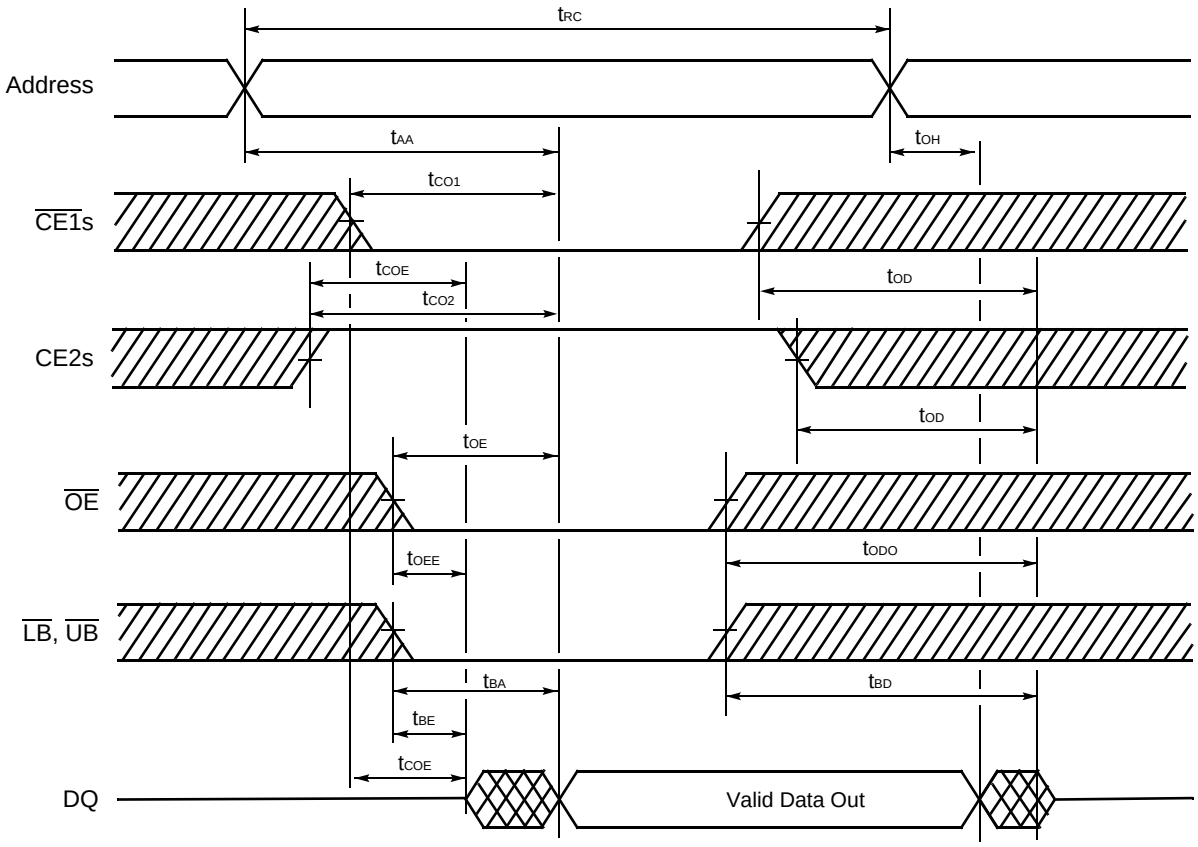
■ 8M SRAM CHARACTERISTICS for MCP

- **Read Cycle (SRAM)**

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle Time	t_{RC}	70	—	ns
Address Access Time	t_{AA}	—	70	ns
Chip Enable ($\overline{CE1}$s) Access Time	t_{CO1}	—	70	ns
Chip Enable (CE2s) Access Time	t_{CO2}	—	70	ns
Output Enable Access Time	t_{OE}	—	35	ns
$\overline{LB}$, $\overline{UB}$ to Output Valid	t_{BA}	—	70	ns
Chip Enable ($\overline{CE1}$s Low and CE2s High) to Output Active	t_{COE}	5	—	ns
Output Enable Low to Output Active	t_{OEE}	0	—	ns
$\overline{LB}$, $\overline{UB}$ Enable Low to Output Active	t_{BE}	0	—	ns
Chip Enable ($\overline{CE1}$s High or CE2s Low) to Output High-Z	t_{OD}	—	25	ns
Output Enable High to Output High-Z	t_{ODO}	—	25	ns
$\overline{LB}$, $\overline{UB}$ Output Enable to Output High-Z	t_{BD}	—	25	ns
Output Data Hold Time	t_{OH}	10	—	ns

Note: Test Conditions–Output Load:1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V or 3.0 V
Timing measurement reference level
Input: 0.5 × V_{CC}s
Output: 0.5 × V_{CC}s

- **Read Cycle (SRAM)**

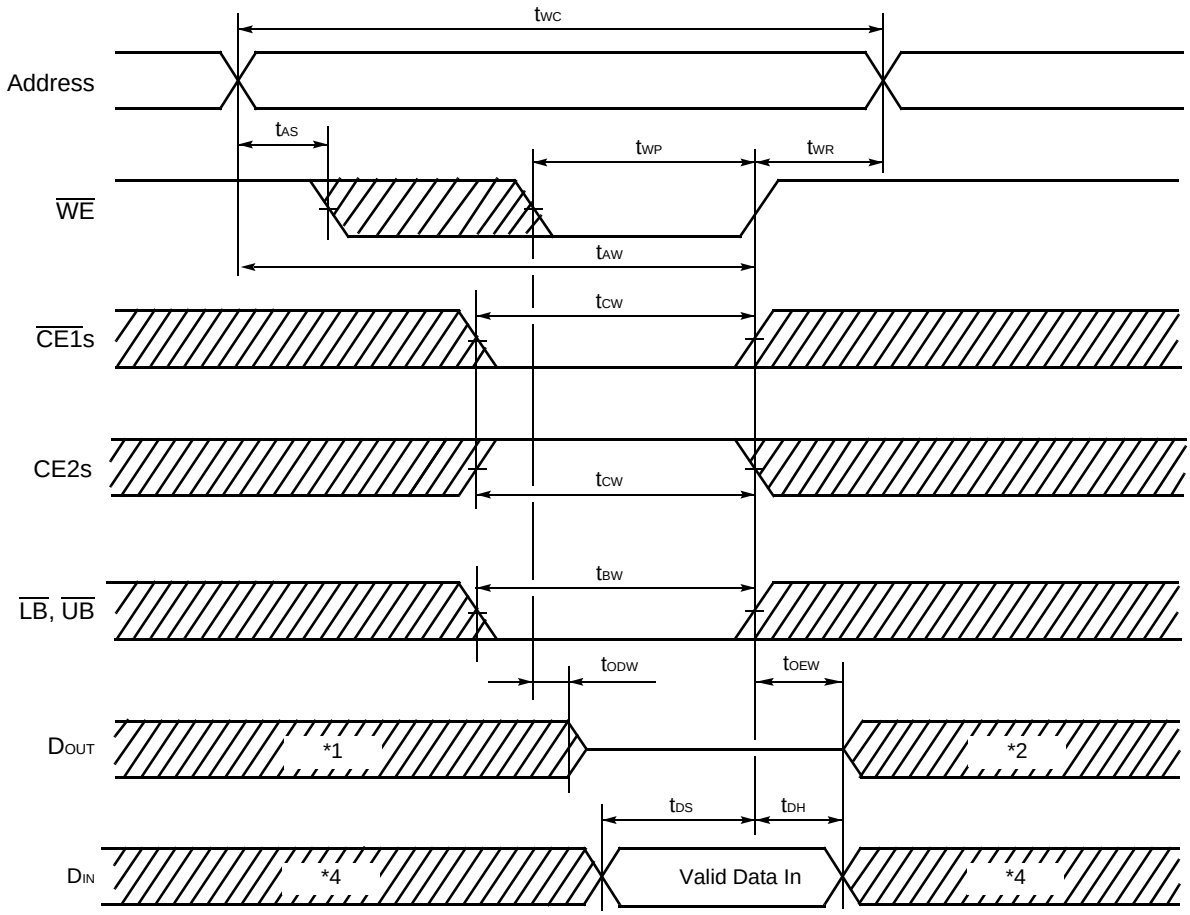


Note: $\overline{WE}$ remains HIGH for the read cycle.

- **Write Cycle (SRAM)**

Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t_{WC}	70	—	ns
Write Pulse Width	t_{WP}	50	—	ns
Chip Enable to End of Write	t_{CW}	55	—	ns
Address valid to End of Write	t_{AW}	55	—	ns
$\overline{LB}$, $\overline{UB}$ to End of Write	t_{BW}	55	—	ns
Address Setup Time	t_{AS}	0	—	ns
Write Recovery Time	t_{WR}	0	—	ns
$\overline{WE}$ Low to Output High-Z	t_{ODW}	—	25	ns
$\overline{WE}$ High to Output Active	t_{OEW}	0	—	ns
Data Setup Time	t_{DS}	30	—	ns
Data Hold Time	t_{DH}	0	—	ns

- **Write Cycle *3 ($\overline{WE}$ control) (SRAM)**



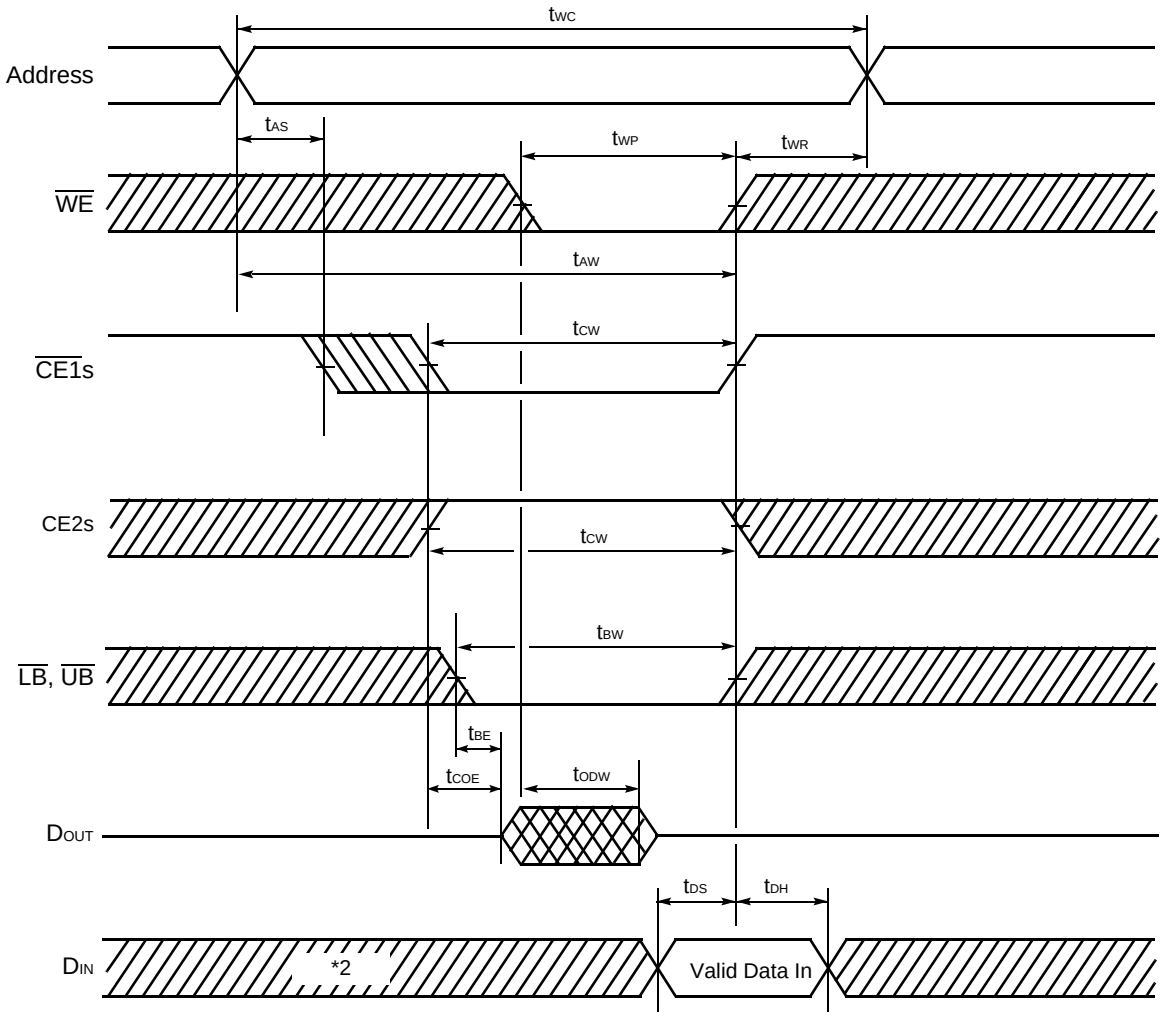
*1 : If $\overline{CE1}$s goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

*2 : If $\overline{CE1}$s goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.

*3 : If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

*4 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

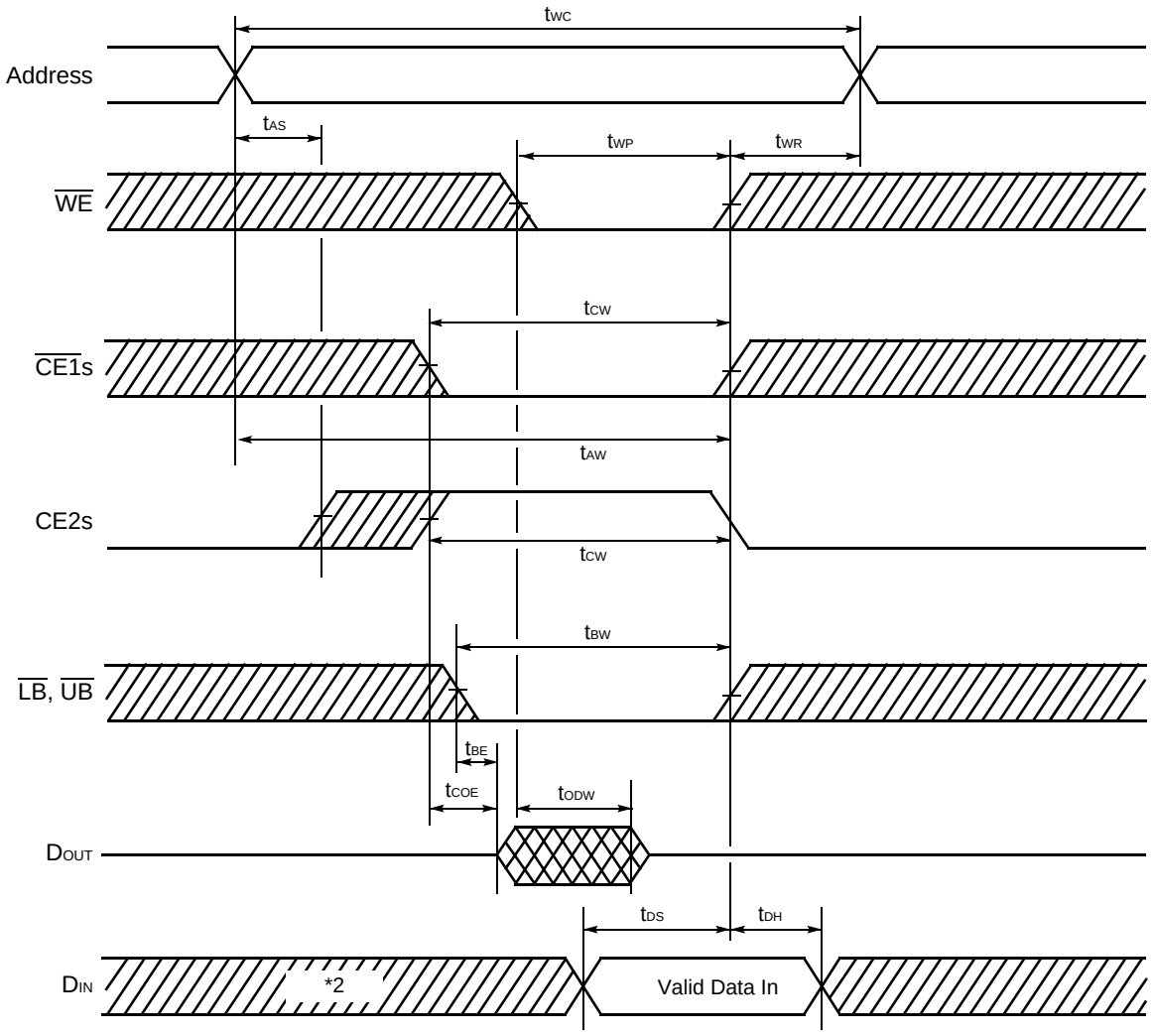
- **Write Cycle *1 ($\overline{CE}$1s control) (SRAM)**



*1 : If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

*2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

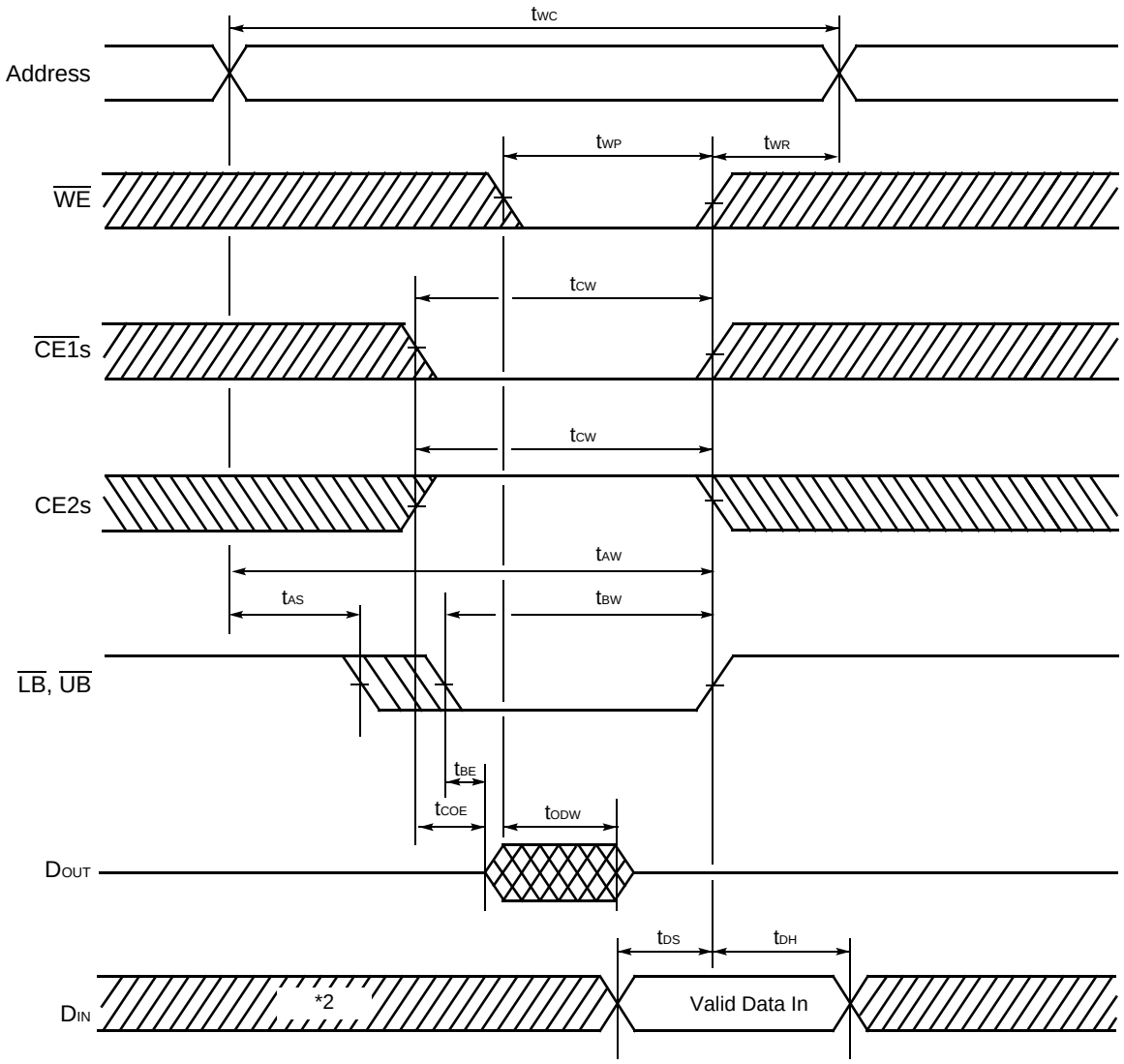
- **Write Cycle *1 (CE2s Control) (SRAM)**



*1 : If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

*2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle *1 ($\overline{LB}$, $\overline{UB}$ Control) (SRAM)**



*1 : If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

*2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector Erase Time	—	0.5	2	s	Excludes programming time prior to erasure
Word Programming Time	—	6	100	µs	Excludes system-level overhead
Byte Programming Time	—	4	80	µs	Excludes system-level overhead
Chip Programming Time	—	25.2	95	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	

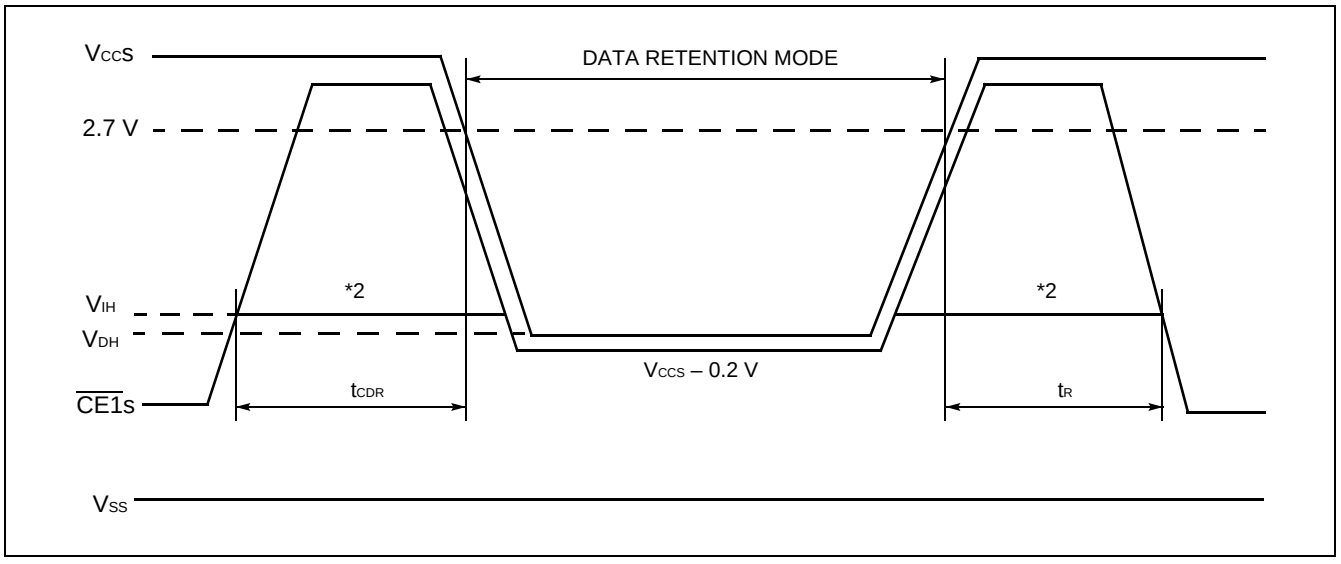
Note : Typical Erase conditions T_A = +25°C, VCCf_1 & VCCf_2 = 2.9 V
Typical Program conditions T_A = +25°C, VCCf_1 & VCCf_2 = 2.9 V Data= Checker

■ DATA RETENTION CHARACTERISTICS (SRAM)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Data Retention Supply Voltage		V_{DH}	1.5	—	3.1	V
Standby Current	V_{DH} = 3.0 V	I_{DDS2}	—	—	15	µA
Chip Deselect to Data Retention Mode Time		t_{CDR}	0	—	—	ns
Recovery Time		t_R	t_{RC}	—	—	ns

Note : t_{RC}: Read cycle time

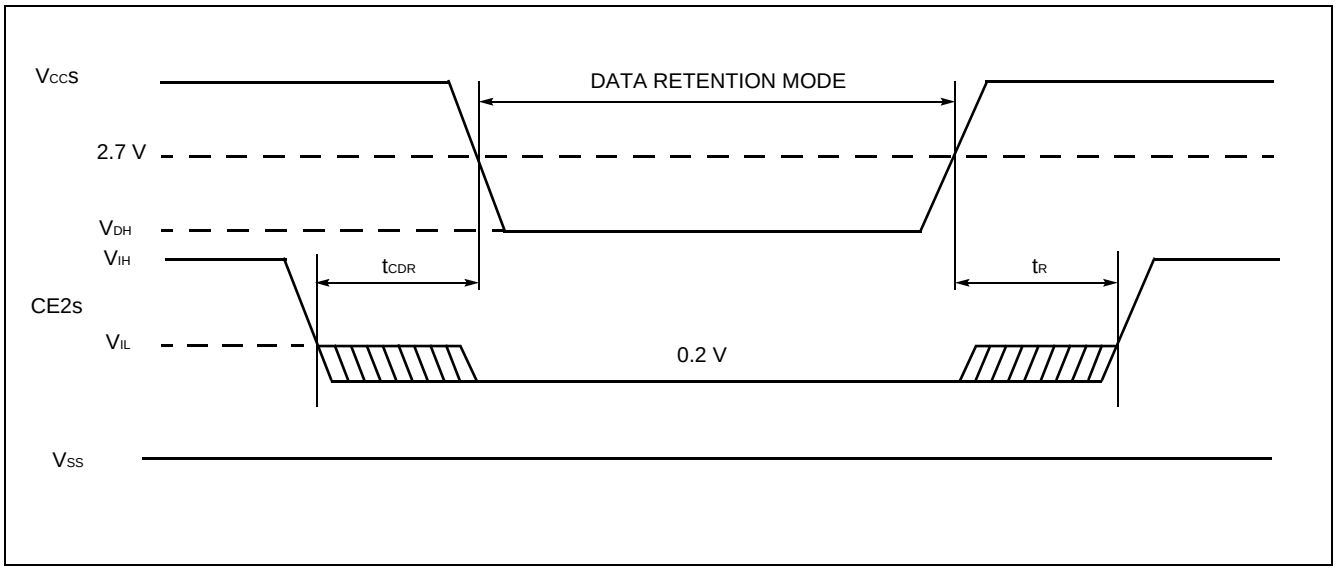
- **$\overline{CE1}$s Controlled Data Retention Mode *1**



*1 : In $\overline{CE1}$s controlled data retention mode, input level of CE2s should be fixed Vccs to V_{CC}s–0.2 V or V_{SS} to 0.2 V during data retention mode. Other input and input/output pins can be used between –0.3 V to V_{CC}s+0.3 V.

*2 : When $\overline{CE1}$s is operating at the V_{IH} Min level, the standby current is given by I_{SB1}s during the transition of V_{CC}s from Vccs Max to V_{IH} Min level.

• **CE2s Controlled Data Retention Mode ***



* : In CE2s controlled data retention mode, input and input/output pins can be used between –0.3 V to Vccs+0.3V.

■ PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	11	14	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	12	16	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	14	16	pF
$\overline{WP}$/ACC Pin Capacitance	C_{IN3}	V_{IN} = 0	21.5	26	pF

Note: Test conditions Ta = +25°C, f = 1.0 MHz

■ HANDLING OF PACKAGE

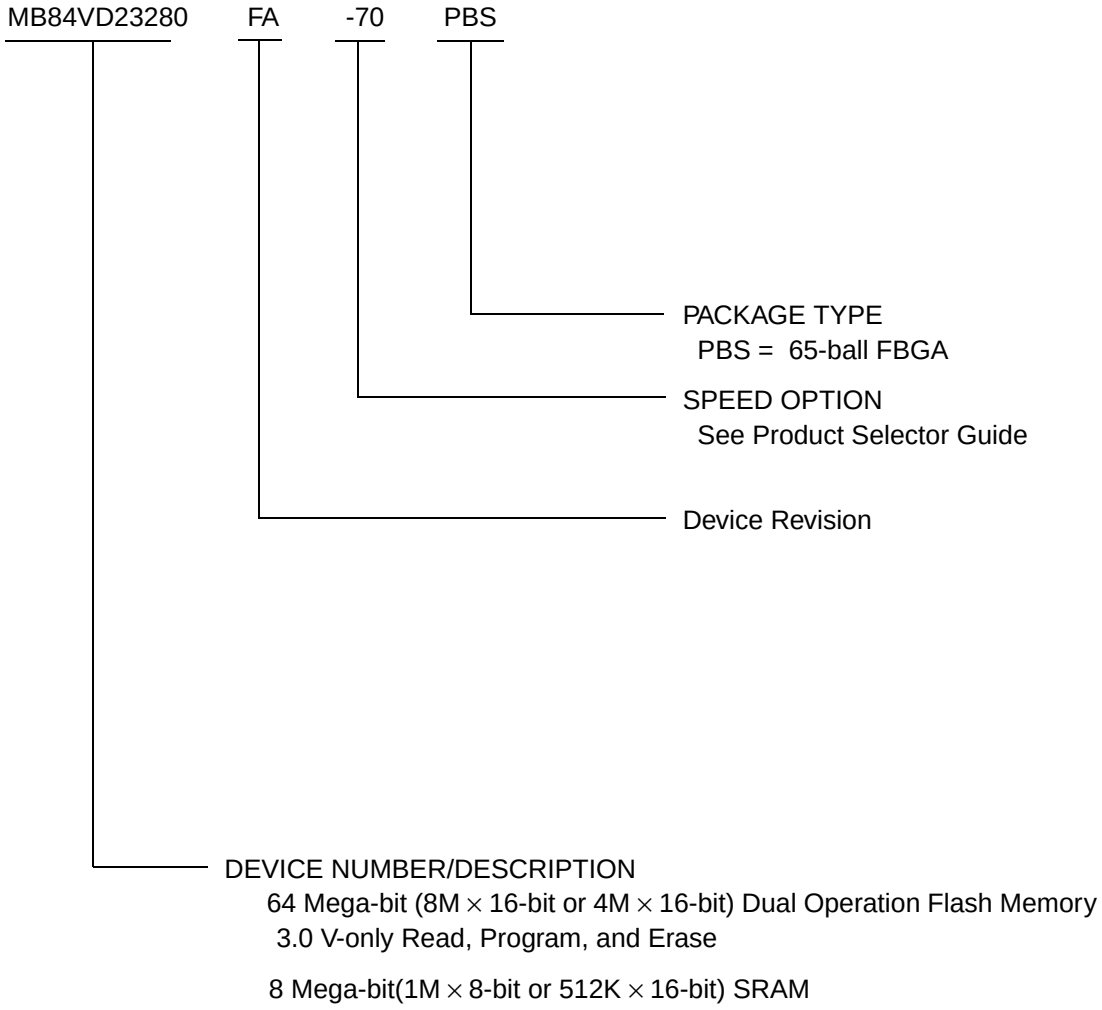
Please handle this package carefully since the sides of packages are right angle.

■ CAUTION

(1) The high voltage (V_{ID}) can not apply to address pins and control pins except $\overline{RESET}$. Therefore, it can not use autoselect and sector protect function by applying the high voltage (V_{ID}) to specific pins.

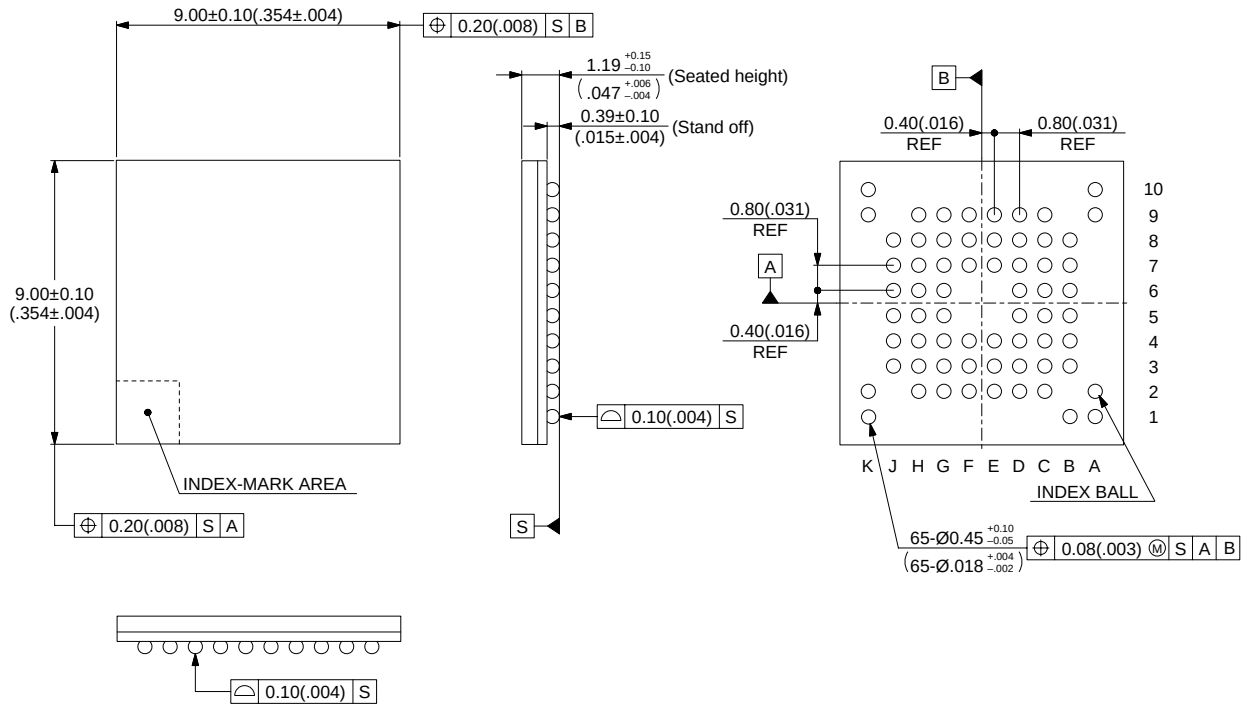
(2) For the sector protection, since the high voltage (V_{ID}) can be applied to the $\overline{RESET}$, it can be protected the sector useing “Extended sector protect” command.

■ ORDERING INFORMATION



■ PACKAGE DIMENSION

65-pin plastic FBGA
(BGA-65P-M01)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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