

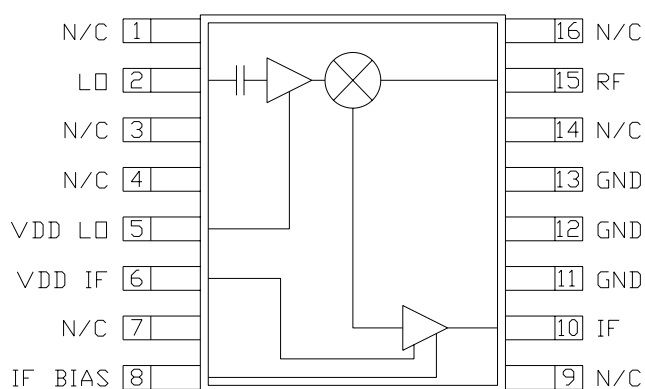
PCS/UMTS HIGH IP3 RFIC DOWNCONVERTER, 1.7 - 2.2 GHz

Typical Applications

The HMC380QS16G is ideal for:

- GSM, GPRS & EDGE Infrastructure
- CDMA, WCDMA Infrastructure
- PHS Infrastructure

Functional Diagram



Features

- +19 dBm Input IP3
- Low LO Drive: -5 dBm
- Conversion Gain: 11 dB
- Noise Figure: 9 dB
- Single Positive Supply: +5V, 120 mA

General Description

The HMC380QS16G is a high linearity down-converter receiver IC suitable for PCS/UMTS infrastructure applications from 1.7 - 2.2 GHz. The receiver IC is designed to support UMTS applications where a high third order intercept point is required. A passive mixer coupled with a high dynamic range IF amplifier achieves an input IP3 of +19 dBm. The converter provides a gain of 11 dB and 9 dB typical single side band noise figure. The IC operates from a positive +5V rail consuming 120 mA of current while only requiring a -5 dBm LO drive. The design requires no external baluns. The mixer supports IF frequencies between 50 MHz and 300 MHz.

Electrical Specifications, $T_A = +25^\circ\text{C}$, LO = -5 dBm, Vdd = 5V, IF = 250 MHz*

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range, RF	1.7 - 2.0			2.0 - 2.2			GHz
Frequency Range, LO	1.4 - 1.95			1.7 - 2.15			GHz
Frequency Range, IF**	50 - 300			50 - 300			MHz
Conversion Gain	9	11		8.5	10.5		dB
Noise Figure (SSB)		9.2	10.5		10	11.5	dB
LO to RF Isolation	18	25		25	30		dB
LO to IF Isolation	24	32		32	40		dB
RF to IF Isolation	38	48		45	50		dB
IP3 (Input)	17	19		17	19		dBm
1 dB Compression (Input)	3	5		3	6		dBm
LO Input Drive Level (Typical)	-5 to 0			-5 to 0			dBm
Supply Current (Idd for LO & IF) (IF bias resistor= 3.3 Ohms)		120			120		mA

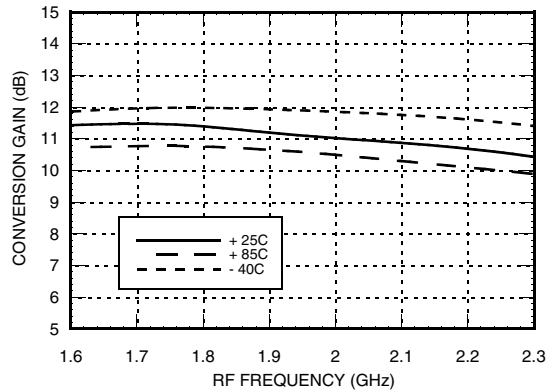
* Unless otherwise noted all measurements with low side LO & IF = 250 MHz.

** If matching must be tuned for optimal results, see application circuit herein.

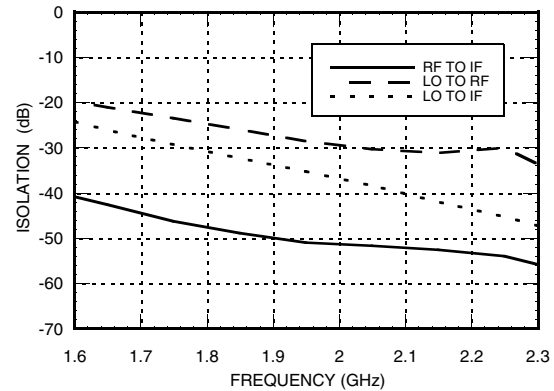
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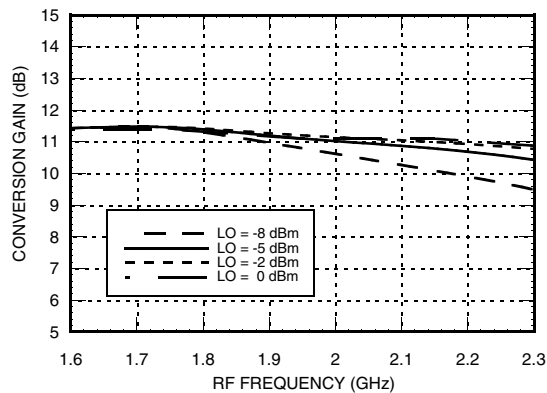
**Conversion Gain
vs. Temperature @ LO = -5 dBm**



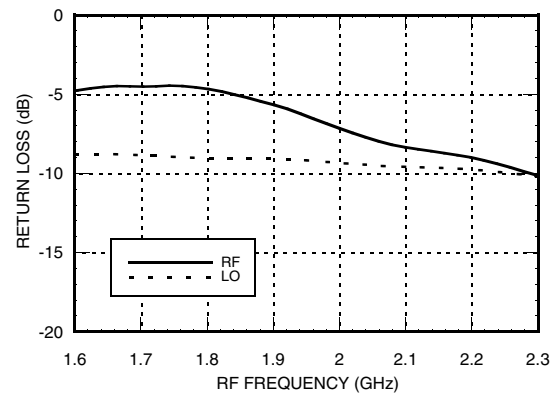
Isolation @ LO = -5 dBm



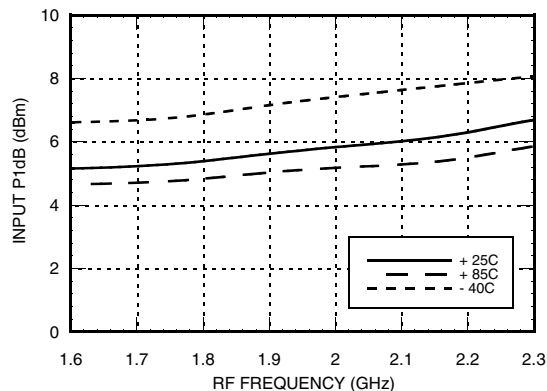
Conversion Gain vs. LO Drive



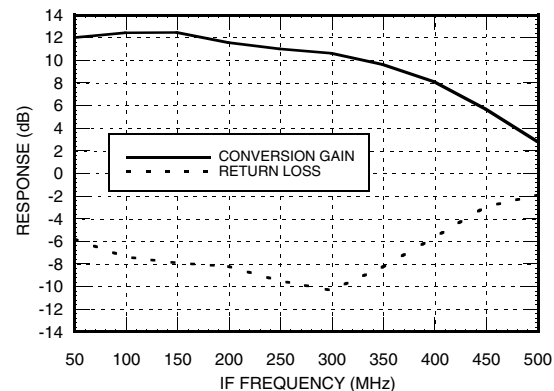
Return Loss @ LO = -5 dBm



**Input P1dB
vs. Temperature @ LO = -5 dBm**



IF Bandwidth @ LO = -5 dBm



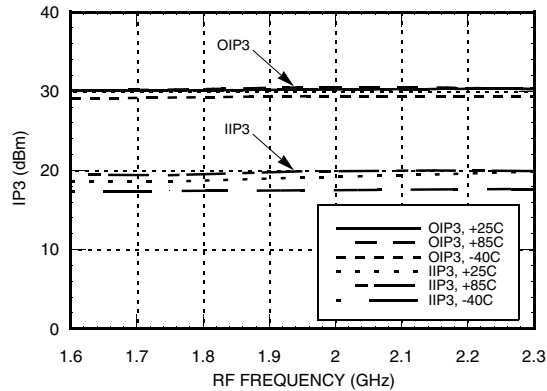
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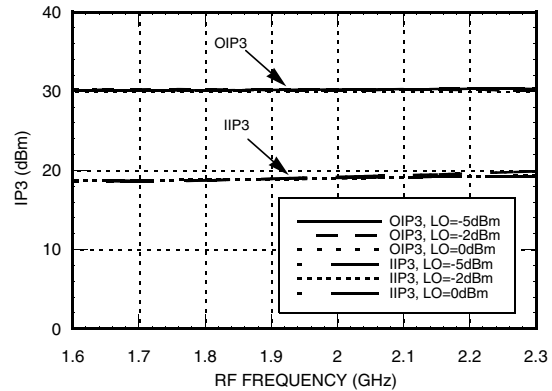
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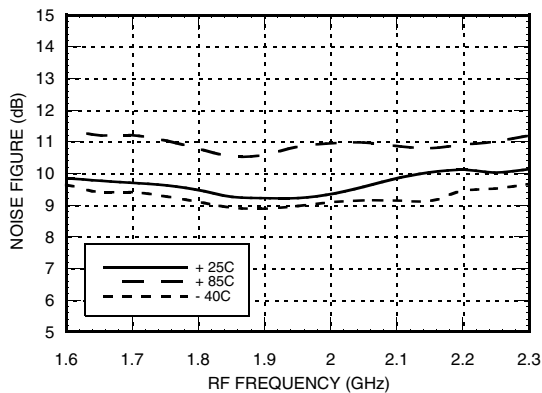
**Input and Output IP3
vs. Temperature @ LO = -5 dBm**



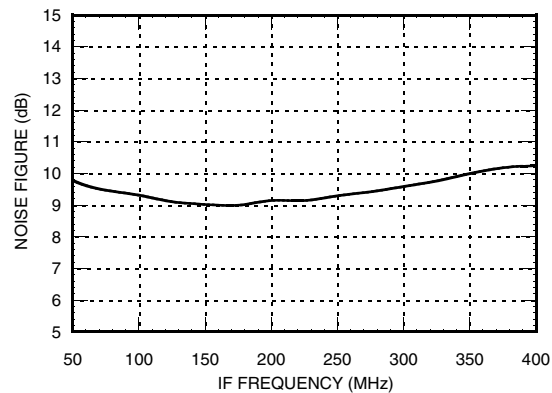
Input and Output IP3 vs LO Drive



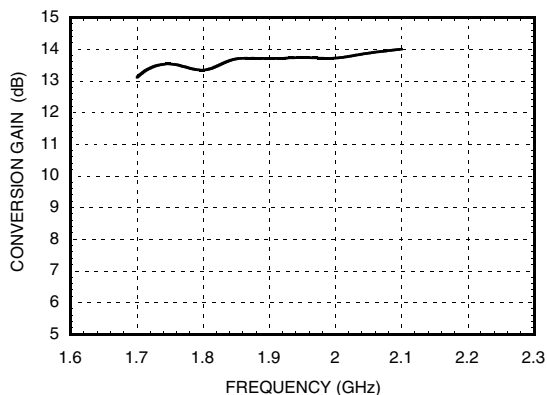
**Noise Figure vs Temperature
Swept LO, Fixed IF = 250 MHz**



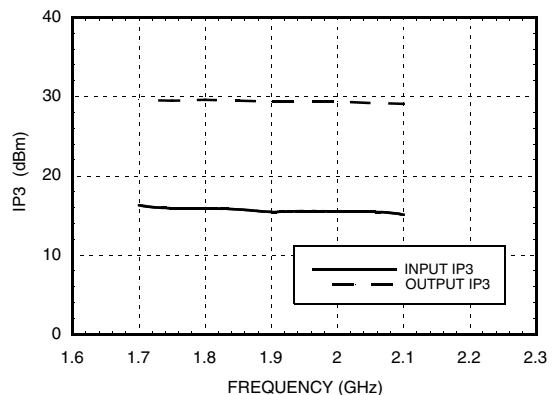
**Noise Figure
Swept IF, Fixed LO = 1.7 GHz**



**Conversion Gain with
IF Tuned for 70 MHz @ LO = -5 dBm**



**IP3 with
IF Tuned for 70 MHz @ LO = -5 dBm**



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MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	40	62	64	37
1	62	0	60	90	92
2	93	92	54	90	92
3	91	93	94	88	93
4	93	92	94	94	93
RF Freq. = 1.9 GHz @ -10 dBm LO Freq. = 1.65 GHz @ -5 dBm All values in dBc relative to the IF power level.					

Harmonics of LO

	nLO Spur @ RF Port			
LO Freq. (GHz)	1	2	3	4
1.4	20	3	20	15
1.6	25	6	20	22
1.8	29	8	15	35
2.0	29	8	15	39
2.2	39	10	17	34
2.4	26	12	25	35
LO = -5 dBm All values in dBc below input LO level measured at RF port.				

Absolute Maximum Ratings

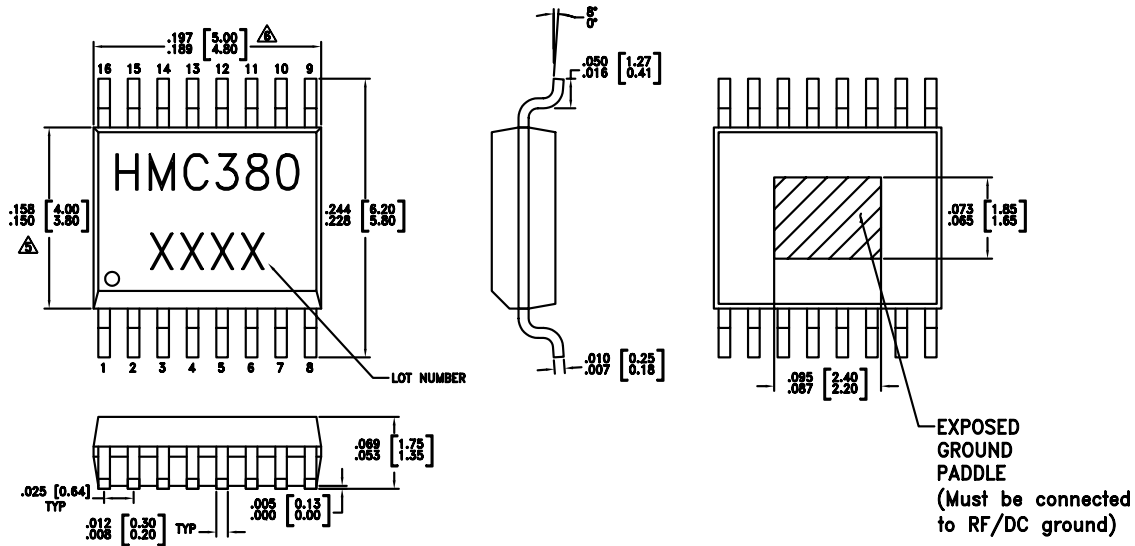
RF / IF Input (Vdd= +5V)	+13 dBm
LO Drive (Vdd= +5V)	+15 dBm
Vdd (LO or IF)	+7 Vdc
Channel Temperature	150°C
Continuous Pdiss (T = 85°C) (derate 13.0 mW/°C above 85°C)	0.854 W
Storage Temperature	-65 to +150°C
Operating Temperature	-40 to +85°C

Typical Supply Current vs. Vdd

Vdd (LO + IF)	Idd (mA)
+4.5	108
+5.0	110
+5.5	111
Downconverter will operate over full voltage range shown above.	

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Outline Drawing

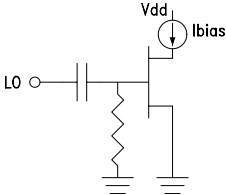
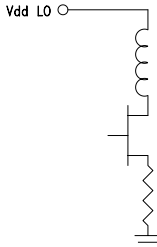
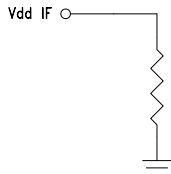
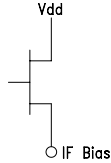
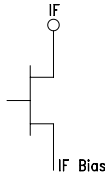
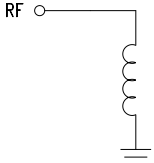


NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
3. LEAD AND GROUND PADDLE PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS]
5. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
6. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

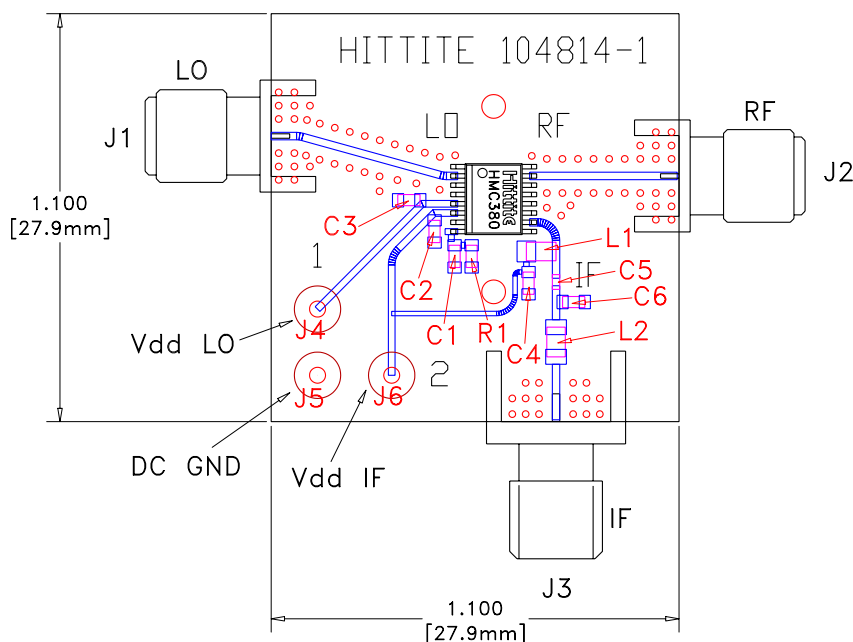
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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 4, 7, 9, 14, 16	N/C	Not Connected	
2	LO Port	This pin is AC coupled and matched to 50 Ohm from 1.4 - 2.2 GHz.	
11, 12, 13	GND	Backside of package has exposed metal ground slug that must also be connected to RF/DC ground.	
5	Vdd LO	Power supply for the LO amplifier. One external RF bypass capacitor (10,000 pF) is required.	
6	Vdd IF	Bias voltage for IF amplifier. One external RF bypass capacitor (10,000 pF) is required.	
8	IF Bias	DC bias setting for IF amplifier.	
10	IF Port	Output of IF and bias port for amplifier. A pull up inductor (L1), output matching network (C5, C6, L2), and 10,000 pF bypass capacitor (C4) are required.	
15	RF Port	This pin is DC coupled and matched to 50 Ohm from 1.7 - 2.2 GHz.	

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Evaluation PCB



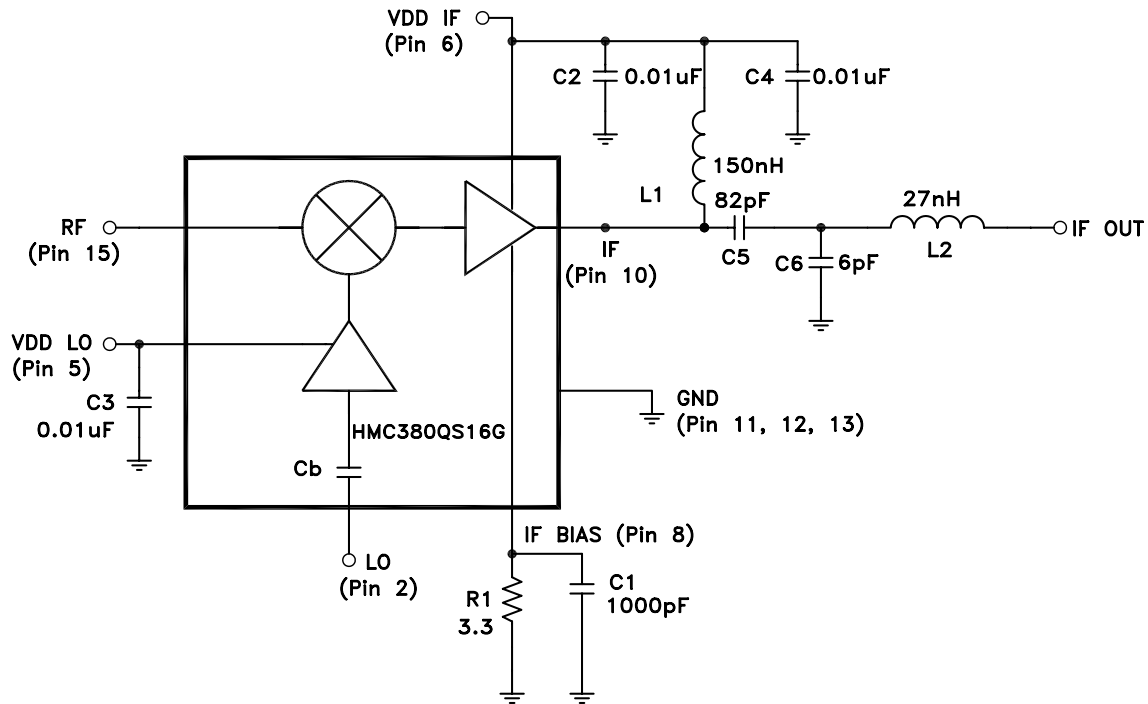
List of Material

Item	Description
J1 - J3	PC Mount SMA RF Connector
J4 - J6	DC Pins
C1	1000 pF Chip Capacitor, 0603 Pkg.
C2, C3, C4	0.01µF Chip Capacitor, 0603 Pkg.
C5	82 pF Chip Capacitor, 0402 Pkg.
C6	6 pF Chip Capacitor, 0603 Pkg.
L1	150 nH Chip Inductor, 0805 Pkg.
L2	27 nH Chip Inductor, 0805 Pkg.
R1	3.3 Ohm Resistor, 0603 Pkg.
U1	HMC380QS16G
PCB*	104814 Evaluation Board, 1.100" x 1.100"
* Circuit Board Material: Rogers 4350	

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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Application Circuit



Note: Pin 5 and Pin 6 may be connected to a common Vdd Supply.

Selection of L2 & C6 For Various Tuned IF Frequencies*

IF	L2	C6
250 MHz	27 nH	6 pF
70 MHz	39 nH	39 pF

* Contact Hittite to optimize tuning topology for desired IF frequency.

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