Overview

HYB 39S13620TQ-6/-7/-8

- High Performance:

	-6	-7	-7	-8	Units
f_{CK}	166	125	125	125	MHz
latency	3	2	3	3	–
t_{CK3}	6	8	7	8	ns
t_{AC3}	5.5	5.5	5.5	6	ns

- Single Pulsed $\overline{RAS}$ Interface
- Programmable $\overline{CAS}$ Latency: 2, 3
- Fully Synchronous to Positive Clock Edge
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8 and full page for sequential 1, 2, 4, 8 for interleave
- Special Mode Registers
- Two color registers
- Burst Read with Single Write Operation
- Block Write and Write-per-Bit Capability
- Byte controlled by DQM0-3
- Auto Precharge and Auto Refresh Modes
- Suspend Mode and Power Down Mode
- 2k refresh cycles/32 ms
- t_{AC} = 5 ns
- t_{SETUP}/t_{HOLD} = 2 ns/1 ns
- Latency 2 @ 125 MHz
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V ± 0.3 V Power Supply
- LVTTL compatible inputs and outputs

The HYB 39S163200TQ are dual bank Synchronous Graphics DRAM's (SGRAM) organized as 2 banks × 256 Kbit × 32 with built-in graphics features. These synchronous devices achieve high speed data transfer rates up to 143 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with an advanced 64MBit DRAM process technology.

The device is designed to comply with all JEDEC standards set for synchronous graphics DRAM products, both electrically and mechanically.

$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF and $\overline{CS}$ are pulsed signals which are examined at the positive edge of each externally applied clock. Internal chip operating modes are defined by combinations of these signals. A ten bit address bus accepts address data in the conventional RAS/CAS multiplexing style. Ten row address bits (A0 - A9) and a bank select BA are strobed with $\overline{RAS}$. Column address bits plus a bank select are strobed with $\overline{CAS}$.

Prior to any access operation, the $\overline{CAS}$ latency, burst length and burst sequence must be programmed into the device by address inputs during a mode register set cycle. An Auto Precharge function may be enabled to provide a self-timed row precharge. This is initiated at the end of the burst sequence. In addition, it features the write per bit, the block write and the masked block write

functions. By having a programmable Mode register and Special Mode register, the system can select the best suitable modes to maximize its performance.

Operating the two memory banks in an interleave fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 143 MHz is possible depending on burst length, $\overline{CAS}$ latency and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported.
These devices operate with a single 3.3 V ± 0.3 V power supply and are available in 100 pin TQFP package.

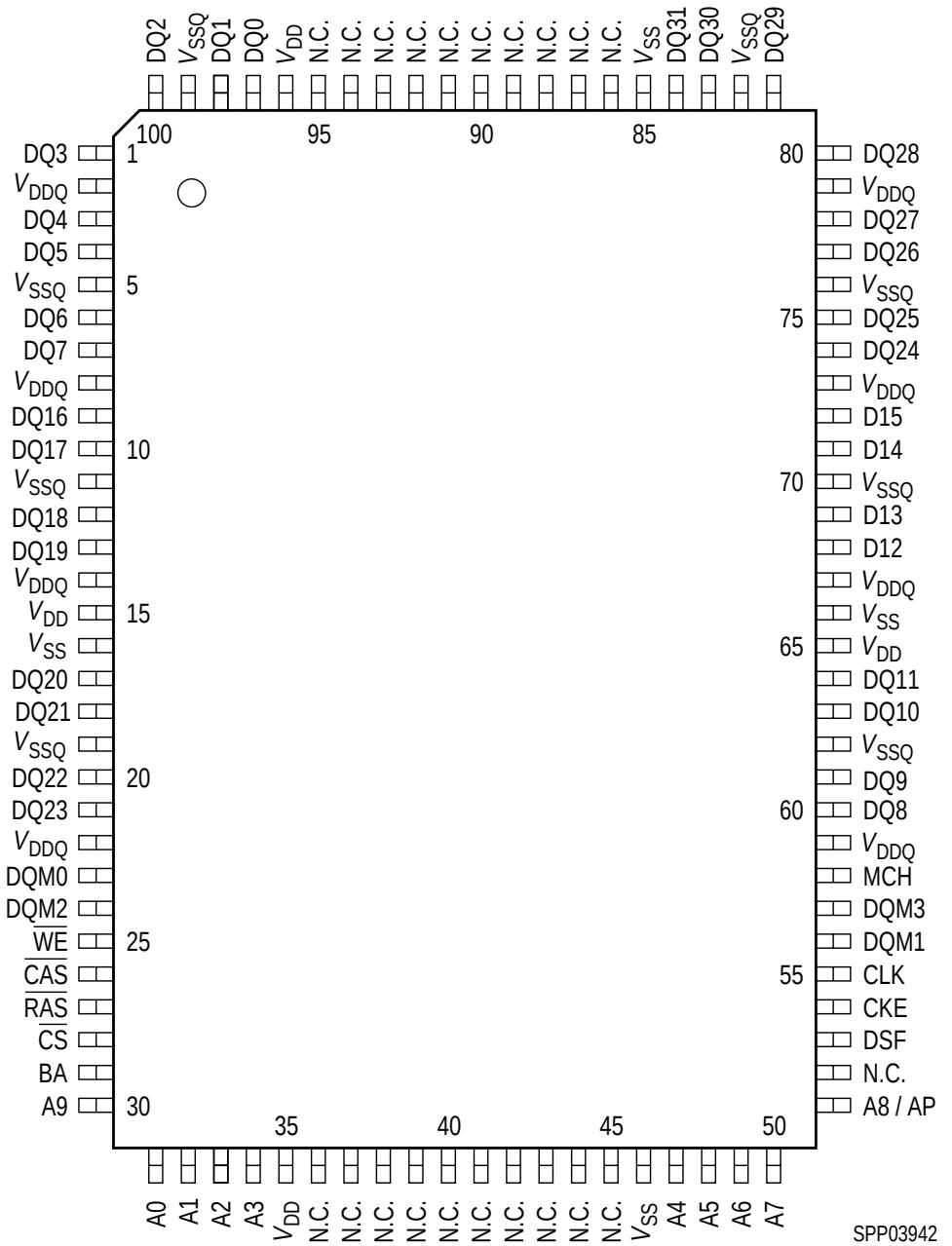
Ordering Information

Type	Ordering Code	Package	Description
SDR LVTTL-Version			
HYB 39S16320TQ-6	on request	TQFP-100-1	256k × 2 × 32 SGRAM
HYB 39S16320TQ-7	on request	TQFP-100-1	256k × 2 × 32 SGRAM
HYB 39S16320TQ-8	on request	TQFP-100-1	256k × 2 × 32 SGRAM
HYB 39S16320TQ-10	on request	TQFP-100-1	256k × 2 × 32 SGRAM

Features

- All signals fully synchronous to the positiv edge of the system clock
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Burst data transfer in sequential or interleaved order
- Burst read with single write
- Programmable $\overline{CAS}$ latency: 2, 3
- 8 column block write and write-per-bit modes
- Independent byte operation via DQM 0 …3 interface
- Auto precharge and auto refresh modes
- 2k refresh cycles/32 ms
- LVTTL compatible I/O
- Hidden auto precharge for read bursts

100 pin TQFP
20 × 14 mm²
0.65 mm pitch
(Marking side)



Pin Configuration

Pin Definitions and Functions

CLK	Clock Input	DQ0 to DQ31	DataInput/Output
CKE	Clock Enable	DQM0 to DQM3	Data Mask
$\overline{CS}$	Chip Select	V_{DD}	Power (+ 3.3 V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	V_{DDQ}	Power for DQ's (+ 3.3 V)
$\overline{WE}$	Write Enable	V_{SSQ}	Ground for DQ's
A0 - A9	Address Inputs	NC	Not connected
A8 - AP	Auto Precharge	DSF	Special Function Enable
BA	Bank Select	MCH	Must Connect High

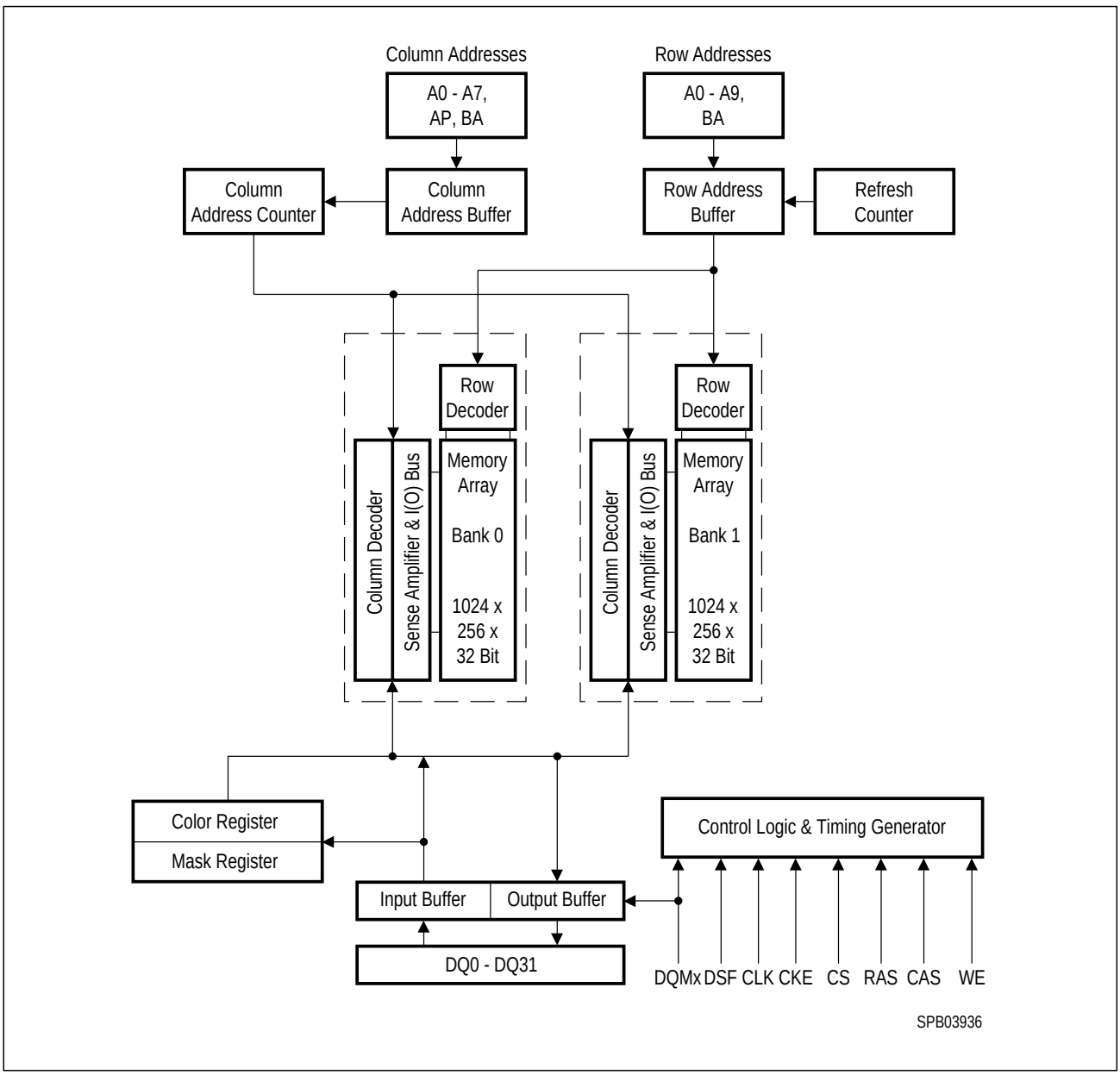
Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SGRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SGRAM.
A0 - A9	Input	Level	–	During a Bank Activate command cycle, A0-A9 defines the row address (RA0-RA9) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A7 defines the column address (CA0-CA7) when sampled at the rising clock edge. In addition to the column address, CA8 is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A8 is high, autoprecharge is selected and BA defines the bank to be precharged (low = bank A, high bank B). If A8 is low, autoprecharge is disabled. During a Precharge command cycle, A8 is used in conjunction with BA to control which bank(s) to precharge. If A8 is high, both bank A and bank B will be precharged regardless of the state of BA. If A8 is low, then BA is used to define which bank to precharge.
BA	Input	Level	–	Selects which bank is activated. BA low selects bank A and BA high selects bank B.
DQ0 - DQ31	Input Output	Level	–	Data Input/Output pins operate in the same manner as on conventional DRAMs, with the exception of the Block Write function. In this case, the DQx pins perform a masking operation.

Signal Pin Description (cont'd)

Pin	Type	Signal	Polarity	Function
DQM0 - DQM3	Input	Pulse	–	During Read, DQM = 1 turns off the output buffers. During Write, DQM = 1 prevents a write to the current memory location. DQM0 corresponds to DQ0 - DQ7 DQM1 corresponds to DQ8 - DQ15 DQM2 corresponds to DQ16 - DQ23 DQM3 corresponds to DQ24 - DQ31
V_{DD} V_{SS}	Supply	–	–	Power and ground for the input buffers and the core logic.
V_{DDQ} V_{SSQ}	Supply	–	–	Isolated power supply and ground for the output buffers to provide improved noise immunity.
DSF	Input	Level	–	DSF is part of the input command to the SGRAM. If DSF is low, SGRAM operates in the same way as SDRAMs. When DSF is high it enables the block write and masked write and special mode register setup cycle.

Functional Block Diagrams



Functional Description

General

The 16 Mbyte SGRAM is a dual bank 1024 × 256 × 32 DRAM with graphics features of Block Write and Masked Write. It consists of two banks. Each bank is organized as 1024 rows × 256 columns × 32 bits.

Read and Write accesses are burst oriented. Accesses begin with the registration of an Activate command which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and the row to be accessed. BA selects the bank and address bits A9 - A0 select the row. Address bits A7 - A0 registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Block Writes are not burst oriented and always apply to eight column locations selected by A7 - A3. DQs registered at Block Write command are used to mask the selected columns. DQs registered coincident with the Load Special Mode Register command are used as Color Data (LC-Bit = 1) or Persistent Mask (LM = 1). If LC and LM are both 1 in the same Load Special Mode Register command cycle, the data of the Mask and the Color Register will be unknown.

Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees, that the device is preconditioned to each users specific needs.
The following sequence is recommended:

- During power on, all V_{DD} and V_{DDQ} pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state.
- The power on voltage must not exceed V_{DD} + 0.3 V on any of the input pins or V_{DD} supplies.
- The CLK signal must be started at the same time.
- After power on, an initial pause of 200 µs is required.
- The pause is followed by a precharge of both banks using the precharge command.
- To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period.
- Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register.
- A minimum of eight Auto Refresh cycles (CBR) are also required.

It is also possible to reverse the last two steps of the initialization procedure:
First send at least 8 CBR commands, then the LMR command.

Failure to follow these steps may lead to unpredictable start-up modes.

Mode Register Programming

The Mode Register is used to define: a Burst Length, a Burst type, a Read Latency and an operating mode. The mode register is programmed via the Load Mode Register command and will retain the stored information until it is programmed again or the device looses power. The mode register must be loaded when both banks are idle and the controller must wait the specified time before initiating the subsequent command. Violating either of these requirements may result in unknown operation.

Burst Length

Read and Write operations to the SGRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types and a Full Page Burst is available for the sequential type. The Full Page Burst is used in conjunction with the Burst Terminate command to generate arbitrary burst lengths.

When a Read or Write command is issued, a block of columns equal to the burst length is selected. The block is defined by address bits A7 - A1 when the burst length is set to 2, by A7-A2 for burst length set to 4 and by A7 - A3 for burst length set to 8. The lower order bit(s) are used to select the starting location within the block. The burst will wrap within the block if a boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved and the type is selected based on the setting of BT bit in the mode register. If BT is set to “0”, the burst type is sequential, if BT is “1”, the burst type is interleave.

Read Latency

The Read Latency is the delay in clock cycles between the registration of a Read command and the availability of the first piece of output data. The latency can be set to 2 or 3 clocks. If a Read command is registered at clock edge n and the Read Latency is 2 clocks, the data will be available by clock edge n + 2. The DQs will start driving already one cycle earlier (n + 1).

Color Register

The Siemens 16M SGRAM offers two Color Registers. If Bit M7 is set to “1”, two Color Register mode is specified.

Operation Mode

In normal operation, the bits M8 and M9 of Mode Register (MR) are set “0”. The programmed burst length applies to both read and write bursts. When bit M8 is set to “1”, burst read and single write mode is selected.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Load Special Mode Register (LSMR)

The Special Mode Register command is used to load the mask and color registers, which are used in Block Write and Masked Write cycles.The data to be written to either the color registers or the Mask Register is applied to the DQs and the control information is applied to the address inputs. During a LSMR cycle, if the address bit A6 is “1”, and all other address inputs are “0”, the Color Register 0 will be loaded with the data on the DQs. If the address bits A6 and A7 are both set equal to “1” and Mode Register M7 bit was already set to “1”, Color Register 1 will be loaded with the data on the DQs.This color data is used for Block Write cycles. Similarly, when input A5 is “1”, and all other address inputs are “0” during a LSMR cycle, the mask register will be loaded with the data on the DQs. Never Set bit A5 to “1” when A6 and/or A7 are set equal to “1” in the same Load Special Mode Register cycle to avoid unknown operation.

Color Registers

Two Color Registers (Color Register 0 and Color Register 1) are available in the devices. Each color register is a 32-bit register which supplies the data during Block Write cycles. The Color Register is loaded via a Load Special Mode Register command, as shown in the Function Truth table and will retain data until loaded again with a new data or until power is removed from the SGRAM.

Mask Register

The Mask Register (or the Write-per-Bit mask register) is a 32-bit register which acts as a per-bit mask during Masked Write and Masked Block Write cycles. The Mask Register is loaded via the Load Special Mode Register command and will retain data until loaded again or until power is removed from the SGRAM.

Commands

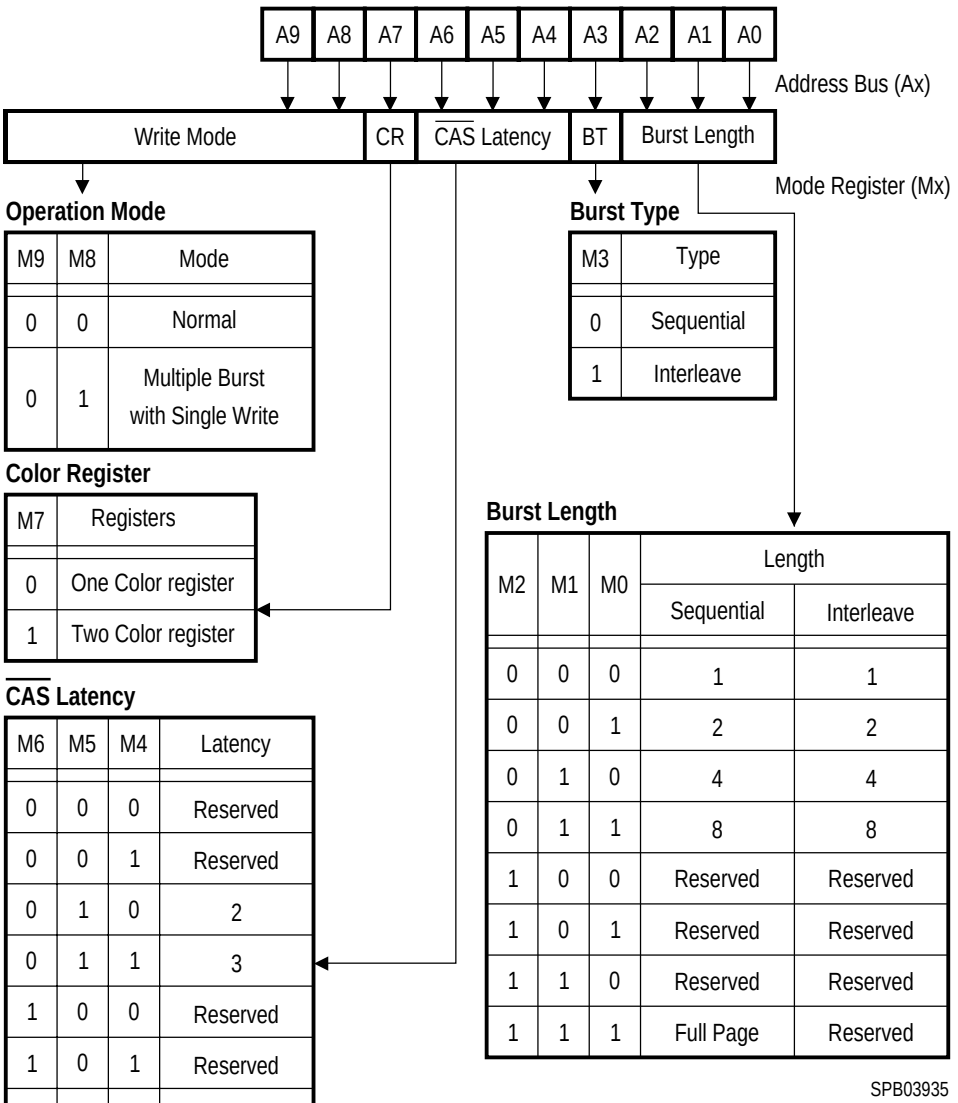
The Function Truth Table provides a quick reference of available commands.

Operation	CKE n – 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA	A8	A0 - A7
Device Deselect (INHBT)	H	X	H	X	X	X	X	X	X	X	X
No Operation (NOP)	H	X	L	H	H	H	X	X	X	X	X
Load Mode Register (LMR)	H	X	L	L	L	L	L	X	X	OPCODE	
Load Special Mode Register (LSMR)	H	X	L	L	L	L	H	X	X	OPCODE	
Row Activate (ACT)	H	X	L	L	H	H	L	X	BA	Row Addr	
Row Active with WpB (ACTM)	H	X	L	L	H	H	H	X	BA	Row Addr	
Read (RD)	H	X	L	H	L	H	X	X	BA	L	Col.
Read with Auto Precharge (RDA)	H	X	L	H	L	H	X	X	BA	H	Col.
Write Command (WR)	H	X	L	H	L	L	L	X	BA	L	Col.
Write Command with Auto Precharge (WRA)	H	X	L	H	L	L	L	X	BA	H	Col.
Block Write (BW)	H	X	L	H	L	L	H	X	BA	L	Col.
Block Write with Auto Precharge (BWA)	H	X	L	H	L	L	H	X	BA	H	Col.
Burst Terminate (BST)	H	X	L	H	H	L	X	X	X	X	X
Precharge Single Bank (PRE)	H	X	L	L	H	L	X	X	BA	L	X
Precharge All Banks (PREAL)	H	X	L	L	H	L	X	X	X	H	X
Auto Refresh (REF)	H	H	L	L	L	H	X	X	X	X	X
Self Refresh Entry (SREF (EN)	H	L	L	L	L	H	X	X	X	X	X
Self Refresh Exit (SREF (EX)	L L	H H	H L	X H	X H	X H	X X	X X	X X	X X	X X
Power Down Mode Entry (PDN-EN)	H H	L L	H L	X H	X H	X H	X X	X X	X X	X X	X X
Power Down Mode Exit (PDN-EX)	L	H	X	X	X	X	X	X	X	X	X

Notes

1. All inputs are latched on the rising edge of the CLK.
2. LMR, REF and SREF commands should be issued only after both banks are deactivated (PREAL command).
3. ACT and ACTM command should be issued only after the corresponding bank has been deactivated (PRE command).
4. WR, WRA, RD, RDA should be issued after the corresponding bank has been activated (ACT command).
5. Auto Precharge command is not valid for full-page burst.
6. BW and BWA commands use mask register data only after ACTM command. DQM byte masking is active regardless of WPB mask.
7. Loading Mask Register: Initiate an LSMR cycle with address pin A5 = 1 to load the mask register with the mask data present on DQ pins. Except A5, all other address pins must be “0” during LSMR cycle while loading the mask register.
8. Loading Color Register: Initiate an LSMR cycle with address pin A6 = 1 to load the color register with the color input data on DQ pins. Address pin A7 selects color register. Except A6 and A7, all other address pins must be “0” during LSMR cycle while loading a color register. If one color register mode is enabled, all address pins, except A6, must be “0” during LSMR cycle.
9. If BW or BWA operation is initiated and 2-Color Register Mode is initialized by the mode register, address A0 selects the desired color register for the operation. If A0 = 0, color register 0 will be used, if A0 = 1, color register 1.
10. Any Write or Block Write cycles to the selected bank/row while active will be masked according to the contents of the mask register, in addition to the DQM signals and the column/byte mask information (the later for Block Writes only).
11. Block Writes are not burst oriented and always apply to the eight column locations selected by A7 - A3.
12. Addressline A9 is always “X” with the exception of two commands:
    In LMR and LSMR commands it provides opcode (see description Mode and Special Mode Register). In ACT and ACTM commands it provides the address bit 9 of the row address.

Address Input for Mode Set (Mode Register Functions)



Address Input for Mode Set (Mode Register Functions)

Burst Length and Sequence

Burst of two

Starting Address (Column Address A0)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

Burst of four

Starting Address (Column Address A1 - A0)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1, 2, 3	0, 1, 2, 3
1	1, 2, 3, 0	1, 0, 3, 2
2	2, 3, 0, 1	2, 3, 0, 1
3	3, 0, 1, 2	3, 2, 1, 0

Burst of eight

Starting Address (Column Address A1 - A0)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
2	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
3	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
4	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
5	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
6	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
7	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page Burst

Full Page Burst is an extension of the above tables of sequential addressing with the burst length being 256.

Special Mode Register Functions

Address Bits										Functions
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	1	0	0	0	0	0	Load Mask Register
0	0	0	1	0	0	0	0	0	0	Load Color Register 0
0	0	1	1	0	0	0	0	0	0	Load Color Register 1

Note: If only one Color Register is in use, A7 is Don't Care.

Special Mode Register Naming Conventions

Address bit name	Special name	Function
A5	LM	Load Mask Enable
A6	LC	Load Color Enable
A7	SCR	Select Color Register

Device Deselect (INHBT)

The device deselect or inhibit function prevents commands from being executed by the SGRAM, regardless of whether the CLK signal is enabled. The device is effectively deactivated (CS is high).

No Operation (NOP)

The NOP command is used to perform a no operation to an SGRAM which is selected (CS is low). This prevents unwanted commands being registered during idle or wait states. The execution of the command(s) already in progress will not be affected.

Load Mode Register (LMR)

The Mode Register is loaded via address input pins A9 - A0 . The LMR command can only be issued when both banks are idle, and a subsequent executable command can not be issued until 2 CLK cycle Latency is met.

Load Special Mode Register (LSMR)

LSMR command is used to load either the Color Register(s) or the Mask Register at a time. The control information is provided on inputs A9 - A0, while the data for the Color or Mask Register is provided on the DQs. The LSMR command can be issued when both banks are idle, or one or both are active but with no Read, Write or Block Write accesses in progress.

Active (ACT)

The ACT command is used to open (or activate) a row in a particular bank. The value on BA selects the bank and the address provided on input pins A9 - A0 selects the row. This row remains open for accesses until a Precharge command is issued to the bank. A Precharge command must be issued before opening a different row in the same bank.

Active with WPB (ACTM)

ACTM command is similar to the ACT command, except that the Write-per-Bit mask is activated. Any Write or Block Write cycles to the selected bank/row while active will be masked according to the contents of the Mask Register.

Read (RD)

The Read command is used to initiate a burst read access from an active row. The value on BA selects the bank and the address provided on inputs A7 - A0 selects the starting column location. The value on A8 determines whether or not Auto Precharge is used. If A8 is “1”, Auto Precharge is used. If Auto Precharge is selected, the row being accessed will be precharged at the end of the read burst; if Auto Precharge is not selected, the row will remain open for subsequent accesses. If a particular DQM was registered high, the corresponding DQs appearing 2 clocks later on the output pins will be High-Z.

Write (WR)

The Write command is used to initiate a burst write access to an active row. The value on BA selects the bank and the address provided on inputs A7 -A0 selects the starting column location. The value on A8 determines whether or not Auto Precharge is used. If A8 is “1”, Auto Precharge is used. If Auto Precharge is selected, the row being accessed will be precharged at the end of write burst; if Auto Precharge is not selected, the row will remain open for subsequent accesses. If a particular DQM is registered high, the corresponding data inputs will be ignored and the write will not be executed to that byte location.

Block Write (BW)

The Block Write command is used to write a single data value to the block of eight consecutive column locations addressed by inputs A7 - A3 . The data is provided by the Color Register which must be loaded prior to the Block Write cycle by invoking LSMR cycle. If the two Color Register option is enabled, the address line A0 is used to select the desired Color Register. A “0” at A0 selects Color Register 0, a “1” Color Register 1. The input data on DQs which is registered coincident with the Block Write command is used to mask specific column/byte combinations within the block. The DQM signals operate the same way as for Write cycles, but are applied to all eight columns in the selected block.

Precharge (PRE)

The Precharge command is used to deactivate the open row in a particular bank or the open row in both banks. The bank(s) will be available for row access some specified time (t_{RP}) after the Precharge command is issued. Input A8 determines whether one or both banks are to be precharged, input BA selects the bank. If A8 is “1”, both banks are to be precharged and BA is “don't care.” Once a bank is precharged (or deactivated), it is in the idle state and must be activated prior to any Read, Write, or Block Write commands being issued to that bank.

Auto Precharge (PREA)

The Auto Precharge feature allows the user to issue a Read, Write, or Block Write command that automatically performs a precharge upon the completion of the Block Write access or Read or Write burst, except in the Full Page Burst mode, where it has no effect. The use of this feature eliminates the need to “manually” issue a Precharge command during the functional operation of the SGRAM.

Burst Terminate (BST)

The Burst Terminate command is used to truncate either fixed-length or Full Page Bursts.

Auto Refresh (REF)

Auto Refresh is used to refresh the various rows in the SGRAM and is analogous to CAS-before-RAS (CBR) in DRAMs. This command must be issued each time a refresh is required. The addressing is generated by the internal refresh counter, therefore, the address bits are “don't care” during a CBR cycle. The SGRAM requires that 2048 rows to be refreshed every 32 ms (t_{REF}). This refresh can be accomplished either by providing an Auto Refresh command every 15.6 µs or all 2048 Auto Refresh commands can be issued in a burst at the minimum cycle rate (t_{RC}) once every 32 ms.

Self Refresh (SREF)

The Self Refresh command can be used to retain data in the SGRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the SGRAM retains data without external clocking. Once the SREF command is registered, all the inputs to the SGRAM become “don't care” with the exception of CKE, which must remain low. Once SREF mode is engaged, the SGRAM provides its own internal clocking, causing it to perform its own Auto Refresh cycles. The SGRAM may remain in Self Refresh mode for an indefinite period. The procedure for exiting requires a sequence of commands. First, the system clock must be stable prior to CKE going high. Once CKE is high, the SGRAM must have NOP commands issued for t_{SRX}, because of the time required for the completion of any bank currently being internally refreshed.

Detailed Description of WRITE COMMANDS (WR, Masked Writes, Block Write)

Write Command (WR)

The following pages illustrate the Write operations for various cases.

Summary Write Commands

Mnemonic	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA	A8	Address Lines
WR	H	L	H	L	L	L	0	BA	L	Column
WRA	H	L	H	L	L	L	0	BA	H	Column
BW	H	L	H	L	L	H	0	BA	L	Column
BWA	H	L	H	L	L	H	0	BA	H	Column

Notes

1. Input data at DQ pins at Block Write command is registed as a column mask for that block of columns
2. Explanation of Mnemonics:
   WR: Write Command
   WRA: Write Command with Auto Precharge
   BW: Block Write
   BWA: Block Write with Auto Precharge
   BA: Bank Select

Write bursts are initiated with a Write command. The starting column and bank address is provided with the Write command, normal or Block Write is selected, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged automatically at the completion of the burst.

During Write bursts, the first valid data-in element will be registered coincident with the Write command. Sub-sequent data elements will be registered on successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z, and any additional data will be ignored. A full-page burst will continue until terminated (at the end of the page, it will wrap to column 0 and continue).

A fixed-length Write burst may be followed by, or truncated with a subsequent Write burst or Block Write command (provided that Auto Precharge was not activated) and a full page Write burst can be truncated with a subsequent Write burst or Block Write command. The new Write or Block Write command can be issued on any clock following the previous Write command, and the data provided coincident with the new command applies to the new command. To truncate a Block Write, the t_{BWC} parameter has to be met.

A fixed-length Write burst may be followed by, or truncated with a subsequent Read burst (provided that Auto Precharge was not activated) and a full-page Write burst can be truncated with a subsequent Read burst. Once the Read command is registered, the data inputs will be ignored, and writes will not be executed.

A fixed-length Write burst may be followed by, or truncated with a Precharge command to the same bank (provided that Auto Precharge was not activated) and a full-page Write burst may be truncated with a Precharge command to the same bank. The Precharge command should be issued x cycles (x = t_{WR}/t_{CK} rounded up to the next whole number) after the clock edge at which the last desired input data element is registered. In addition, the DQM signals must be used to mask input data, starting with the clock edge following the last desired data element and ending with the clock edge on which the Precharge command is entered. A Precharge command issued at the optimum time provides the same operation that would result from the same fixed-length Burst with Auto Precharge.

Disadvantages of Write Command with Auto Precharge

1. Back to back Read/Write bursts can not be initiated. The Read/Write command with Auto Precharge will automatically initiate a precharge of the row in the selected bank. Most of the applications require subsequent Read/Write bursts in the same page.
2. The Auto Precharge command does not allow truncation of fixed-length bursts. It also does not apply to Full Page bursts.

Terminating a Write Burst

The fixed-length or Full-Page Write bursts can be truncated with the Burst Terminate command. When truncating a Write burst, the input data applied one clock edge prior to the Burst Terminate command will be the last data written.

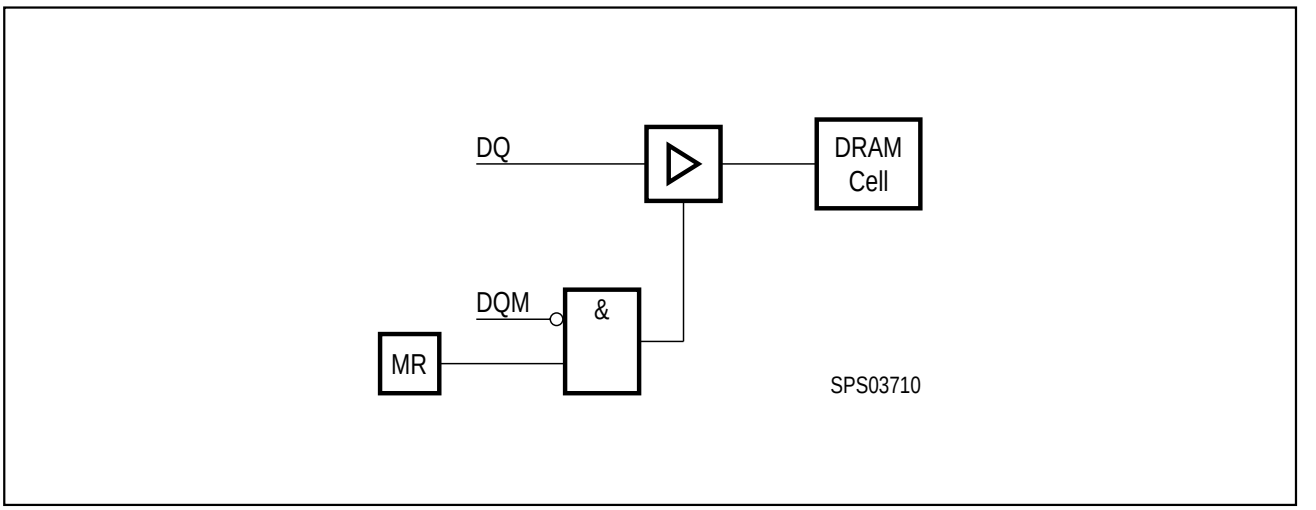
Masked Writes

Any Write performed to a row that was activated via an Active with WPB command is a Write-per-Bit-Mask (WPBM). Data is written to the 32 cells at the selected column location subject to the mask stored in the WPB mask register. The data to be written in the DRAM cell will be according to the following mask:

Write Masking Function Representation

DQM	MR	DRAM Cell
0	0	Mask
1	0	Mask
1	1	Mask
0	1	Write

Symbolic Representation of Write Masking Function



If a particular bit in the WPB mask register is a “0”, the data appearing on the corresponding DQ input will be ignored, and the existing data in the corresponding DRAM cell will remain unchanged. If a mask data is a “1”, the data appearing on the corresponding DQ input will be written to the corresponding DRAM cell. The overall Write mask consists of a combination of the DQM inputs, which will mask on a per-byte basis, and the WPB mask register, which masks on a per-bit basis.

If a particular DQM signal was registered high, the corresponding byte will be masked. A given bit is written if the corresponding DQM signal registered is “0”and the corresponding WPB mask register bit is “1”.

Note that the DQM Latency for Write is zero.

Block Write (BW)

Each Block Write cycle writes a single data value from a Color Register to the block of eight consecutive column locations addressed by A7 - A3. If Single Color Register Mode is enabled, the content of Color Register 0 is written. If both Color Registers are enabled, address pin A0 selects the desired Color Register. Address A0 = 0 selects Color Register 0, address pin A0 = 1 Color Register 1. The information on the DQs which is registered coincident with the Block Write command is used to mask specific column/byte combinations within the block.

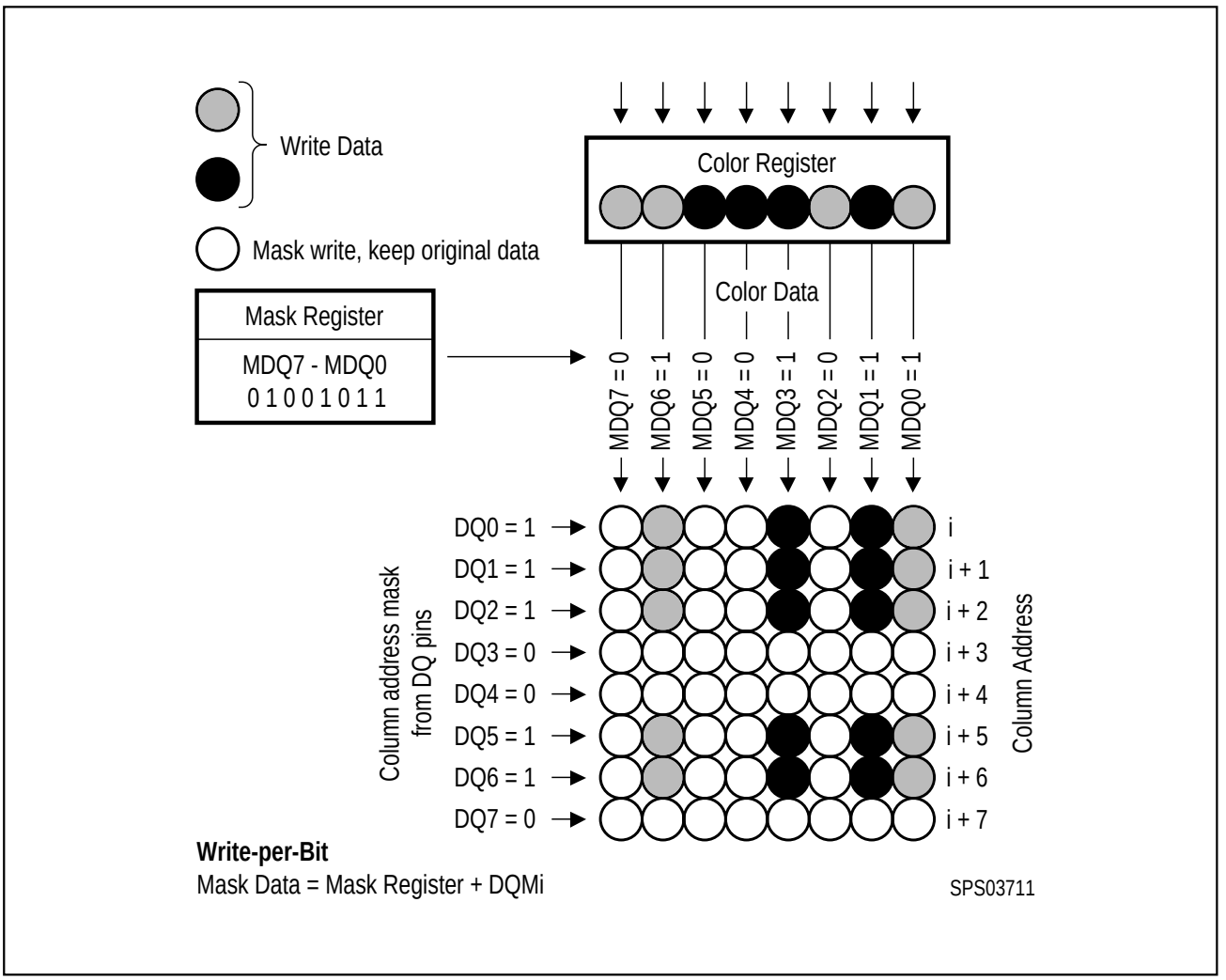
Bit Mask mapping of DQ bits

Address within Written Block	Byte within Data Word			
	Byte 3	**Byte 2**	**Byte 1**	**Byte 0**
0	DQ24	DQ16	DQ8	DQ0
1	DQ25	DQ17	DQ9	DQ1
2	DQ26	DQ18	DQ10	DQ2
3	DQ27	DQ19	DQ11	DQ3
4	DQ28	DQ20	DQ12	DQ4
5	DQ29	DQ21	DQ13	DQ5
6	DQ30	DQ22	DQ14	DQ6
7	DQ31	DQ23	DQ15	DQ7

The table shows the masking of data caused by the registered value on the DQ pins, when data is transfered from Color Register to the 8 succeeding memory locations addressed in the Write Block command.
When a “1” is registered, the Color Register data will be written to the corresponding DRAM cells, subject to the DQM and the WPB masking. The overall Block Write mask consists of a combination of the DQM signals, the WPB mask register and the column/byte mask information.

Block Write Timing Considerations

A Block Write access requires a time period of t_{BWC} to execute, so in general, the cycle after the Block Write command should be a NOP. However, Active or Precharge commands to the other bank are allowed. When following a Block Write with a Precharge command to the same bank, t_{BPL} must be met.



Block Write Illustration

Note: Only single Color Register and Byte 0 of Color Register is used in this example.

Electrical Characteristics

Absolute Maximum Ratings

Operating temperature range .....0 to + 70 °C
Storage temperature range..... – 55 to + 150 °C
Input/output voltage ..... – 0.3 to V_{DD} + 0.3 V
Power supply voltage V_{DD}/V_{DDQ}..... – 0.3 to + 4.6 V
Power Dissipation ..... 1 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operation and DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; $V_{DD,}V_{DDQ}$ = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input low voltage	V_{IL}	– 0.3	0.8	V	1, 2
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V	
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 5	5	µA	
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{DD})	$I_{O(L)}$	– 5	5	µA	

Notes

1. All voltages are referenced to V_{SS}
2. V_{IH} may overshoot to V_{DD} + 2.0 V for pulse width of < 4 ns with 3.3 V. V_{IL} may undershoot to –2.0 V for pulse width < 4 ns with 3.3 V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	max. Values	Unit
Input capacitance (A0 to A9, BA)	C_{I1}	4	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CLK, CKE, DQM, DSF)	C_{I2}	4	pF
Output capacitance (DQ)	C_{IO}	6	pF

Operating Currents

T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.3 V
(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition		Symb.	-6	-7	-8	Unit	Note
				max.			
Operating current $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	$t_{RC} \geq t_{RC(MIN.)}$, $t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA	I_{CC1}	 200 180	 200 180	 180 170	mA	2
Precharge standby current in Power Down Mode	CKE ≤ $V_{IL(MAX.)}$ $t_{CK} = t_{CK(MIN.)}$ CKE ≤ $V_{IL(MAX.)}$, t_{CK} = infinite	I_{CC2P} I_{CC2PS}	3 2	3 2	3 2	mA	2
Precharge standby current in Non Power Down Mode	CKE ≥ $V_{IH(MIN.)}$ $t_{CK} \geq t_{CK(MIN.)}$, input changed once in 30 ns CKE ≥ $V_{IH(MIN.)}$, t_{CK} = infinite, no input change	I_{CC2N} I_{CC2NS}	60 15	60 15	60 15	mA mA	2
Active standby current in Power Down Mode	CKE ≤ $V_{IL(MAX.)}$, $t_{CK} \geq t_{CK(MIN.)}$ CKE ≤ $V_{IL(MAX.)}$, t_{CK} = infinite	I_{CC3P} I_{CC3PS}	3 3	3 3	3 3	mA mA	
Active standby current in Non-Power Down Mode	CKE ≥ $V_{IH(MIN.)}$, $t_{CK} \geq t_{CK(MIN.)}$ input changed every 30 ns CKE ≥ $V_{IH(MIN.)}$, t_{CK} = infinite, no input change	I_{CC3N} I_{CC3NS}	90 30	90 30	90 25	mA mA	
Burst Operating Current $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	Burst Length = full page t_{RC} = infinite $t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA, 2 banks interleave	I_{CC4}	 200 200	 200 200	 190 190	 mA mA	2, 3
Auto (CBR) Refresh Current $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	$t_{RC} \geq t_{RC(MIN.)}$	I_{CC5}	 170 160	 170 160	 160 160	 mA	2
Self Refresh Current	CKE ≤ 0,2 V		2	2	2	mA	
Operating Current (Block Write)	$t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA $t_{BWC} = t_{BWC(MIN.)}$		200	200	190	mA	

Notes

1. All values are preliminary and subject to future change
2. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}.
3. These parameters depend on output loading. Specified values are obtained with output open.

AC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symb.	Limit Values						Unit	Note
		-6		-7		-8			
		min.	max.	min.	max.	min.	max.		
Clock and Clock Enable									
Clock Cycle Time									
$\overline{CAS}$ Latency = 3	t_{CK3}	6	–	7	–	8	–	ns	
$\overline{CAS}$ Latency = 2	t_{CK2}	8	–	8	–	10	–	ns	
System frequency									
$\overline{CAS}$ Latency = 3	–	–	166	–	143	–	125	MHz	
$\overline{CAS}$ Latency = 2	–	–	125	–	125	–	100	MHz	
Clock Access time (for 30 pF load)									
$\overline{CAS}$ Latency = 3	t_{AC3}	–	5.5	–	5.5	–	6	ns	2
$\overline{CAS}$ Latency = 2	t_{AC2}	–	5.5	–	5.5	–	6	ns	2
Clock High Pulse width	t_{CH}	2.5	–	3	–	3	–	ns	
Clock Low Pulse width	t_{CL}	2.5	–	2.5	–	3	–	ns	
CKE Setup time	t_{CKS}	2	–	2	–	2.5	–	ns	
CKE Hold time	t_{CKH}	1	–	1	–	1	–	ns	
Transition time (rise and fall)	t_T	0.5	10	0.5	10	0.5	10	ns	
Common Parameters									
Command Setup time	t_{CS}	2	–	2	–	2.5	–	ns	3
Command Hold time	t_{CH}	1	–	1	–	1	–	ns	
Address Setup time	t_{AS}	2	–	2	–	2.5	–	ns	3
Address Hold time	t_{AH}	1	–	1	–	1	–	ns	
Active to Read or Write delay	t_{RCD}	18	–	21	–	24	–	ns	4
Cycle time	t_{RC}	66	–	70	–	80	–	ns	4
Active to Precharge command period	t_{RAS}	48	100k	49	100k	56	100k	ns	4
Row Precharge time	t_{RP}	18	–	21	–	24	–	ns	4
Active Bank A to Active Bank B command period	t_{RRD}	12	–	14	–	16	–	ns	4
$\overline{CAS}$ to $\overline{CAS}$ delay time (same bank)	t_{CCD}	1	–	1	–	1	–	CLK	

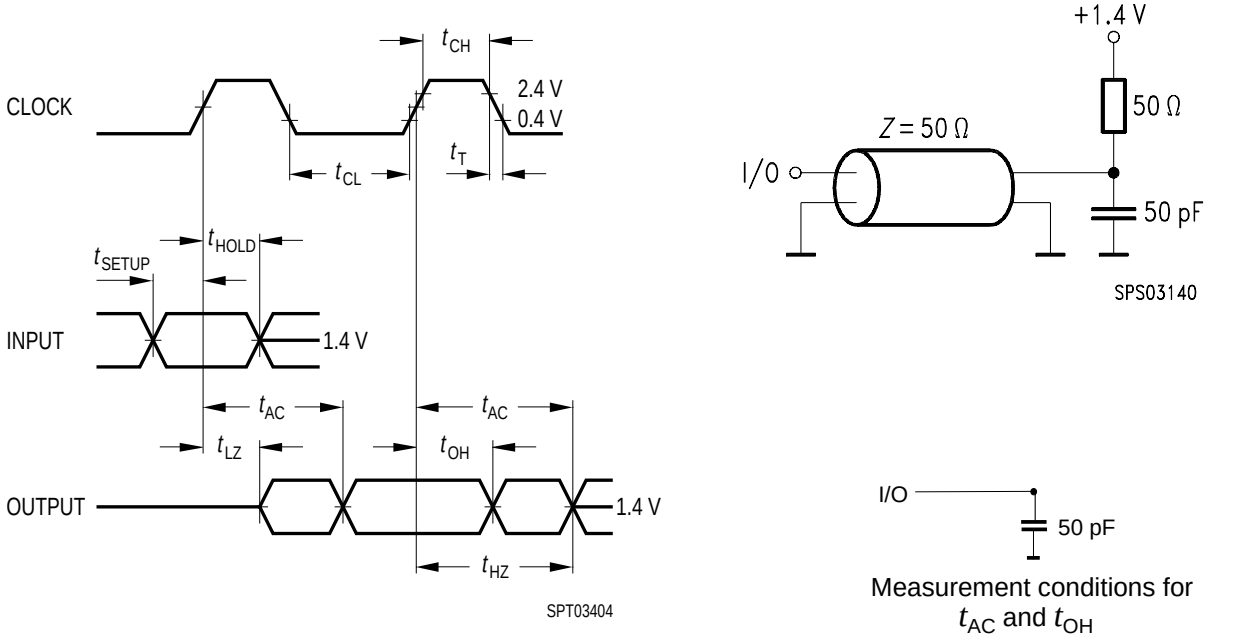
AC Characteristics (cont'd)

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symb.	Limit Values						Unit	Note
		-6		-7		-8			
		min.	max.	min.	max.	min.	max.		
Refresh Cycle									
Self Refresh Exit time	t_{SREX}	2	–	2	–	2	–	CLK	5
Total Self Refresh Exit time	–			2 CLKs + t_{RC}				–	5
Refresh Period for Non-Self Refresh	t_{REF}	–	32	–	32	–	32	ms	6
Read Cycle									
Data Out Hold time	t_{OH}	2.5	–	2.5	–	3	–	ns	
Data Out to Low Impedance time	t_{LZ}	0	–	0	–	0	–	ns	
Data Out to High Impedance time	t_{HZ}	3	8	3	8	3	8	ns	7
Write Cycle									
Data In Setup time	t_{DS}	3	–	2	–	2.5	–	ns	
Data In Hold time	t_{DH}	1	–	1	–	1	–	ns	
Write recovery time	t_{WR}	6	–	7	–	8	–	ns	
Block Write Cycle									
Block Write Cycle Time	t_{BWC}	12	–	14	–	16	–	ns	
Block Write to Precharge delay	t_{BWR}	12	–	14	–	16	–	ns	
Miscellaneous									
Mode Register command to command	t_{RSC}	2	–	2	–	2	–	CLK	

Notes

1. AC timing tests have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown.



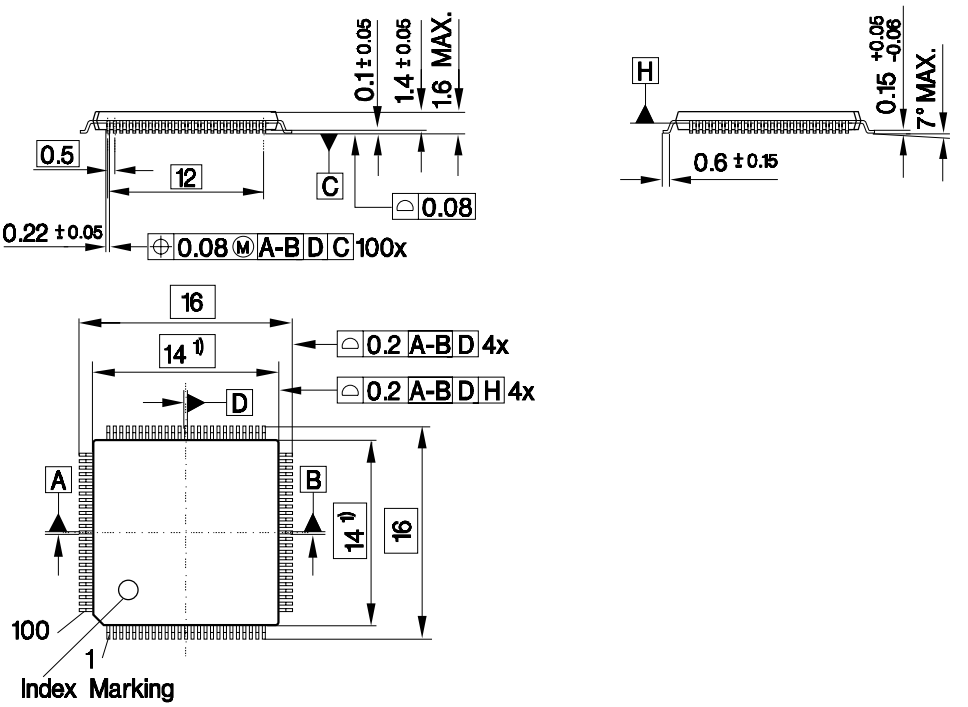
2. If clock rising time is longer than 1ns, a time (t_T/2 – 0.5) ns has to be added to this parameter.
3. If t_T is longer than 1 ns, a time (t_T – 1) ns has to be added to this parameter.
4. These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows: Number of clock cycle = specified value of timing period (counted in fractions as a whole number)
5. Self Refresh Exit is a synchronous operation and begins on the second positiv edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
6. Any time that the refresh Period has been exceeded, a minimum of two Auto (CRB) Refresh commands must be given to “wake-up“ the device.
7. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

Clock Frequency and Latency

Parameter		Symbol	Speed Sort					Unit
			-6		-7		-8	
Clock Frequency	max.	–	166	125	143	125	125	MHz
Clock Cycle time	min.	t_{CK}	6	8	7	8	8	ns
$\overline{CAS}$ Latency	min.	t_{AA}	3	2	3	2	3	CLK
$\overline{RAS}$ to $\overline{CAS}$ delay	min.	t_{RCD}	3	3	3	3	3	CLK
Bank Active Cycle time	min.	t_{RAS}	8	6	7	6	7	CLK
Bank Active Cycle time	max.	t_{RAS}	100	100	100	100	100	µs
Precharge time	min.	t_{RP}	3	3	3	3	3	CLK
Bank Cycle time	min.	t_{RC}	11	9	10	9	10	CLK
Last Data In to Precharge	min.	t_{WR}	1	1	1	1	1	CLK
Last Data In to Active/Refresh	min.	$t_{WR} + t_{RP}$	4	4	4	4	4	CLK
Bank to Bank delay time	min.	t_{RRD}	2	2	2	2	2	CLK
$\overline{CAS}$ to $\overline{CAS}$ delay time	min.	t_{CCD}	1	1	1	1	1	CLK
Write Latency	fixed	t_{WL}	0	0	0	0	0	CLK
DQM Write Mask Latency	fixed	t_{DQW}	0	0	0	0	0	CLK
DQM Data Disable Latency	fixed	t_{DQZ}	2	2	2	2	2	CLK
Clock Suspend Latency	fixed	t_{CSL}	1	1	1	1	1	CLK
Block Write Cycle time	fixed	t_{BWC}	2	2	2	2	2	CLK

Package Outlines

Plastic Package, P-TQFP-100
(20×14 mm^2, 0.65 mm lead pitch)
Thin Small Outline Package, SMD



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Timing Diagrams

1 Bank Activate Command Cycle

2 Burst Read Operation

3 Read Interrupted by a Read

4 Read to Write Interval
4.1 Read to Write Interval
4.2 Minimum Read to Write Interval
4.3 Non-Minimum Read to Write Interval
4.4 Single Bit Write Cycle

5 Burst Write Operation
5.1 Burst Write
5.2 Load Mode Register and Block Write Cycle
5.3 Read and DQM Function
5.4 Write and DQM Function

6 Write and Read Interrupt
6.1 Write Interrupted by a Write
6.2 Write Interrupted by a Read

7 Burst Write and Read with Auto Precharge
7.1 Burst Write with Auto Precharge
7.2 Burst Read with Auto Precharge

8 Burst Termination
8.1 Termination of a Full Page Burst Read Operation
8.2 Termination of a Full Page Burst Write Operation

9 AC Parameters
9.1 AC Parameters for Write Timing
9.2 AC Parameters for Read Timing

10 Mode Register Set

11 Power on Sequence and Auto Refresh (CBR)

12 Clock Suspension (Using CKE)
12.1 Clock Suspension During Burst Read $\overline{\text{CAS}}$ Latency = 2
12.2 Clock Suspension During Burst Read $\overline{\text{CAS}}$ Latency = 3
12.3 Clock Suspension During Burst Write $\overline{\text{CAS}}$ Latency = 2
12.4 Clock Suspension During Burst Write $\overline{\text{CAS}}$ Latency = 3

13 Power Down Mode and Clock Suspend

14 Self Refresh (Entry and Exit)

Timing Diagrams (cont'd)

15 Auto Refresh (CBR)

16 Random Column Read (Page within same Bank)
16.1 $\overline{CAS}$ Latency = 2
16.2 $\overline{CAS}$ Latency = 3

17 Random Column Write (Page within same Bank)
17.1 $\overline{CAS}$ Latency = 2
17.2 $\overline{CAS}$ Latency = 3

18 Random Row Read (Interleaving Banks) with Precharge
18.1 $\overline{CAS}$ Latency = 2
18.2 $\overline{CAS}$ Latency = 3

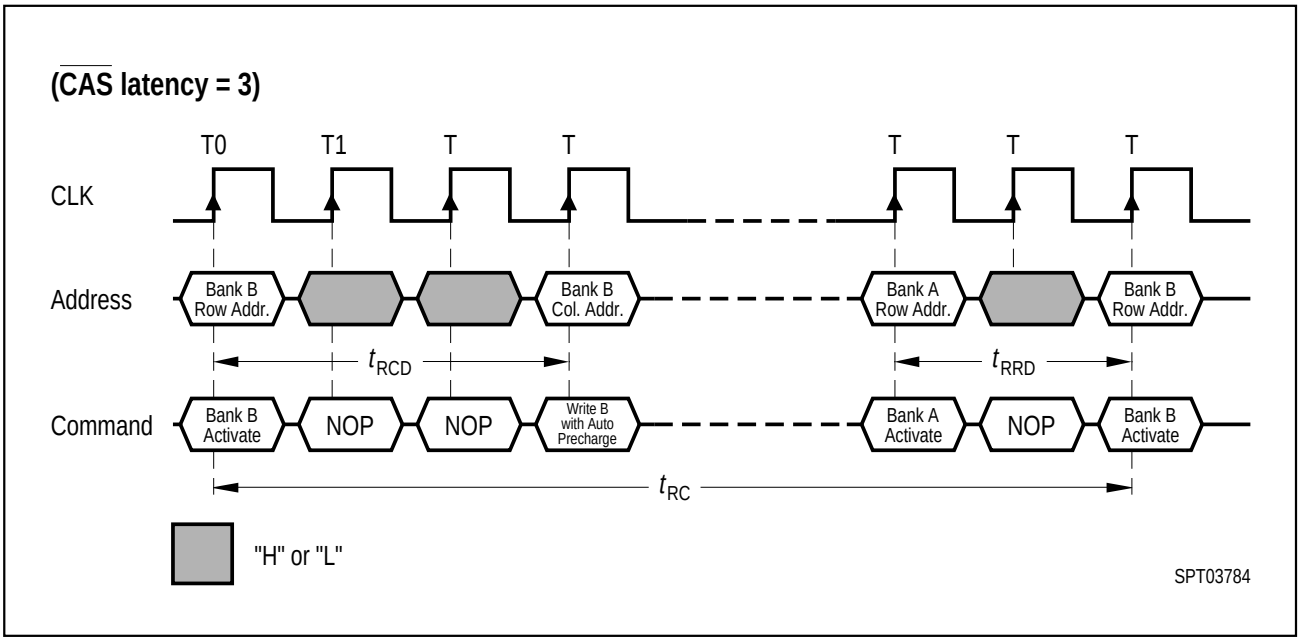
19 Random Row Write (Interleaving Banks) with Precharge
19.1 $\overline{CAS}$ Latency = 2
19.2 $\overline{CAS}$ Latency = 3

20 Full Page Read Cycle
20.1 $\overline{CAS}$ Latency = 2
20.2 $\overline{CAS}$ Latency = 3

21 Full Page Write Cycle
21.1 $\overline{CAS}$ Latency = 2
21.2 $\overline{CAS}$ Latency = 3

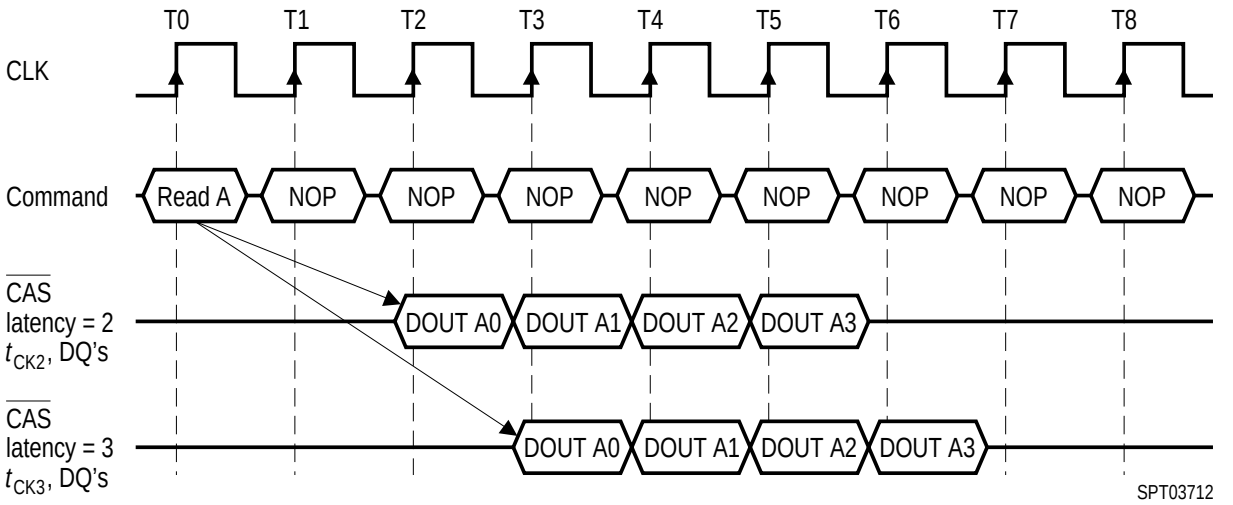
22 Precharge Termination of a Burst
22.1 $\overline{CAS}$ Latency = 2

1. Bank Activate Command Cycle

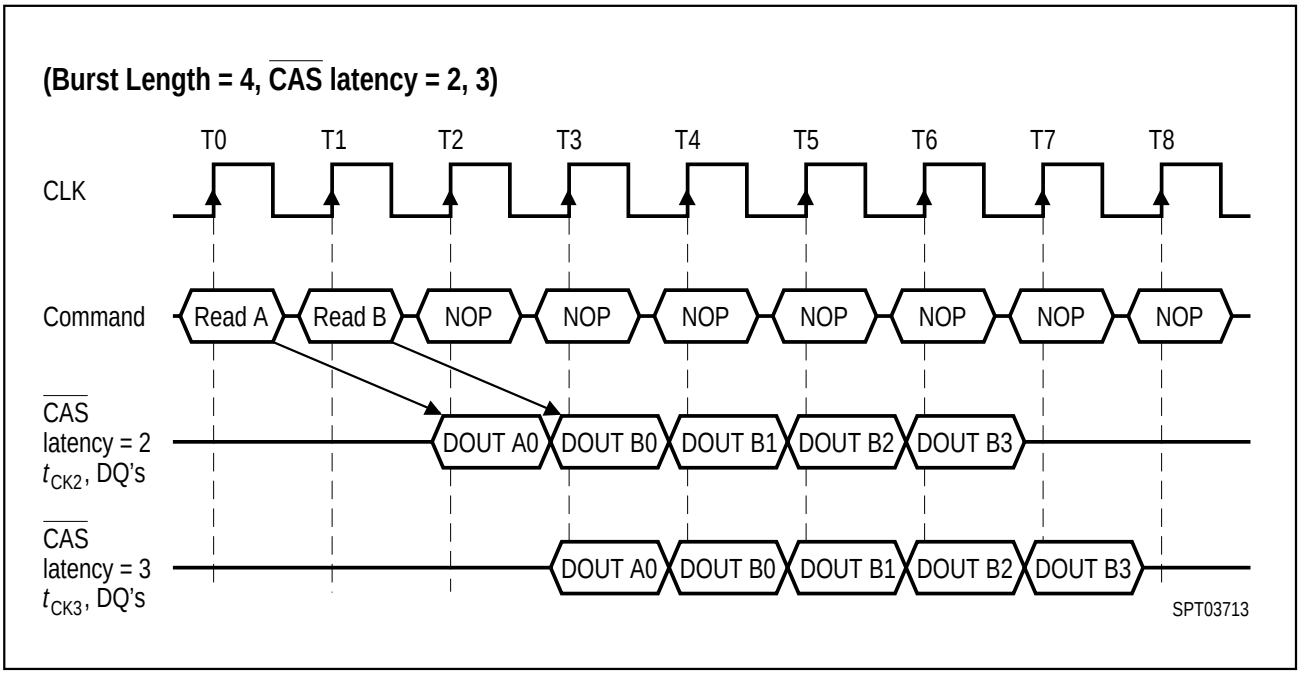


2. Burst Read Operation

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)

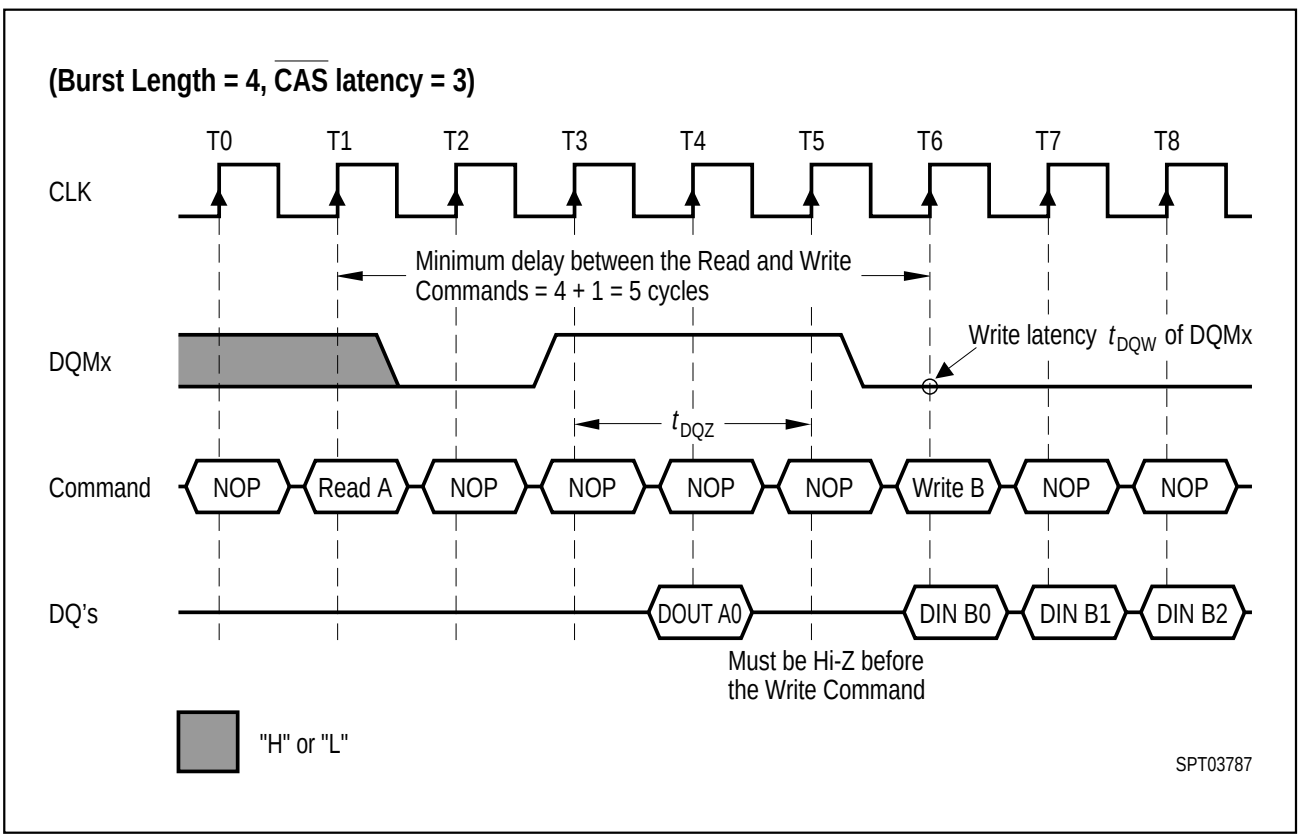


3. Read Interrupted by a Read

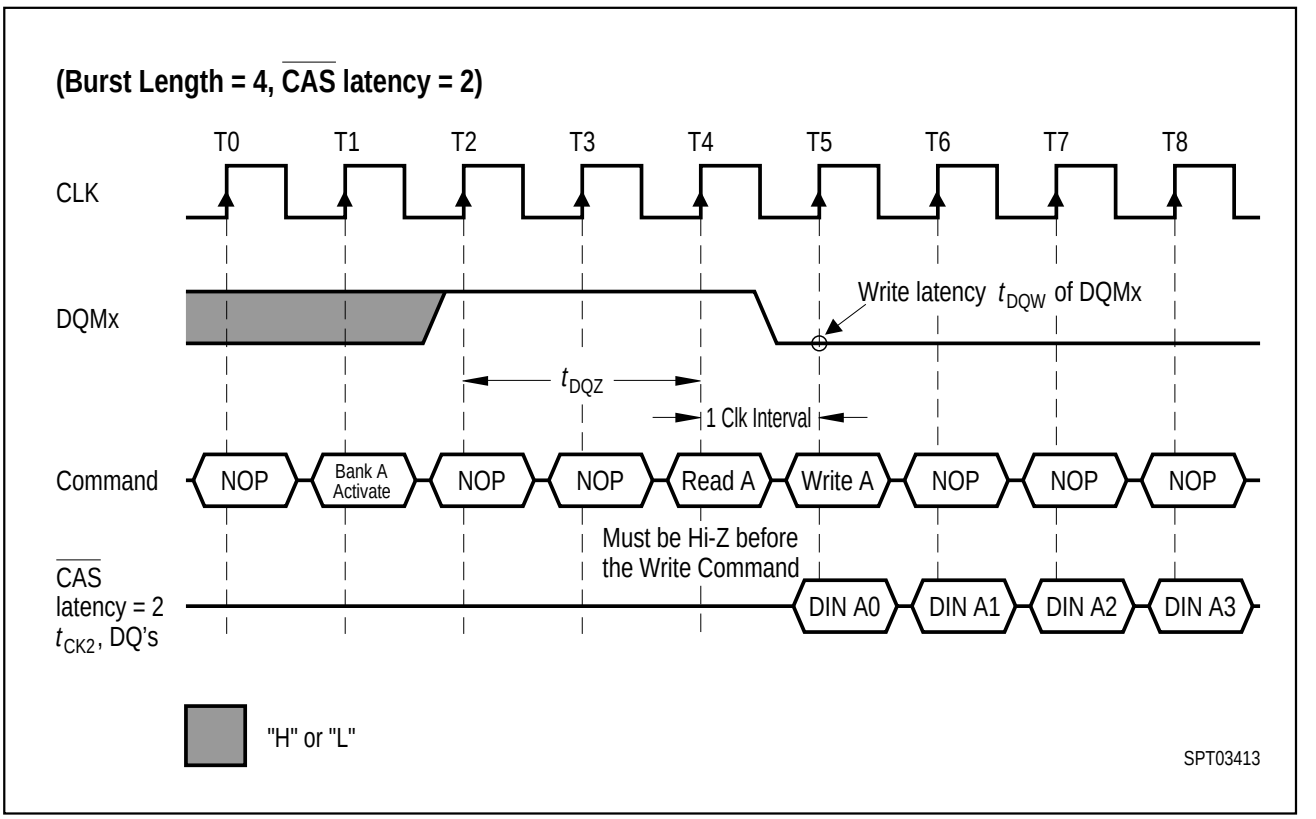


4. Read to Write Interval

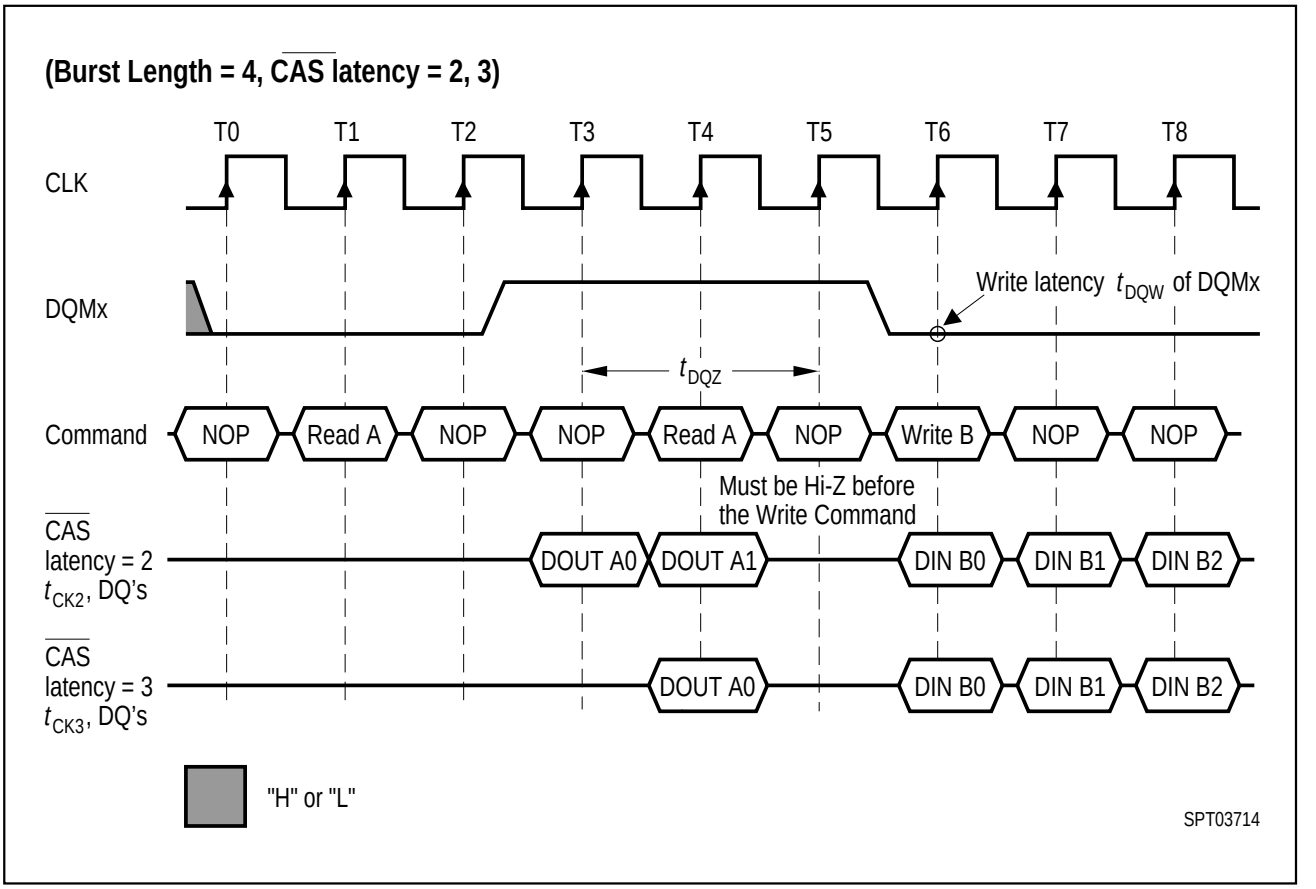
4.1. Read to Write Interval



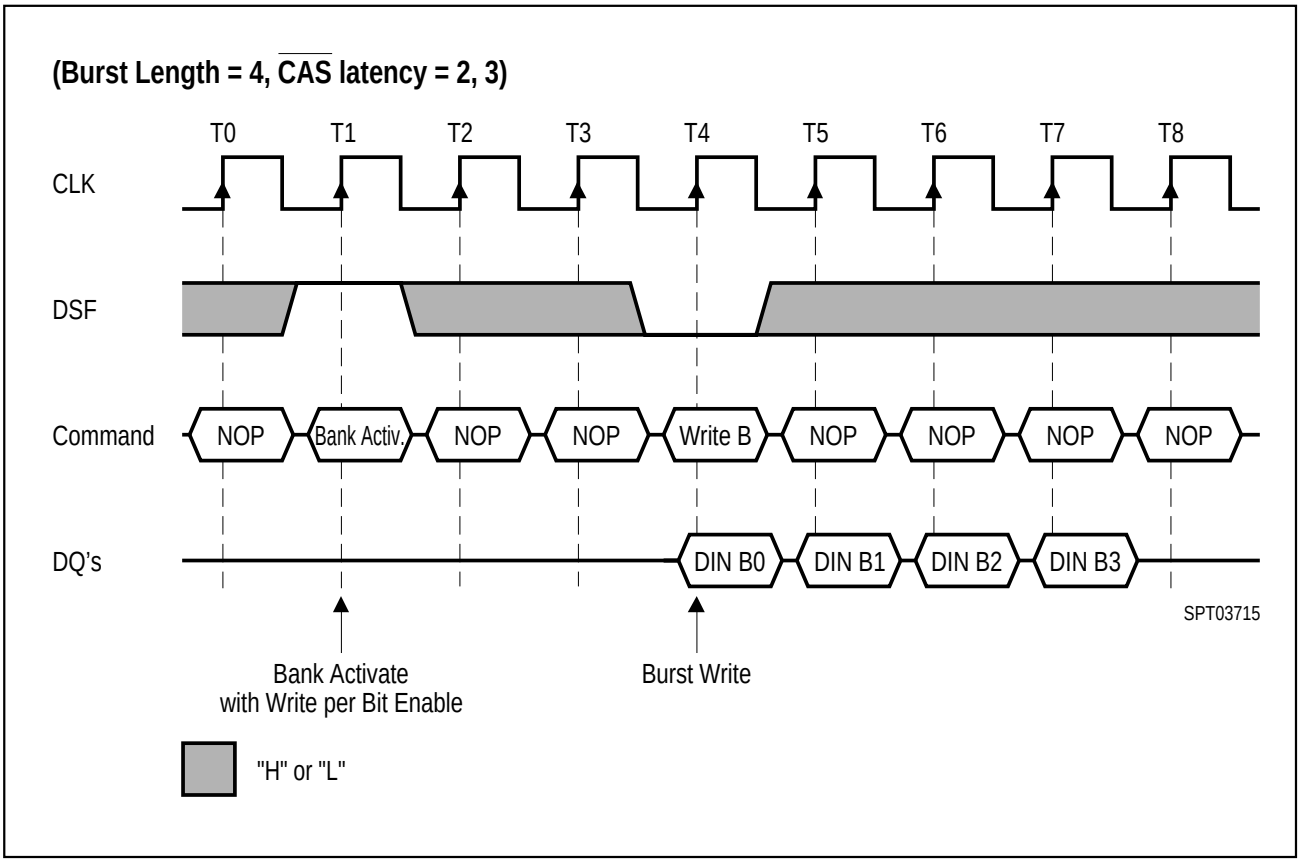
4.2. Minimum Read to Write Interval



4.3. Non-Minimum Read to Write Interval



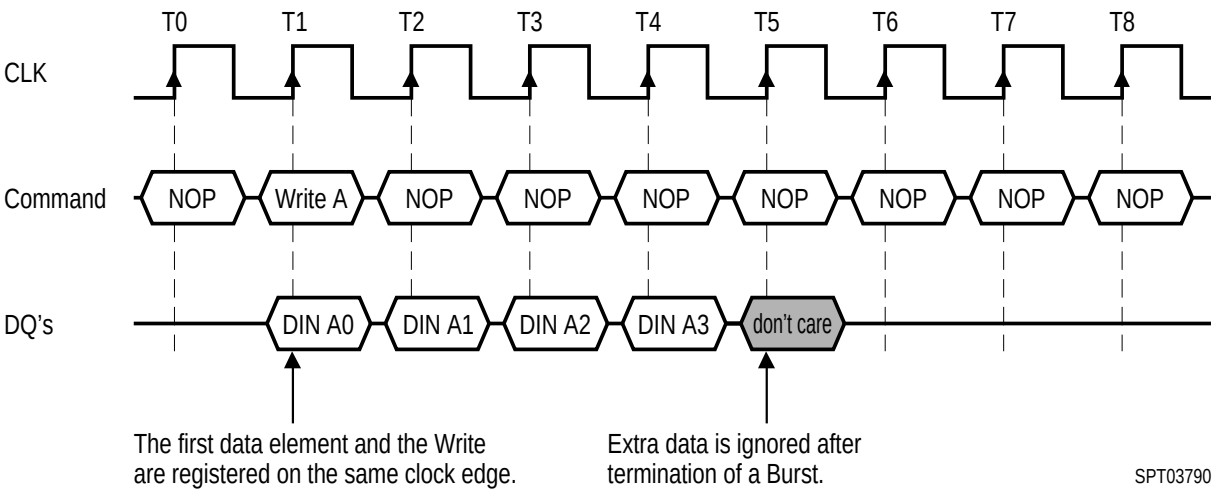
4.4. Single Bit Write Cycle



5. Burst Write Operation

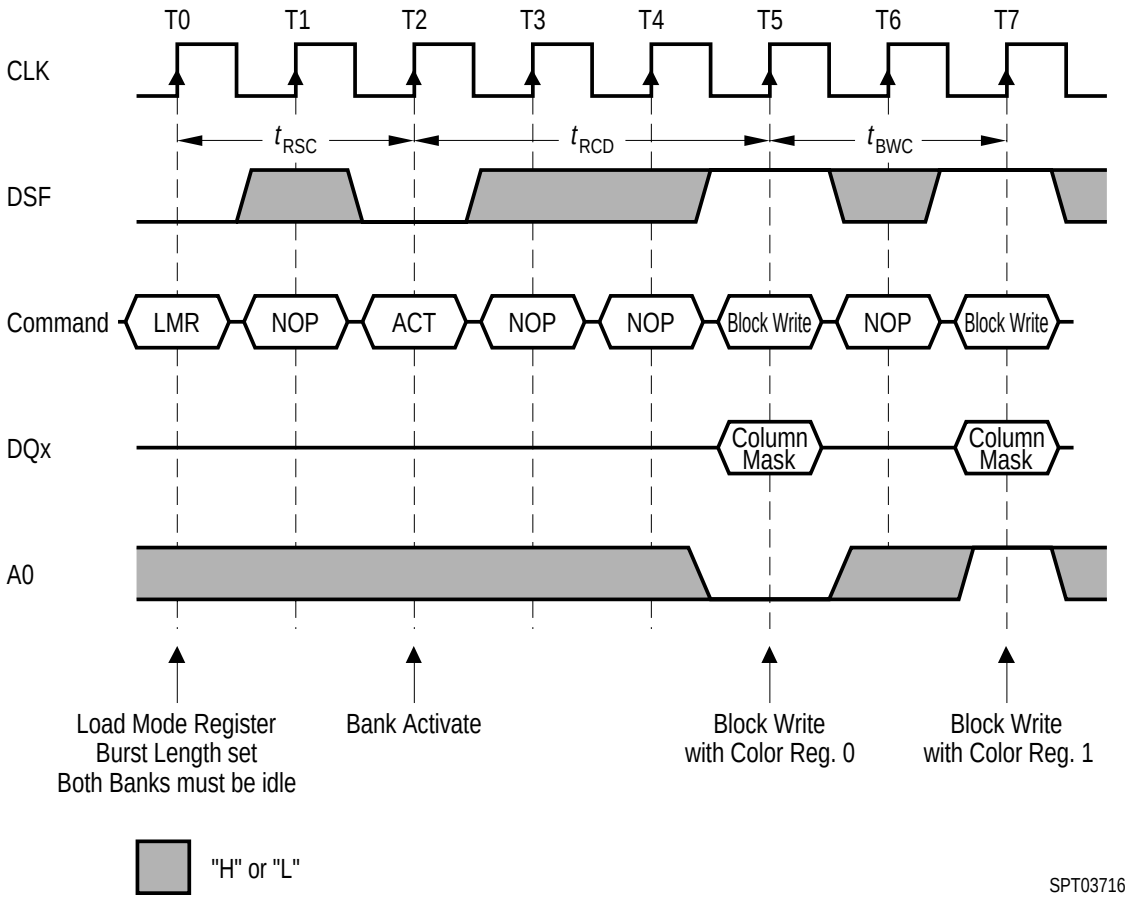
5.1. Burst Write

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)



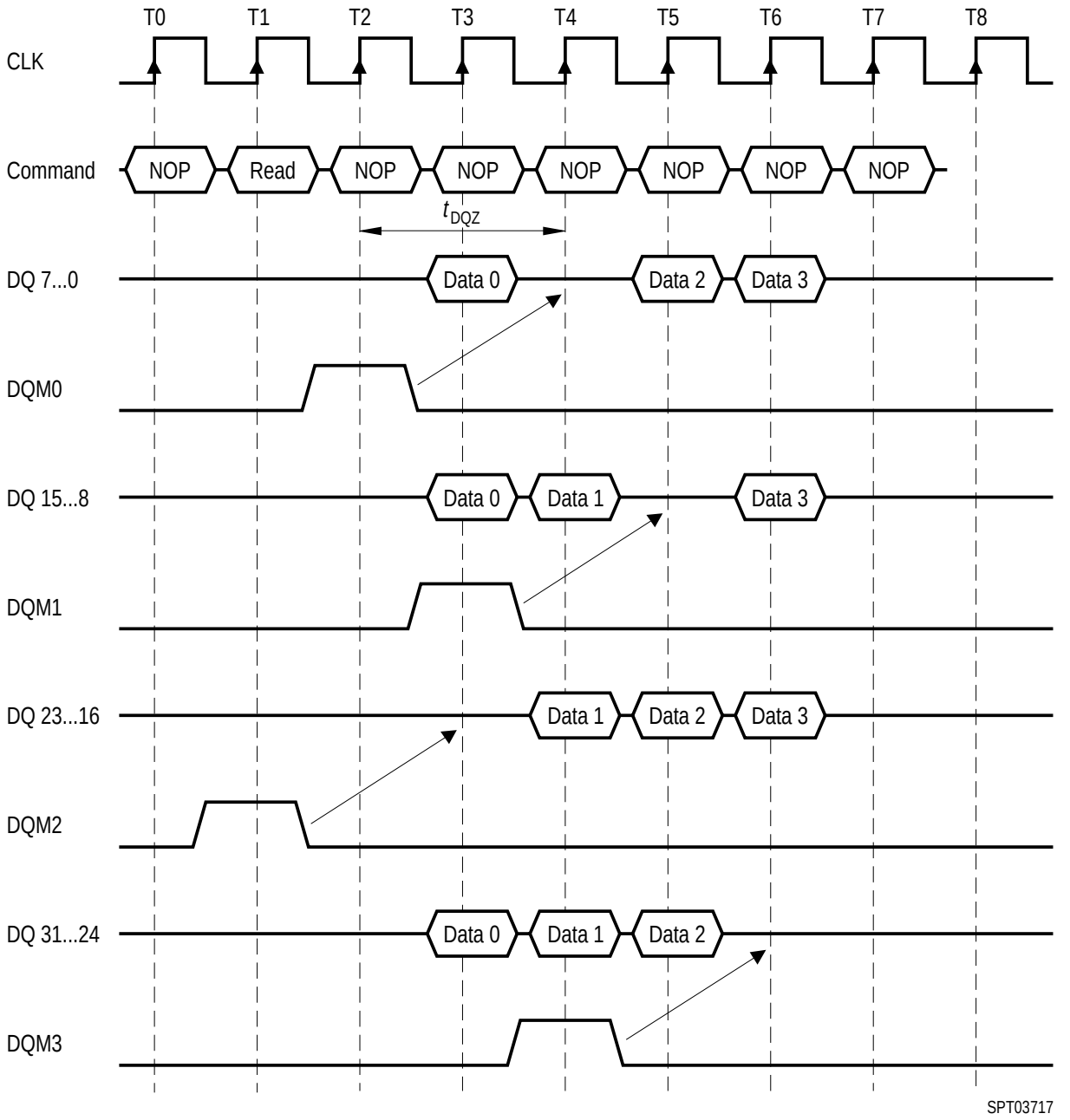
5.2. Load Mode Register and Block Write Cycle

(Burst Length = 8, $\overline{\text{CAS}}$ latency = 2, 3)

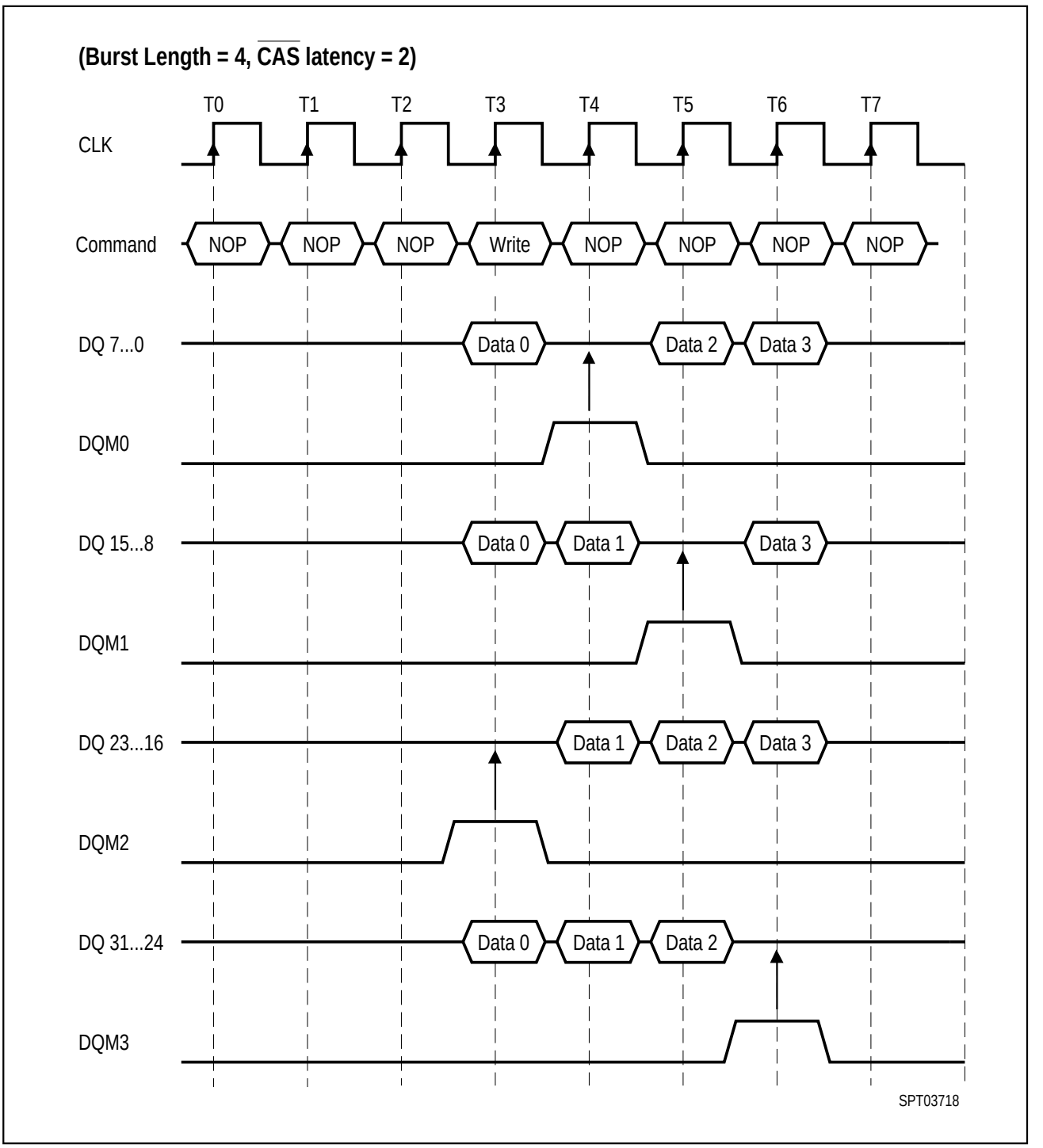


5.3. Read and DQM Function

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2)



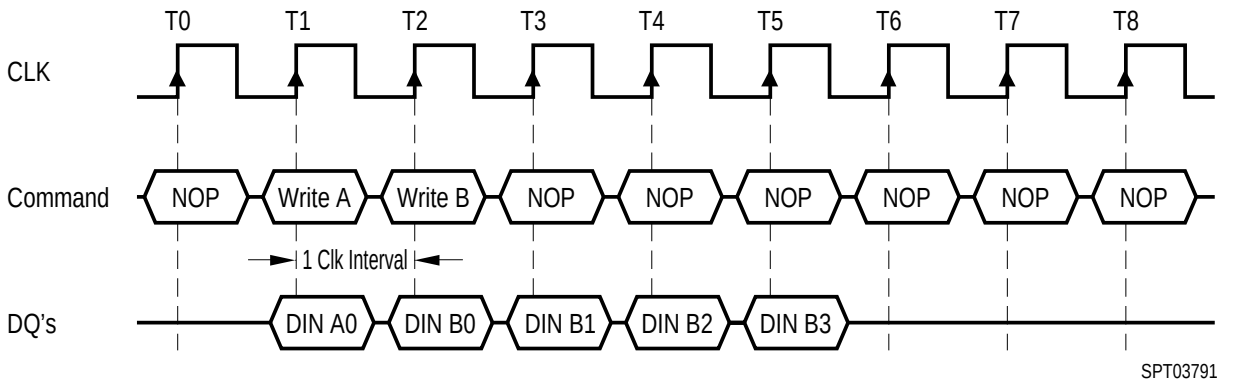
5.4. Write and DQM Function



6. Write and Read Interrupt

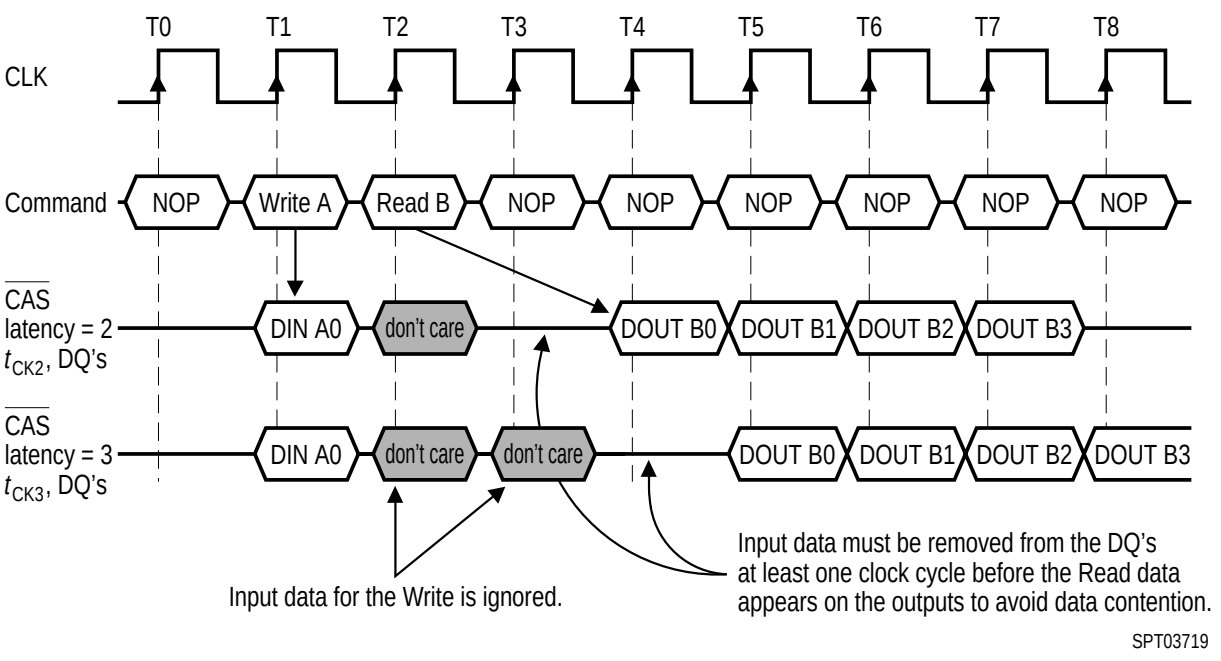
6.1. Write Interrupted by a Write

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)



6.2. Write Interrupted by a Read

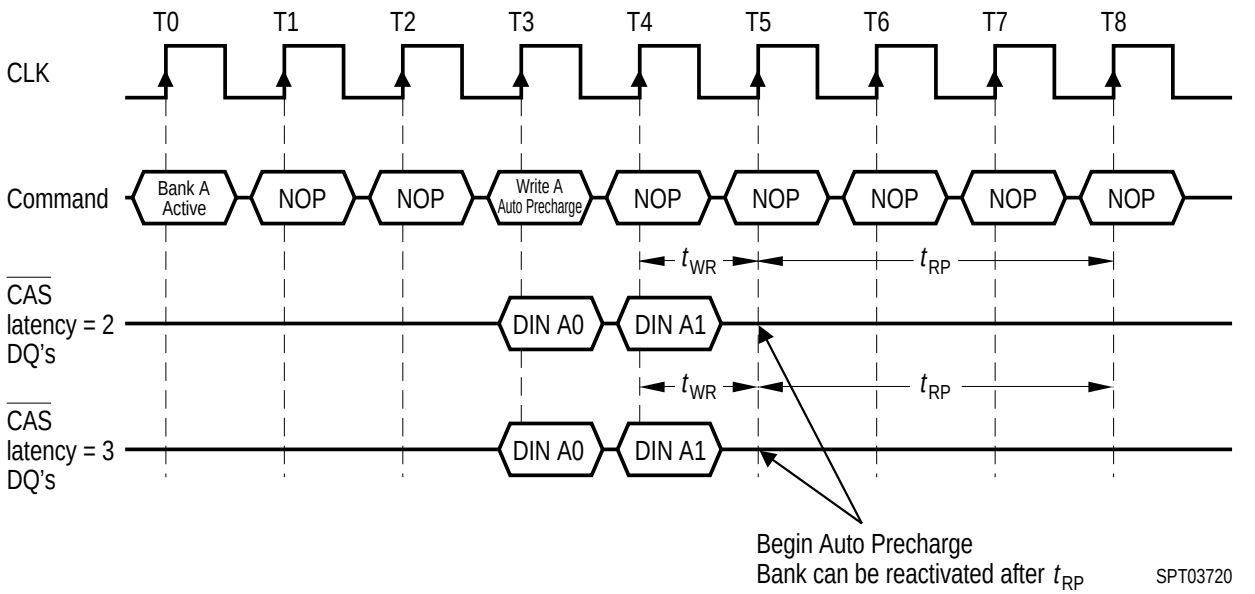
(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)



7. Burst Write and Read with Auto Precharge

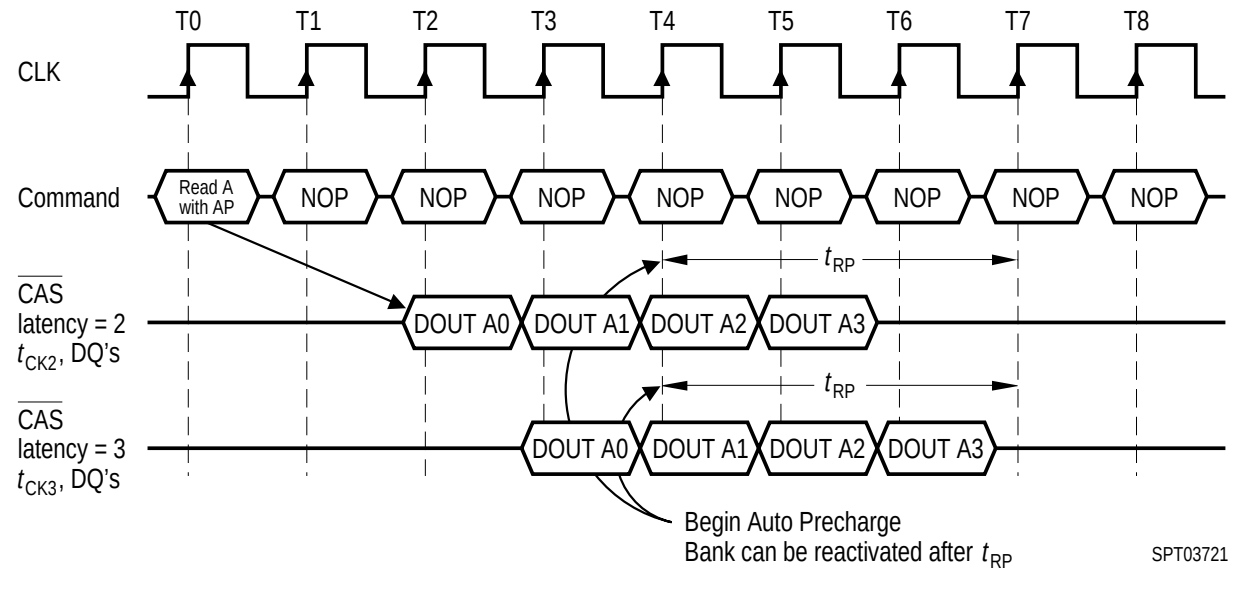
7.1. Burst Write with Auto Precharge

(Burst Length = 2, $\overline{\text{CAS}}$ latency = 2, 3)



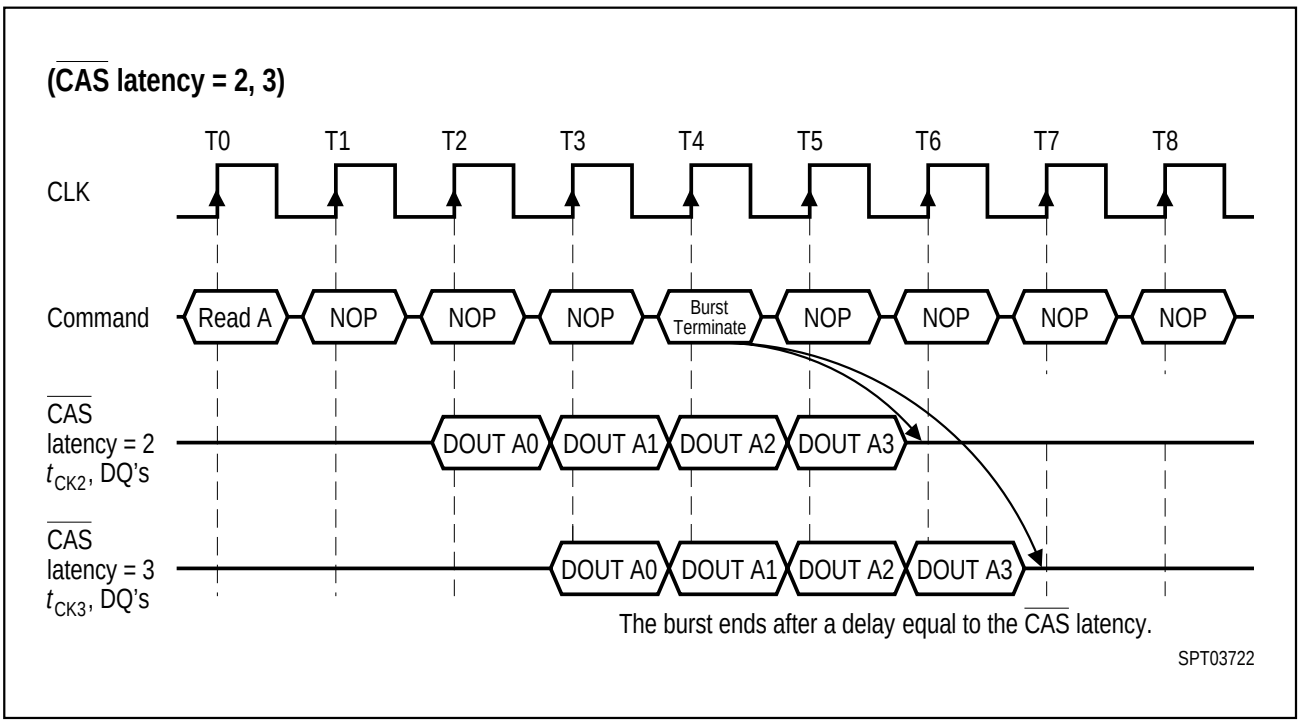
7.2. Burst Read with Auto Precharge

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)

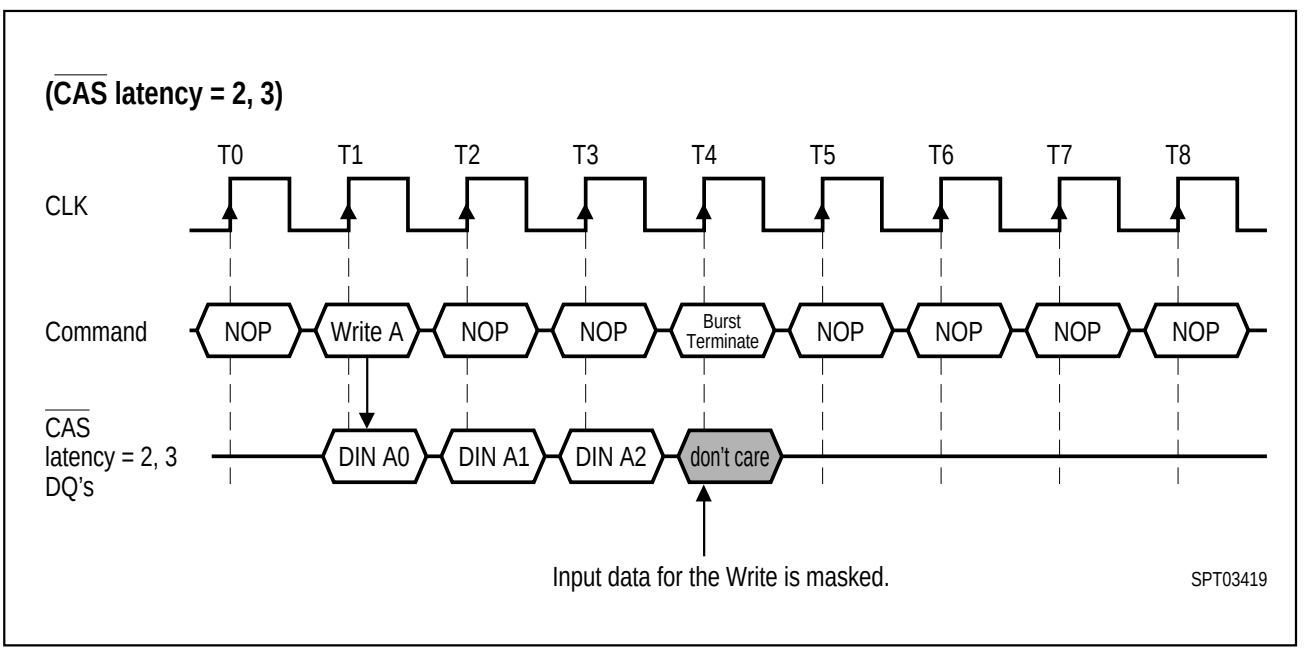


8. Burst Termination

8.1. Termination of a Full Page Burst Read Operation

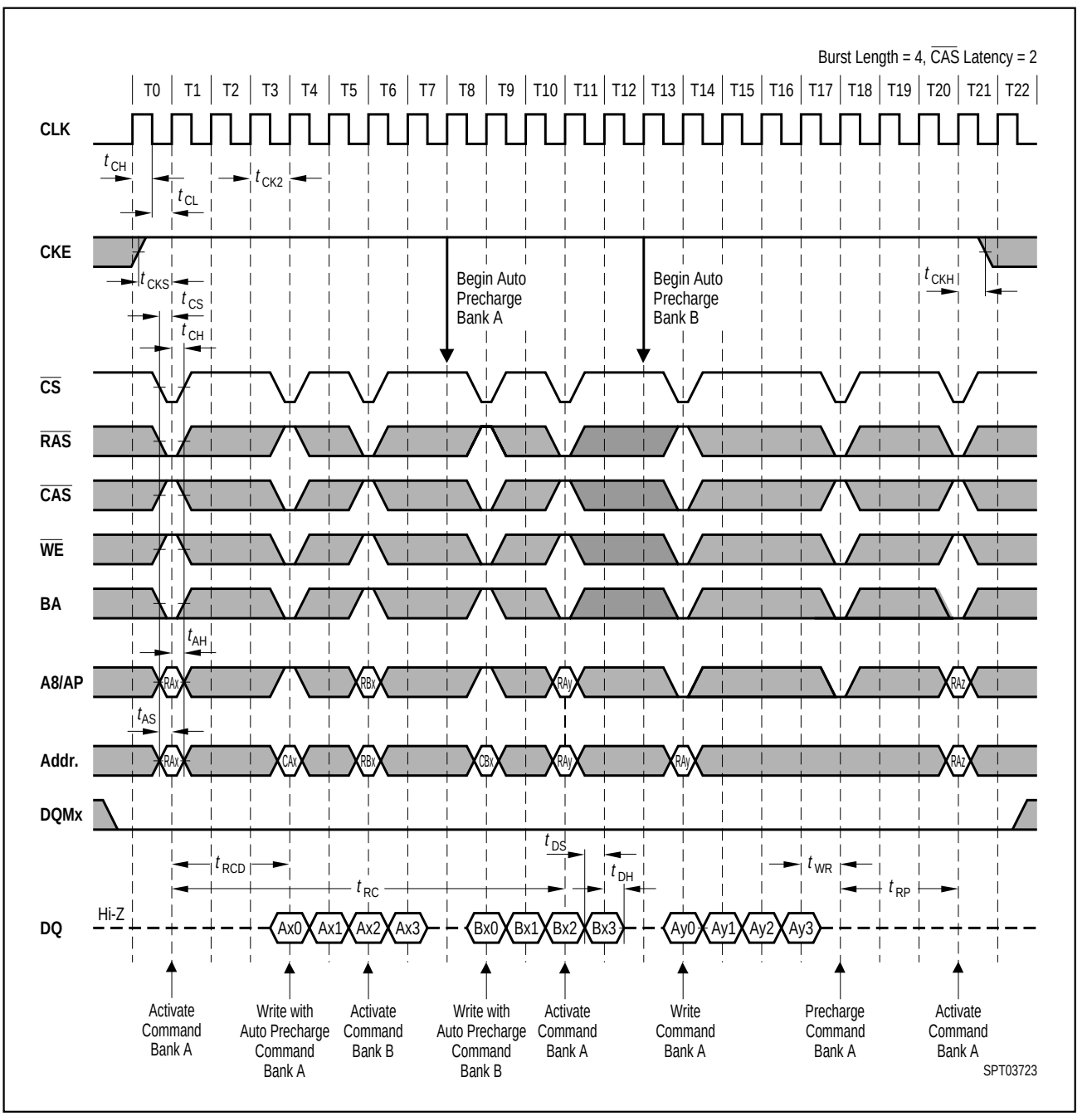


8.2. Termination of a Full Page Burst Write Operation

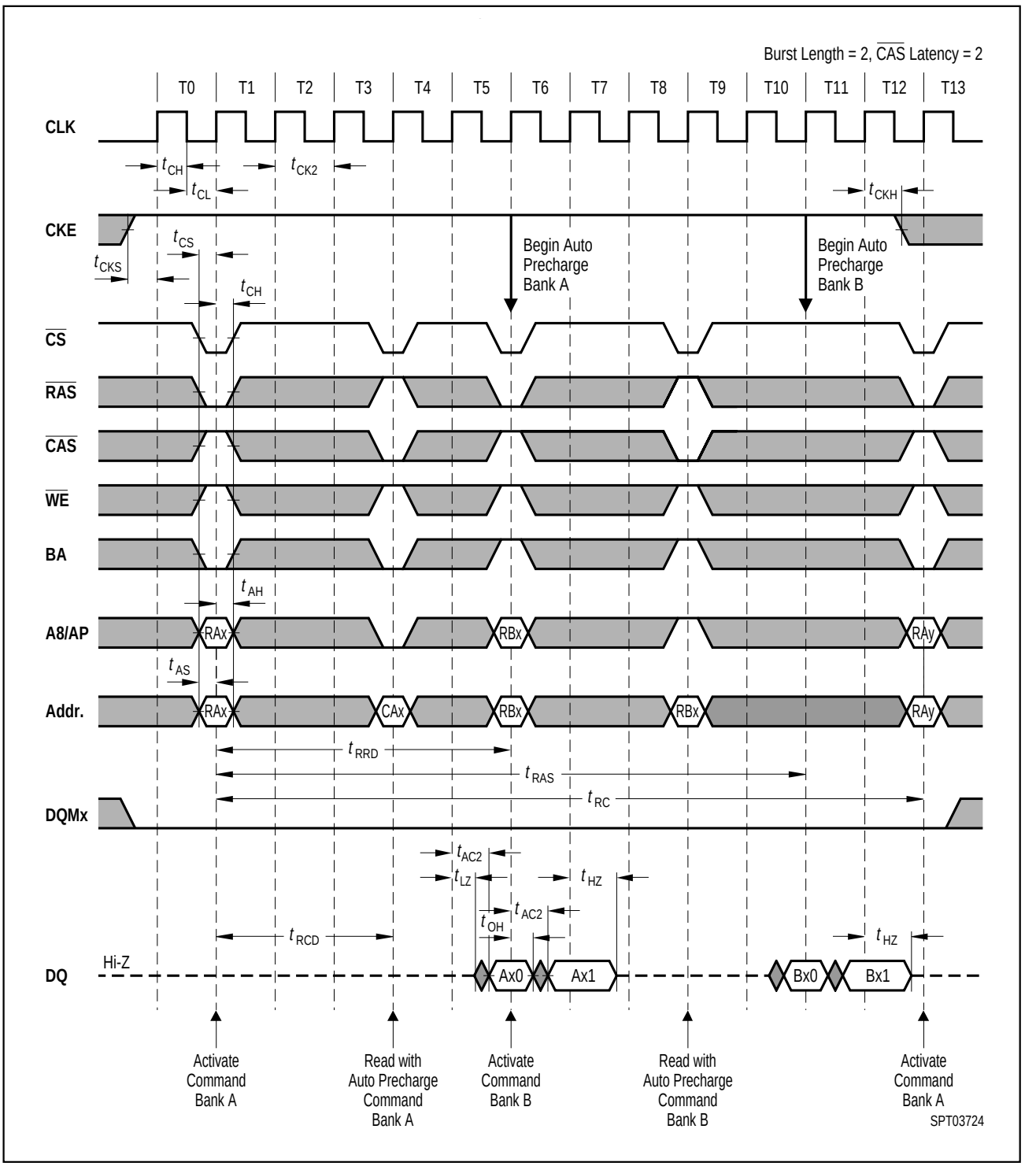


9. AC Parameters

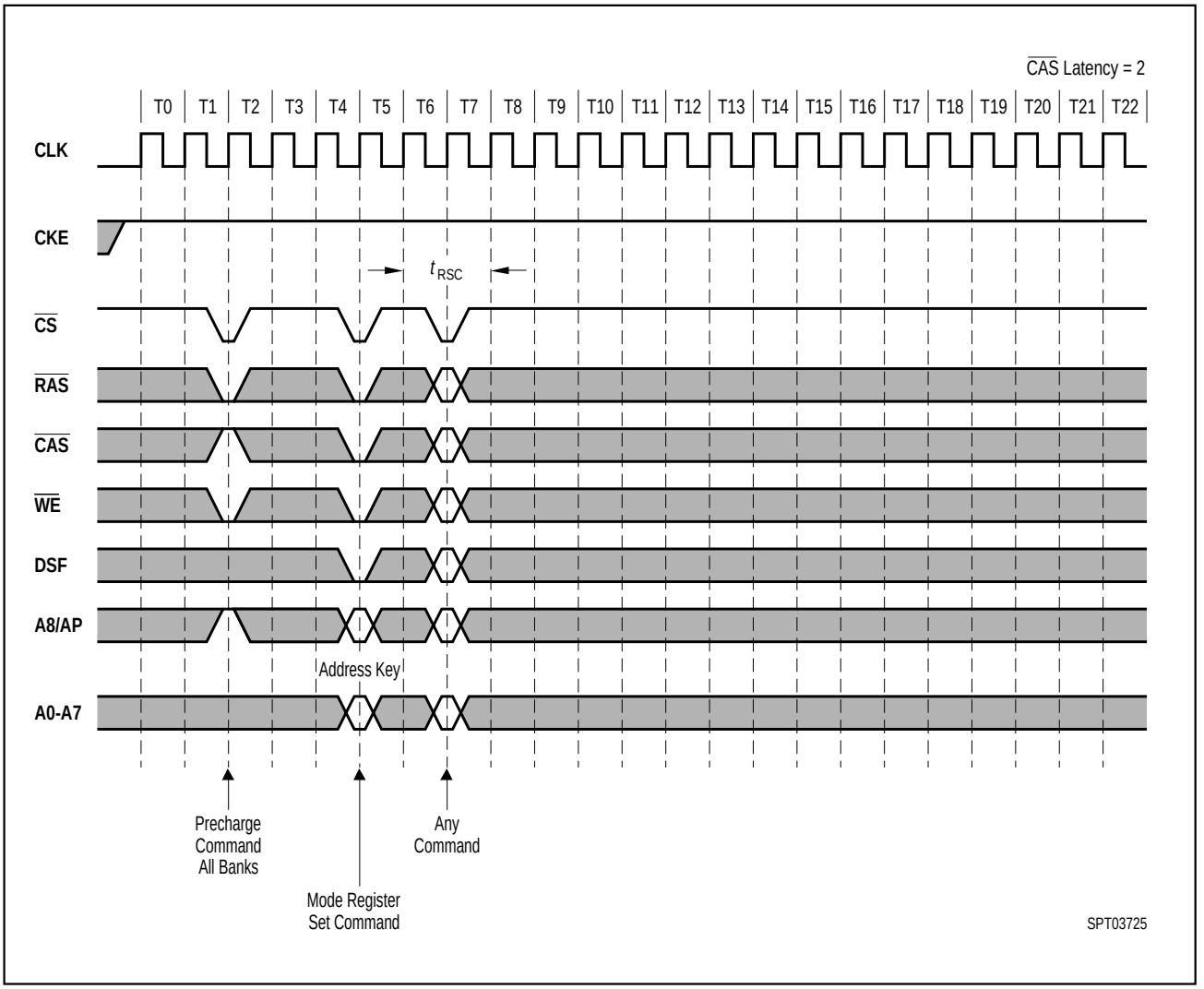
9.1. AC Parameters for a Write Timing



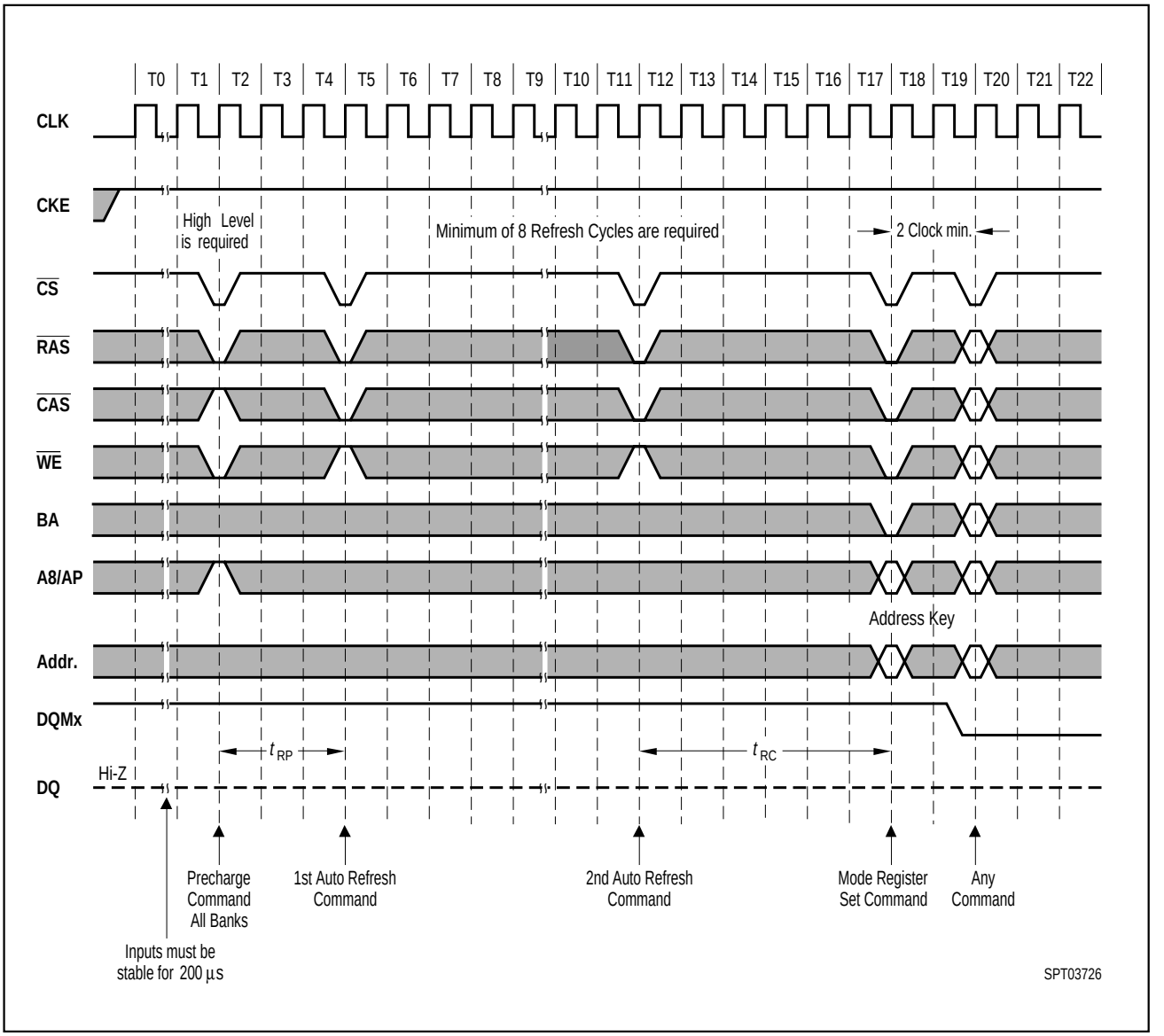
9.2. AC Parameters for a Read Timing



10. Mode Register Set

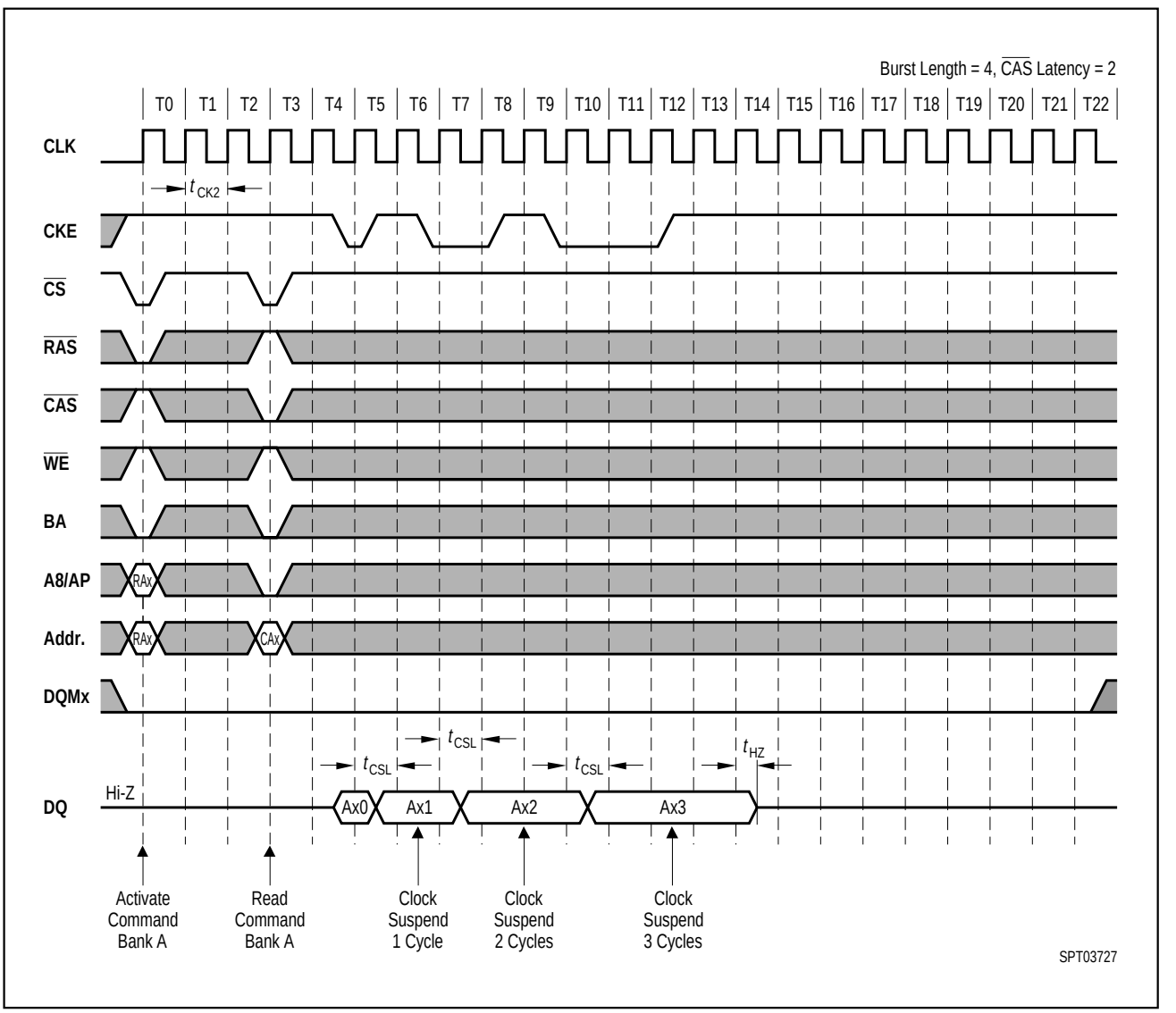


11. Power on Sequence and Auto Refresh (CBR)

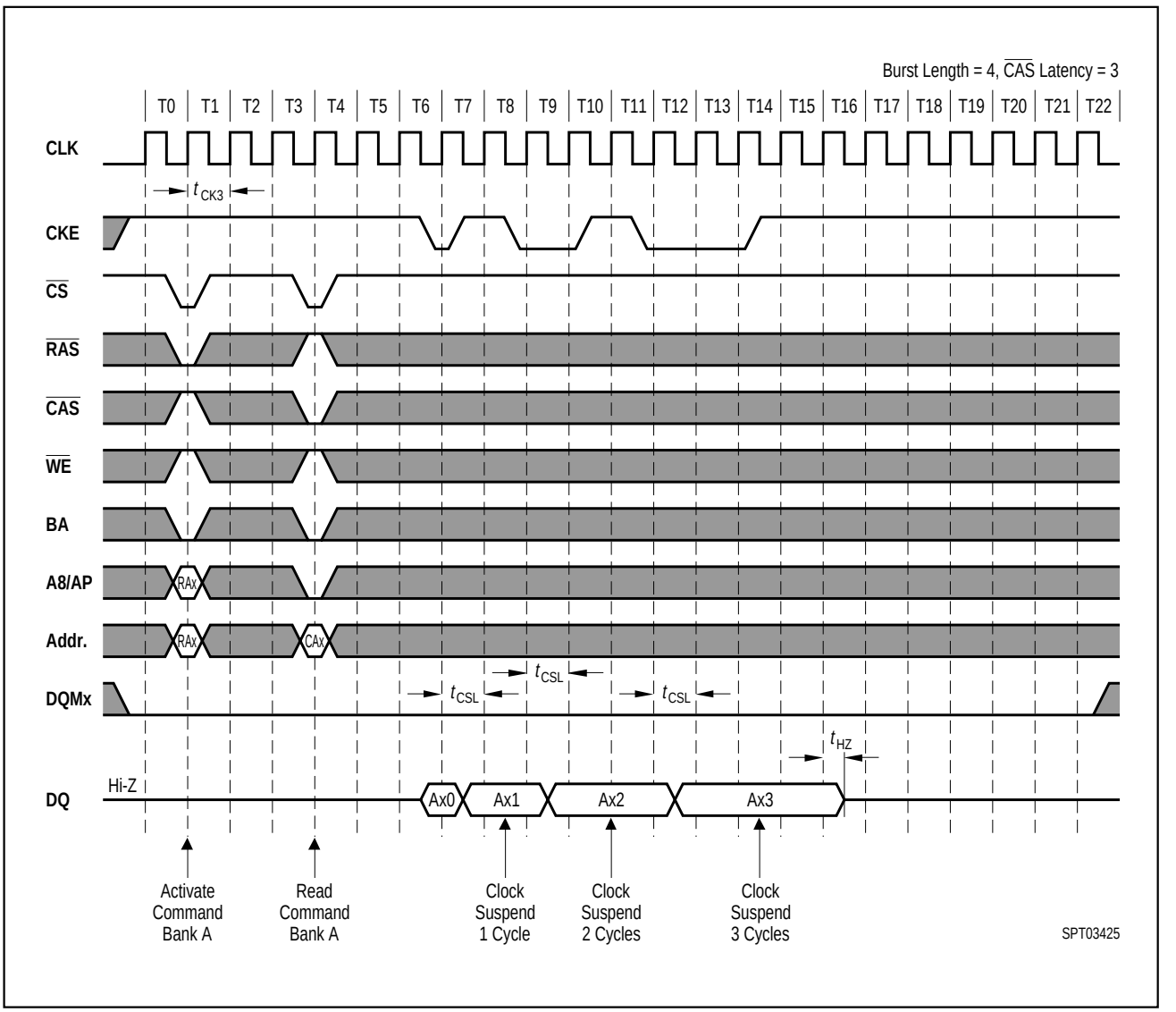


12. Clock Suspension (Using CKE)

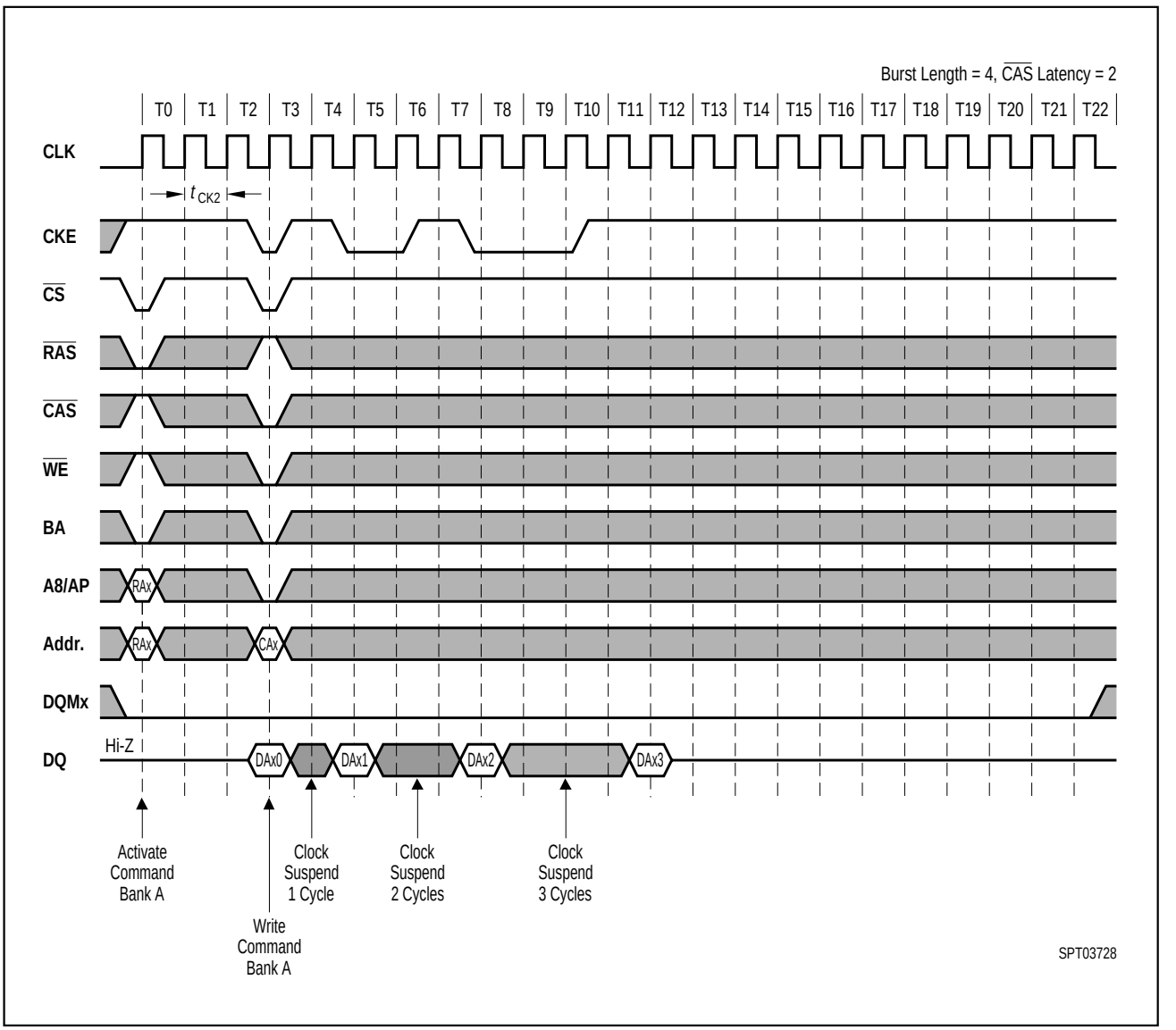
12.1. Clock Suspension During Burst Read $\overline{CAS}$ Latency = 2



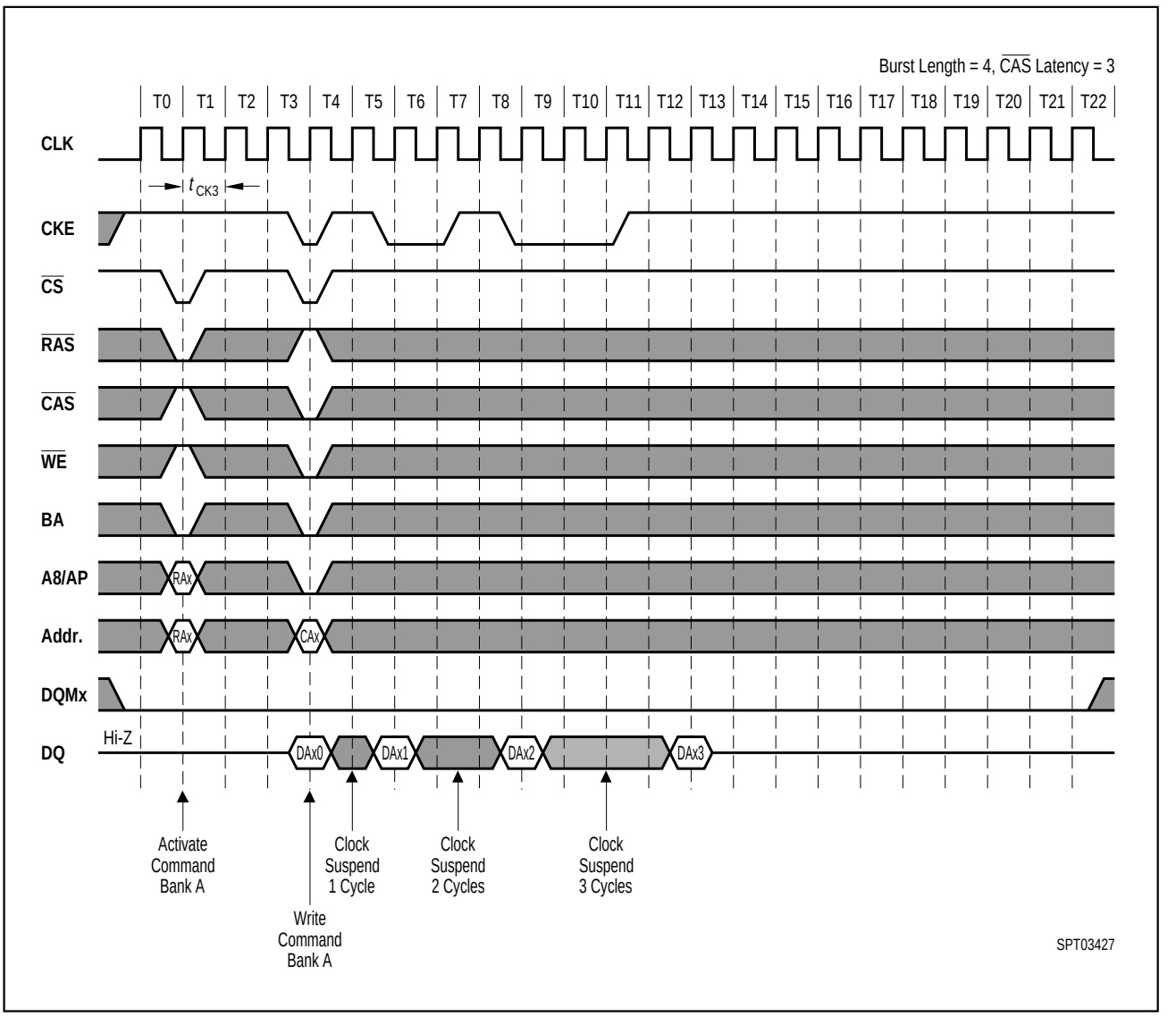
12.2. Clock Suspension During Burst Read $\overline{CAS}$ Latency = 3



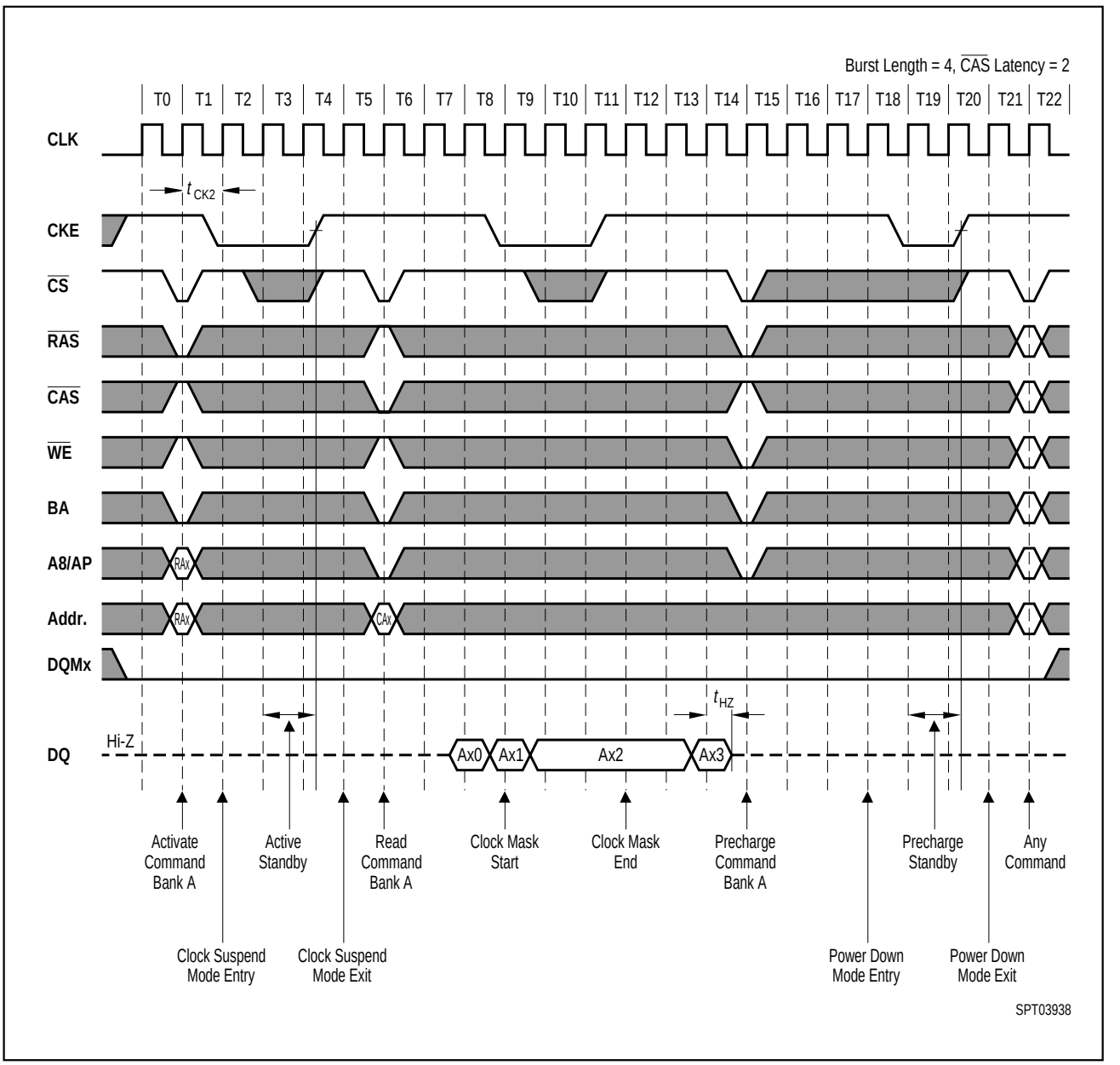
12.3. Clock Suspension During Burst Write $\overline{CAS}$ Latency = 2



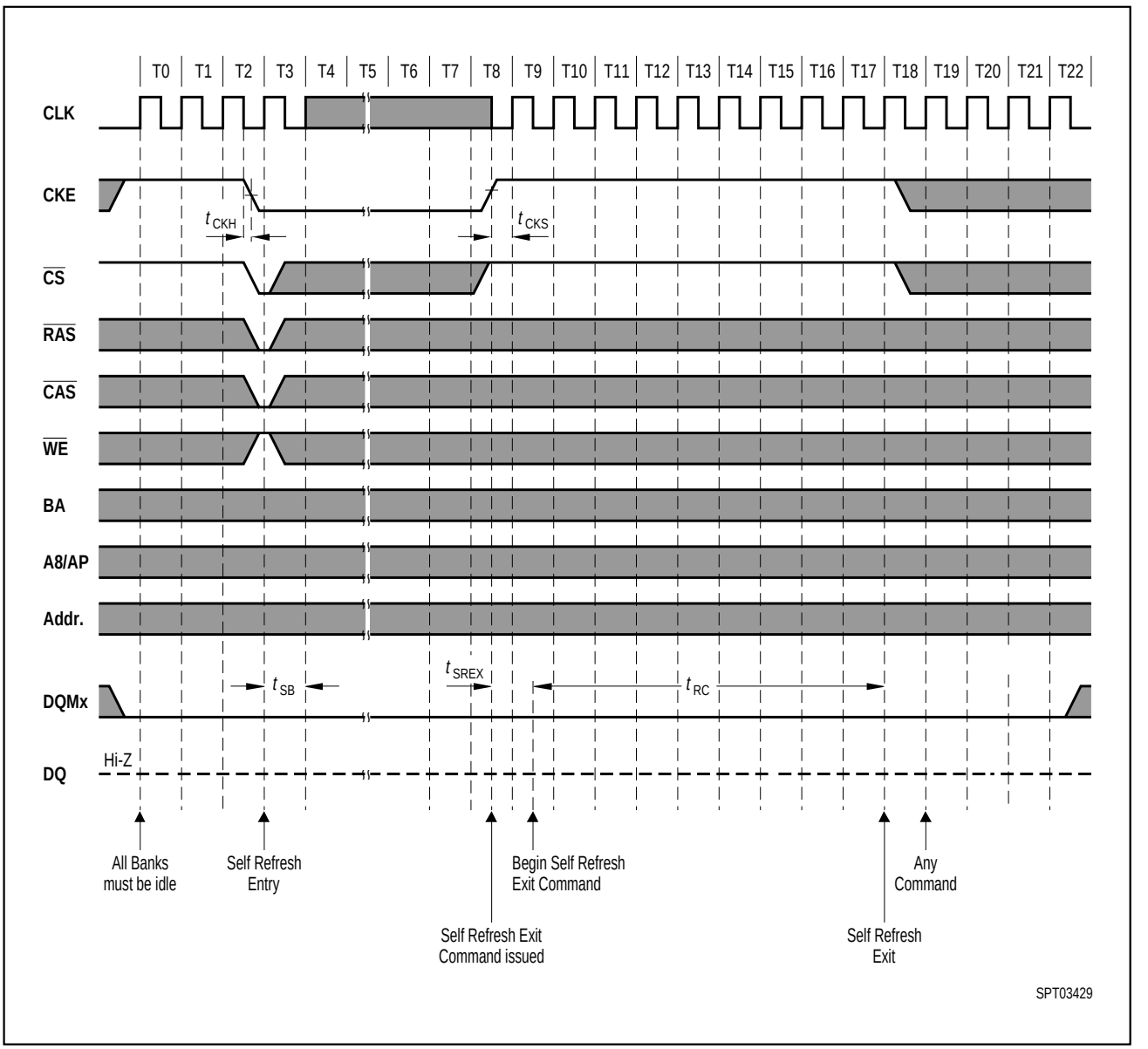
12.4. Clock Suspension During Burst Write $\overline{CAS}$ Latency = 3



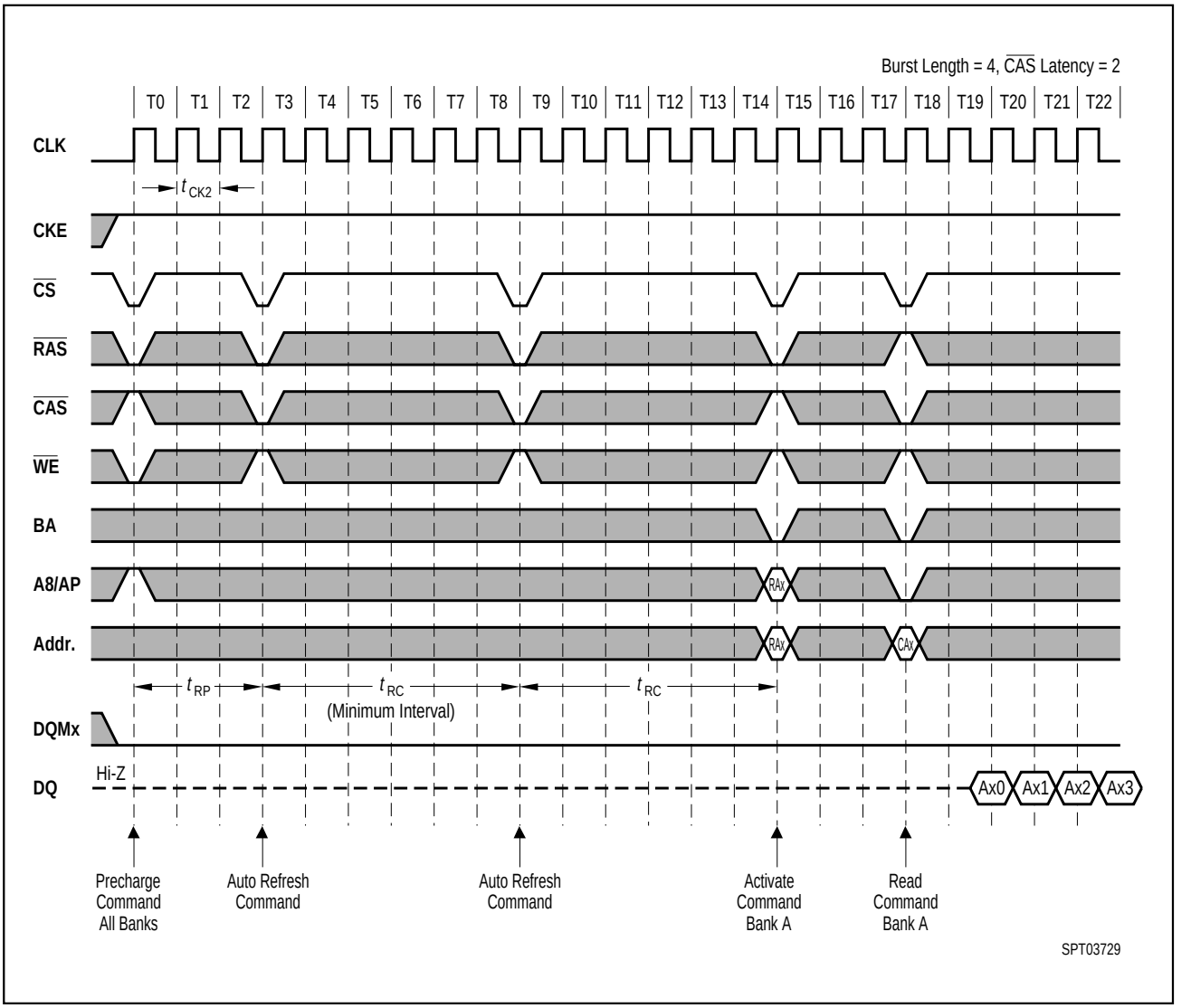
13. Power Down Mode and Clock Suspend



14. Self Refresh (Entry and Exit)

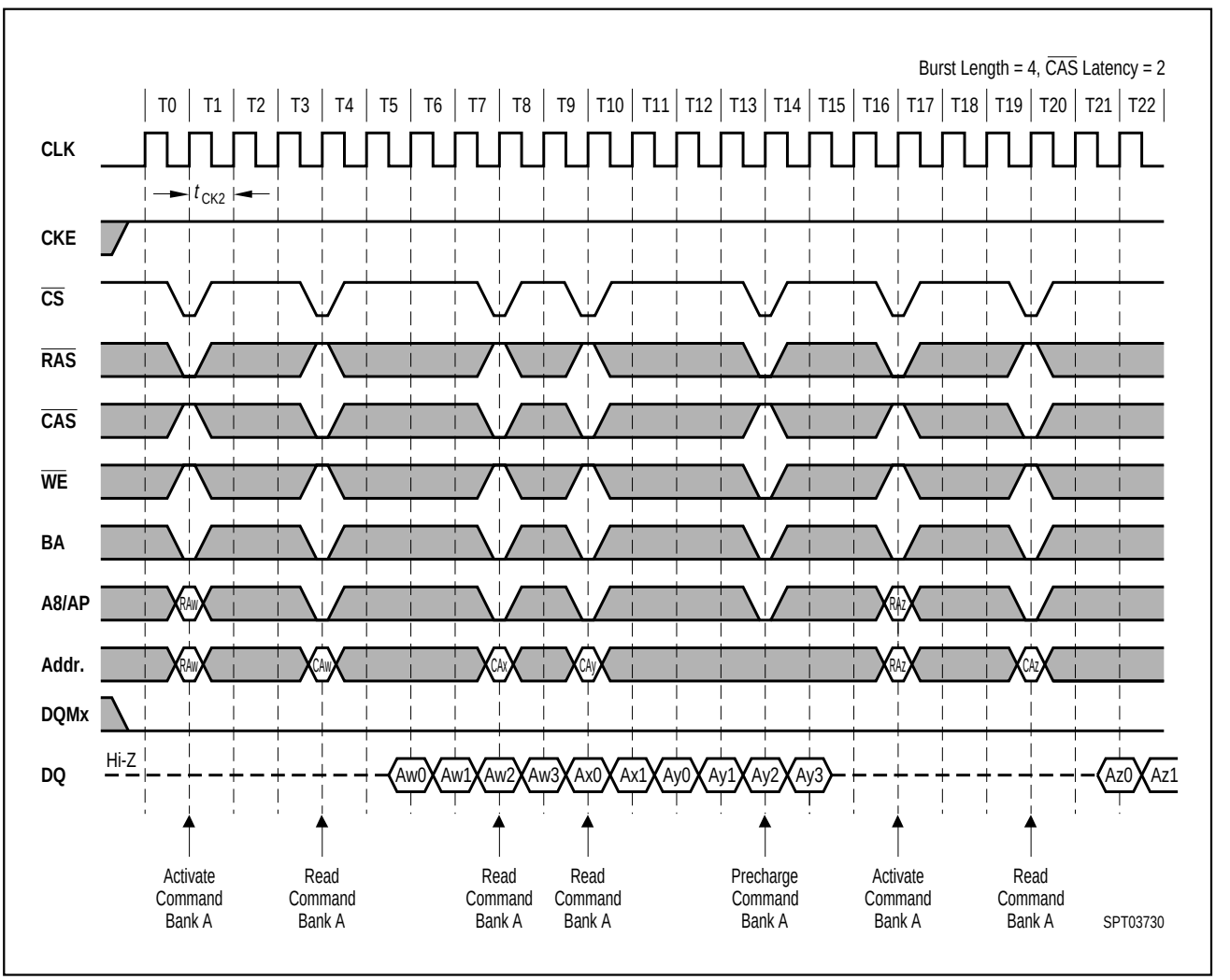


15. Auto Refresh (CBR)

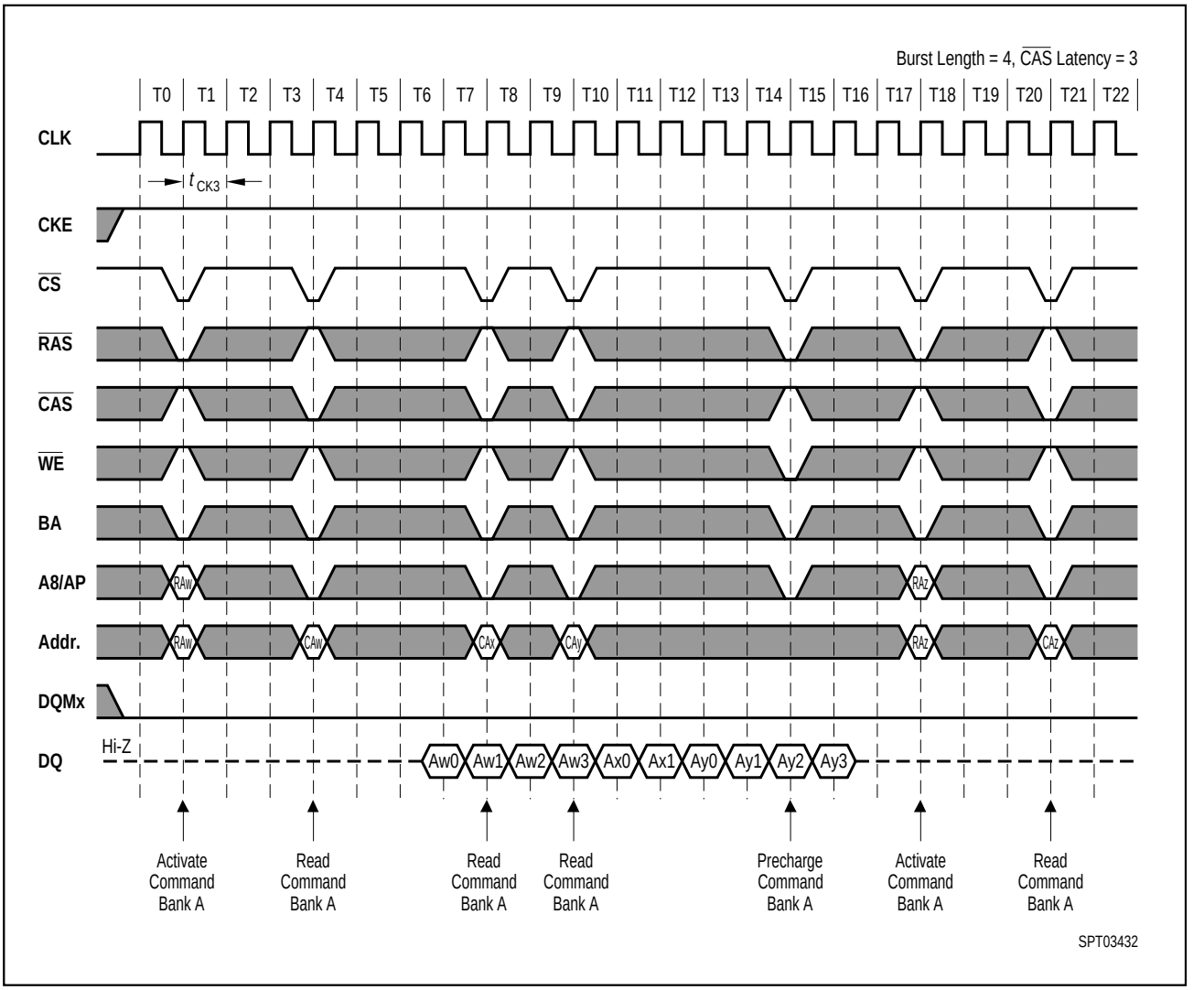


16. Random Column Read (Page within same Bank)

16.1. $\overline{CAS}$ Latency = 2

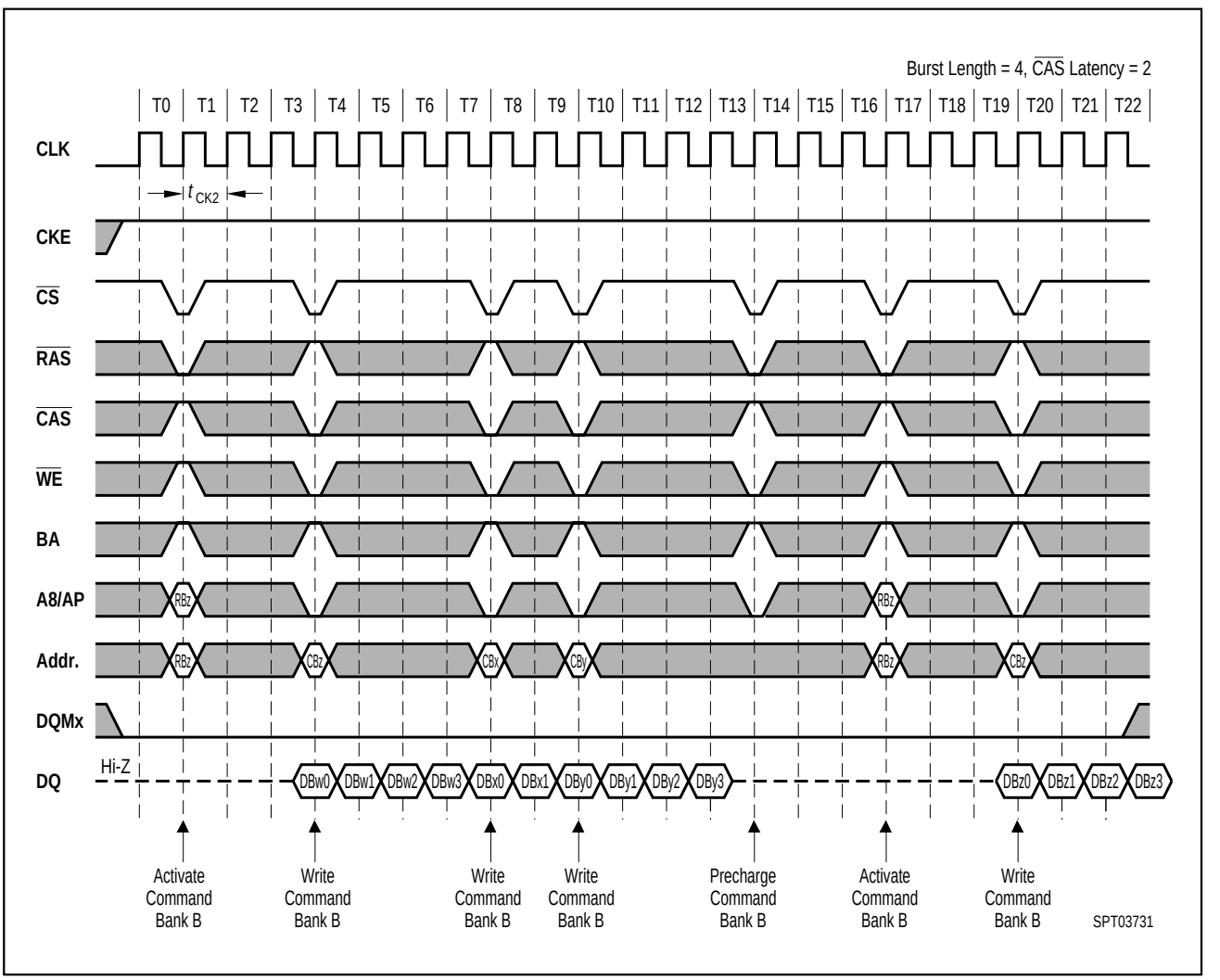


16.2. $\overline{\text{CAS}}$ Latency = 3

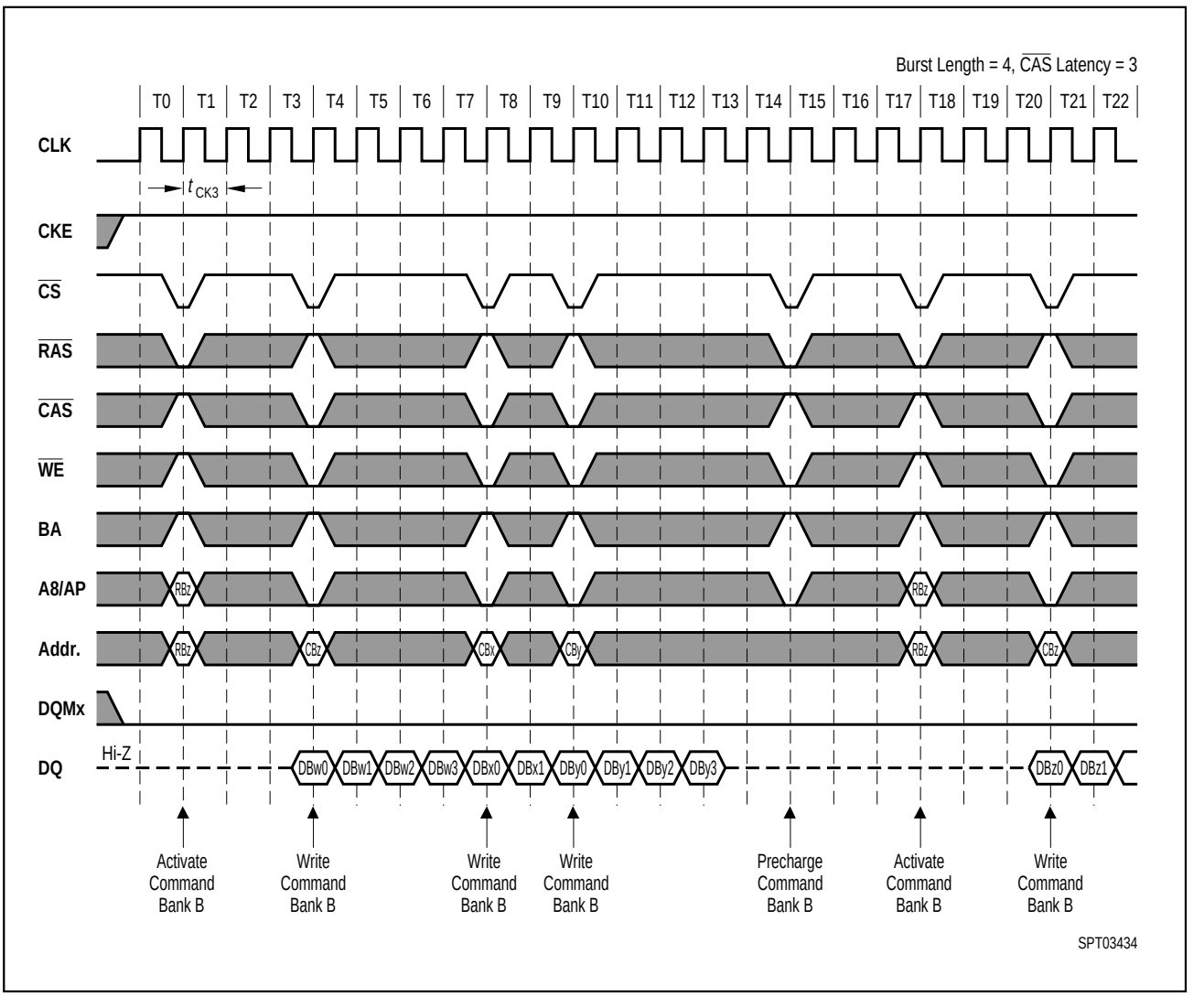


17. Random Column Write (Page within same Bank)

17.1. $\overline{CAS}$ Latency = 2

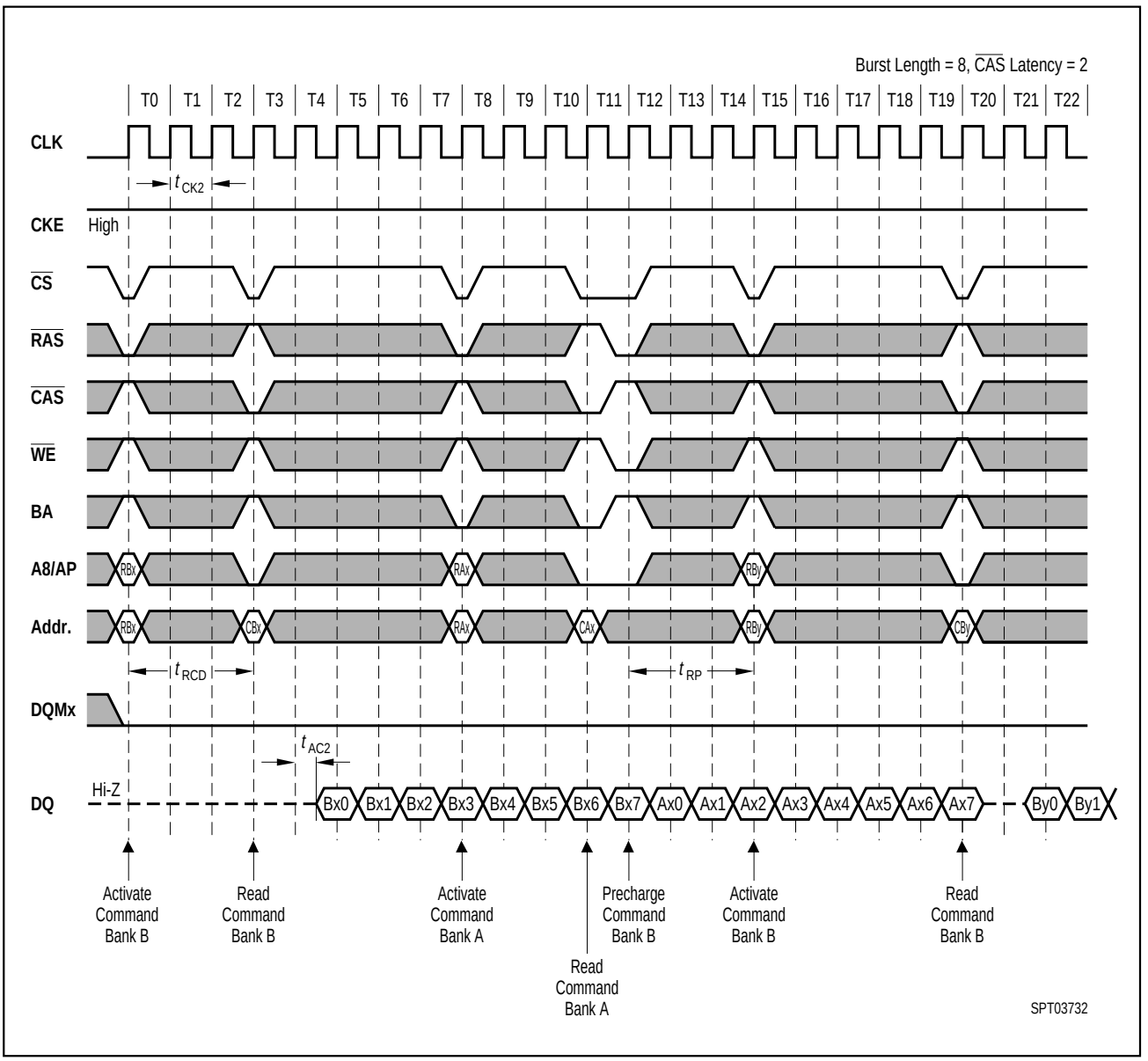


17.2. $\overline{\text{CAS}}$ Latency = 3

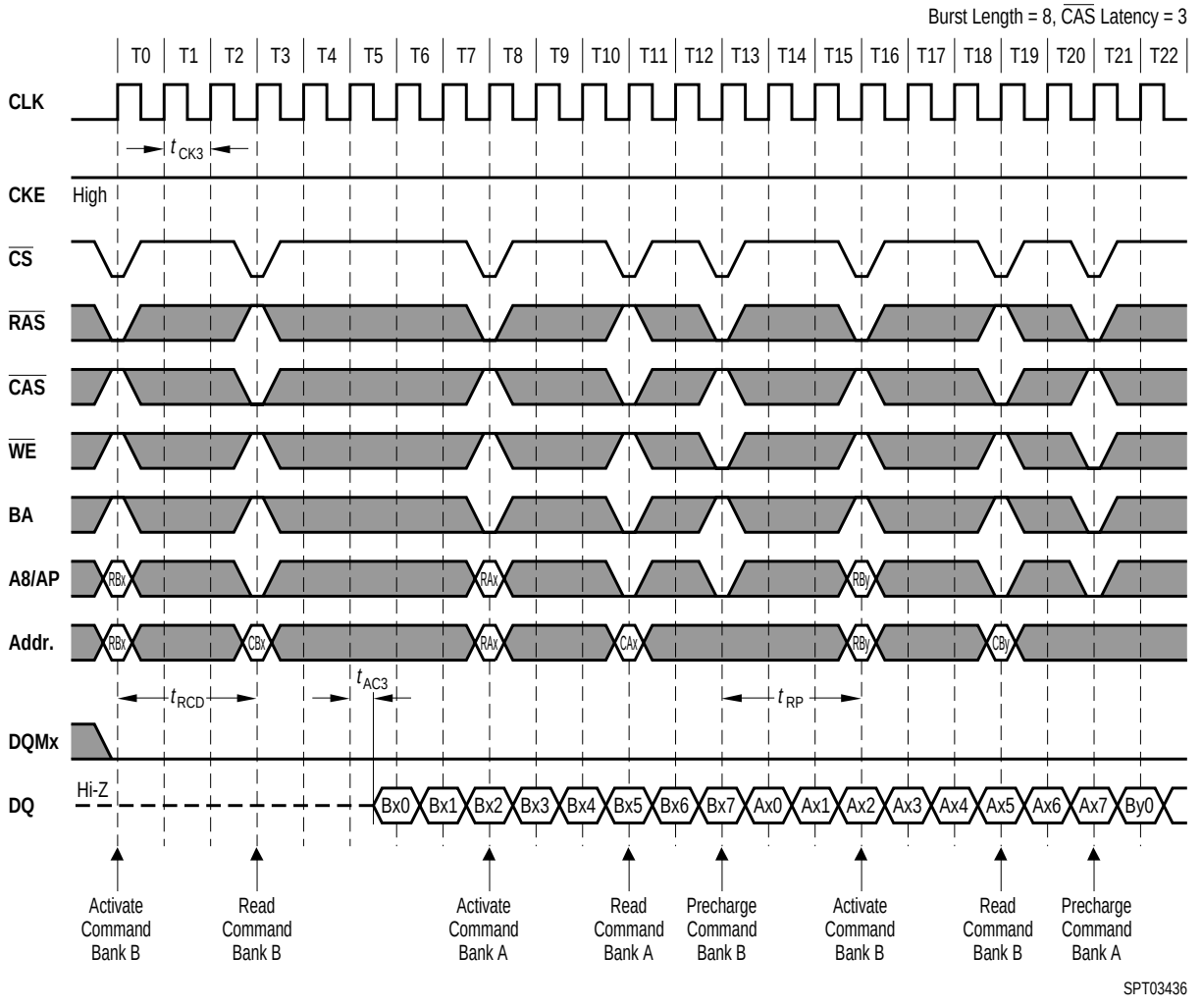


18. Random Row Read (Interleaving Banks) with Precharge

18.1. $\overline{CAS}$ Latency = 2

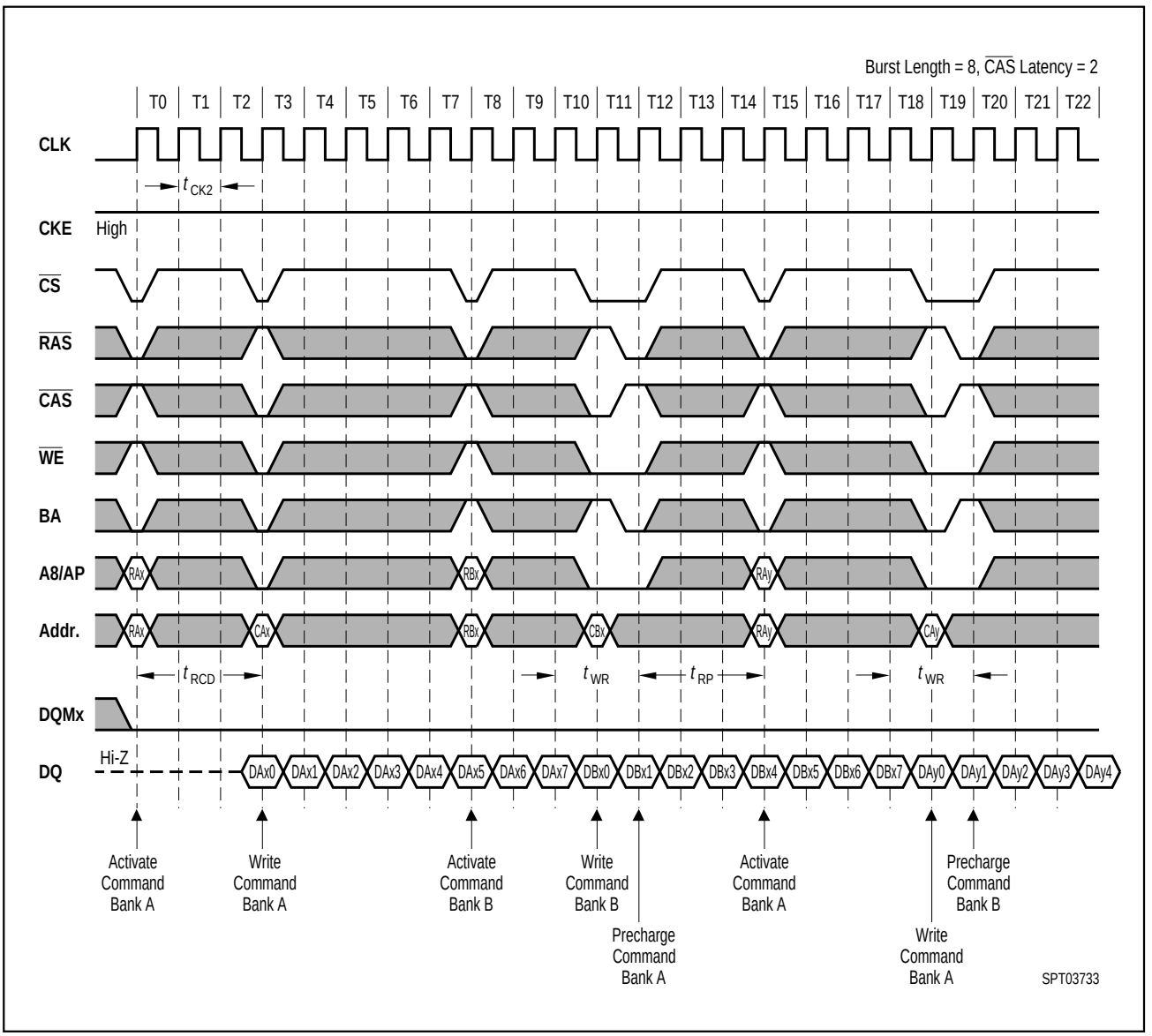


18.2. $\overline{CAS}$ Latency = 3

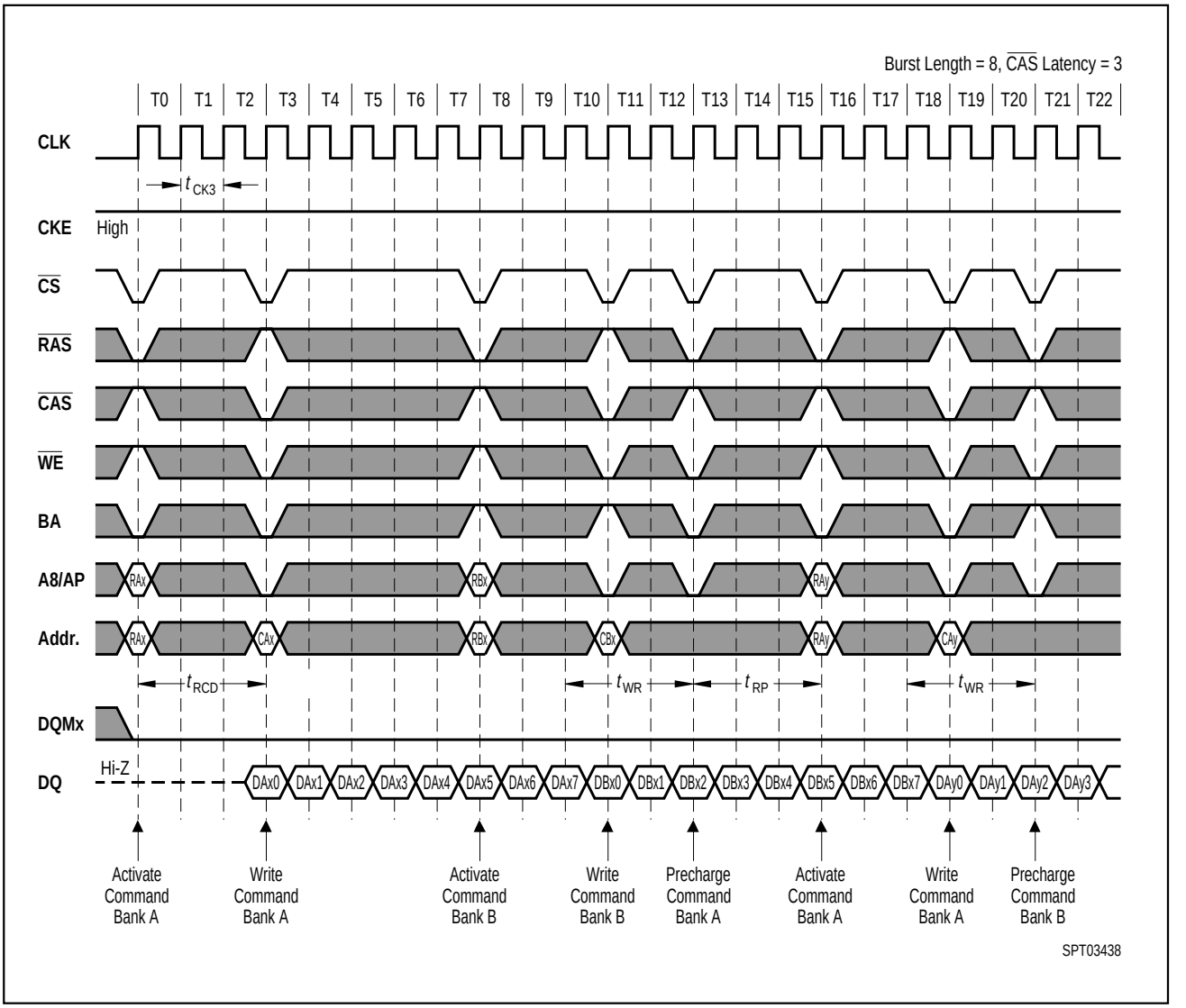


19. Random Row Write (Interleaving Banks) with Precharge

19.1. $\overline{CAS}$ Latency = 2

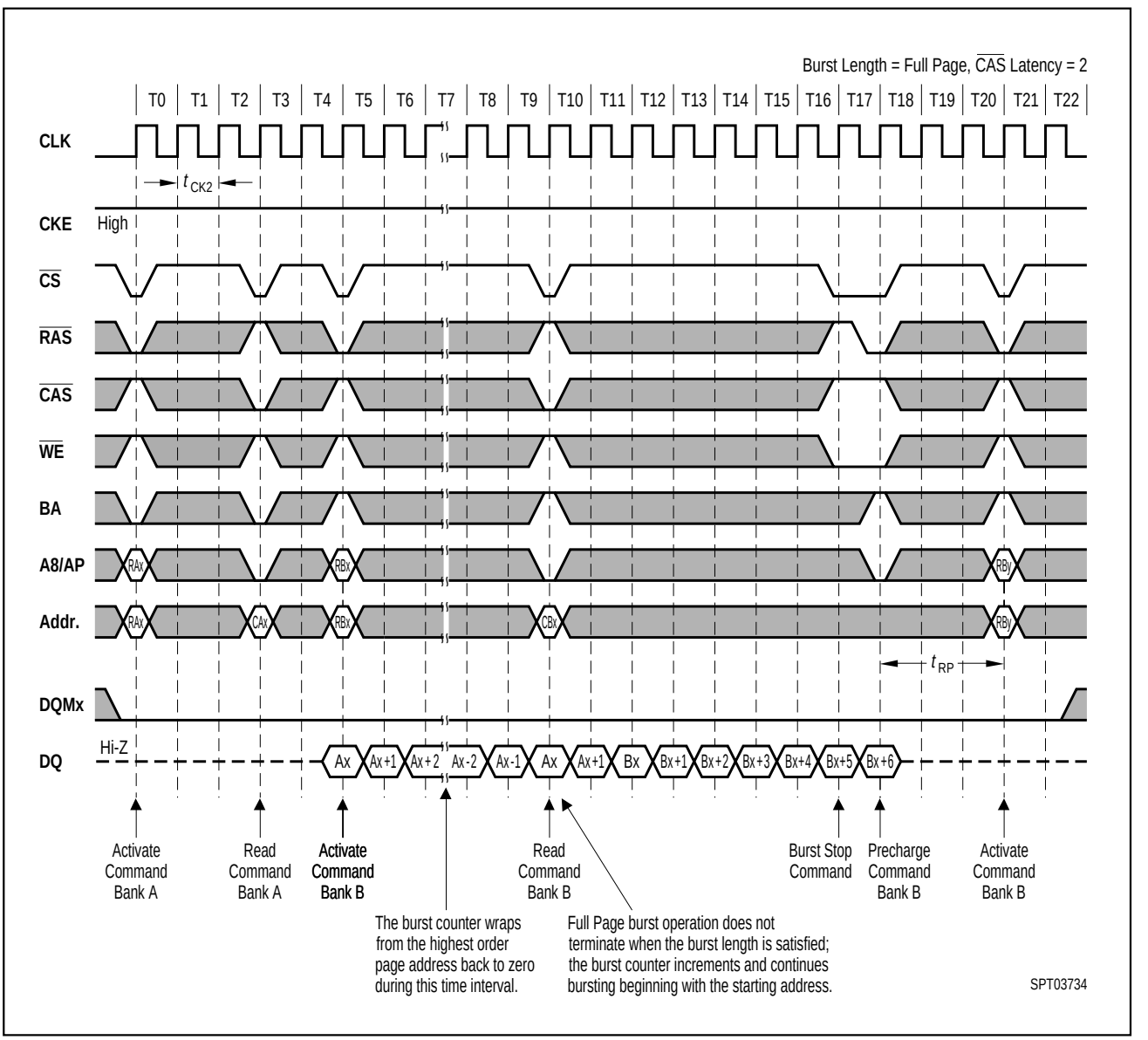


19.2. $\overline{CAS}$ Latency = 3

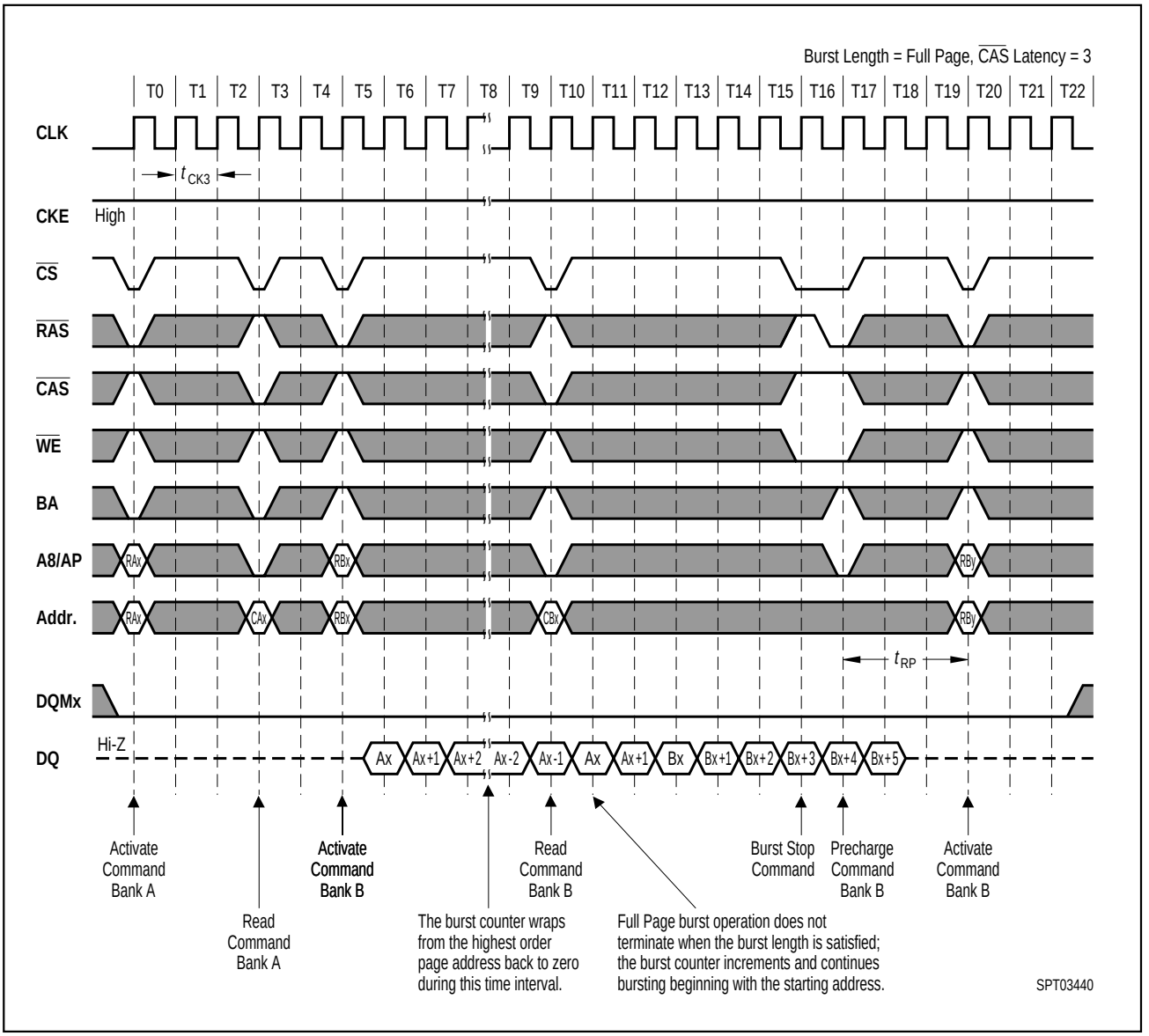


20. Full Page Read Cycle

20.1. $\overline{CAS}$ Latency = 2

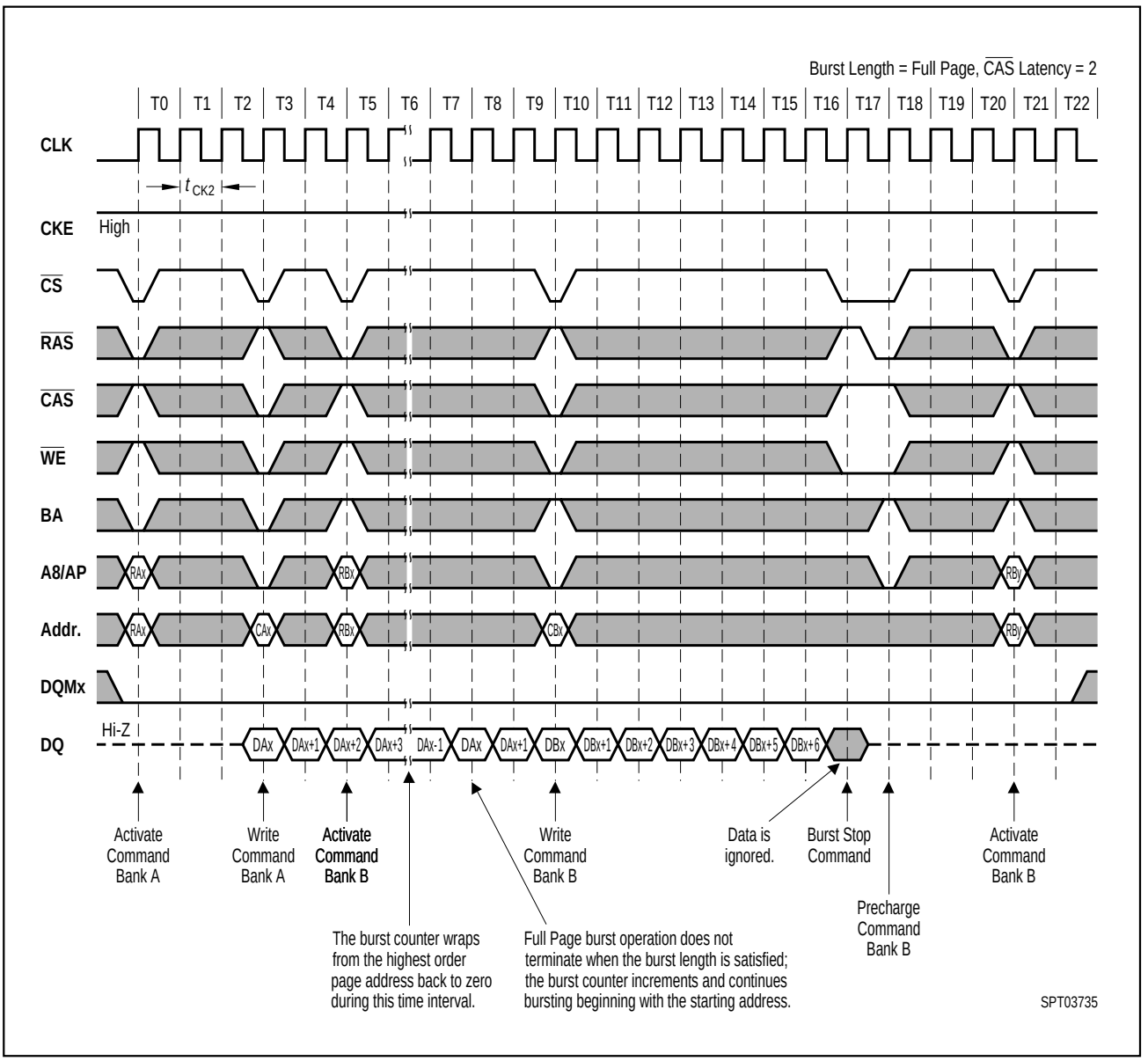


20.2. $\overline{CAS}$ Latency = 3

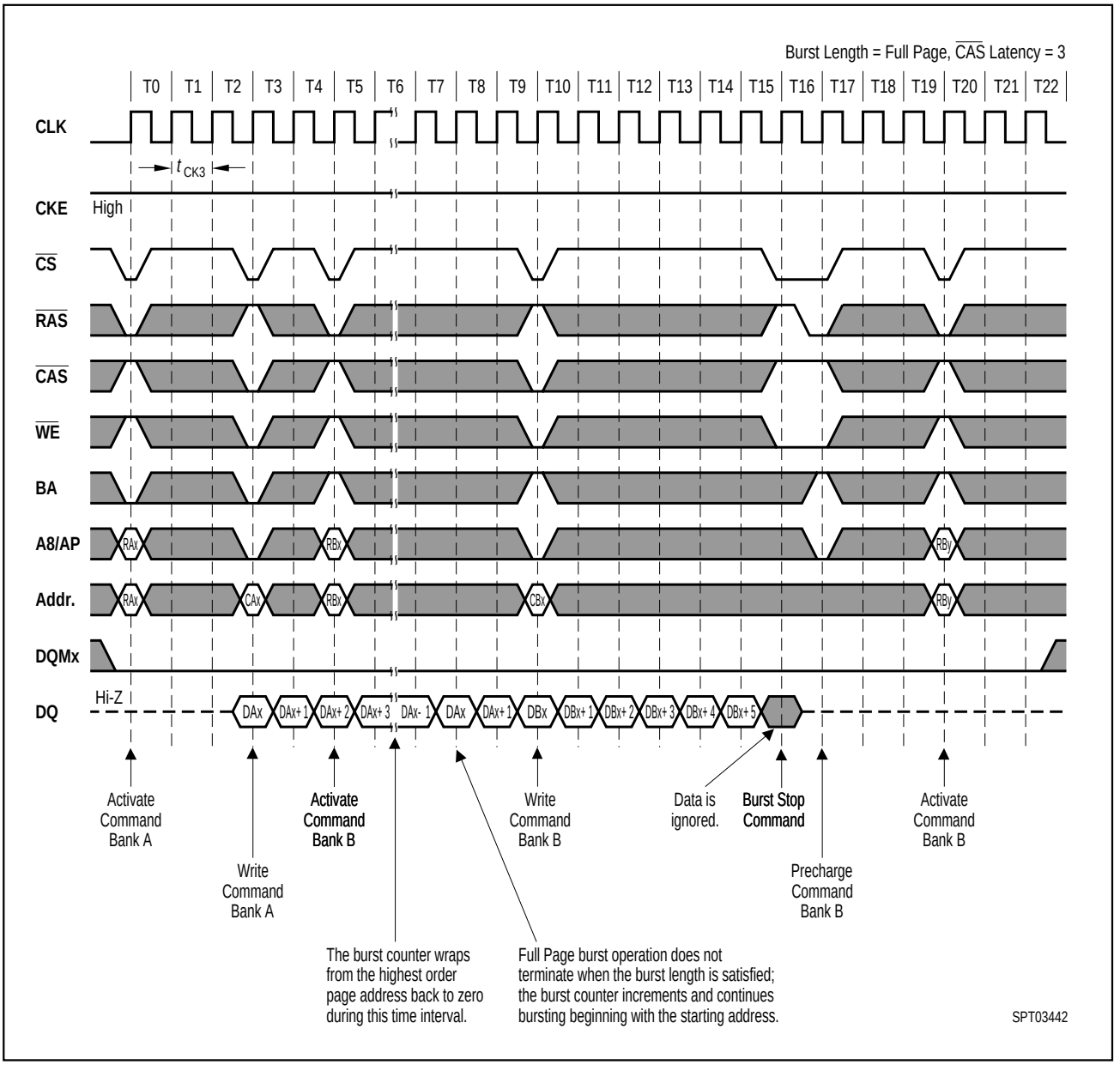


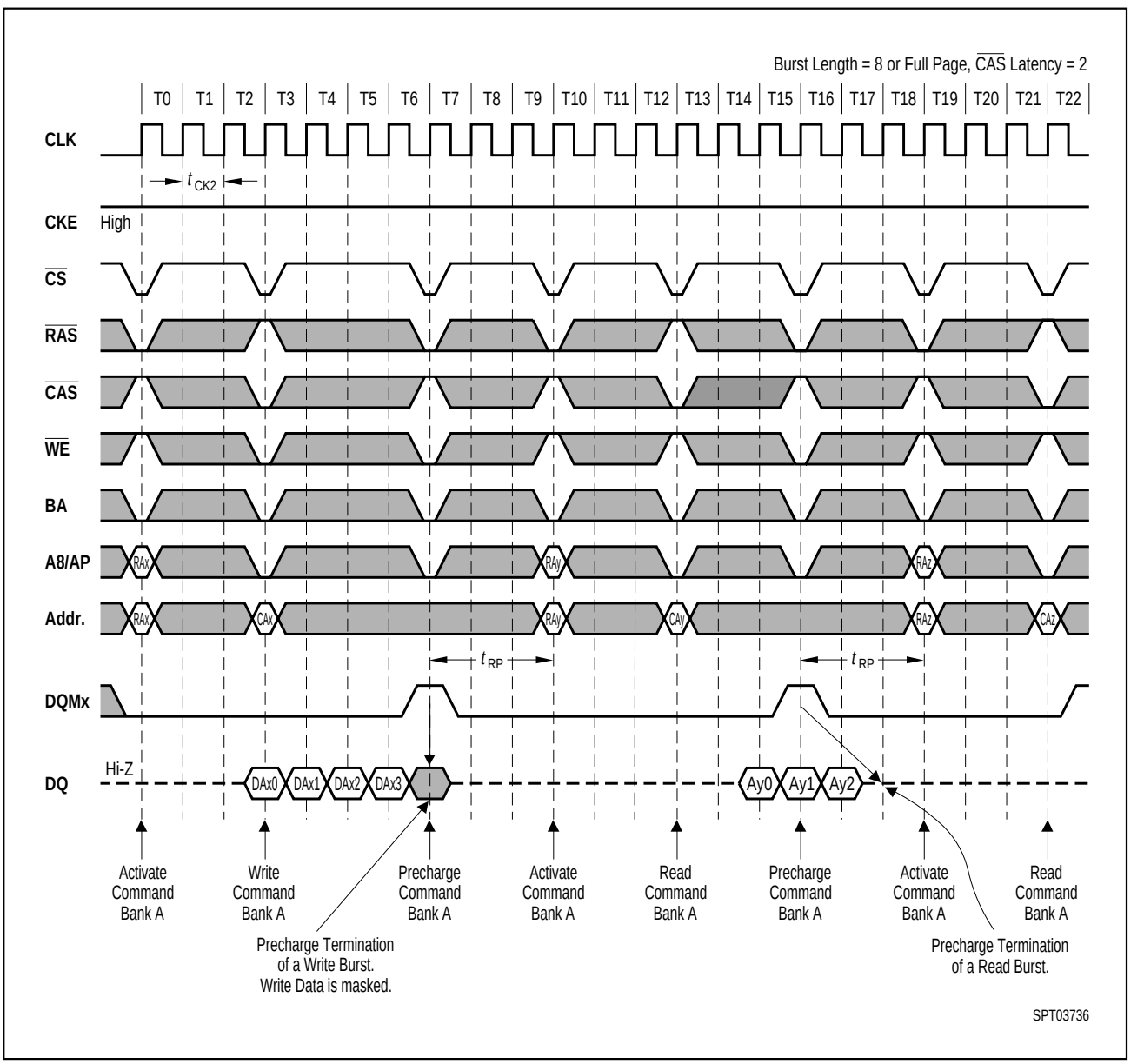
21. Full Page Write Cycle

21.1. $\overline{CAS}$ Latency = 2



21.2. $\overline{CAS}$ Latency = 3



22. Precharge Termination of a Burst

22.1. $\overline{CAS}$ Latency = 2