## FEATURES

- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 9.5 ns at 5 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Support Mixed-Mode Voltage Operation on All Ports**

- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
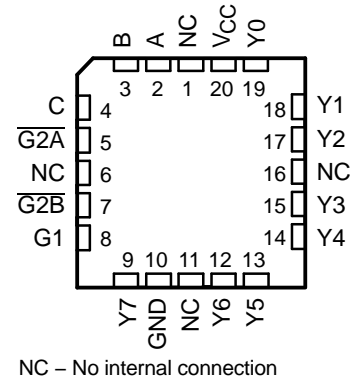 - **1000-V Charged-Device Model (C101)**

SN54LV138A . . . J OR W PACKAGE
SN74LV138A . . . D, DB, DGV, NS OR PW PACKAGE
(TOP VIEW)
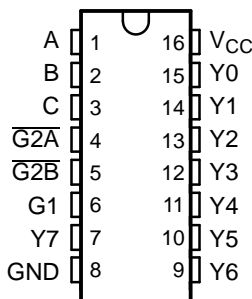
SN74LV138A . . . RGY PACKAGE
(TOP VIEW)
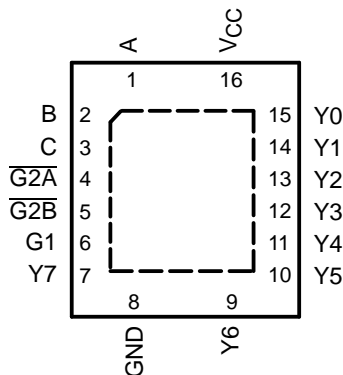
SN54LV138A . . . FK PACKAGE
(TOP VIEW)

NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The 'LV138A devices are 3-line to 8-line decoders/demultiplexers designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV138ARGYR	LV138A
	SOIC – D	Tube of 40	SN74LV138AD	LV138A
		Reel of 2500	SN74LV138ADR	
	SOP – NS	Reel of 2000	SN74LV138ANSR	74LV138A
	SSOP – DB	Reel of 2000	SN74LV138ADBR	LV138A
	TSSOP – PW	Tube of 90	SN74LV138APW	LV138A
		Reel of 2000	SN74LV138APWR	
		Reel of 250	SN74LV138APWT	
	TVSOP – DGV	Reel of 2000	SN74LV138ADGVR	LV138A
−55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV138AJ	SNJ54LV138AJ
	CFP – W	Tube of 150	SNJ54LV138AW	SNJ54LV138AW
	LCCC – FK	Tube of 55	SNJ54LV138AFK	SNJ54LV138AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

These devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs (A, B, C) and the three enable inputs (G1, $\overline{G2A}$, $\overline{G2B}$) select one of eight output lines. The two active-low ($\overline{G2A}$, $\overline{G2B}$) and one active-high (G1) enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y20	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)
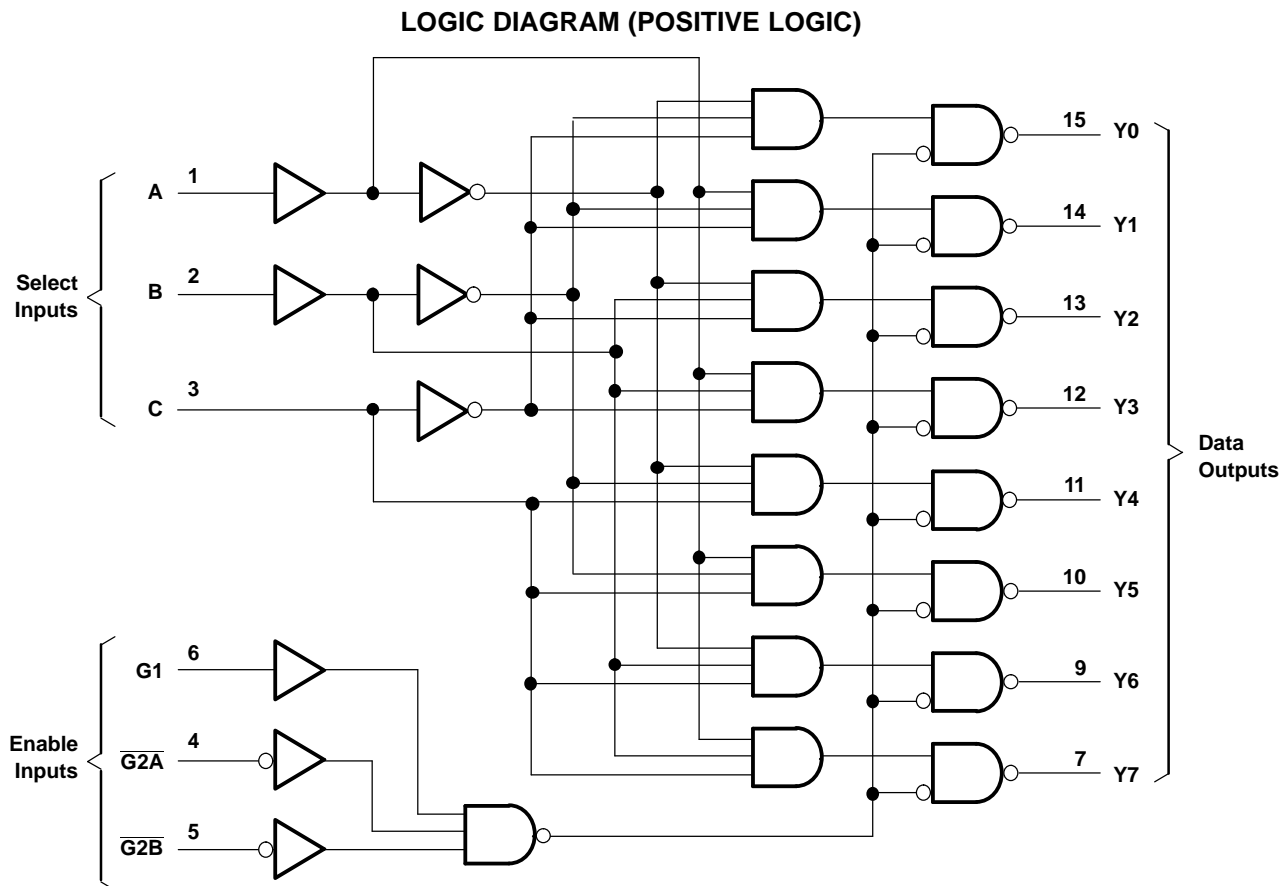
Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	7	V
V_O	Output voltage range[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance	D package[4]		73	°C/W
		DB package[4]		82	
		DGV package[4]		120	
		NS package[4]		64	
		PW package[4]		108	
		RGY package[5]		39	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

![Texas Instruments logo] www.ti.com

Recommended Operating Conditions[1]

			SN54LV138A[2] MIN	SN54LV138A[2] MAX	SN74LV138A MIN	SN74LV138A MAX	UNIT
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		−50		−50	µA
		$V_{CC} = 2.3$ V to 2.7 V		−2		−2	mA
		$V_{CC} = 3$ V to 3.6 V		−6		−6	
		$V_{CC} = 4.5$ V to 5.5 V		−12		−12	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		50	µA
		$V_{CC} = 2.3$ V to 2.7 V		2		2	mA
		$V_{CC} = 3$ V to 3.6 V		6		6	
		$V_{CC} = 4.5$ V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V		200		200	ns/V
		$V_{CC} = 3$ V to 3.6 V		100		100	
		$V_{CC} = 4.5$ V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Product Preview

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV138A[1] MIN	SN54LV138A[1] TYP	SN54LV138A[1] MAX	SN74LV138A MIN	SN74LV138A TYP	SN74LV138A MAX	UNIT
V_{OH}	$I_{OH} = -50$ µA	2 V to 5.5 V	$V_{CC} - 0.1$			$V_{CC} - 0.1$			V
	$I_{OH} = -2$ mA	2.3 V	2			2			
	$I_{OH} = -6$ mA	3 V	2.48			2.48			
	$I_{OH} = -12$ mA	4.5 V	3.8			3.8			
V_{OL}	$I_{OL} = 50$ µA	2 V to 5.5 V			0.1			0.1	V
	$I_{OL} = 2$ mA	2.3 V			0.4			0.4	
	$I_{OL} = 6$ mA	3 V			0.44			0.44	
	$I_{OL} = 12$ mA	4.5 V			0.55			0.55	
I_I	$V_I = 5.5$ V or GND	0 to 5.5 V			±1			±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20			20	µA
I_{off}	V_I or $V_O = 0$ to 5.5 V	0		5			5		µA
C_i	$V_I = V_{CC}$ or GND	3.3 V		2.1			2.1		pF

(1) Product Preview

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV138A[1]		SN74LV138A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	C_L = 15 pF		11.7[2]	17.6[2]	1[2]	21[2]	1	21	ns
	G1				12.3[2]	19.2[2]	1[2]	22[2]	1	22	
	$\overline{G2A}$ or $\overline{G2B}$				11.4[2]	18.2[2]	1[2]	21[2]	1	21	
t_{pd}	A, B, or C	Y	C_L = 50 pF		14.9	21.4	1	25	1	25	ns
	G1				15.7	22.6	1	26	1	26	
	G2A or G2B				14.8	22	1	25	1	25	

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV138A[1]		SN74LV138A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	C_L = 15 pF		8.1[2]	11.4[2]	1[2]	13.5[2]	1	13.5	ns
	G1				8.4[2]	12.8[2]	1[2]	15[2]	1	15	
	$\overline{G2A}$ or $\overline{G2B}$				7.8[2]	11.4[2]	1[2]	13.5[2]	1	13.5	
t_{pd}	A, B, or C	Y	C_L = 50 pF		10.3	15.8	1	18	1	18	ns
	G1				10.6	16.3	1	18.5	1	18.5	
	G2A or G2B				10	14.9	1	17	1	17	

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

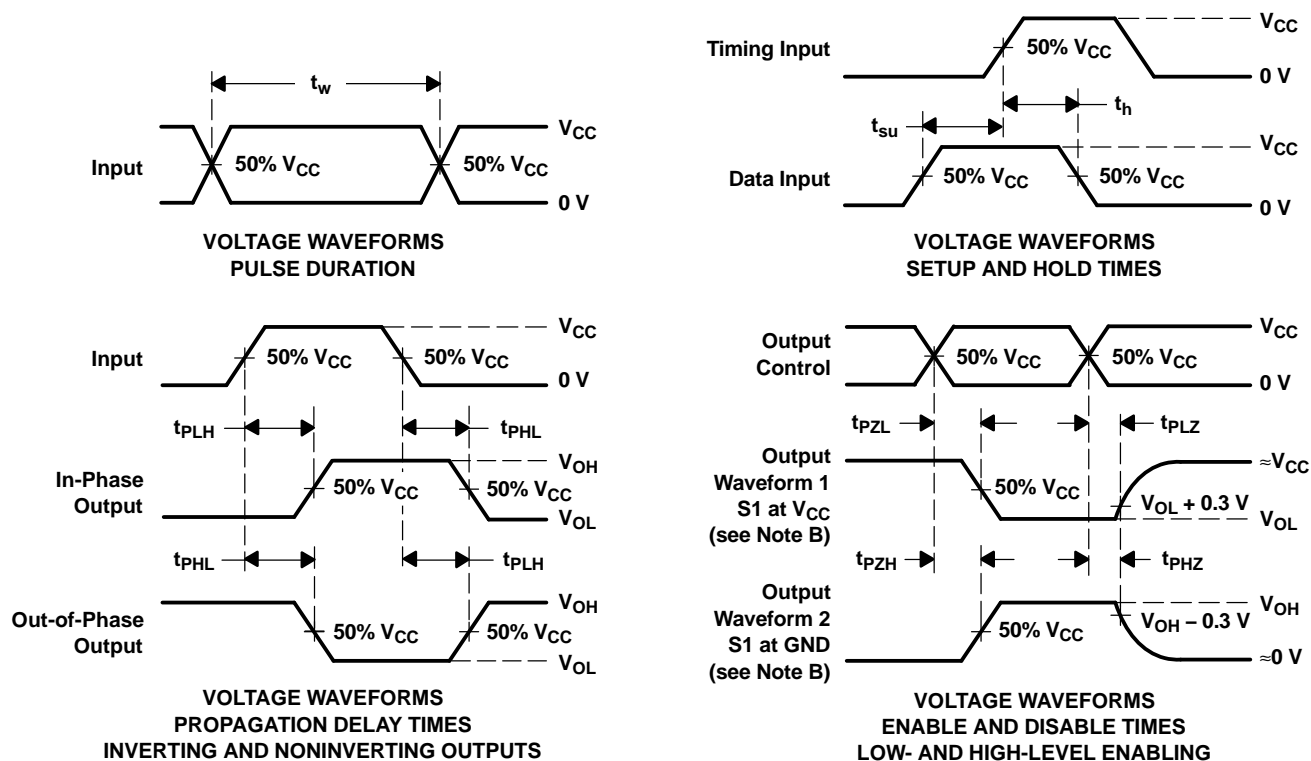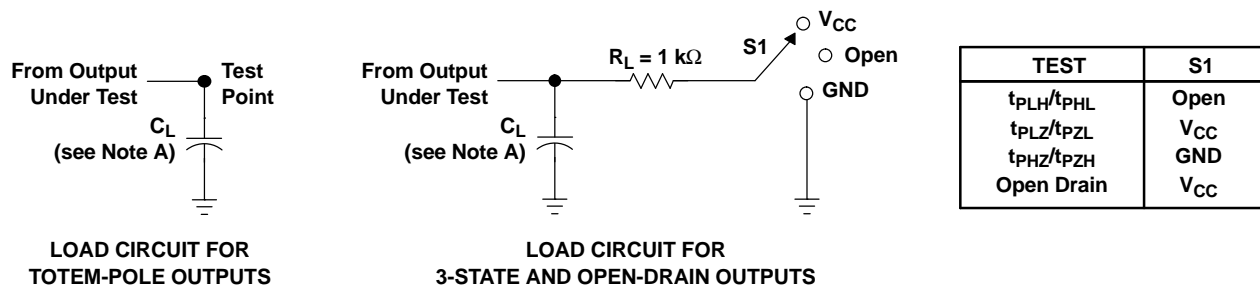| PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV138A[1]		SN74LV138A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	C_L = 15 pF		5.6[2]	8.1[2]	1[2]	9.5[2]	1	9.5	ns
	G1				5.7[2]	8.1[2]	1[2]	9.5[2]	1	9.5	
	$\overline{G2A}$ or $\overline{G2B}$				5.4[2]	8.1[2]	1[2]	9.5[2]	1	9.5	
t_{pd}	A, B, or C	Y	C_L = 50 pF		7	10.1	1	11.5	1	11.5	ns
	G1				7.1	10.1	1	11.5	1	11.5	
	G2A or G2B				6.8	10.1	1	11.5	1	11.5	

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	16.8	pF
			5 V	19.1	

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
     B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
     C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
     D. The outputs are measured one at a time, with one input transition per measurement.
     E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
     F. t_{PZL} and t_{PZH} are the same as t_{en}.
     G. t_{PHL} and t_{PLH} are the same as t_{pd}.
     H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LV138AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138APWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV138ARGYR	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LV138ARGYRG4	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
         D. Falls within JEDEC: 24/48 Pins – MO-153
   14/16/20/56 Pins – MO-194

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)

16 9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1 8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25) 0°–8°

0.050 (1,27)
0.016 (0,40)

4040047–4/F 07/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS–012 variation AC.

RGY (R−PQFP−N16) PLASTIC QUAD FLATPACK
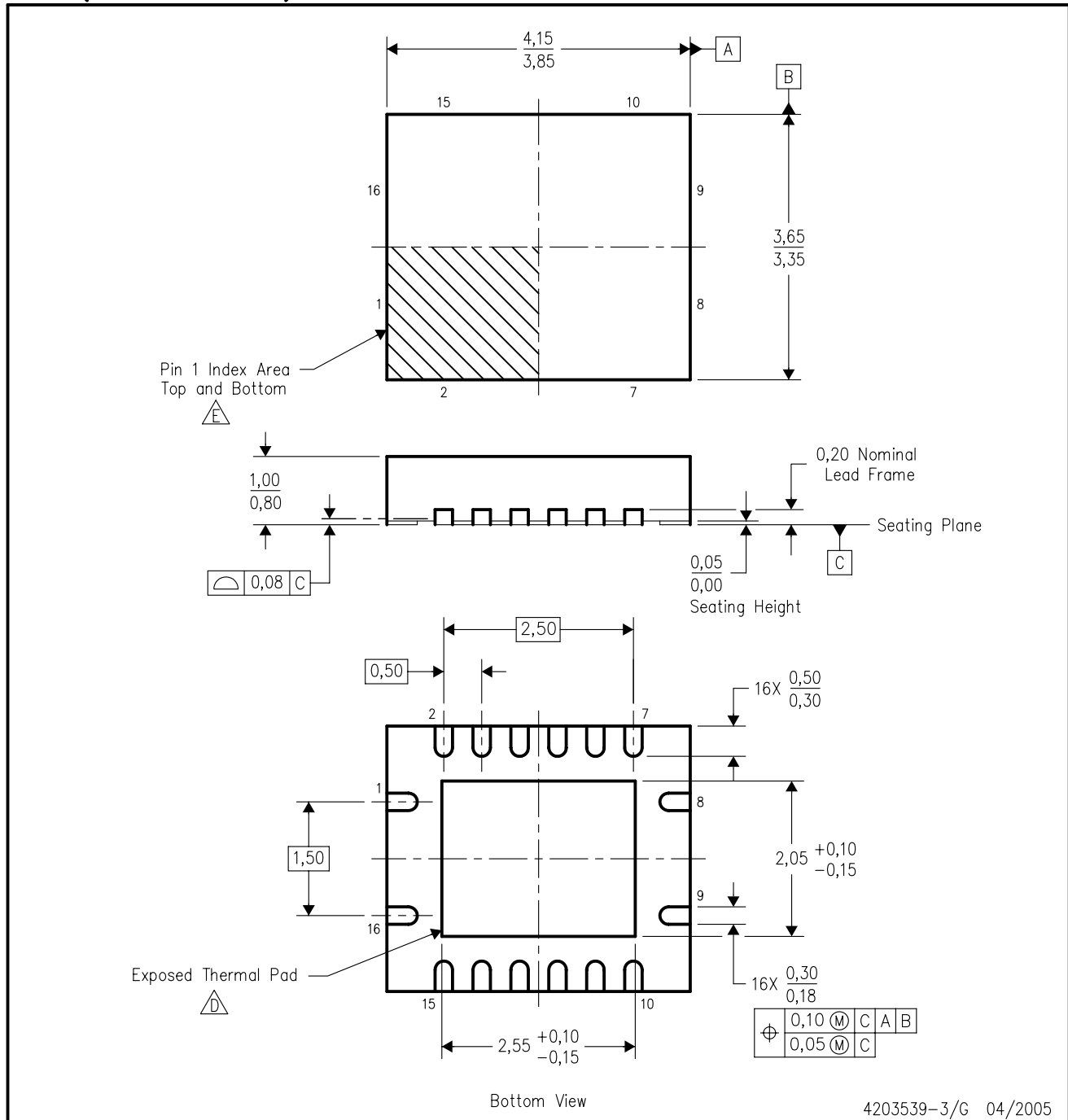
4203539−3/G 04/2005

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
    B. This drawing is subject to change without notice.
    C. QFN (Quad Flatpack No−Lead) package configuration.
    D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
    E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
       The Pin 1 identifiers are either a molded, marked, or metal feature.
    F. Package complies to JEDEC MO−241 variation BB.

MECHANICAL DATA

1,27

0,51 / 0,35   ⊕ 0,25 Ⓜ

5,60 / 5,00   8,20 / 7,40

A

0,15 NOM

Gage Plane

0,25

0°–10°

1,05 / 0,55

0,15 / 0,05

2,00 MAX

Seating Plane

⬜ 0,10

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
       B. This drawing is subject to change without notice.
       C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
       D. Falls within JEDEC MO-150

PW (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

	PINS **	8	14	16	20	24	28
DIM							
A MAX		3,10	5,10	5,10	6,60	7,90	9,80
A MIN		2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

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