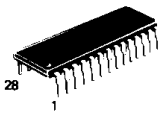
MC145151-2

Parallel-Input PLL Frequency Synthesizer

Interfaces with Single-Modulus Prescalers



P SUFFIX
PLASTIC
CASE 710

FN SUFFIX
PLCC
CASE 776

ORDERING INFORMATION

MC145151P2	Plastic DIP
MC145151FN2	PLCC Package

The MC145151-2 is programmed by 14 parallel input-data lines for the N counter and 3 input lines for the R counter. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, and 14-bit programmable divide-by-N counter.

The MC145151-2 is an improved-performance drop-in replacement for the MC145151-1. The power consumption has decreased and ESD and latch-up performance have improved.

- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- ÷ N Counter Output Available
- Single Modulus/Parallel Programming
- 8 User-Selectable ÷ R Values: 8, 128, 256, 512, 1024, 2048, 2410, 8192
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single Ended (Three-State) or Double Ended
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates

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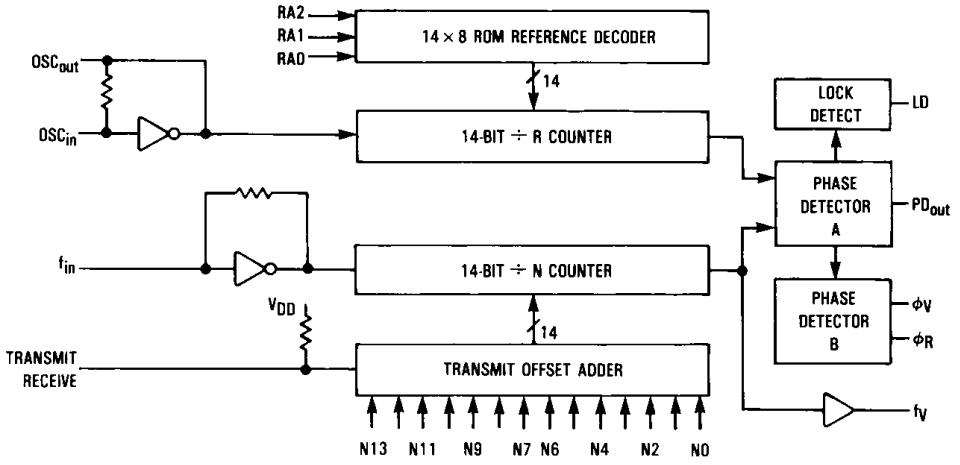
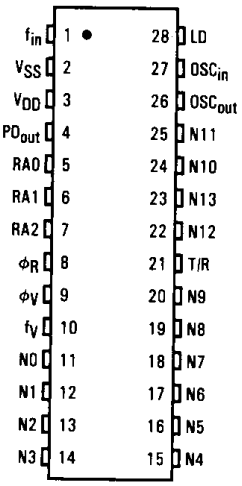
BLOCK DIAGRAM

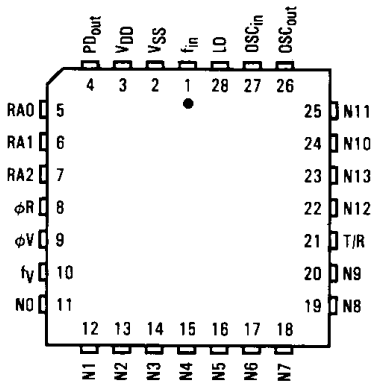


NOTE: N0 through N13 inputs and inputs RA0, RA1, and RA2 have pullup resistors not shown.

PIN ASSIGNMENTS



PLASTIC DIP



PLCC PACKAGE

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PIN DESCRIPTIONS

INPUTS

f_{in}—Frequency Input

Input to the ÷ N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0, RA1, RA2—Reference Address Inputs

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

N Inputs—N Counter Programming Inputs

These inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is least significant and N13 is most significant. Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

Transmit/Receive—Offset Adder Input

This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the VCO frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pullup resistor ensures that no connection will appear as a logic one causing no offset addition.

OSC_{in}, OSC_{out}—Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUTS

PD_{out}—Phase Detector A Output

Three-state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕV and ϕR).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕR, ϕV—Phase Detector B Outputs

These phase detector outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_V—N Counter Output

This is the buffered output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

LD—Lock Detector Output

Lock detector signal. Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

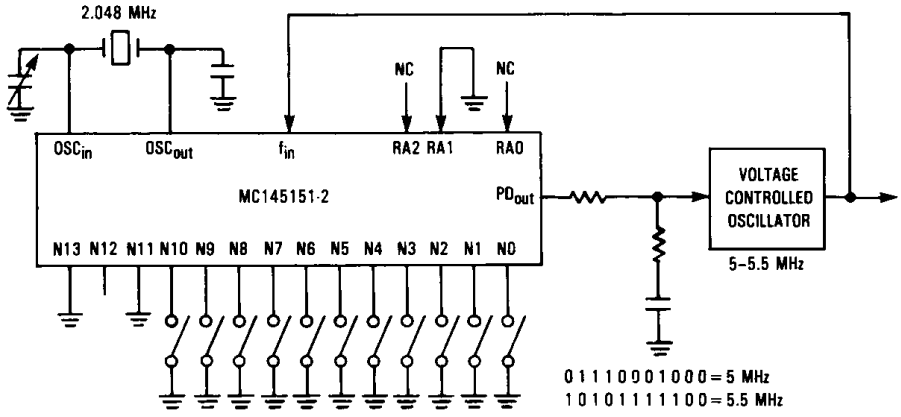
V_{DD}

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

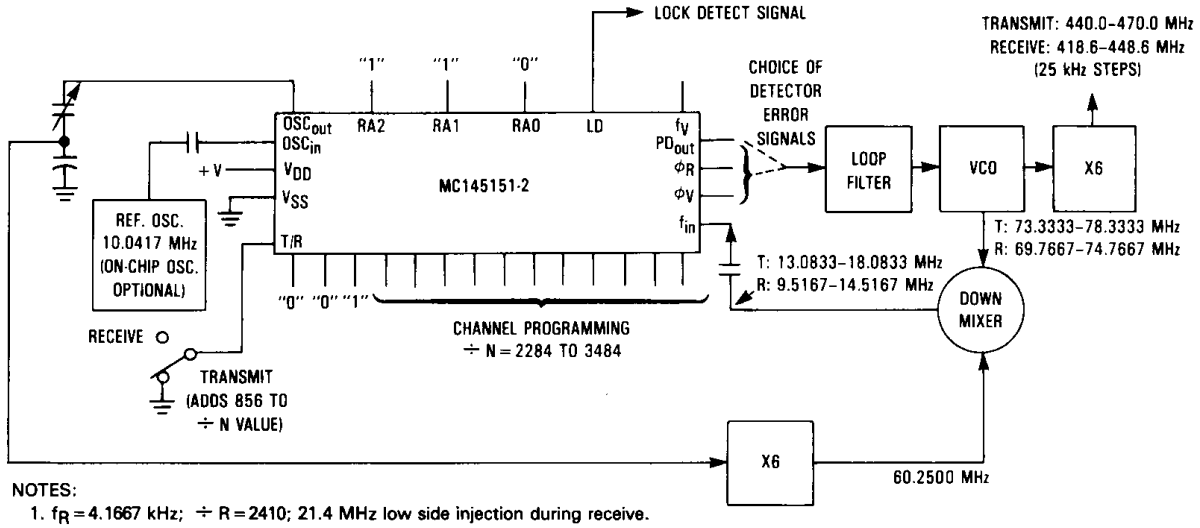
V_{SS}

The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



5 MHz to 5.5 MHz Local Oscillator Channel Spacing = 1 kHz



NOTES:
1. f_R = 4.1667 kHz; ÷ R = 2410; 21.4 MHz low side injection during receive.
2. Frequency values shown are for the 440-470 MHz band. Similar implementation applies to the 406-440 MHz band. For 470-512 MHz, consider reference oscillator frequency X9 for mixer injection signal (90.3750 MHz).

Synthesizer for Land Mobile Radio UHF Bands