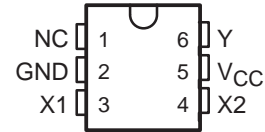


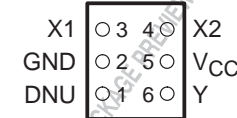
- Available in Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- One Unbuffered Inverter (SN74LVC1GU04) and One Buffered Inverter (SN74LVC1G04)
- Suitable for Commonly Used Clock Frequencies:
 - 15 kHz, 3.58 MHz, 4.43 MHz, 13 MHz, 25 MHz, 26 MHz, 27 MHz, 28 MHz
- Max t_{pd} of 2.4 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DBV OR DCK PACKAGE
(TOP VIEW)



NC – No internal connection

YEP OR YZP PACKAGE
(BOTTOM VIEW)



DNU – Do not use

description/ordering information

The SN74LVC1GX04 is designed for 1.65-V to 5.5-V V_{CC} operation. This device incorporates the SN74LVC1GU04 (inverter with unbuffered output) and the SN74LVC1G04 (inverter) functions into a single device. The LVC1GX04 is optimized for use in crystal oscillator applications.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74LVC1GX04YEPR	----
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1GX04YZPR	
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1GX04DBVR	CX4_
		Reel of 250	SN74LVC1GX04DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1GX04DCKR	D2_
		Reel of 250	SN74LVC1GX04DCKT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN74LVC1GX04
CRYSTAL OSCILLATOR DRIVER

SCES581 – JULY 2004

description/ordering information (continued)

The X1 and X2 can be connected to a crystal or resonator in oscillator applications. The device provides an additional buffered inverter (Y) for signal conditioning (see Figure 3). The additional buffered inverter improves the signal quality of the crystal oscillator output by making it rail to rail.

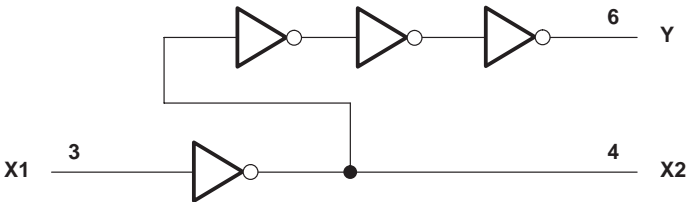
NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} (Y output only). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE

INPUT X1	OUTPUTS	
	X2	Y
H	L	H
L	H	L

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to Y output in the high-impedance or power-off state, V _O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V _O (see Notes 1 and 2)	–0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DBV package	165°C/W
DCK package	259°C/W
YEP/YZP package	123°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
		Crystal oscillator use	2		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 5.5 V	0.75 × V _{CC}		V
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 5.5 V	0.25 × V _{CC}		V
V _I	Input voltage		0	5.5	V
V _O	Output voltage	X2, Y	0	V _{CC}	V
		Y output only, Power-down mode, V _{CC} = 0 V	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4		mA
		V _{CC} = 2.3 V	−8		
		V _{CC} = 3 V	−16		
			−24		
		V _{CC} = 4.5 V	−32		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 3 V	16		
			24		
		V _{CC} = 4.5 V	32		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20		ns/V
		V _{CC} = 3.3 V ± 0.3 V	10		
		V _{CC} = 5 V ± 0.5 V	10		
T _A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC1GX04

CRYSTAL OSCILLATOR DRIVER

SCES581 – JULY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}		I _{OH} = -100 µA	1.65 V to 5.5 V	V _{CC} - 0.1			V
		I _{OH} = -4 mA	1.65 V	1.2			
		I _{OH} = -8 mA	2.3 V	1.9			
		I _{OH} = -16 mA	3 V	2.4			
		I _{OH} = -24 mA		2.3			
		I _{OH} = -32 mA	4.5 V	3.8			
V _{OL}		I _{OL} = 100 µA	1.65 V to 5.5 V	0.1			V
		I _{OL} = 4 mA	1.65 V	0.45			
		I _{OL} = 8 mA	2.3 V	0.3			
		I _{OL} = 16 mA	3 V	0.4			
		I _{OL} = 24 mA		0.55			
		I _{OL} = 32 mA	4.5 V	0.55			
I _I	X1 input	V _I = 5.5 V or GND	0 to 5.5 V			±5	µA
I _{off}	X1, Y	V _I or V _O = 5.5 V	0			±10	µA
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V			10	µA
C _i		V _I = V _{CC} or GND	3.3 V	7			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	X1	X2	1	4	0.8	2.6	0.6	2.4	0.5	2	ns
		Y‡	3.5	10	2.2	6	2	5	1.5	3.5	

‡ X2 – no external load

switching characteristics over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	X1	X2	1.1	7	0.8	4	0.8	3.7	0.8	3	ns
		Y‡	3.8	18	2	7.4	2	7.8	2	5	

‡ X2 – no external load

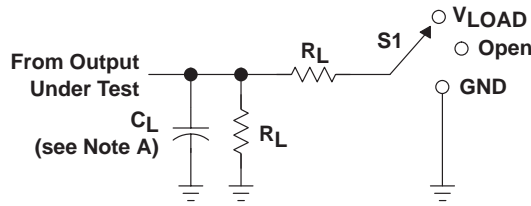
operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 5 V ± 0.5 V	UNIT
		TYP	TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz	22	22	24	35	pF



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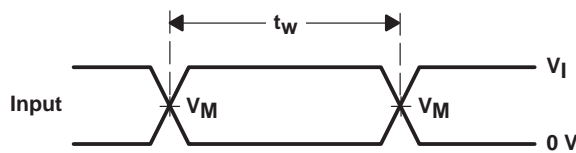
PARAMETER MEASUREMENT INFORMATION



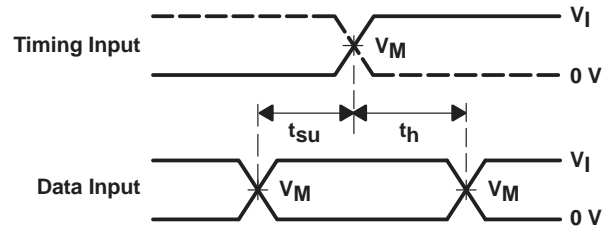
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

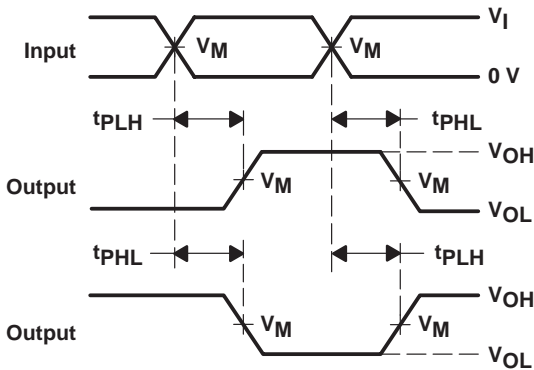
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



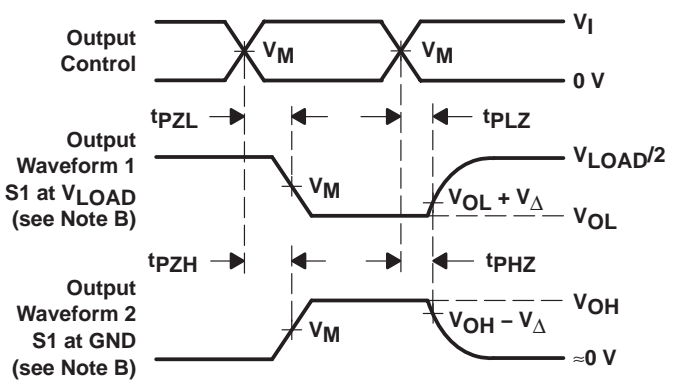
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

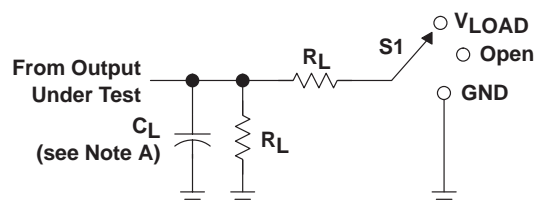
- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC1GX04 CRYSTAL OSCILLATOR DRIVER

SCES581 – JULY 2004

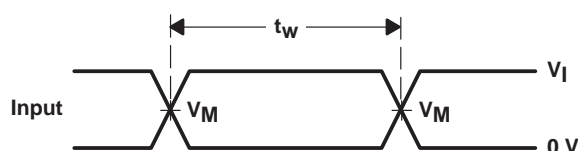
PARAMETER MEASUREMENT INFORMATION



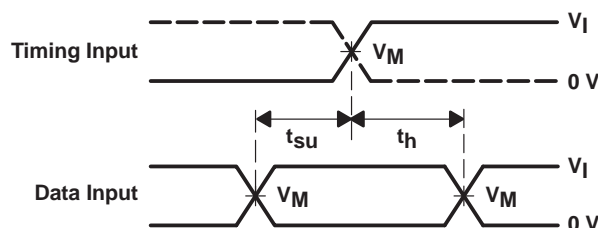
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

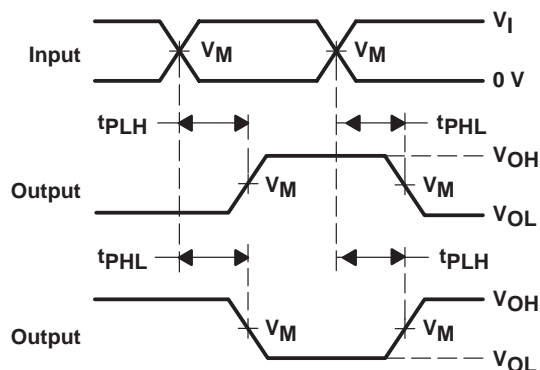
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



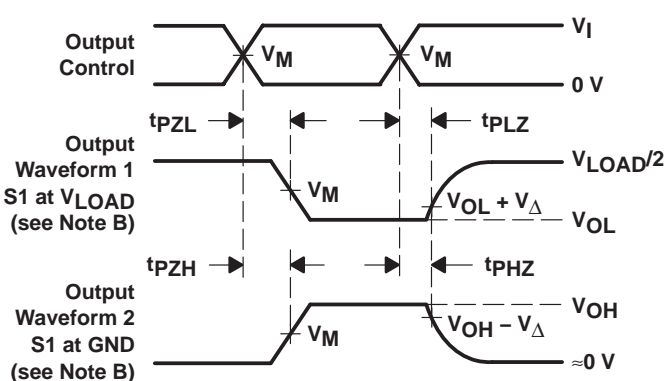
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

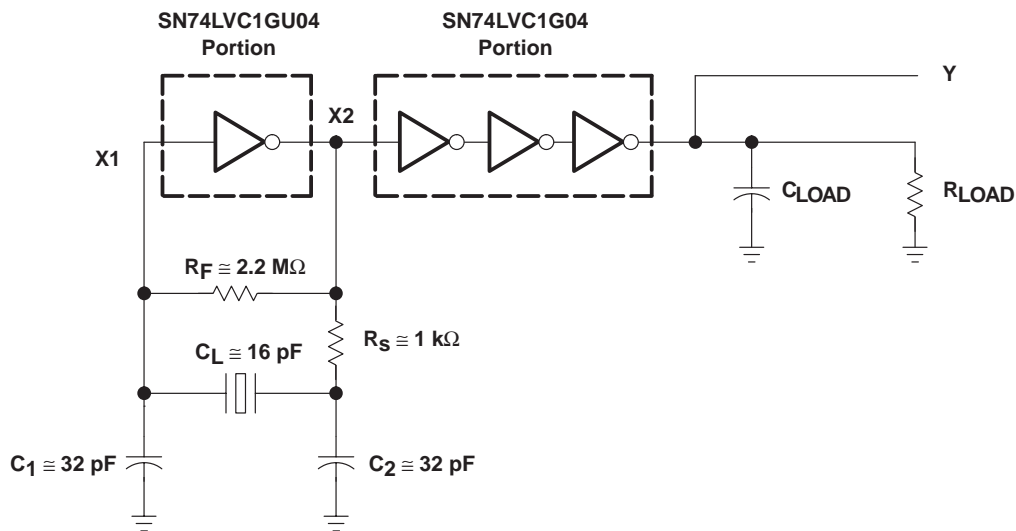
- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Figure 3 shows a typical application of the SN74LVC1X04 in a Pierce oscillator circuit. The buffered inverter (SN74LVC1G04 portion) produces a rail-to-rail voltage waveform. The recommended load for the crystal shown in this example is 16 pF. The value of the recommended load (C_L) can be found in the crystal manufacturer's data sheet.

Values of C_1 and C_2 are chosen so that $C_L = \frac{C_1 C_2}{C_1 + C_2}$ and $C_1 \cong C_2$. R_S is the current-limiting resistor and the value depends on the maximum power dissipation of the crystal. Generally, the recommended value of R_S is specified in the crystal manufacturer's data sheet and, usually, this value is approximately equal to the reactance of C_2 at resonance frequency, i.e., $R_S = X_{C_2}$. R_F is the feedback resistor that is used to bias the inverter in the linear region of operation. Usually, the value is chosen to be within 1 M Ω to 10 M Ω .



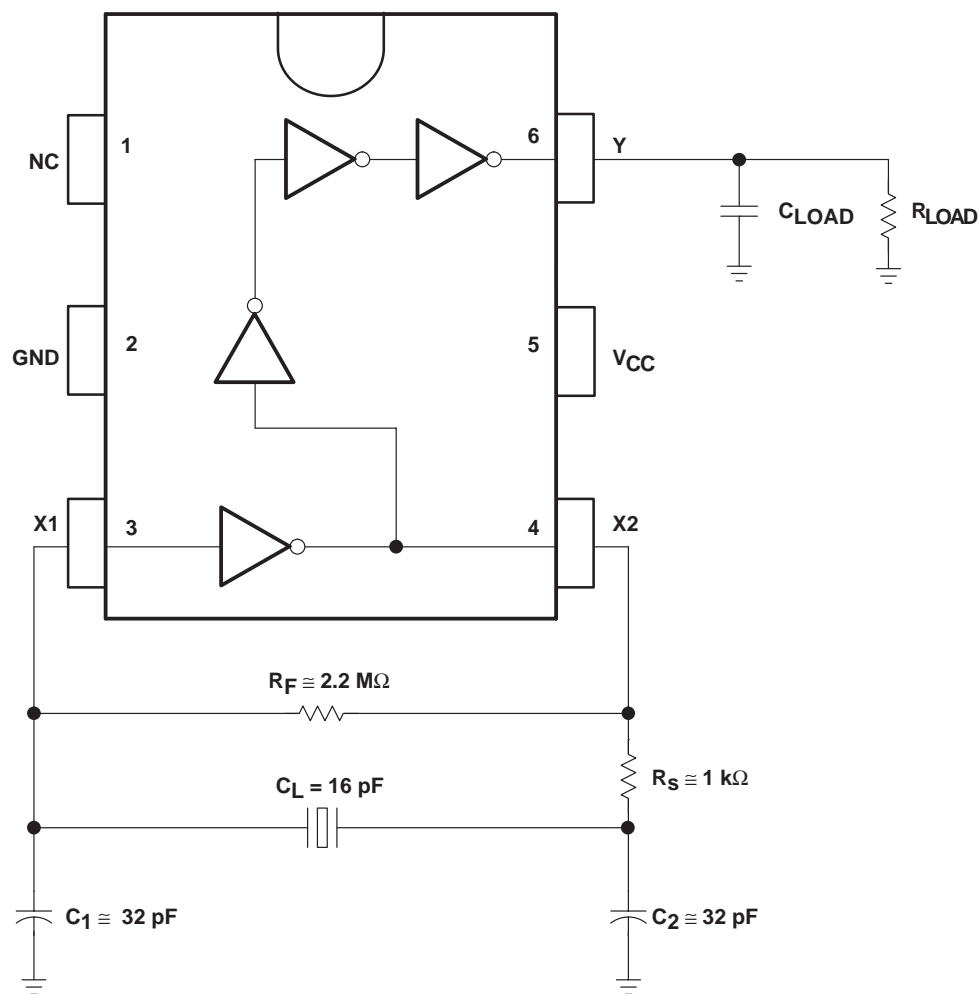
a) Logic Diagram View

Figure 3. Oscillator Circuit

SN74LVC1GX04 CRYSTAL OSCILLATOR DRIVER

SCES581 – JULY 2004

APPLICATION INFORMATION



b) Oscillator Circuit in DBV or DCK Pinout

Figure 3. Oscillator Circuit (Continued)

practical design tips

- The open-loop gain of the unbuffered inverter decreases as power-supply voltage decreases. This decreases the closed-loop gain of the oscillator circuit. The value of R_S can be decreased to increase the closed-loop gain, while maintaining the power dissipation of the crystal within the maximum limit.
- R_S and C_2 form a low-pass filter and reduce spurious oscillations. Component values can be adjusted, based on the desired cutoff frequency.
- C_2 can be increased over C_1 to increase the phase shift and help in start-up of the oscillator. Increasing C_2 may affect the duty cycle of the output voltage.
- At high frequency, phase shift due to R_S becomes significant. In this case, R_S can be replaced by a capacitor to reduce the phase shift.

APPLICATION INFORMATION

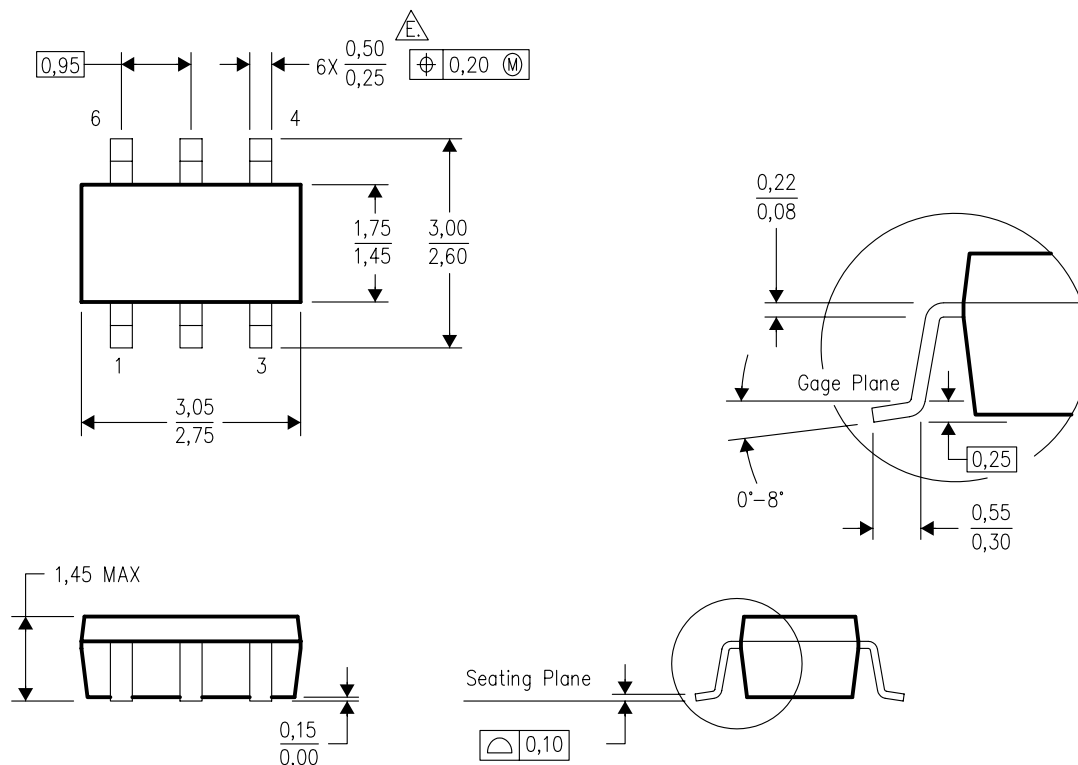
testing

After the selection of proper component values, the oscillator circuit should be tested using these components. To ensure that the oscillator circuit performs within the recommended operating conditions, follow these steps:


1. Without a crystal, the oscillator circuit should not oscillate. To check this, the crystal can be replaced by its equivalent parallel-resonant resistance.
2. When the power-supply voltage drops, the closed-loop gain of the oscillator circuit reduces. Ensure that the circuit oscillates at the appropriate frequency at the lowest V_{CC} and highest V_{CC} .
3. Ensure that the duty cycle, start-up time, and frequency drift over time is within the system requirements.

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

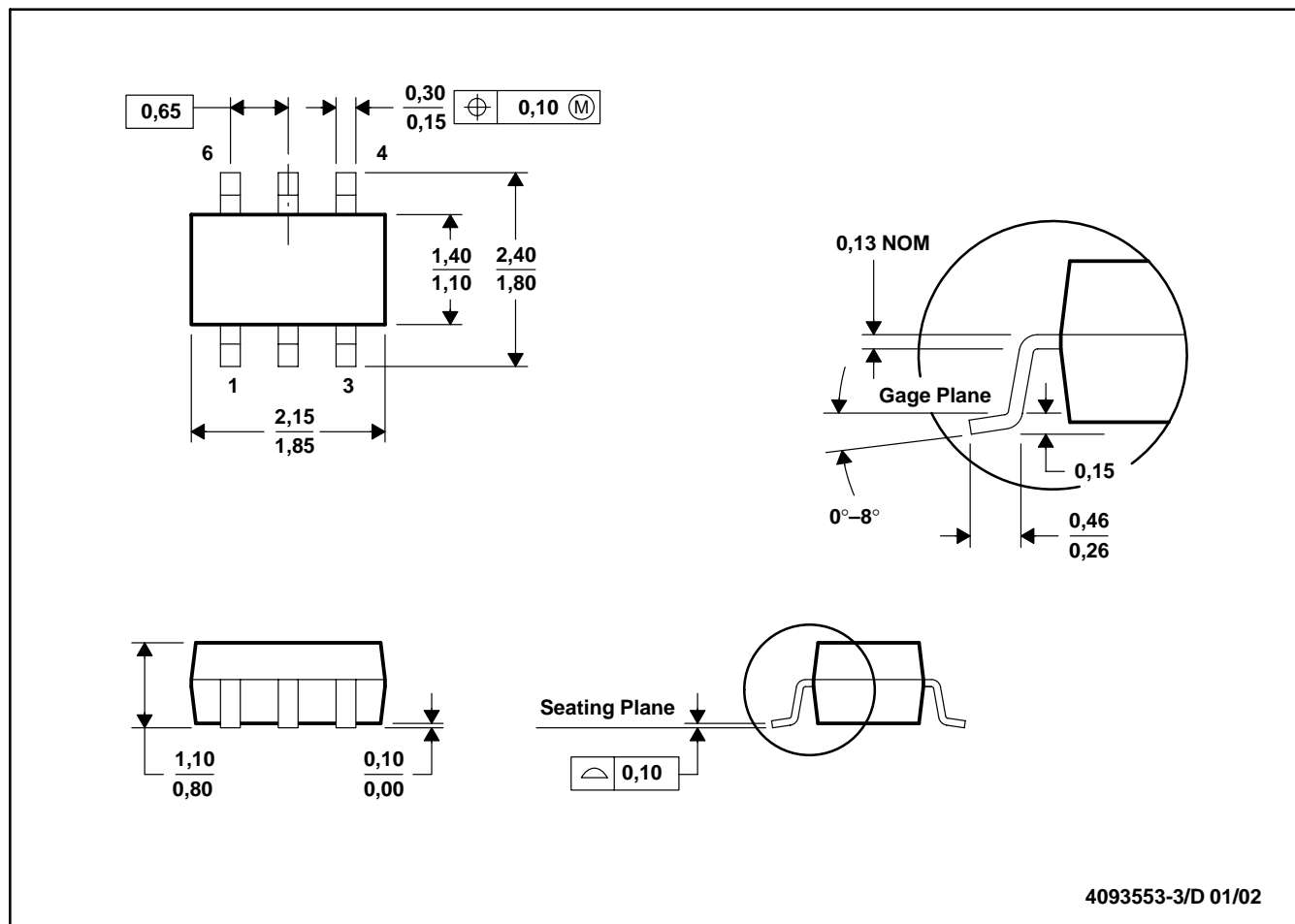


4073253-5/1 04/2005

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
 -  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DCK (R-PDSO-G6)

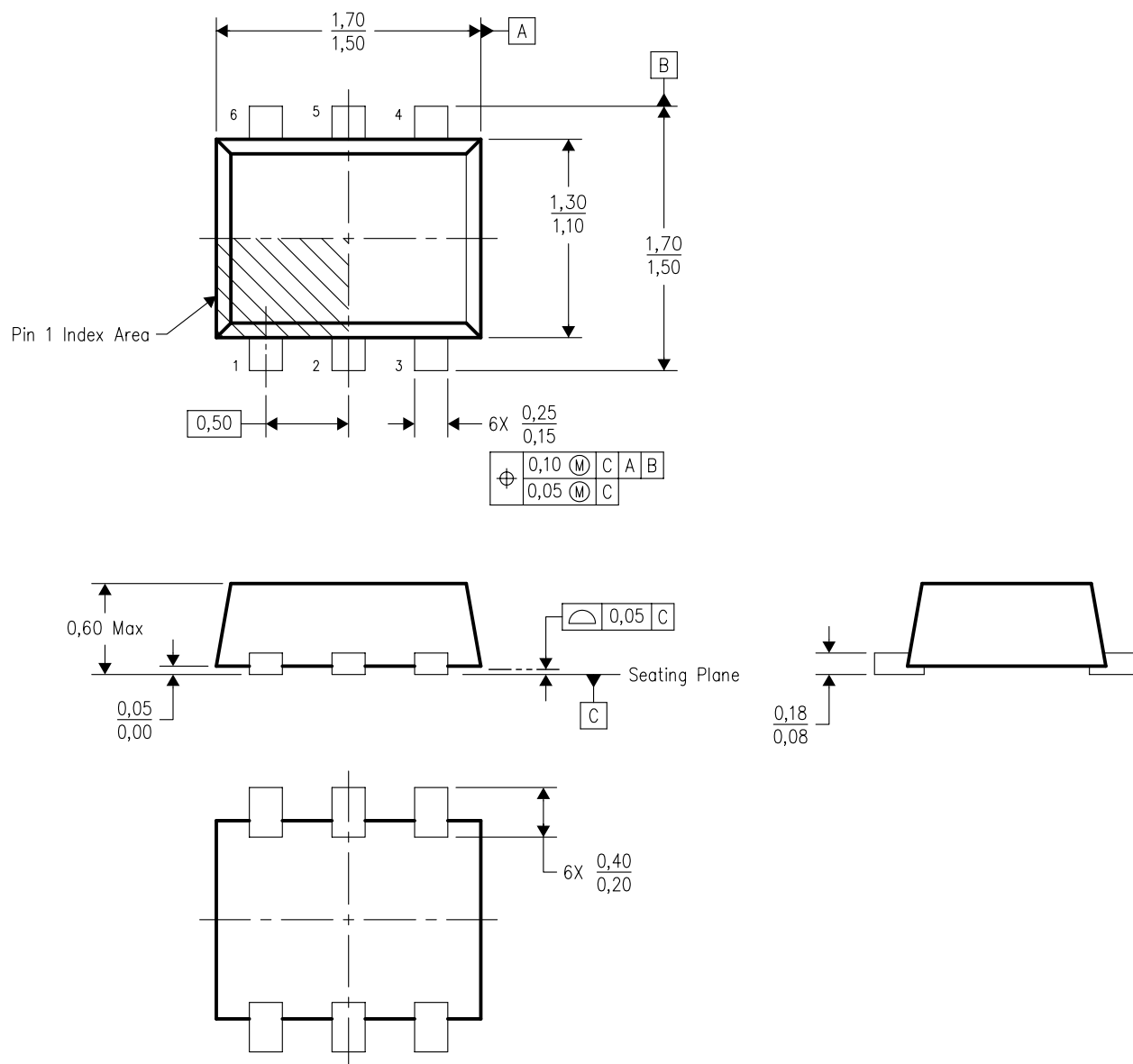
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-203

DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE



4205622-3/B 07/2004

- NOTES:
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 - B. This drawing is subject to change without notice.
 - C. JEDEC package registration is pending.

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