

TLV2401, TLV2402, TLV2404

FAMILY OF 900-nA/Ch RAIL-TO-RAIL INPUT/OUTPUT

OPERATIONAL AMPLIFIERS WITH REVERSE BATTERY PROTECTION

SLOS244 – FEBRUARY 2000

- Micro-Power Operation . . . $< 1 \mu\text{A}/\text{Channel}$
- Input Common-Mode Range Exceeds the Rails . . . -0.1 V to $V_{\text{CC}} + 5 \text{ V}$
- Rail-to-Rail Input/Output
- Gain Bandwidth Product . . . 5.5 kHz
- Supply Voltage Range . . . 2.5 V to 16 V
- Specified Temperature Range
 - $T_A = 0^\circ\text{C}$ to 70°C . . . Commercial Grade
 - $T_A = -40^\circ\text{C}$ to 125°C . . . Industrial Grade
- Ultra-Small Packaging
 - 5-Pin SOT-23 (TLV2401)
 - 8-Pin MSOP (TLV2402)
- Universal OpAmp EVM

description

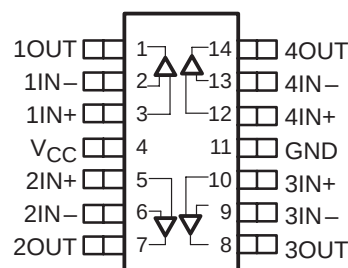
The TLV240x family of single-supply operational amplifiers has the lowest supply current available today at only 900 nA per channel. Added to this is reverse battery protection making the device even more ideal for battery powered systems. And for harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

The low supply current is coupled with extremely low input bias currents enabling them to be used with mega- Ω resistors making them ideal for portable, long active life, applications. DC accuracy is ensured with a low typical offset voltage as low as $390 \mu\text{V}$, CMRR of 120 dB and minimum open loop gain of 130 V/mV at 2.7 V.

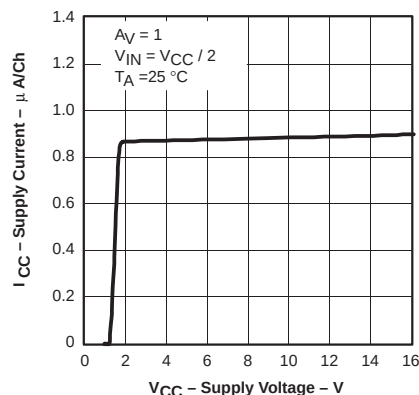
The maximum recommended supply voltage is as high as 16 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V and 15 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micro-power microcontrollers available today including TI's MSP430.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in TSSOP.

TLV2404
D, N, OR PW PACKAGE
(TOP VIEW)



SUPPLY CURRENT
vs
SUPPLY VOLTAGE



FAMILY PACKAGE TABLE

DEVICE	NO. OF Ch	PACKAGE TYPES					UNIVERSAL EVM
		PDIP	SOIC	SOT-23	TSSOP	MSOP	
TLV2401†	1	8	8	5	—	—	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2402†	2	8	8	—	—	8	
TLV2404	4	14	14	—	14	—	

† This device is in the Product Preview stage of development. Contact your local TI sales office for more information



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TLV2401 AVAILABLE OPTIONS

T_A	V_{IOmax} AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D)	SOT-23 [†] (DBV)	PLASTIC DIP (P)
0°C to 70°C	1500 μ V	TLV2401CD	TLV2401CDBV	TLV2401CP
-40°C to 125°C		TLV2401ID	TLV2401IDBV	TLV2401IP

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2401CDR).

TLV2402 AVAILABLE OPTIONS

T_A	V_{IOmax} AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE [†] (D)	MSOP (DGK)	PLASTIC DIP (P)
0°C to 70°C	1500 μ V	TLV2402CD	TLV2402CDGK	TLV2402CP
-40°C to 125°C		TLV2402ID	TLV2402IDGK	TLV2402IP

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2402CDR).

TLV2404 AVAILABLE OPTIONS

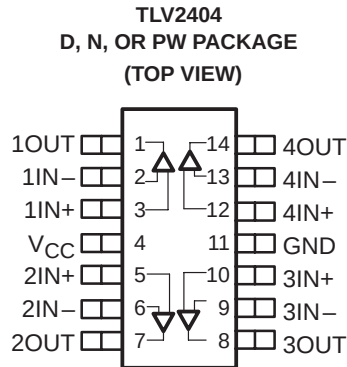
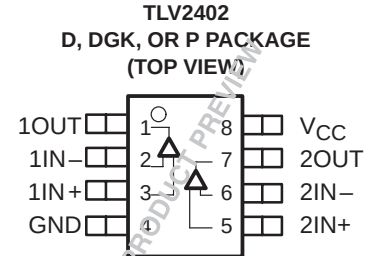
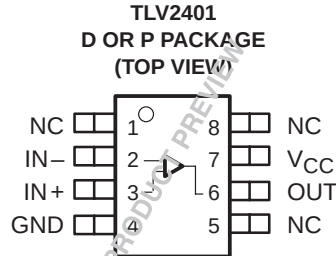
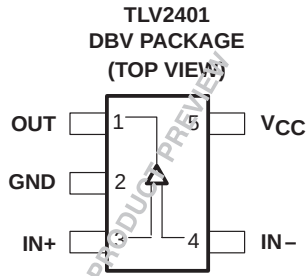
T_A	V_{IOmax} AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	1500 μ V	TLV2404CD	TLV2404CN	TLV2404CPW
-40°C to 125°C		TLV2404ID	TLV2404IN	TLV2404IPW

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2404CDR).

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TLV240x PACKAGE PINOUTS



NC – No internal connection

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	17 V
Differential input voltage, V_{ID}	± 20 V
Input current, I_I (any input)	± 10 mA
Output current, I_O	± 10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 125°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND

DISSIPATION RATING TABLE

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.6	1022 mW
DBV (5)	55	324.1	385 mW
DGK (8)	54.23	259.96	481 mW
N (14)	32	78	1600 mW
P (8)	41	104	1200 mW
PW (14)	29.3	173.6	720 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}	Single supply	2.5	16	V
	Split supply	± 1.25	± 8	
Common-mode input voltage range, V_{ICR}		–0.1	$V_{CC}+5$	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	–40	125	



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electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 15 V (unless otherwise noted)

dc performance

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$V_O = V_{CC}/2 \text{ V}$, $V_{IC} = V_{CC}/2 \text{ V}$, $R_S = 50 \Omega$	TLV240x	25°C	390	1200	μV
αV_{IO} Offset voltage draft			Full range		1500	
CMRR Common-mode rejection ratio	$V_{IC} = 0 \text{ to } V_{CC}$, $R_S = 50 \Omega$	25°C	70	120		dB
		Full range	65			
A_{VD} Large-signal differential voltage amplification	$V_{O(pp)} = 4 \text{ V}$, $R_L = 500 \text{ k}\Omega$	$V_{CC} = 2.7 \text{ V}$	25°C	130	400	V/mV
			Full range	30		
		$V_{CC} = 5 \text{ V}$	25°C	300	1000	
			Full range	100		
		$V_{CC} = 15 \text{ V}$	25°C	1000	1800	
			Full range	120		

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

input characteristics

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
V_{ICR} Common-mode input voltage range	Measured over CMRR range, $R_S = 50 \Omega$	$V_{CC} = 2.7 \text{ V}$	25°C or Full range	–0.1 to 7.7		V
		$V_{CC} = 5 \text{ V}$	25°C or Full range	–0.1 to 10		V
		$V_{CC} = 15 \text{ V}$	25°C or Full range	–0.1 to 20		V
I_{IO} Input offset current	$V_O = V_{CC}/2 \text{ V}$, $V_{IC} = V_{CC}/2 \text{ V}$, $R_S = 50 \Omega$	TLV240xC	25°C	25	250	pA
		TLV240xI	Full range		300	
					400	
I_{IB} Input bias current		TLV240xC	25°C	100	300	pA
		TLV240xI	Full range		350	
					900	
$r_{i(d)}$ Differential input resistance		25°C		300		M Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 100 \text{ kHz}$	25°C		3		pF

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electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 15 V (unless otherwise noted) (continued)

output characteristics

PARAMETER	TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	$V_{IC} = V_{CC}/2$, $I_{OH} = -2 \mu\text{A}$	$V_{CC} = 2.7 \text{ V}$	25°C	2.65	2.68		V
			Full range	2.63			
		$V_{CC} = 5 \text{ V}$	25°C	4.95	4.98		
			Full range	4.93			
		$V_{CC} = 15 \text{ V}$	25°C	14.95	14.98		
			Full range	14.93			
	$V_{IC} = V_{CC}/2$, $I_{OH} = -50 \mu\text{A}$	$V_{CC} = 2.7 \text{ V}$	25°C	2.62	2.65		
			Full range	2.6			
		$V_{CC} = 5 \text{ V}$	25°C	4.92	4.95		
			Full range	4.9			
		$V_{CC} = 15 \text{ V}$	25°C	14.92	14.95		
			Full range	14.9			
V_{OL} Low-level output voltage	$V_{IC} = V_{CC}/2$, $I_{OL} = 2 \mu\text{A}$	25°C		90	150		mV
		Full range			180		
	$V_{IC} = V_{CC}/2$, $I_{OL} = 50 \mu\text{A}$	25°C		180	230		
		Full range			260		
I_O Output current	$V_O = 0.5 \text{ V}$ from rail		25°C	± 200			μA
Z_O Closed-loop output impedance	$f = 100 \text{ Hz}$, $A_V = 10$		25°C	1200			Ω

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

power supply

PARAMETER	TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
I_{CC} Supply current (per channel)	$V_O = V_{CC}/2$	$V_{CC} = 2.7 \text{ V}$ or 5 V	25°C		880	950	nA
			Full range			1290	
		$V_{CC} = 15 \text{ V}$	25°C		900	990	
			Full range			1350	
PSRR Power supply rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC} = 2.7$ to 5 V , $V_{IC} = V_{CC}/2 \text{ V}$	No load,	25°C	100	120		dB
			Full range	100			
	$V_{CC} = 5$ to 15 V , $V_{IC} = V_{CC}/2 \text{ V}$	No load,	25°C	100	120		
			Full range	100			

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

dynamic performance

PARAMETER	TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
UGBW Unity gain bandwidth	$R_L = 500 \text{ k}\Omega$,	$C_L = 100 \text{ pF}$	25°C		5.5		kHz
SR Slew rate at unity gain	$V_{O(pp)} = 0.8 \text{ V}$, $R_L = 500 \text{ k}\Omega$,	$C_L = 100 \text{ pF}$	25°C		2.5		V/ms
ϕ_M Phase margin	$R_L = 500 \text{ k}\Omega$, $C_L = 100 \text{ pF}$		25°C		60		
Gain margin					15		dB
t_s Settling time	$V_{CC} = 2.7$ or 5 V , $V_{(STEP)PP} = 1 \text{ V}$, $A_V = -1$, $C_L = 100 \text{ pF}$, $R_L = 100 \text{ k}\Omega$	0.1%	25°C		1.84		ms
		0.1%			6.1		
	$V_{CC} = 15 \text{ V}$, $V_{(STEP)PP} = 1 \text{ V}$, $A_V = -1$, $C_L = 100 \text{ pF}$, $R_L = 100 \text{ k}\Omega$	0.01%			32		

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.



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electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 15 V (unless otherwise noted) (continued)

noise/distortion performance

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
V_n	Equivalent input noise voltage	$f = 10 \text{ Hz}$	25°C		800		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 100 \text{ Hz}$			500		
I_n	Equivalent input noise current	$f = 100 \text{ Hz}$			8		$\text{fA}/\sqrt{\text{Hz}}$

† Full range is 0°C to 70°C for the C suffix and -40°C to 125°C for the I suffix. If not specified, full range is -40°C to 125°C .

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input Offset Voltage	vs Common-mode input voltage	1, 2, 3
I_{IB}	Input Bias Current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
I_{IO}	Input Offset Current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
CMRR	Common-mode rejection ratio	vs Frequency	10
V_{OH}	High-level output voltage	vs High-level output current	11, 13, 15
V_{OL}	Low-level output voltage	vs Low-level output current	12, 14, 16
$V_{O(PP)}$	Output voltage peak-to-peak	vs Frequency	17
Z_o	Output impedance	vs Frequency	18
I_{CC}	Supply current	vs Supply voltage	19
PSRR	Power supply rejection ratio	vs Frequency	20
A_{VD}	Differential voltage gain	vs Frequency	21
	Phase	vs Frequency	21
	Gain-bandwidth product	vs Supply voltage	22
SR	Slew rate	vs Free-air temperature	23
ϕ_m	Phase margin	vs Load capacitance	24
	Gain margin	vs Load capacitance	25
	Large-signal voltage follower		26, 27, 28
	Small-signal voltage follower		29
	Large-signal inverted pulse response		30, 31, 32
	Small-signal inverted pulse response		33
	Crosstalk	vs Frequency	34



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TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT
VOLTAGE

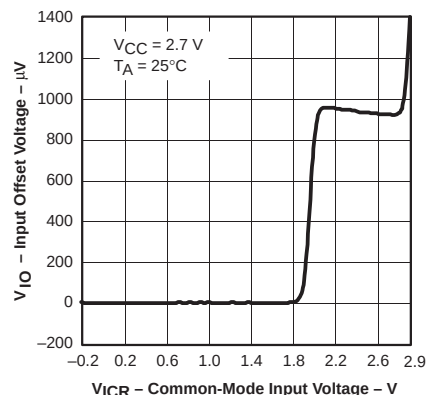


Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT
VOLTAGE

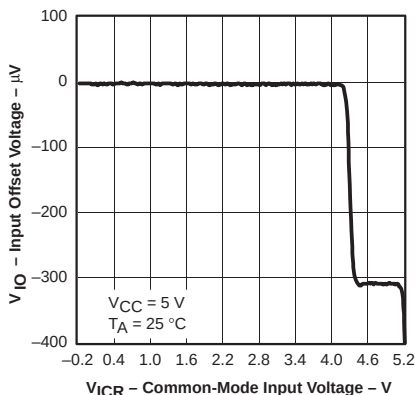


Figure 2

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT
VOLTAGE

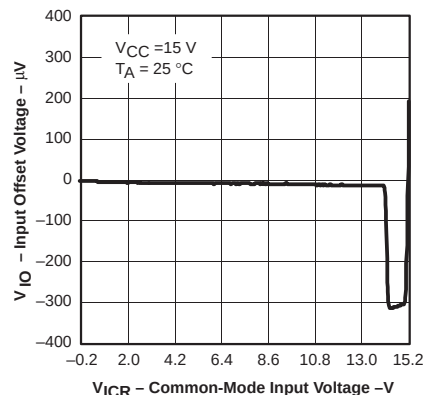


Figure 3

INPUT BIAS / OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

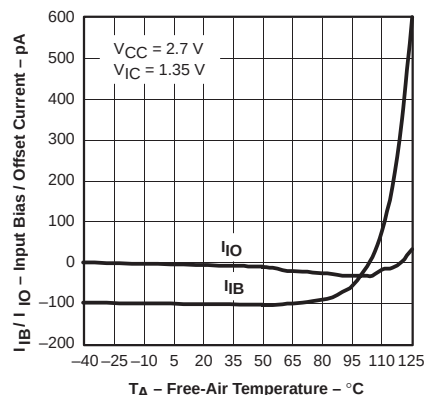


Figure 4

INPUT BIAS / OFFSET CURRENT
vs
COMMON MODE INPUT
VOLTAGE

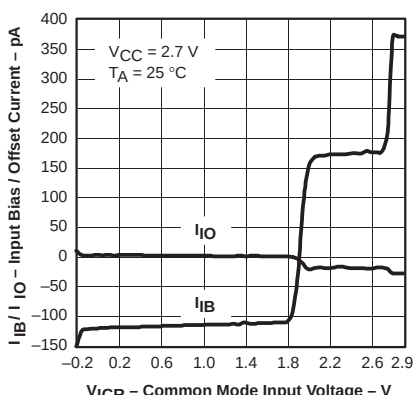


Figure 5

INPUT BIAS / OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

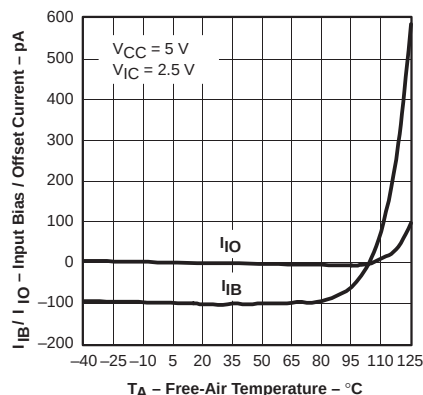


Figure 6

INPUT BIAS / OFFSET CURRENT
vs
COMMON-MODE INPUT
VOLTAGE

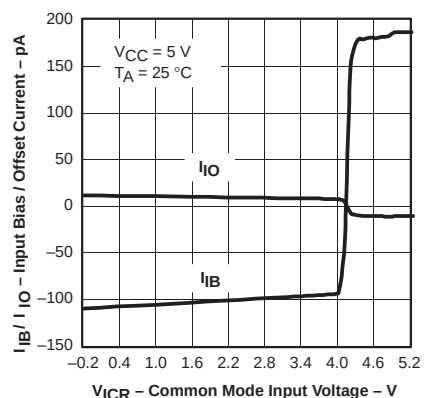


Figure 7

INPUT BIAS / OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

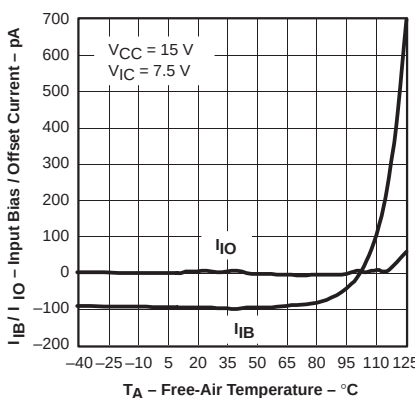


Figure 8

INPUT BIAS / OFFSET CURRENT
vs
COMMON-MODE INPUT
VOLTAGE

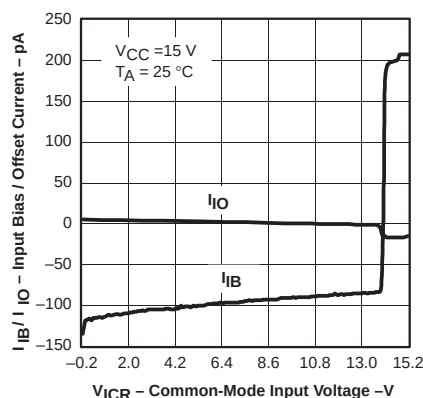


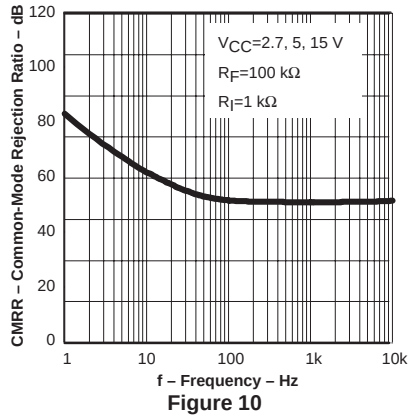
Figure 9



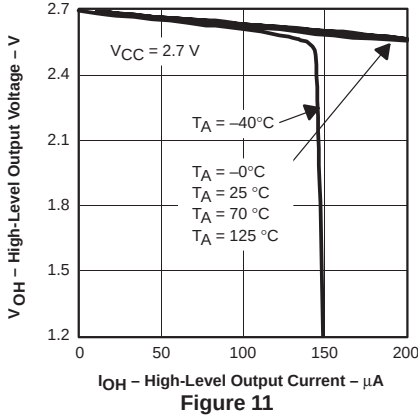
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TYPICAL CHARACTERISTICS

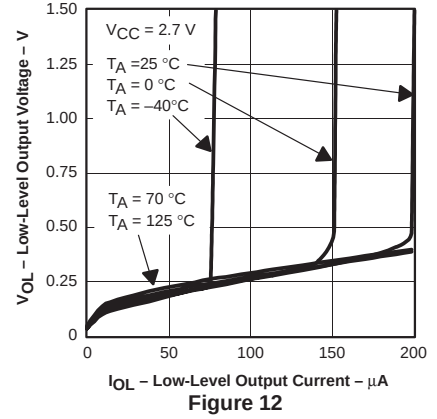
**COMMON-MODE REJECTION RATIO
VS
FREQUENCY**



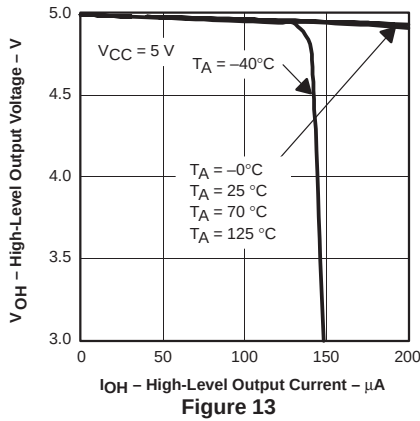
**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**



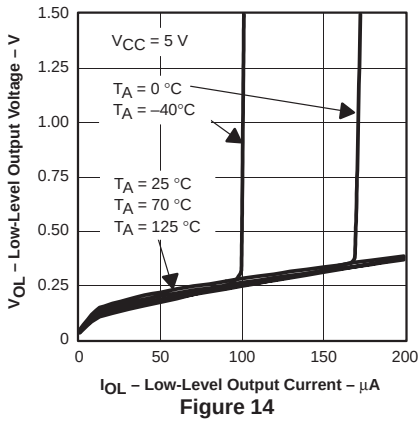
**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**



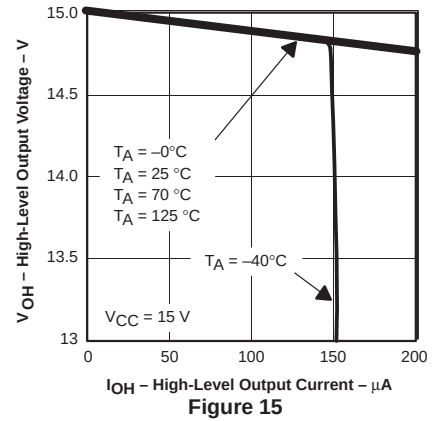
**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**



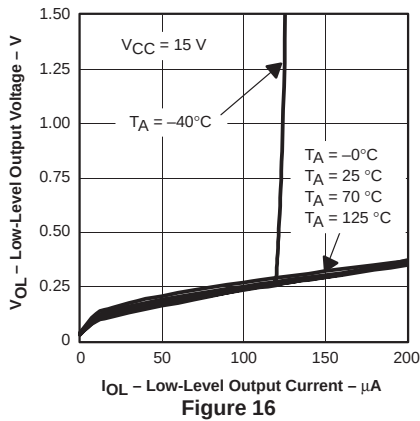
**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**



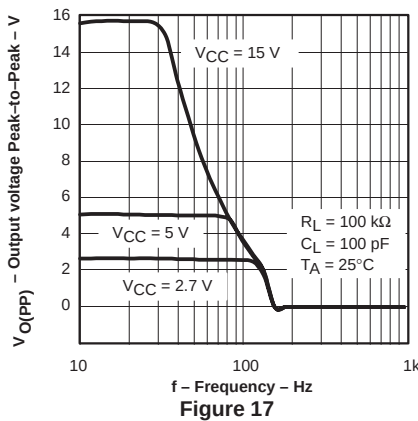
**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**



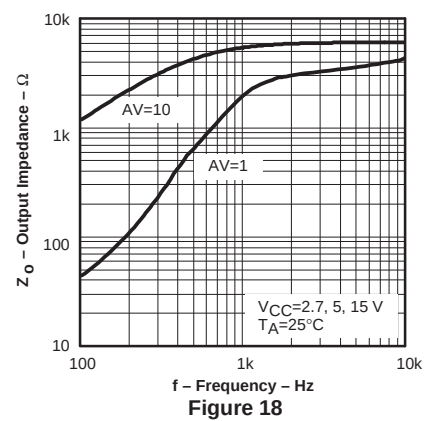
**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**



**OUTPUT VOLTAGE
PEAK-TO-PEAK
VS
FREQUENCY**



**OUTPUT IMPEDANCE
VS
FREQUENCY**



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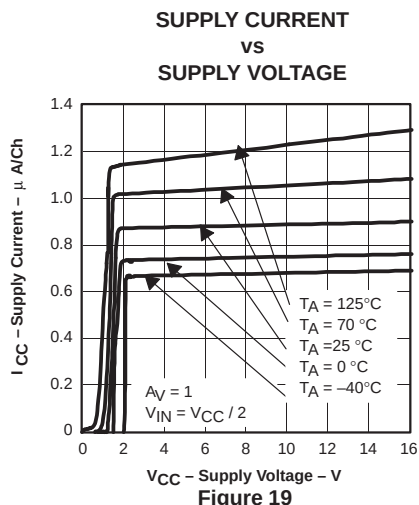


Figure 19

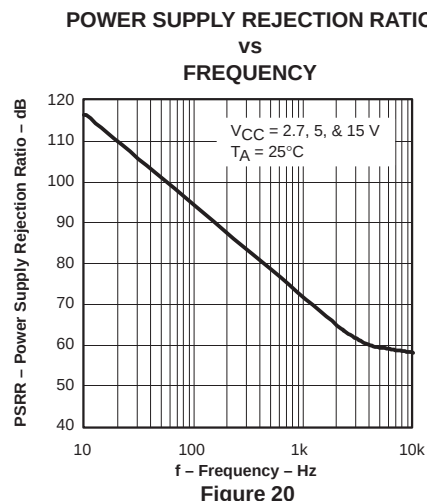


Figure 20

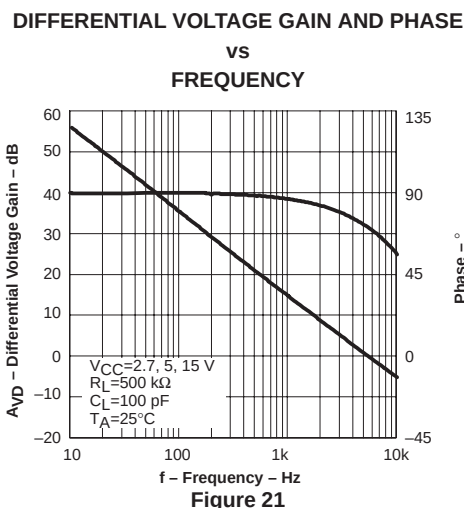


Figure 21

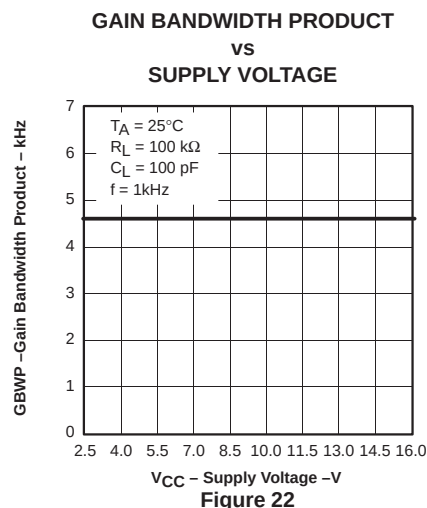


Figure 22

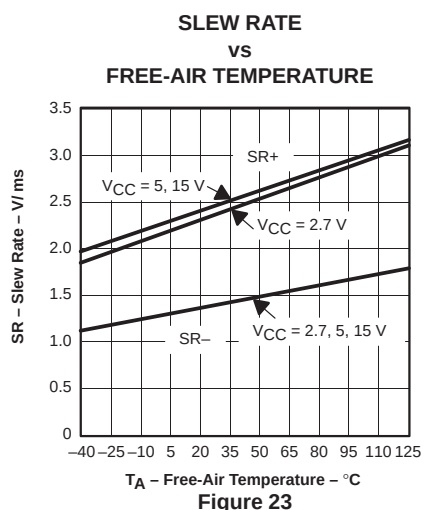


Figure 23

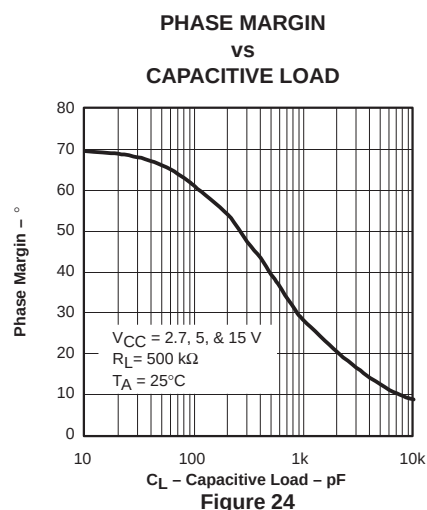


Figure 24

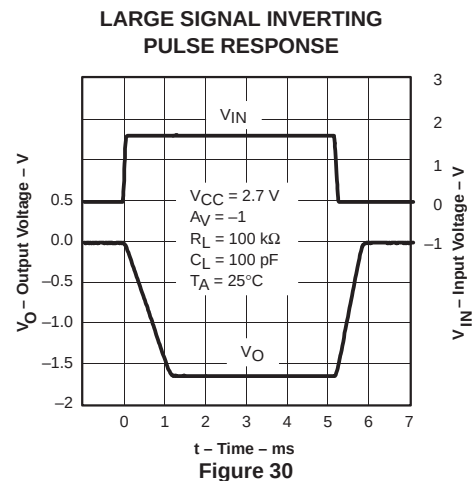
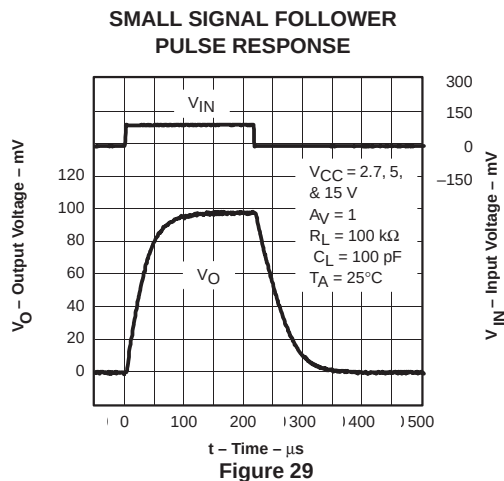
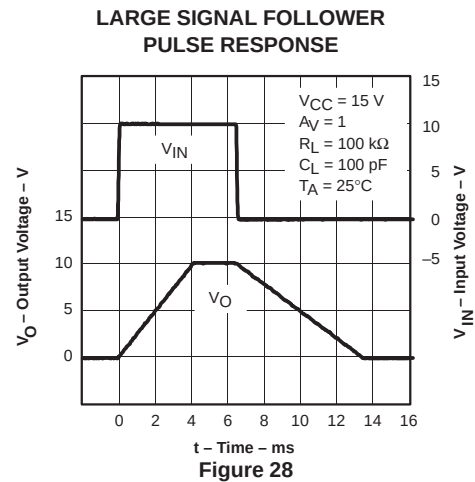
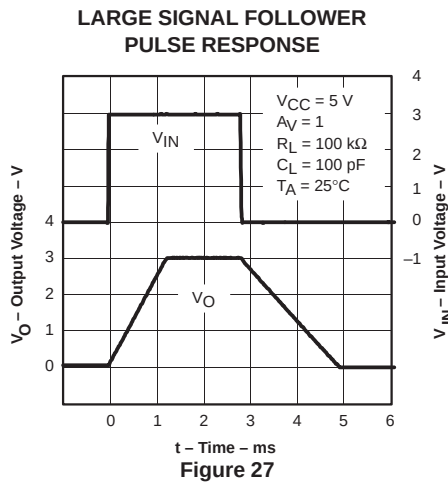
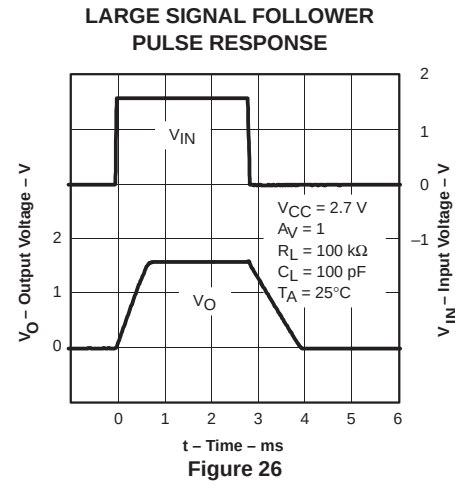
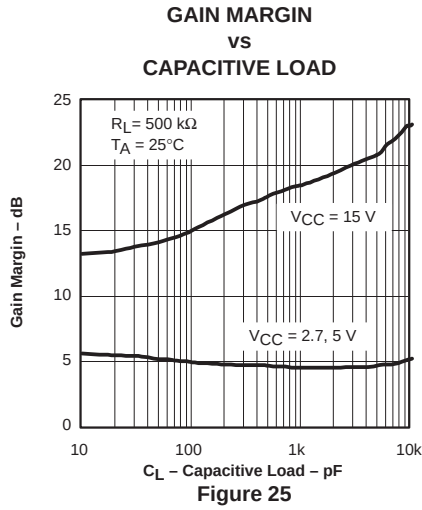


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TLV2401, TLV2402, TLV2404
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TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

LARGE SIGNAL INVERTING PULSE RESPONSE

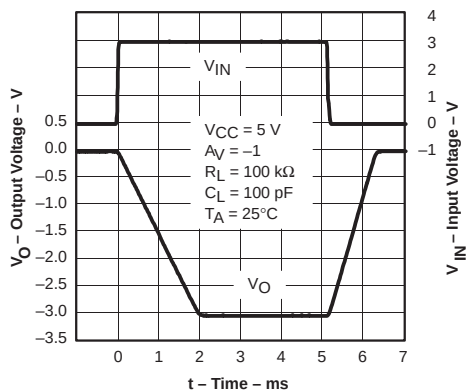


Figure 31

LARGE SIGNAL INVERTING PULSE RESPONSE

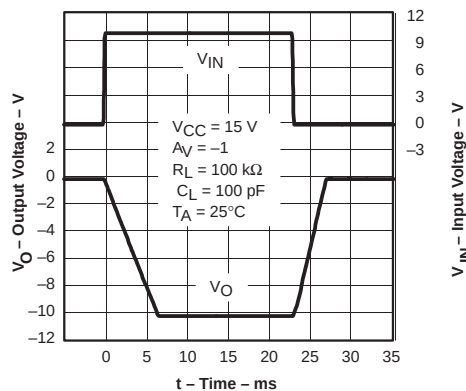


Figure 32

SMALL SIGNAL INVERTING PULSE RESPONSE

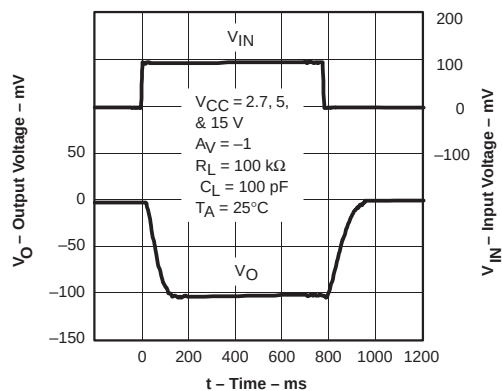


Figure 33

CROSSTALK vs FREQUENCY

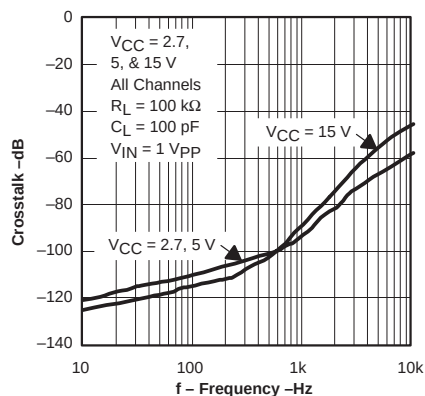


Figure 34

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

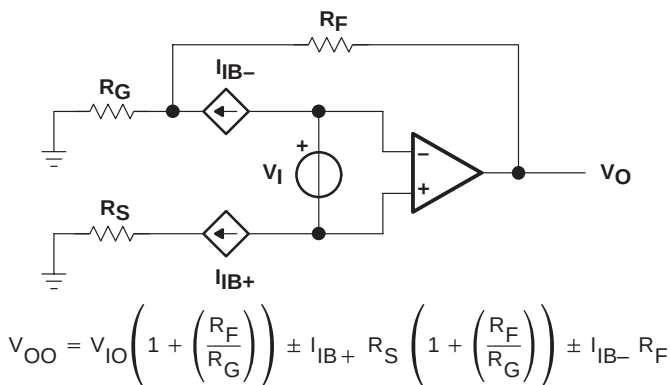


Figure 35. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 36).

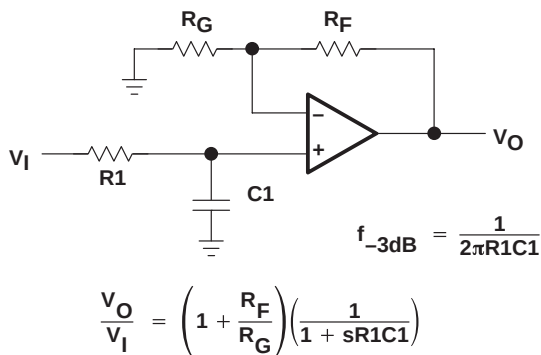


Figure 36. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

APPLICATION INFORMATION

general configurations (continued)

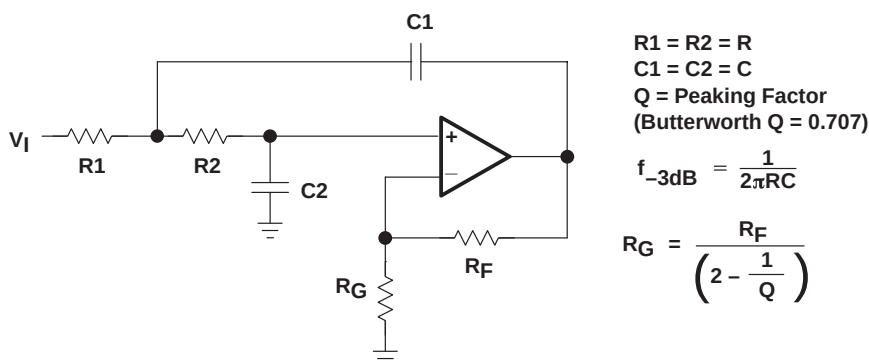


Figure 37. 2-Pole Low-Pass Sallen-Key Filter

circuit layout considerations

To achieve the levels of high performance of the TLV240x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

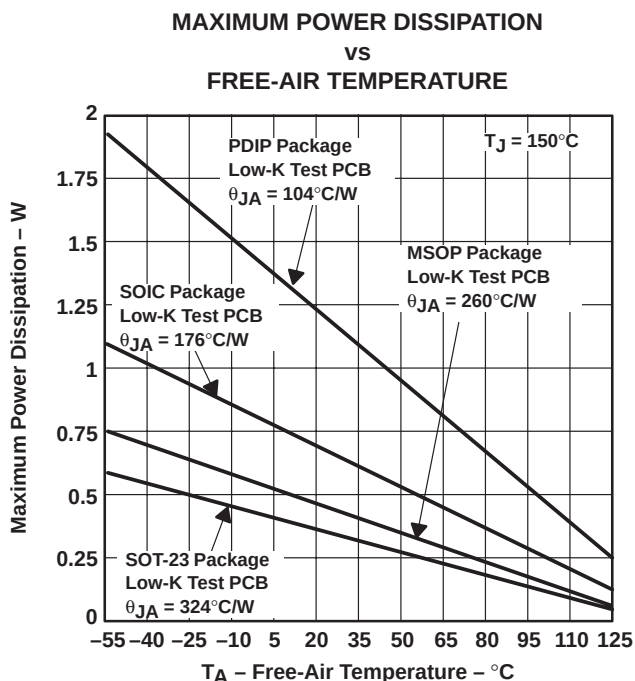
general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 38 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- P_D = Maximum power dissipation of THS240x IC (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} = Thermal coefficient from junction to case
- θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 38. Maximum Power Dissipation vs Free-Air Temperature

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macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 39 are generated using the TLV240x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

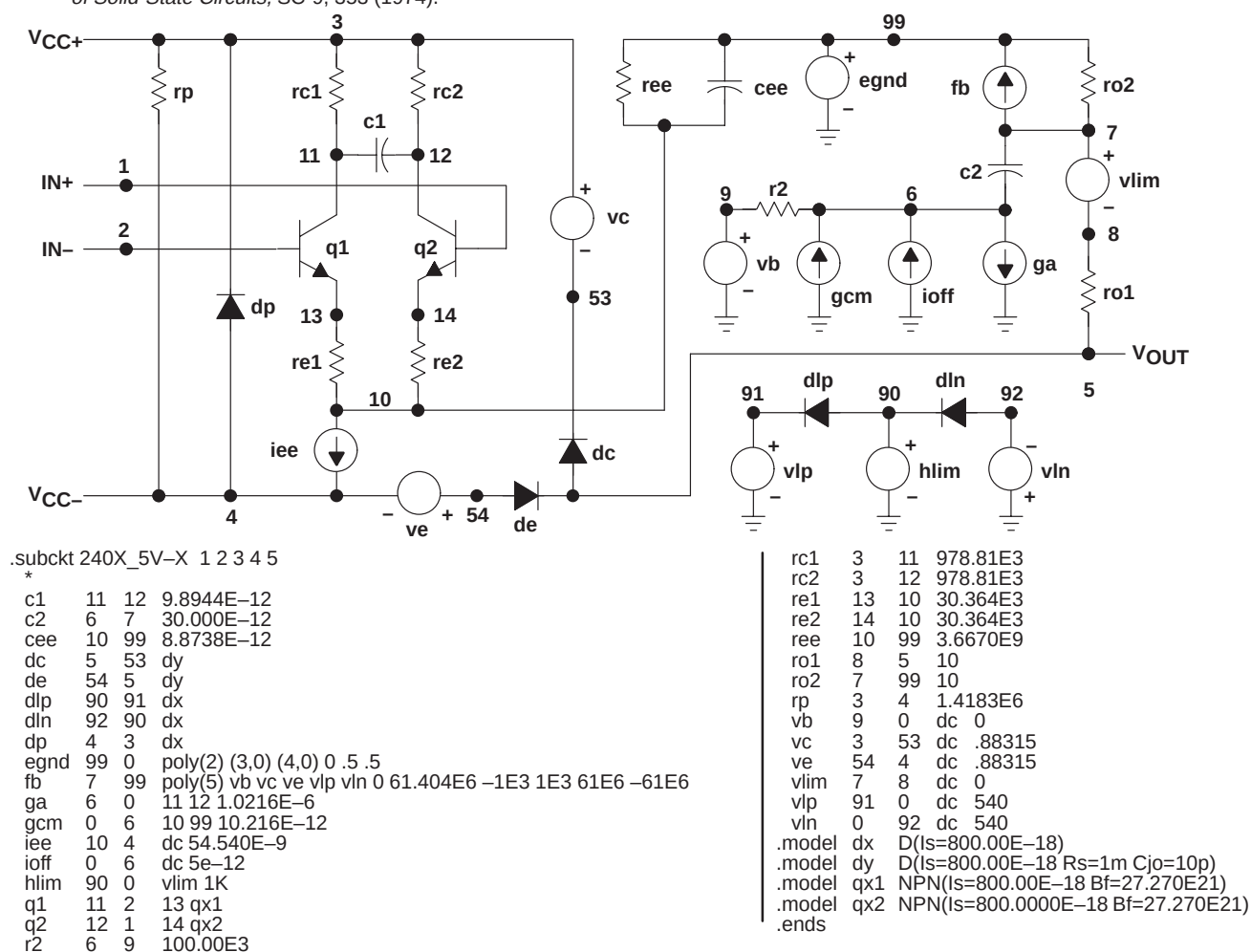


Figure 39. Boyle Macromodels and Subcircuit

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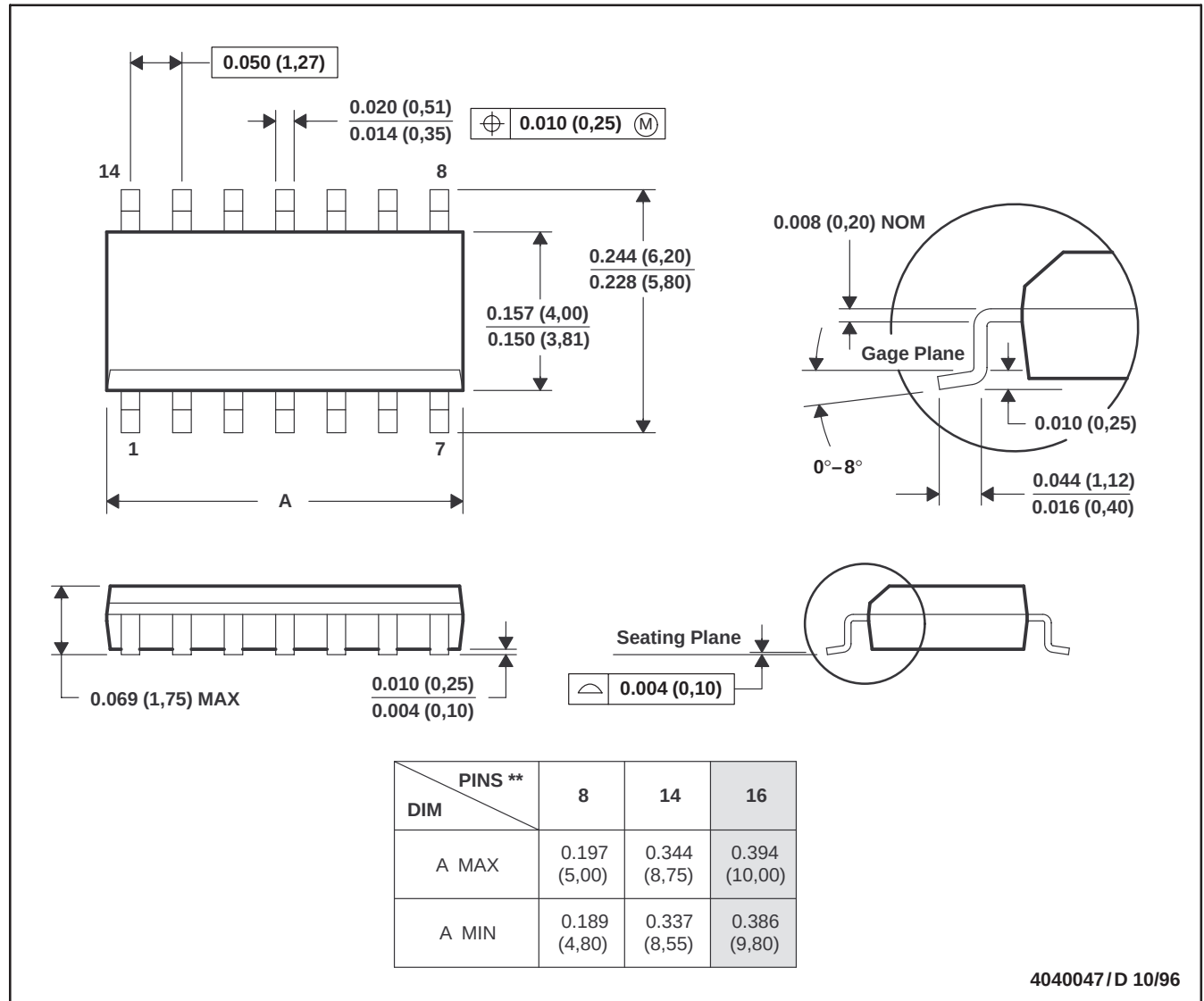
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MECHANICAL DATA

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

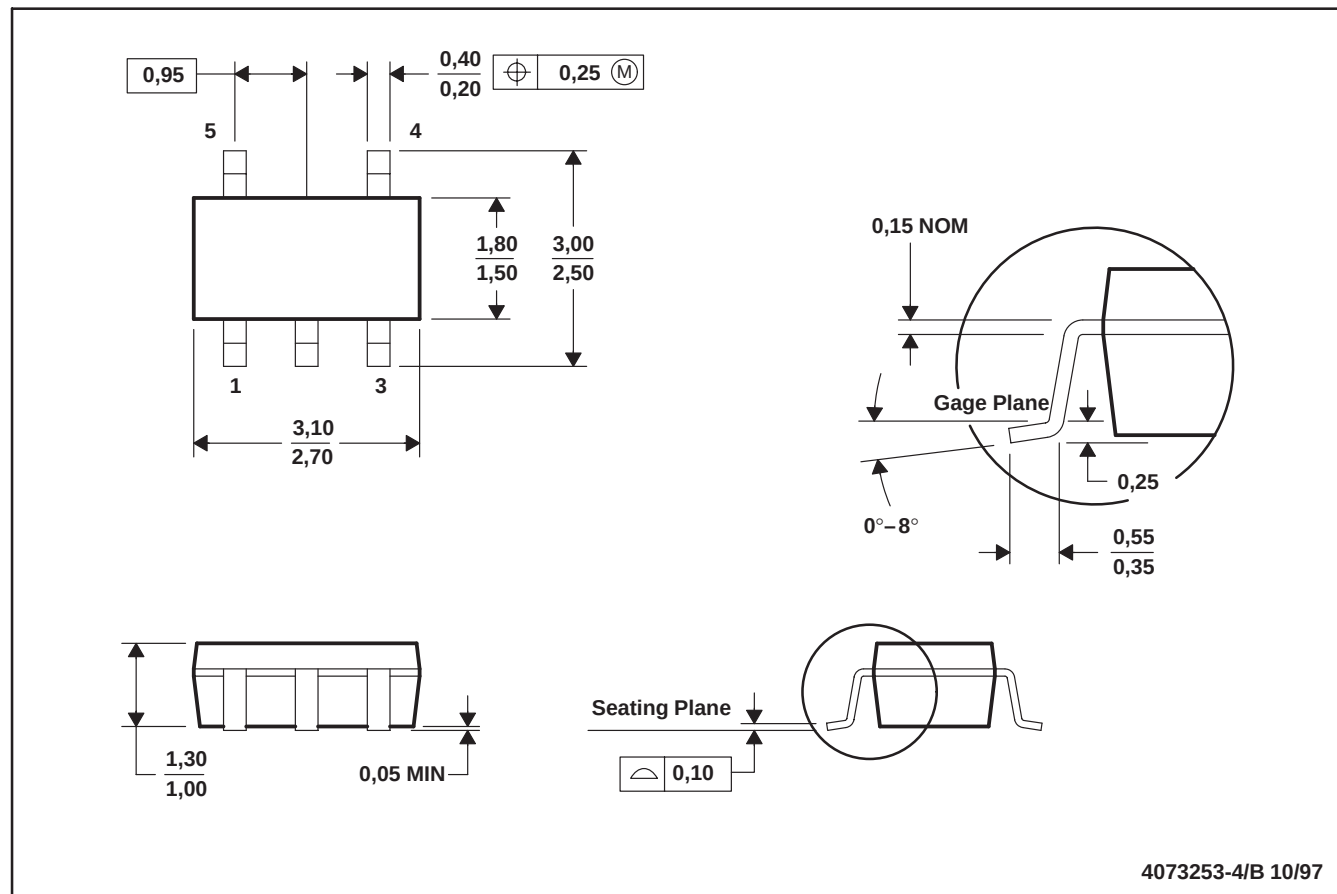
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MECHANICAL INFORMATION

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

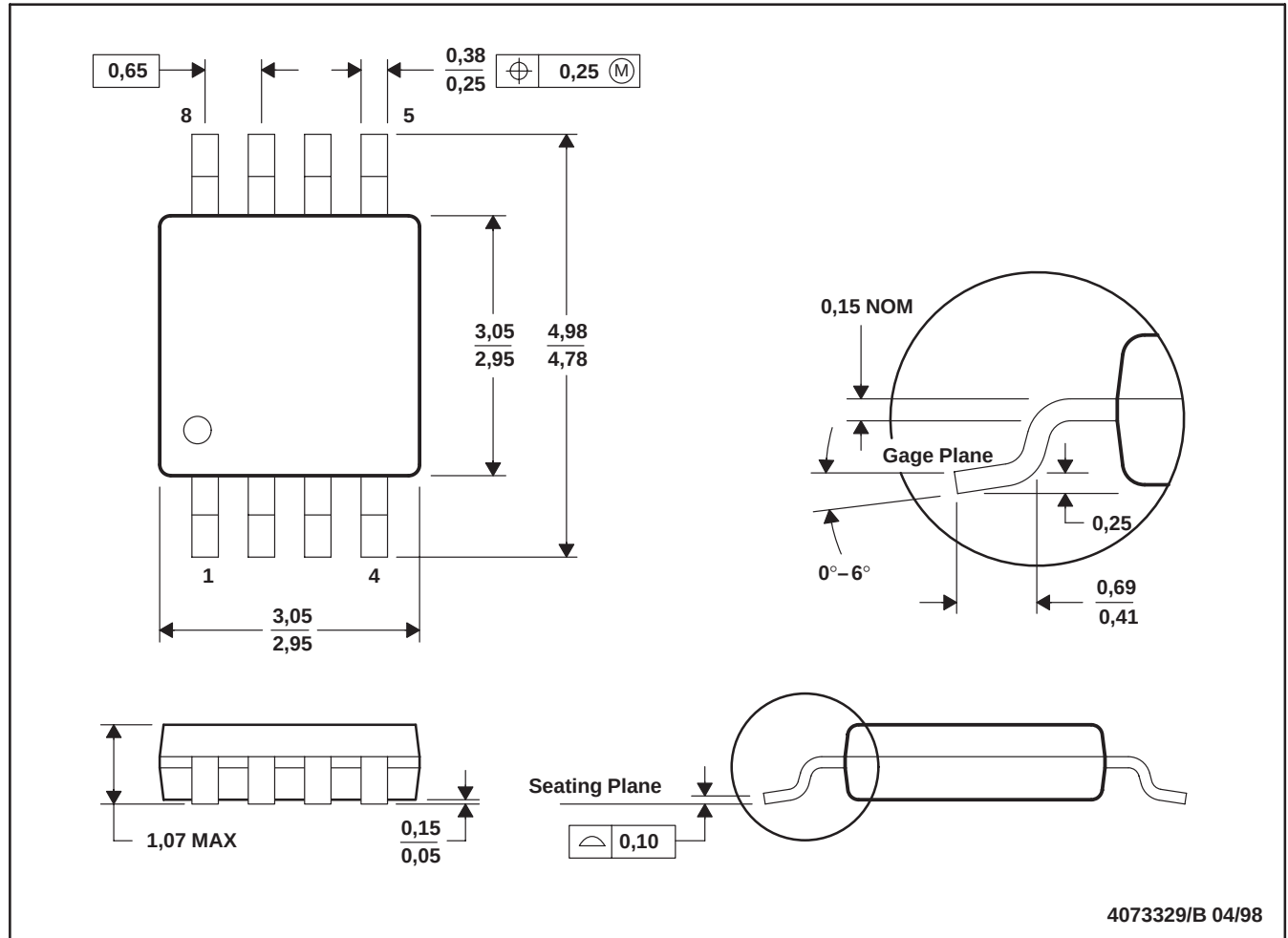


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusion.

MECHANICAL INFORMATION

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187

TLV2401, TLV2402, TLV2404
FAMILY OF 900-nA/Ch RAIL-TO-RAIL INPUT/OUTPUT
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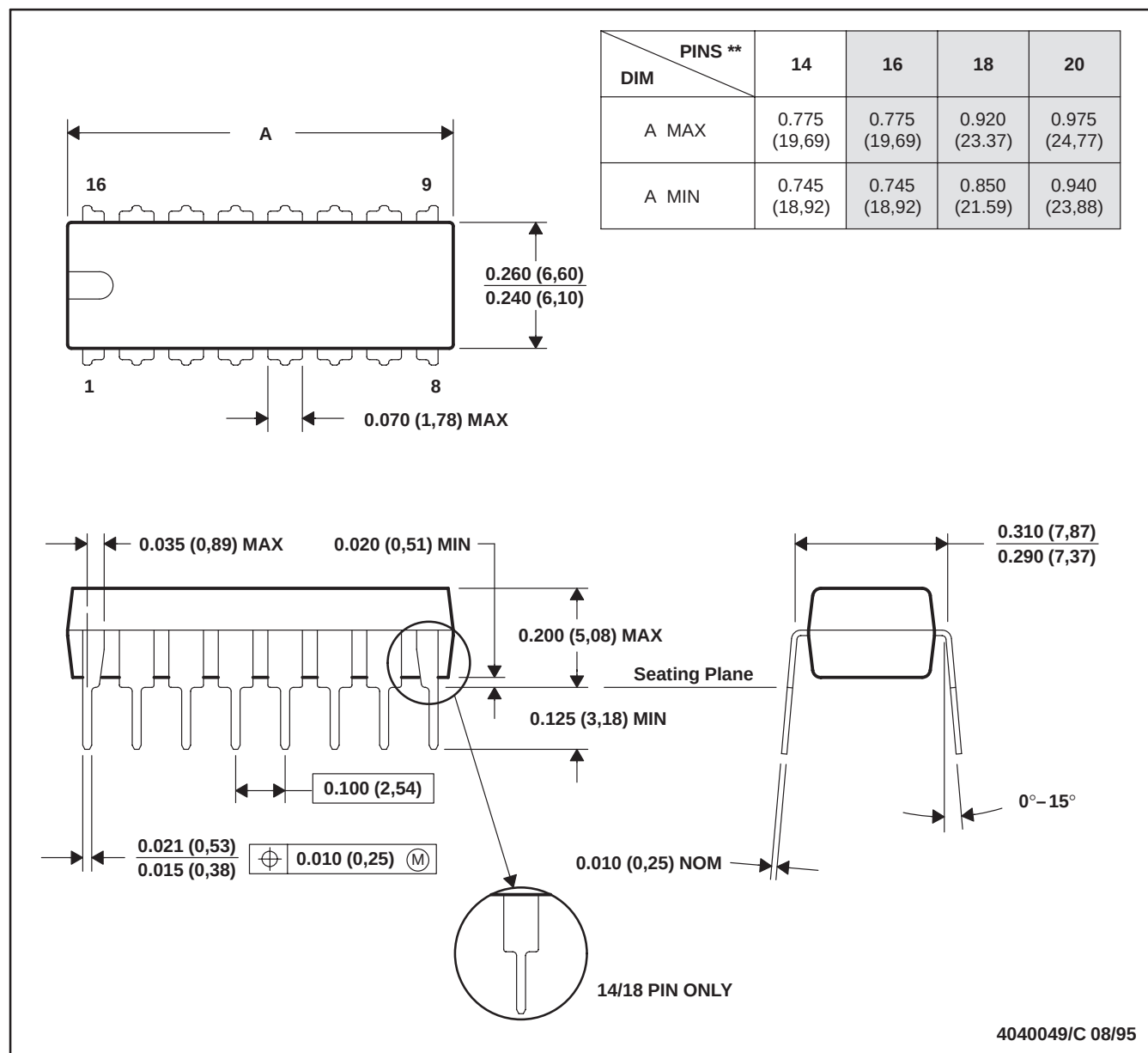
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MECHANICAL INFORMATION

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN

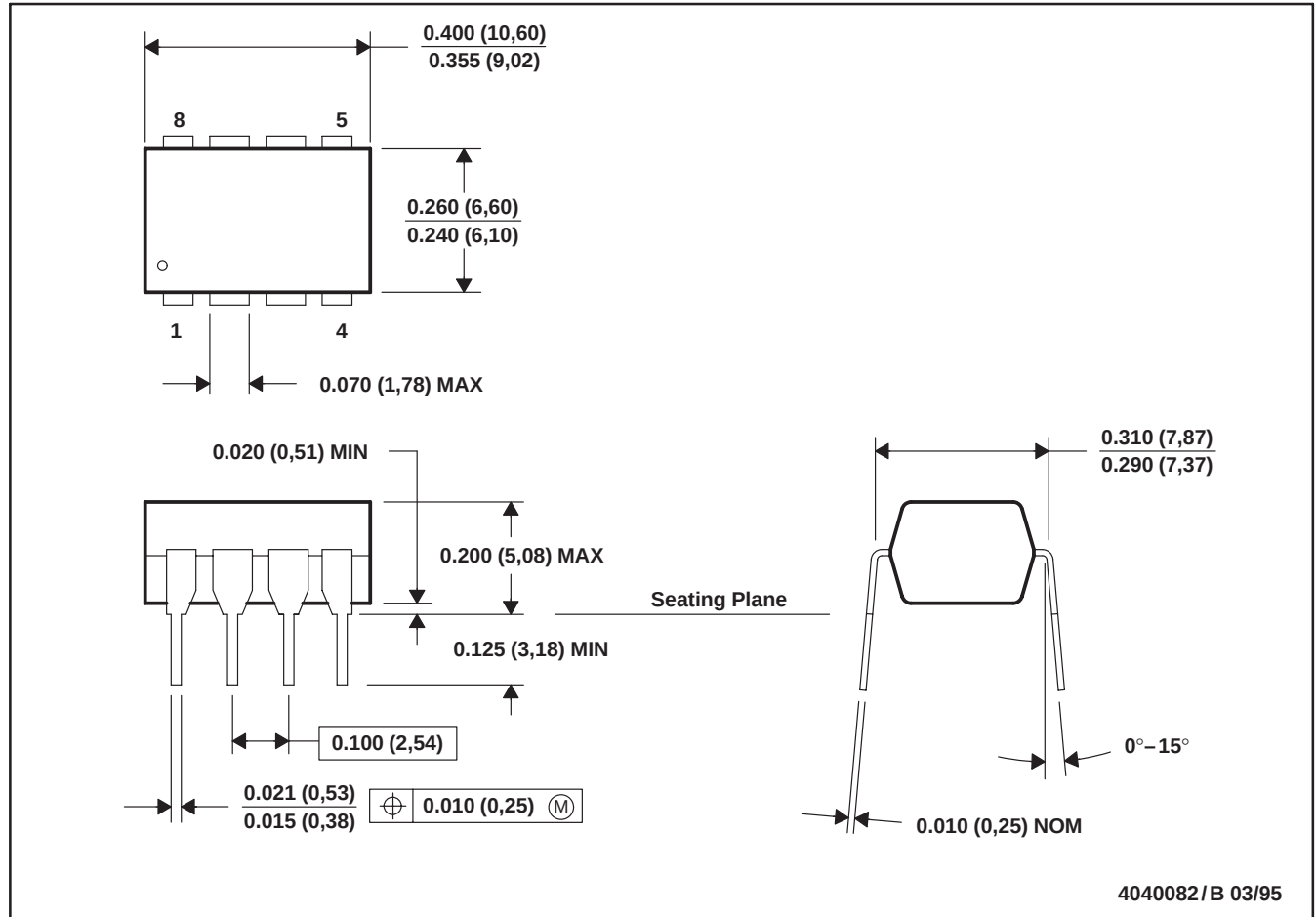


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

MECHANICAL INFORMATION

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

TLV2401, TLV2402, TLV2404
FAMILY OF 900-nA/Ch RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH REVERSE BATTERY PROTECTION

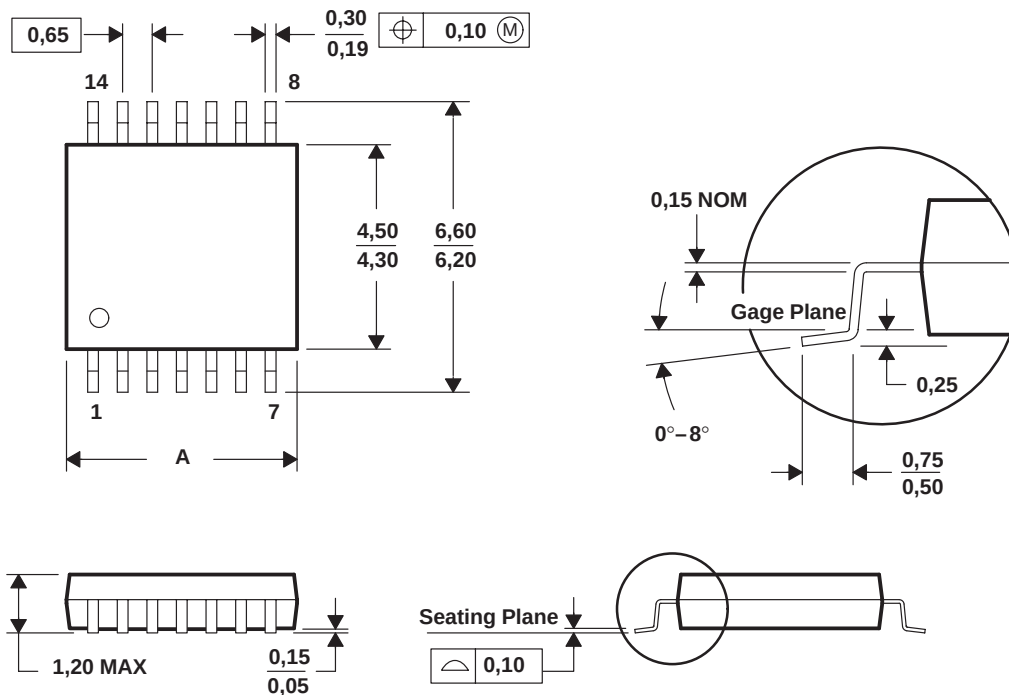
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MECHANICAL INFORMATION

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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