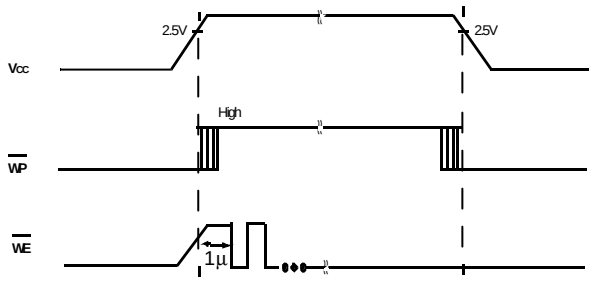
Document Title

128M x 8 Bit NAND Flash Memory

Revision History

Revision No	History	Draft Date	Remark
0.0	1. Initial issue	Apr. 7th 2001	
0.1	1.[Page 31] device code (76h) --> device code (79h)	Jul. 3rd 2001	
0.2	1.Powerup sequence is added : Recovery time of minimum 1µs is required before internal circuit gets ready for any command sequences	Jul. 23th 2001	



2. AC parameter tCLR(CLE to $\overline{RE}$ Delay, min 50ns) is added.
3. [Page28] Only address A_{14} to A_{25} is valid while A_9 to A_{13} is ignored
   --> Only address A_{14} to A_{26} is valid while A_9 to A_{13} is ignored

0.3	(page 30) A14 and A15 must be the same between source and target page --> A14 , A15 and A26 must be the same between source and target page	Sep. 13th 2001	

Note : For more detailed features and specifications including FAQ, please refer to Samsung' s Flash web site.
http://www.intl.samsungsemi.com/Memory/Flash/datasheets.html

128M x 8 Bit NAND Flash Memory

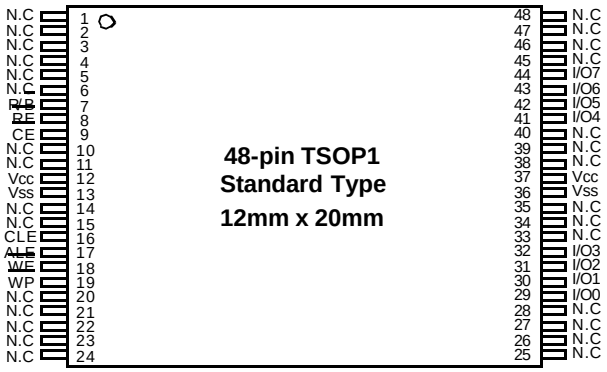
Features

- Voltage Supply : 2.7V~3.6V
- Organization
  - Memory Cell Array : (128M + 4,096K)bit x 8bit
  - Data Register : (512 + 16)bit x8bit multipled by eight planes
- Automatic Program and Erase
  - Page Program : (512 + 16)Byte
  - Block Erase : (16K + 512)Byte
- 528-Byte Page Read Operation
  - Random Access : 12µs(Max.)
  - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
  - Program time : 200µs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Intelligent Copy-Back Operation
- Package :
  - K9K1G08U0M-YCB0, K9K1G08U0M-YIB0 :
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
- Simultaneous Four Page/Block Program/Erase

General Description

The K9K1G08U0M is a 128M(134,217,728)x8bit NAND Flash Memory with a spare 4.096K(4,194,304)x8bit. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 200µs on the 528-byte page and an erase operation can be performed in typical 2ms on a 16K-byte block. Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9K1G08U0M' s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9K1G08U0M-YCB0/YIB0 is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

Pin Configuration



Pin Description

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	Data Input/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
$R/\overline{B}$	Ready/Busy output
V_{CC}	Power(+2.7V~3.6V)
V_{SS}	Ground
N.C	No Connection

NOTE : Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.
Do not leave V_{CC} or V_{SS} disconnected.

Figure 1. Functional Block Diagram

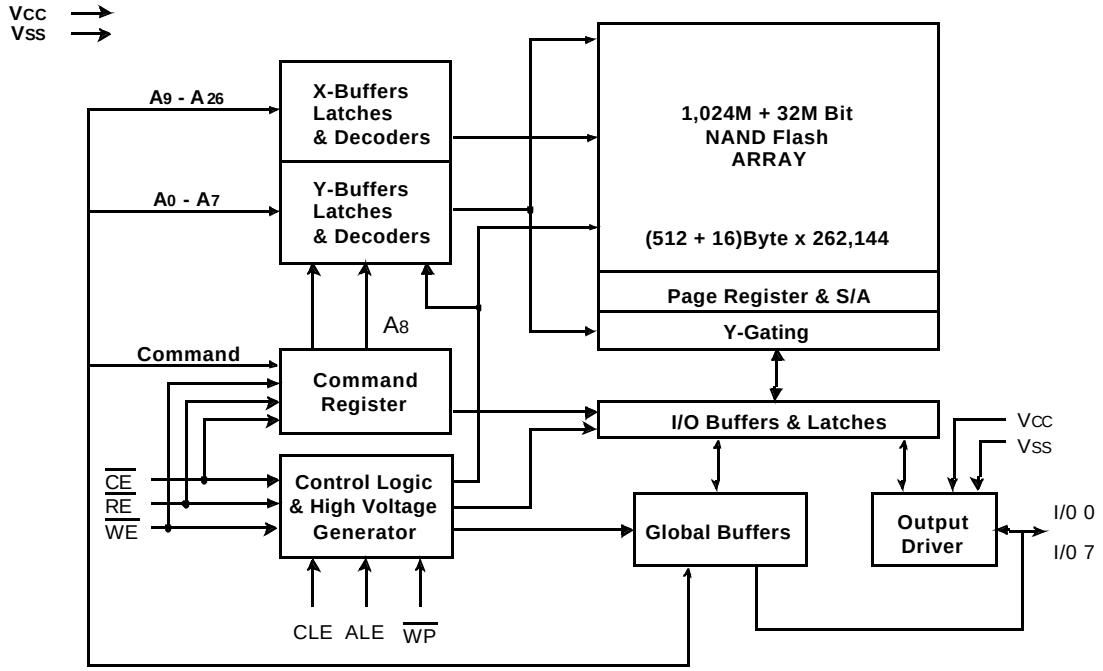
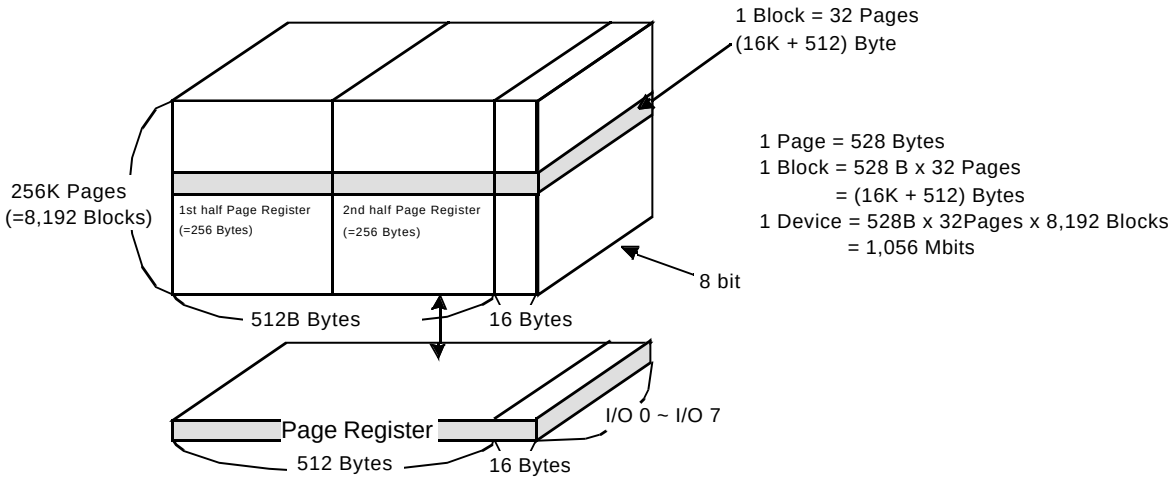


Figure 2. Array Organization



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16	Row Address (Page Address)
3rd Cycle	A17	A18	A19	A20	A21	A22	A23	A24	
4th Cycle	A25	A26	*L	*L	*L	*L	*L	*L	

NOTE : Column Address : Starting Address of the Register.

00h Command(Read) : Defines the starting address of the 1st half of the register.

01h Command(Read) : Defines the starting address of the 2nd half of the register.

* A8 is set to "Low" or "High" by the 00h or 01h Command.

* L must be set to "Low".

* The device ignores any additional input of address cycles than reguired.

Product Introduction

The K9K1G08U0M is a 1,026Mbit(1,107,296,436 bit) memory organized as 262,144 rows(pages) by 528 columns. Spare sixteen columns are located from column address of 512 to 527. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of the 32 pages formed by two NAND structures, totaling 16,384 NAND structures of 16 cells. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 8,192 separately erasable 16K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9K1G08U0M.

The K9K1G08U0M has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. The 128M byte physical space requires 27 addresses, thereby requiring four cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9K1G08U0M.

The device provides simultaneous program/erase capability up to four pages/blocks. By dividing the memory array into eight 128Mbit separate planes, simultaneous multi-plane operation dramatically increases program/erase performance by 4X while still maintaining the conventional 512 byte structure.
The extended pass/fail status for multi-plane program/erase allows system software to quickly identify the failing page/block out of selected multiple pages/blocks. Usage of multi-plane operations will be described further throughout this document.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another of the same plane without the need for transporting the data to and from the external buffer memory. Since the time-consuming burst-reading and data-input cycles are removed, system performance for solid-state disk application is significantly increased.

Table 1. Command Sets

Function	1st. Cycle	2nd. Cycle	3rd. Cycle	Acceptable Command during Busy
Read 1	00h/01h(1)	-	-	
Read 2	50h	-	-	
Read ID	90h	-	-	
Reset	FFh	-	-	O
Page Program (True)(2)	80h	10h	-	
Page Program (Dummy)(2)	80h	11h	-	
Copy-Back Program(True)(2)	00h	8Ah	10h	
Copy-Back Program(Dummy)(2)	03h	8Ah	11h	
Block Erase	60h	D0h	-	
Multi-Plane Block Erase	60h----60h	D0h	-	
Read Status	70h	-	-	O
Read Multi-Plane Status	71h(3)	-	-	O

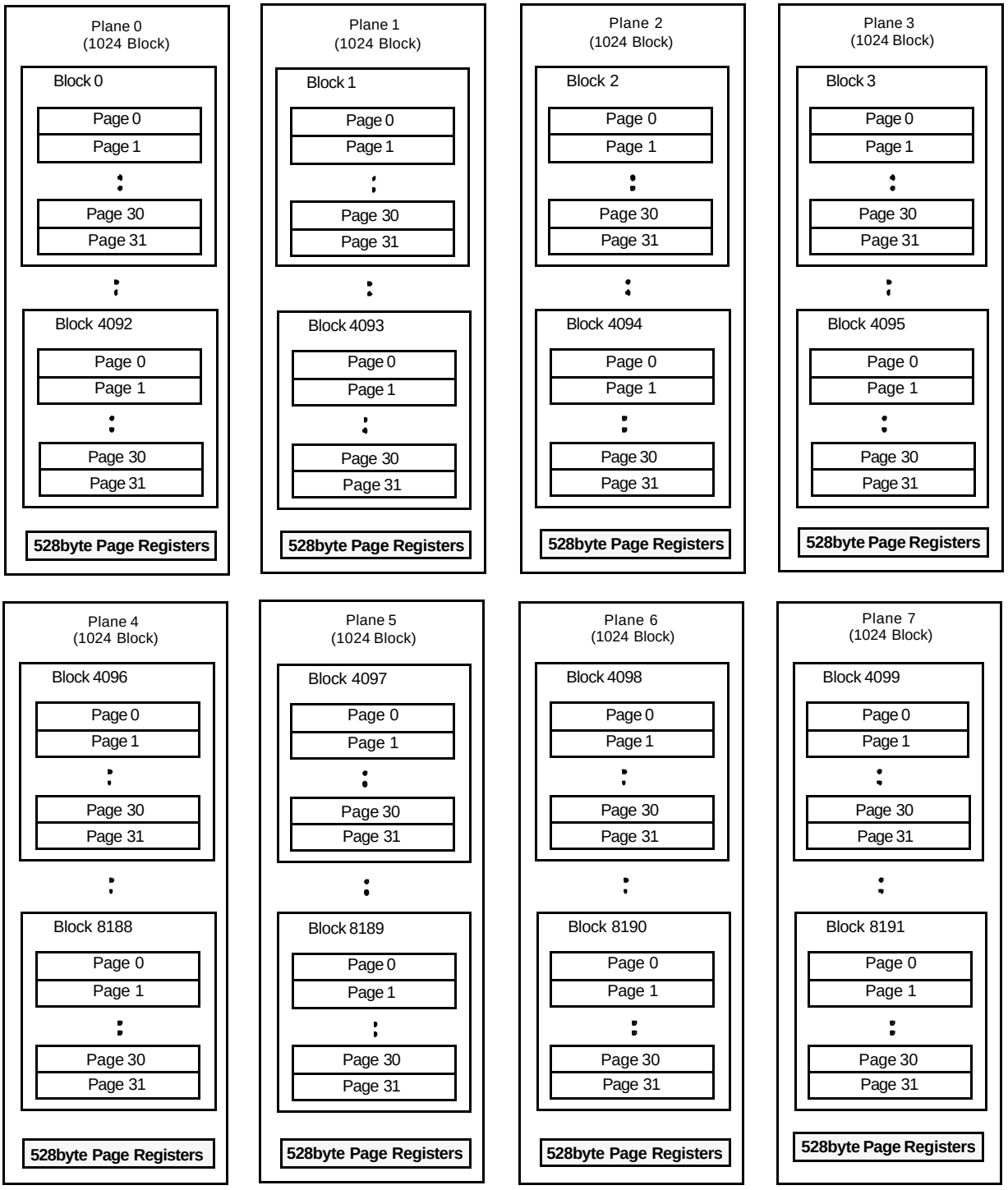
NOTE : 1. The 00h command defines starting address of the 1st half of registers.
The 01h command defines starting address of the 2nd half of registers.
After data access on the 2nd half of register by the 01h command, the status pointer is automatically moved to the 1st half register(00h) on the next cycle.
2. Page Program(True) and Copy-Back Program(True) are available on 1 plane operation.
Page Program(Dummy) and Copy-Back Program(Dummy) are available on the 2nd,3rd,4th plane of multi plane operation.
3. The 71h command should be used for read status of Multi Plane operation.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

Memory Map

The device is arranged in eight 128Mbit memory planes. Each plane contains 1,024 blocks and 528 byte page registers. This allows it to perform simultaneous page program and block erase by selecting one page or block from each plane. The block address map is configured so that multi-plane program/erase operations can be executed for every four sequential blocks by dividing the memory array into plane 0~3 or plane 4~7 separately. For example, multi-plane program/erase operations into plane 2,3,4 and 5 are prohibited.

Figure 3. Memory Array Map



Pin Description

Command Latch Enable(CLE)

The CLE input controls the path activation for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.

Address Latch Enable(ALE)

The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.

Chip Enable($\overline{CE}$)

The $\overline{CE}$ input is the device selection control. When $\overline{CE}$ goes high during a read operation the device is returned to standby mode. However, when the device is in the busy state during program or erase, $\overline{CE}$ high is ignored, and does not return the device to standby mode.

Write Enable($\overline{WE}$)

The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
The $\overline{WE}$ must be held high when outputs are activated.

Read Enable($\overline{RE}$)

The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.

I/O Port : I/O 0 ~ I/O 7

The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.

Write Protect($\overline{WP}$)

The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.

Ready/$\overline{Busy}$(R/$\overline{B}$)

The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{IN}	-0.6 to + 4.6	V
		V_{CC}	-0.6 to + 4.6	
Temperature Under Bias	K9K1G08U0M-YCB0	T_{BIAS}	-10 to +125	°C
	K9K1G08U0M-YIB0		-40 to +125	
Storage Temperature		T_{STG}	-65 to +150	°C

NOTE:
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

(Voltage reference to GND, K9K1G08U0M-YCB0 :T_A=0 to 70°C, K9K1G08U0M-YIB0:T_A=-40 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

Dc and Operating Characteristics (Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Sequential Read	I_{CC1}	tRC=50ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	10	30	mA
	Program	I_{CC2}	-	-	10	30	
	Erase	I_{CC3}	-	-	10	30	
Stand-by Current(TTL)		I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$= 0V/V_{CC}	-	-	1	
Stand-by Current(CMOS)		I_{SB2}	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$ = 0V/V_{CC}	-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to 3.6V	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to 3.6V	-	-	±10	
Input High Voltage		V_{IH}	-	2.0	-	V_{CC}+0.3	V
Input Low Voltage, All inputs		V_{IL}	-	-0.3	-	0.8	
Output High Voltage Level		V_{OH}	I_{OH}=-400µA	2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

Valid Block

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	8,052	-	8,192	Blocks

NOTE :
1. The K9K1G08U0M may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for an appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

AC Test Condition

(K9K1G08U0M-YCB0 :TA=0 to 70°C, K9K1G08U0M-YIB0:TA=-40 to 85°C, VCC=2.7V~3.6V unless otherwise)

Parameter	Value
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load (3.0V +/-10%)	1 TTL GATE and CL=50pF
Output Load (3.3V +/-10%)	1 TTL GATE and CL=100pF

Capacitance (TA=25°C, VCC=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	20	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	20	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	⎍	H	X	Read Mode	Command Input
L	H	L	⎍	H	X		Address Input(4clock)
H	L	L	⎍	H	H	Write Mode	Command Input
L	H	L	⎍	H	H		Address Input(4clock)
L	L	L	⎍	H	H	Data Input	
L	L	L	H	⎍	X	Sequential Read & Data Output	
L	L	L	H	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/VCC(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	500	µs
Dummy Busy Time for Multi Plane Program		t_{DBSY}		1	10	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	1	cycle
	Spare Array		-	-	2	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE setup Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
$\overline{CE}$ setup Time	t_{CS}	0	-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25(1)	-	ns
ALE setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	50	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	-	ns

NOTE: 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	12	µs
ALE to $\overline{RE}$ Delay(ID read)	t_{AR1}	10	-	ns
ALE to $\overline{RE}$ Delay(Read cycle)	t_{AR2}	50	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	50	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	30	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	50	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	35	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	15	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	20	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
Last RE High to Busy(at sequential read)	t_{RB}	-	100	ns
$\overline{CE}$ High to Ready(in case of interception by $\overline{CE}$ at read)	t_{CRY}	-	50 +tr(R/$\overline{B}$)(1)	ns
$\overline{CE}$ Access Time	t_{CEA}	-	45	ns
$\overline{CE}$ High Hold Time(at the last serial read)(2)	t_{CEH}	100	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500(3)	µs

NOTE :
1. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.
2. To break the sequential read cycle, $\overline{CE}$ must be held high for longer time than tCEH.
3. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level or as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block of the NAND Flash, however, is fully guaranteed to be a valid block. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 6th byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every invalid block has non-FFh data at the column address of 517. Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 4). Any intentional erasure of the original invalid block information is prohibited.

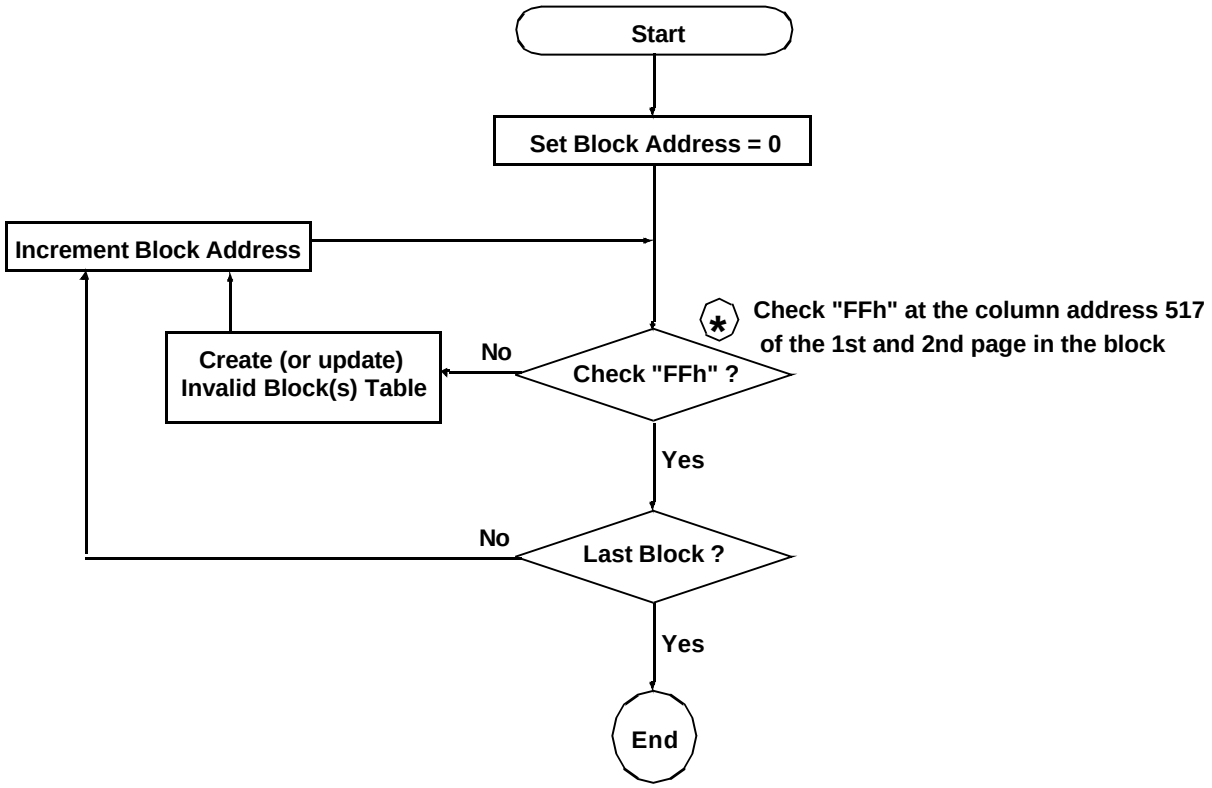


Figure 4. Flow chart to create invalid block table.

NAND Flash Technical Notes (Continued)

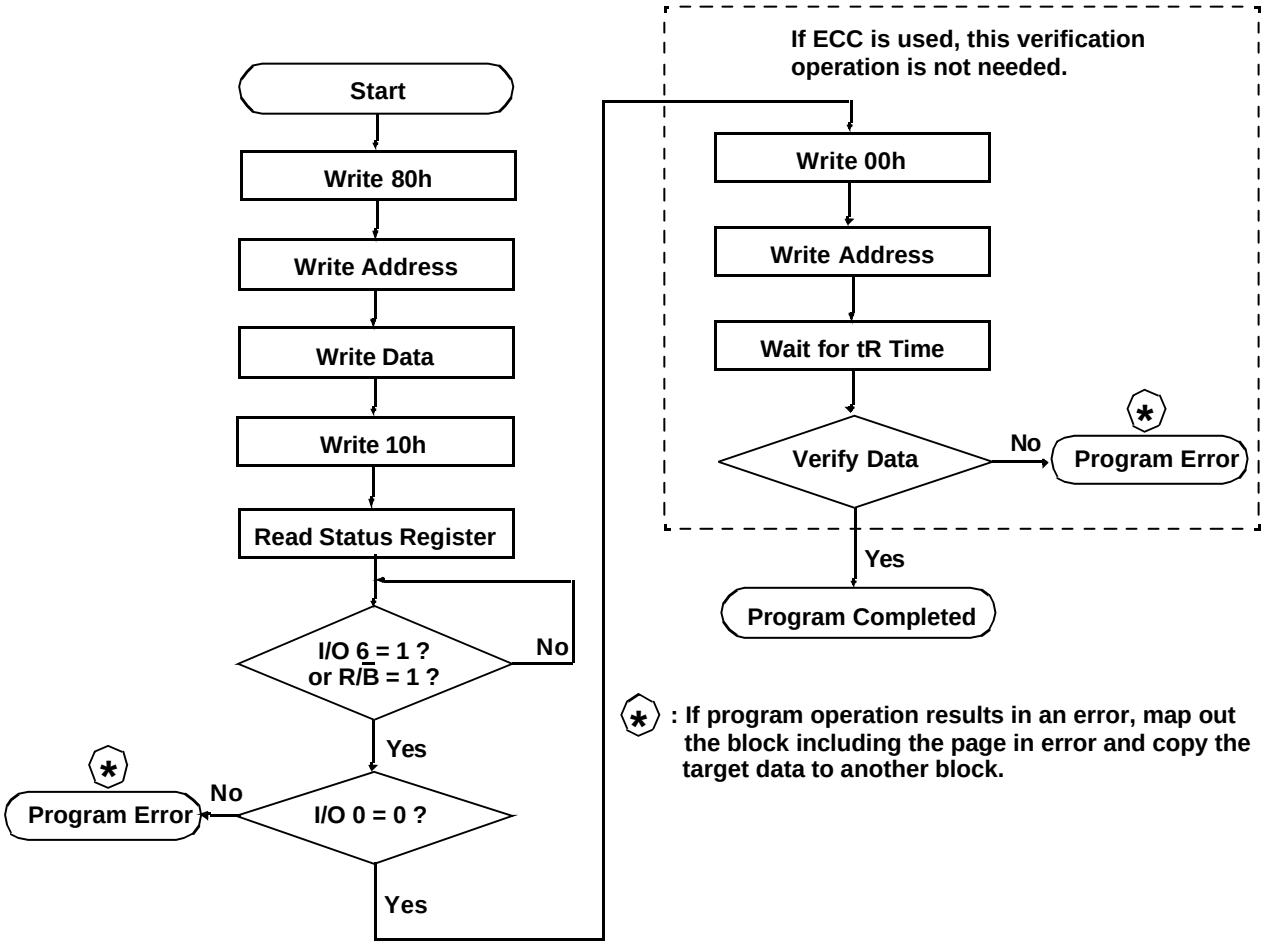
Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

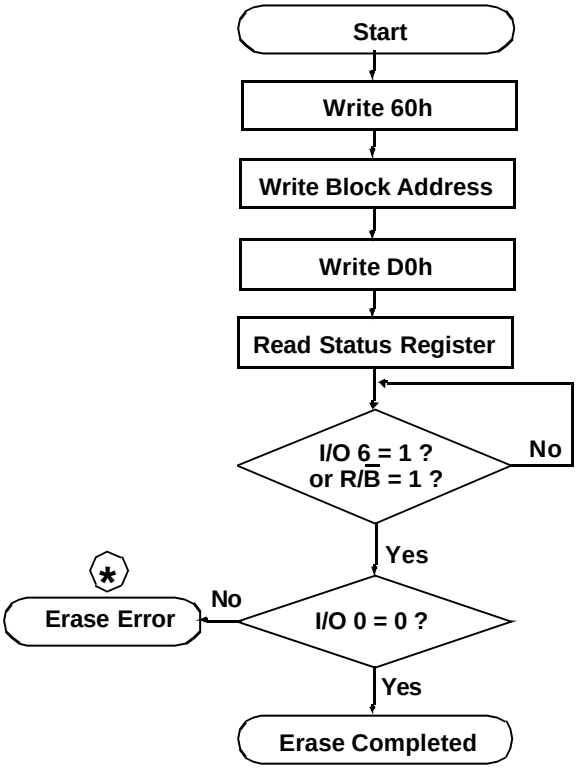
ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Program Flow Chart

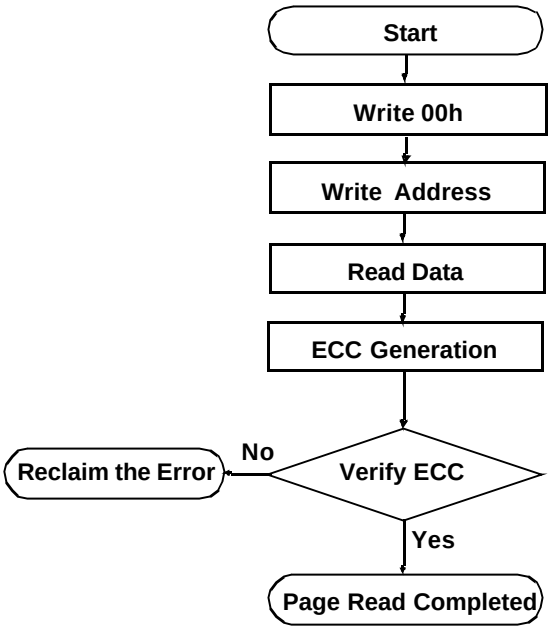


NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

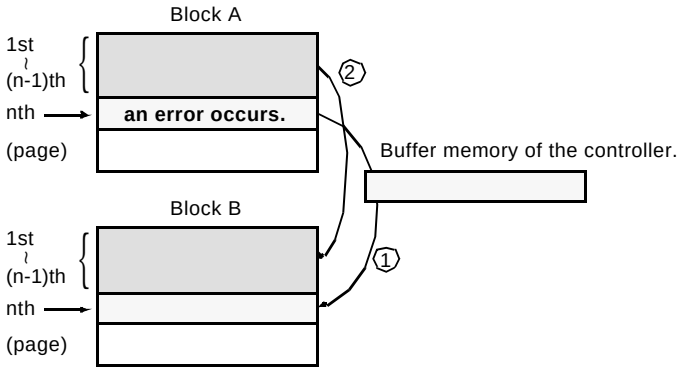


Read Flow Chart



*** : If erase operation results in an error, map out the failing block and replace it with another block.**

Block Replacement



* Step1
When an error happens in the nth page of the Block ' A' during erase or program operation.
* Step2
Copy the nth page data of the Block ' A' in the buffer memory to the nth page of another free block. (Block ' B')
* Step3
Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block ' B' .
* Step4
Do not erase or program to Block ' A' by creating an ' invalid Block' table or other appropriate scheme.

Pointer Operation of K9K1G08U0M

Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. ' 00h' command sets the pointer to ' A' area(0~255byte), ' 01h' command sets the pointer to ' B' area(256~511byte), and ' 50h' command sets the pointer to ' C' area(512~527byte). With these commands, the starting column address can be set to any of a whole page(0~527byte). ' 00h' or ' 50h' is sustained until another address pointer command is inputted. ' 01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power_Up is executed once with ' 01h' command, the address pointer returns to ' A' area by itself. To program data starting from ' A' or ' C' area, ' 00h' or ' 50h' command must be inputted before ' 80h' command is written. A complete read operation prior to ' 80h' command is not necessary. To program data starting from ' B' area, ' 01h' command must be inputted right before ' 80h' command is written.

Table 2. Destination of the pointer

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)

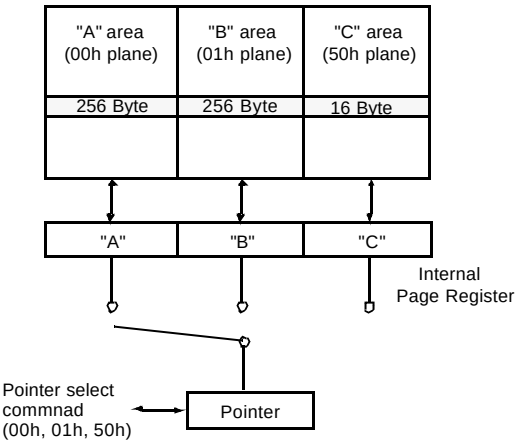
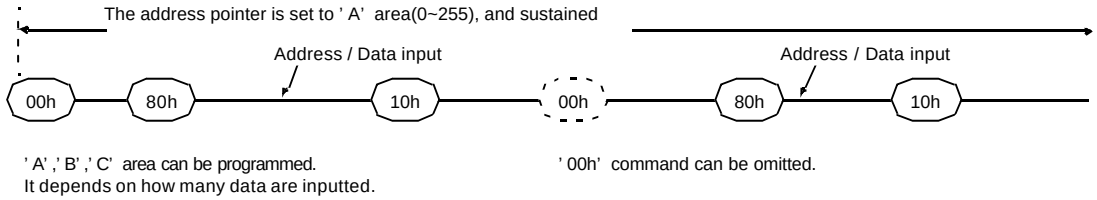


Figure 5 Block Diagram of Pointer Operation

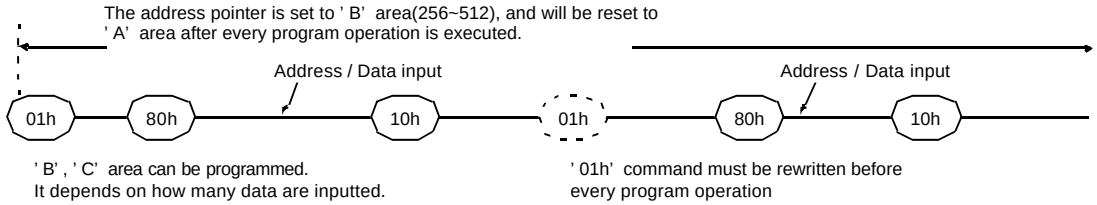
(1) Command input sequence for programming ' A' area



' A' ,' B' ,' C' area can be programmed.
It depends on how many data are inputted.

' 00h' command can be omitted.

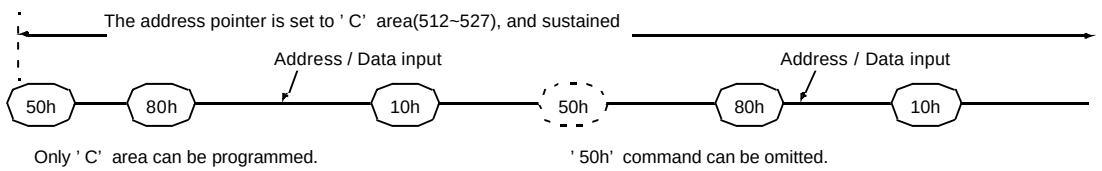
(2) Command input sequence for programming ' B' area



' B' , ' C' area can be programmed.
It depends on how many data are inputted.

' 01h' command must be rewritten before every program operation

(3) Command input sequence for programming ' C' area



Only ' C' area can be programmed.

' 50h' command can be omitted.

SAMSUNG ELECTRONICS

System Interface Using $\overline{CE}$ don' t-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential data-reading as shown below. The internal 528byte page registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

Figure 6. Program Operation with $\overline{CE}$ don' t-care.

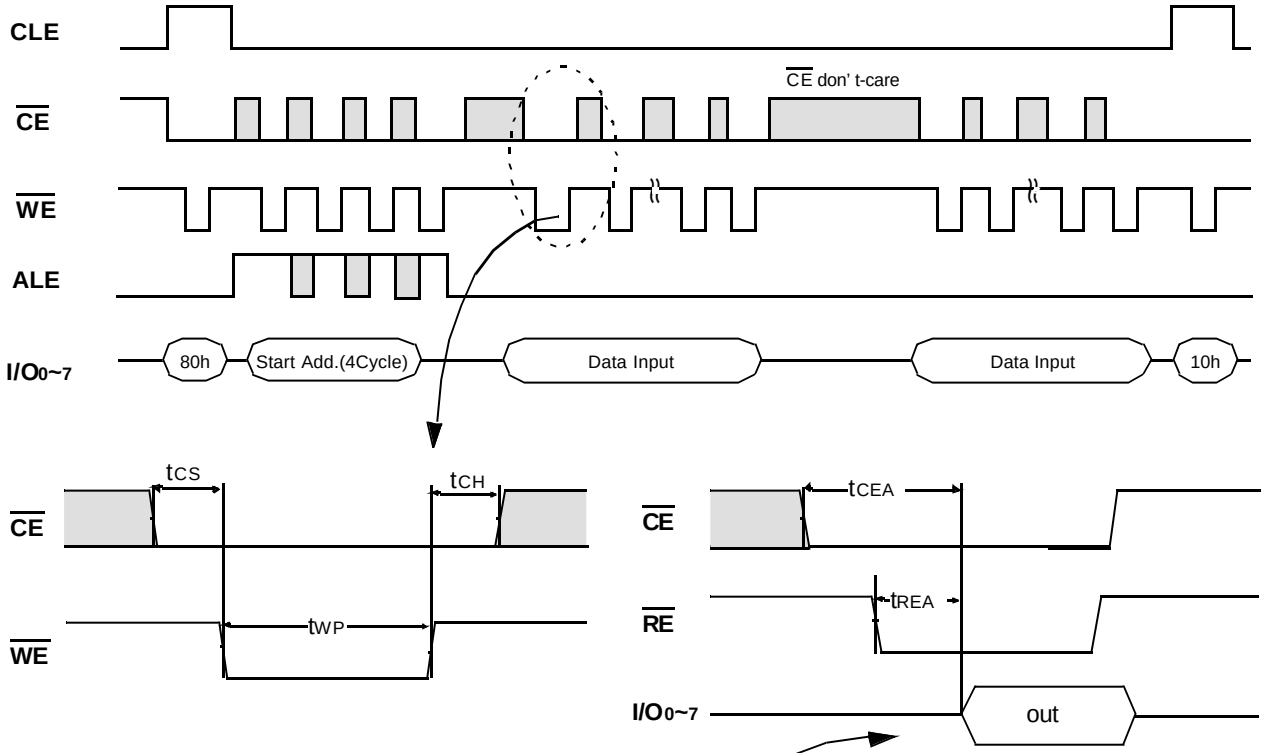
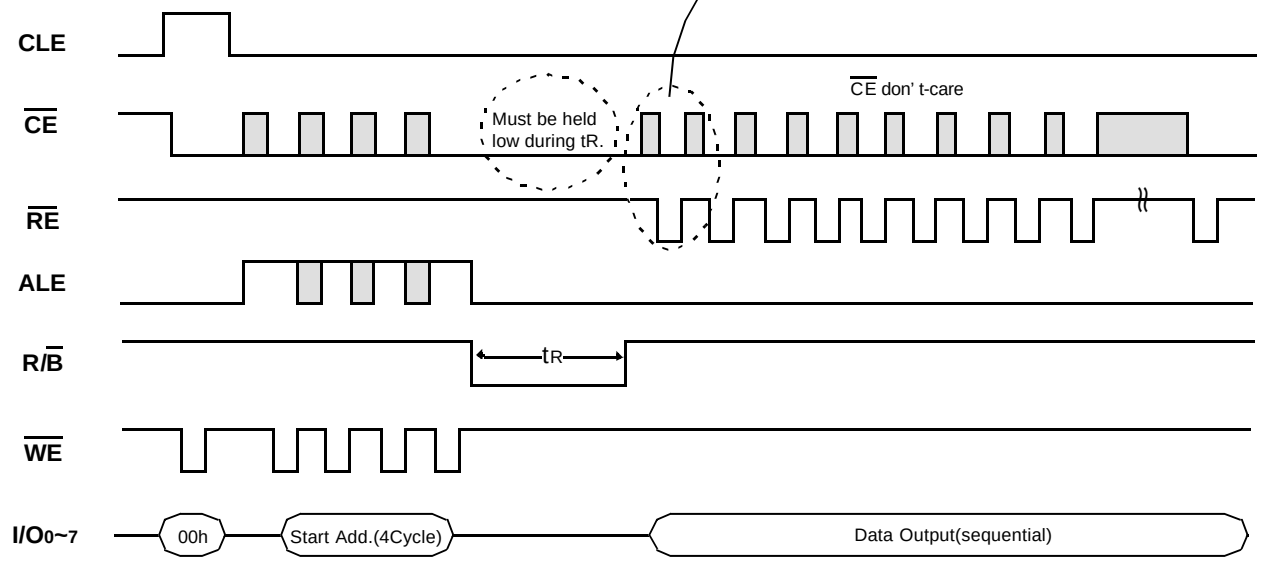
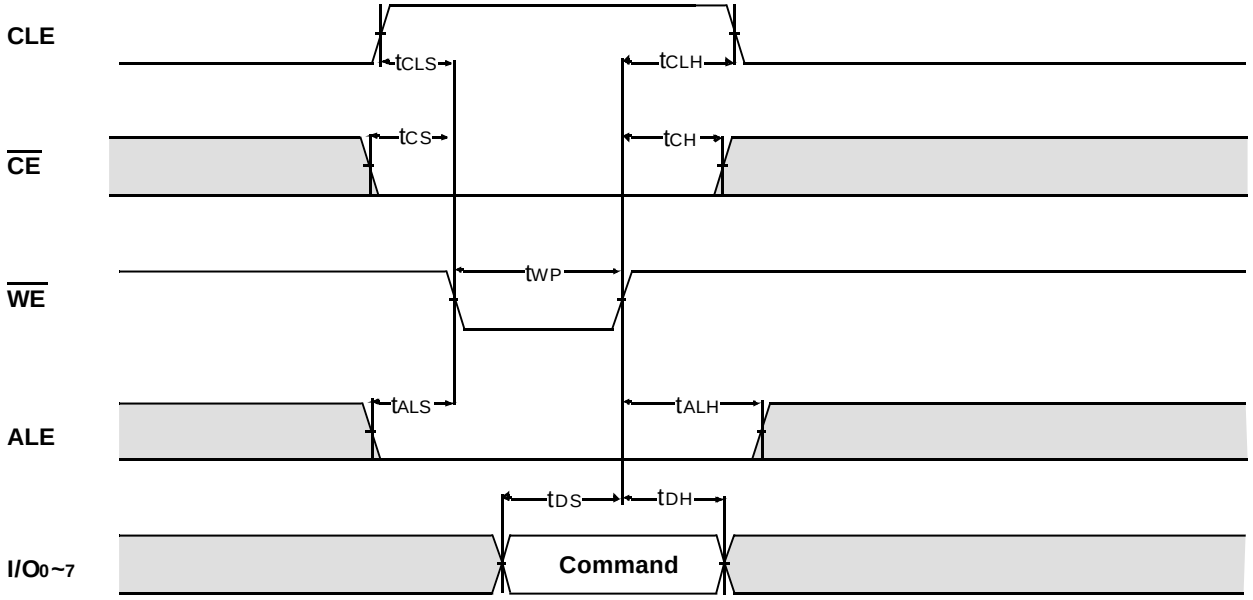


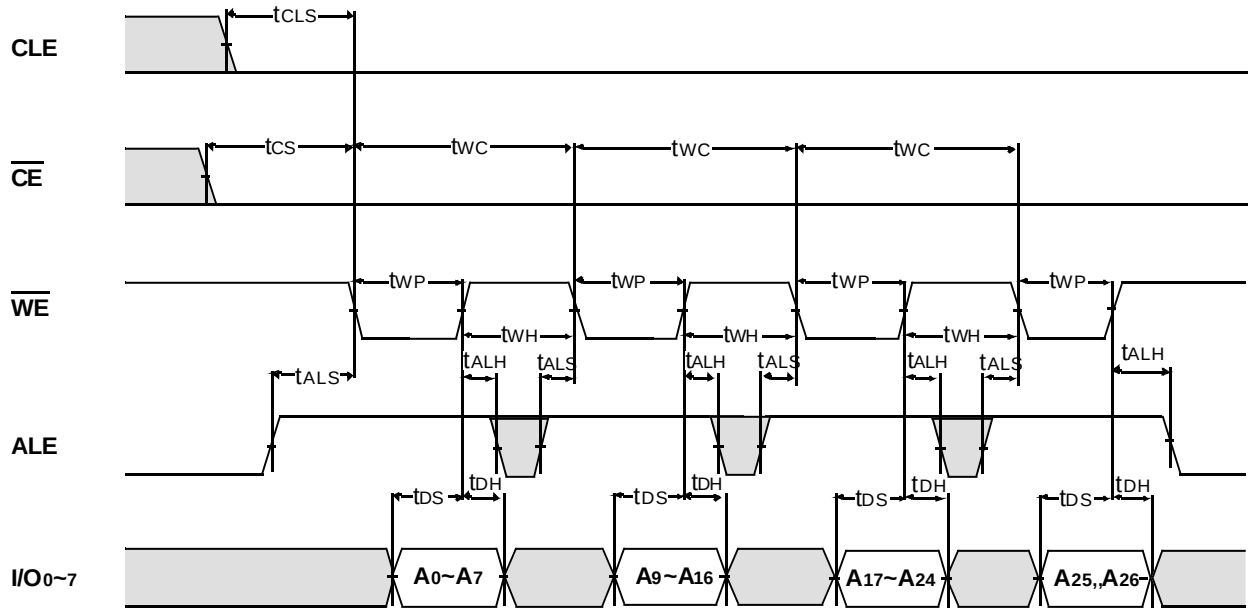
Figure 7. Read Operation with $\overline{CE}$ don' t-care.



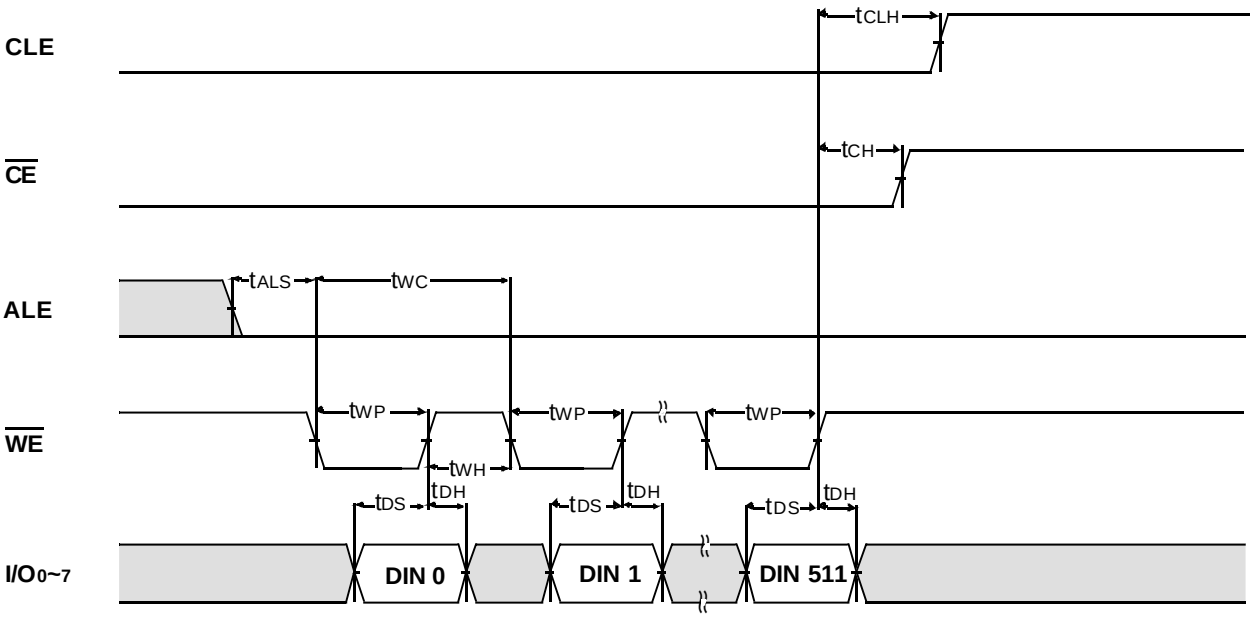
*** Command Latch Cycle**



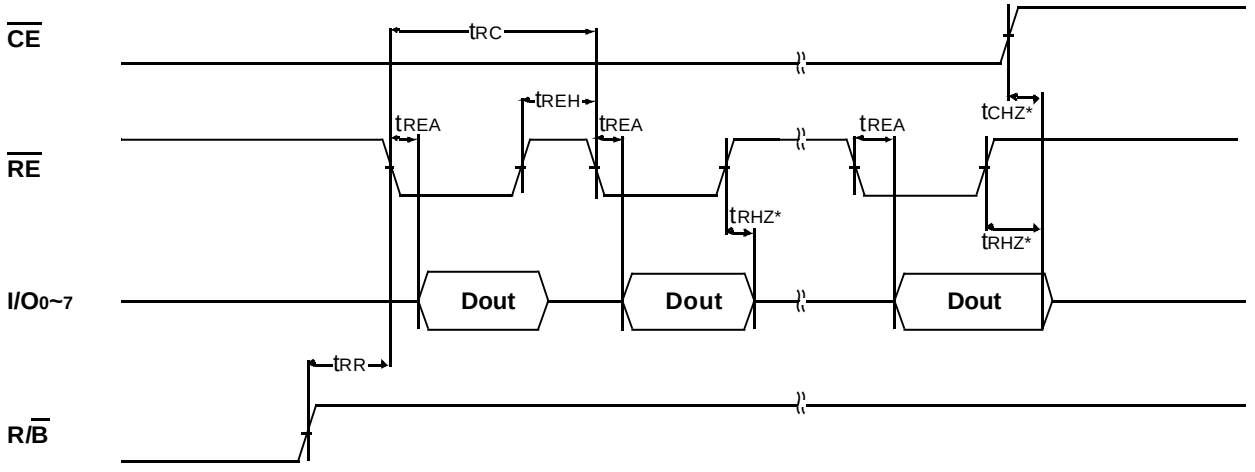
*** Address Latch Cycle**



*** Input Data Latch Cycle**

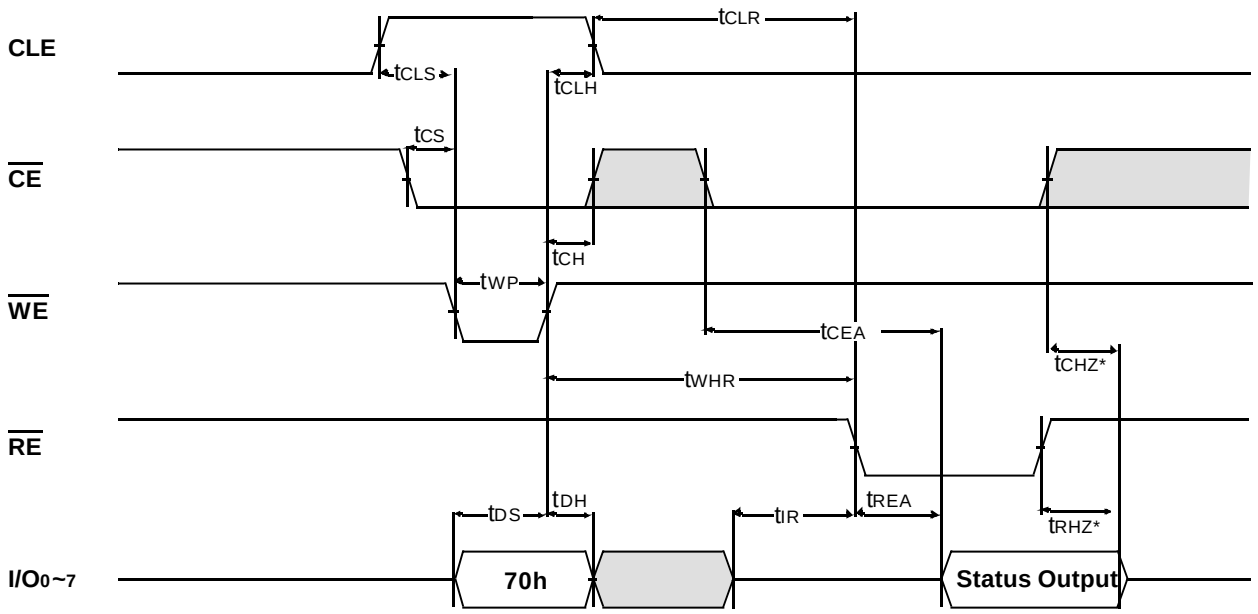


*** Serial Access Out Cycle after Read** (CLE=L, $\overline{WE}$=H, ALE=L)

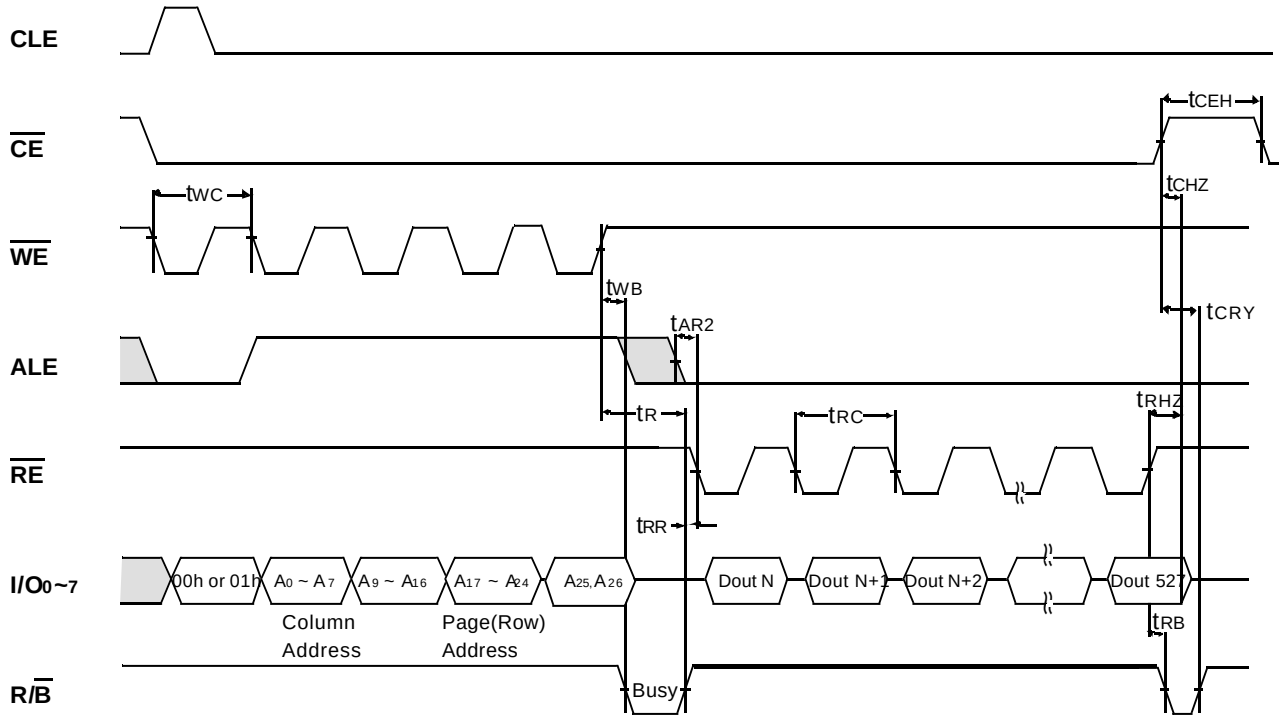


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

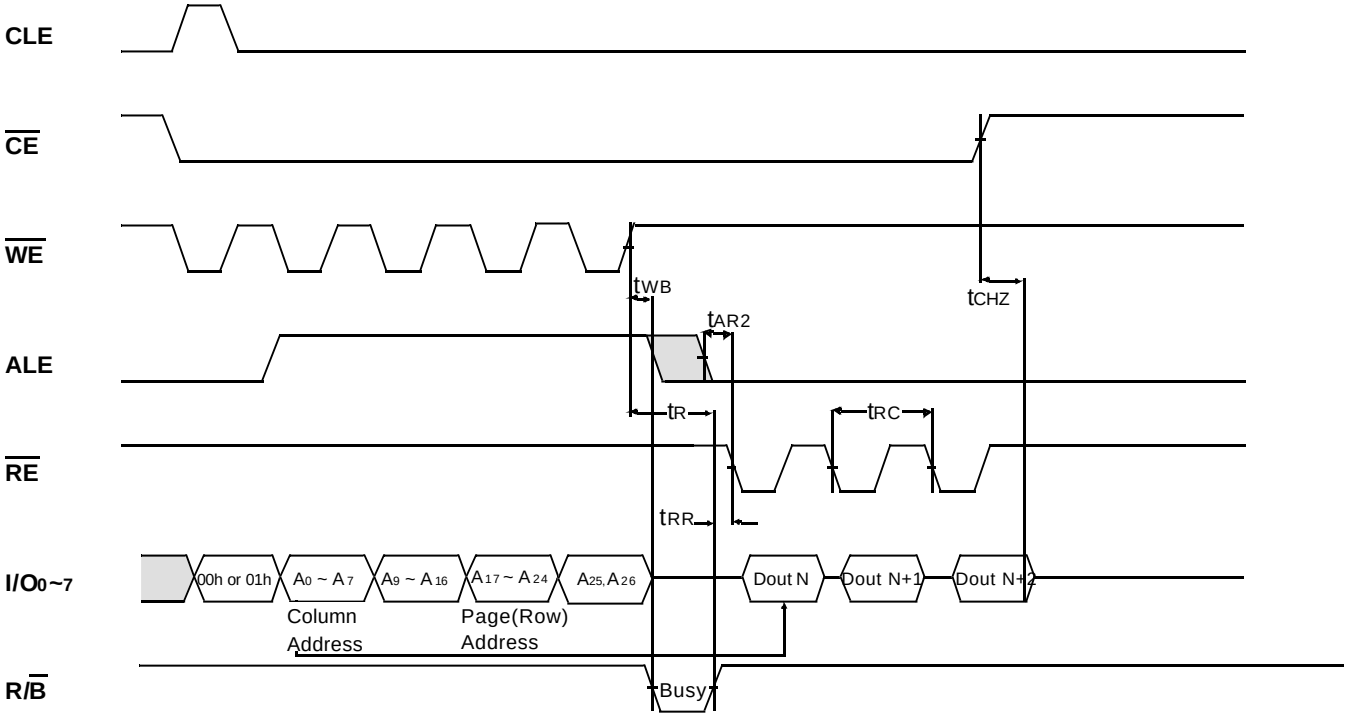
*** Status Read Cycle**



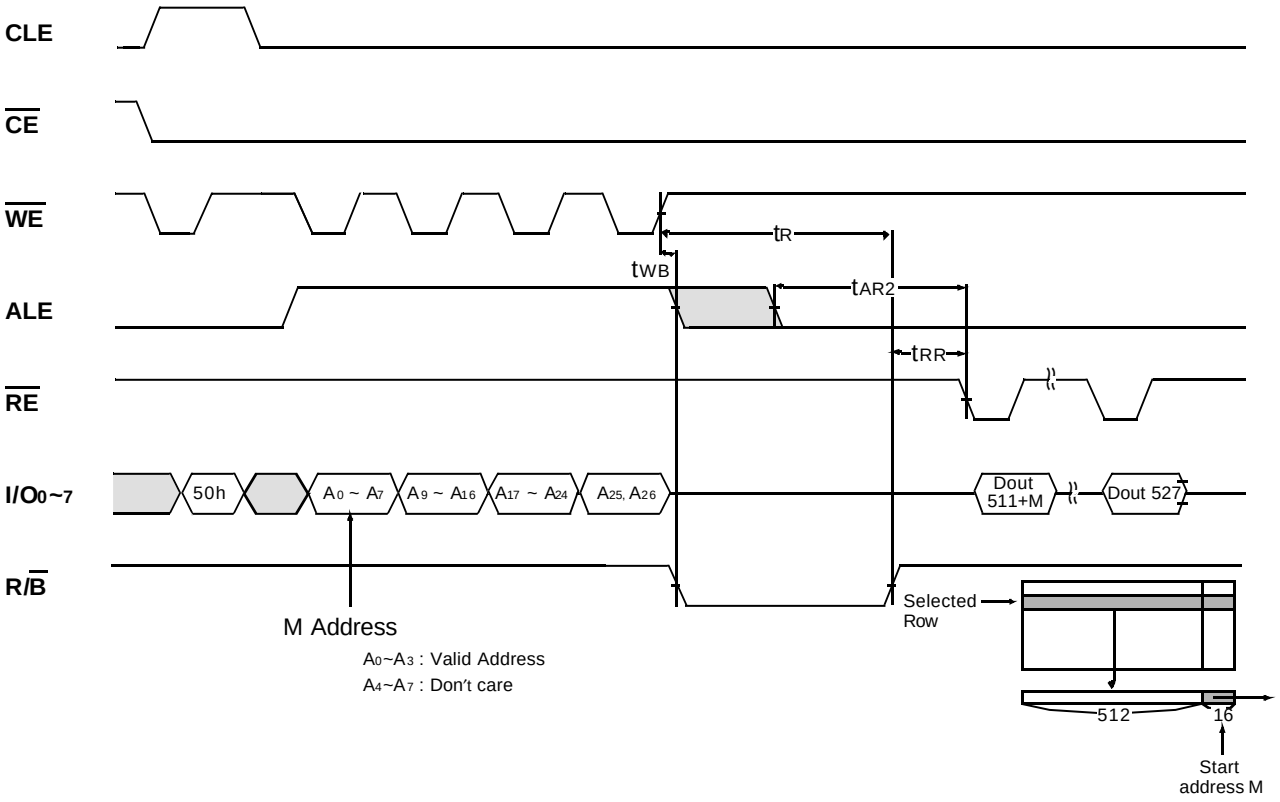
Read1 Operation (Read One Page)



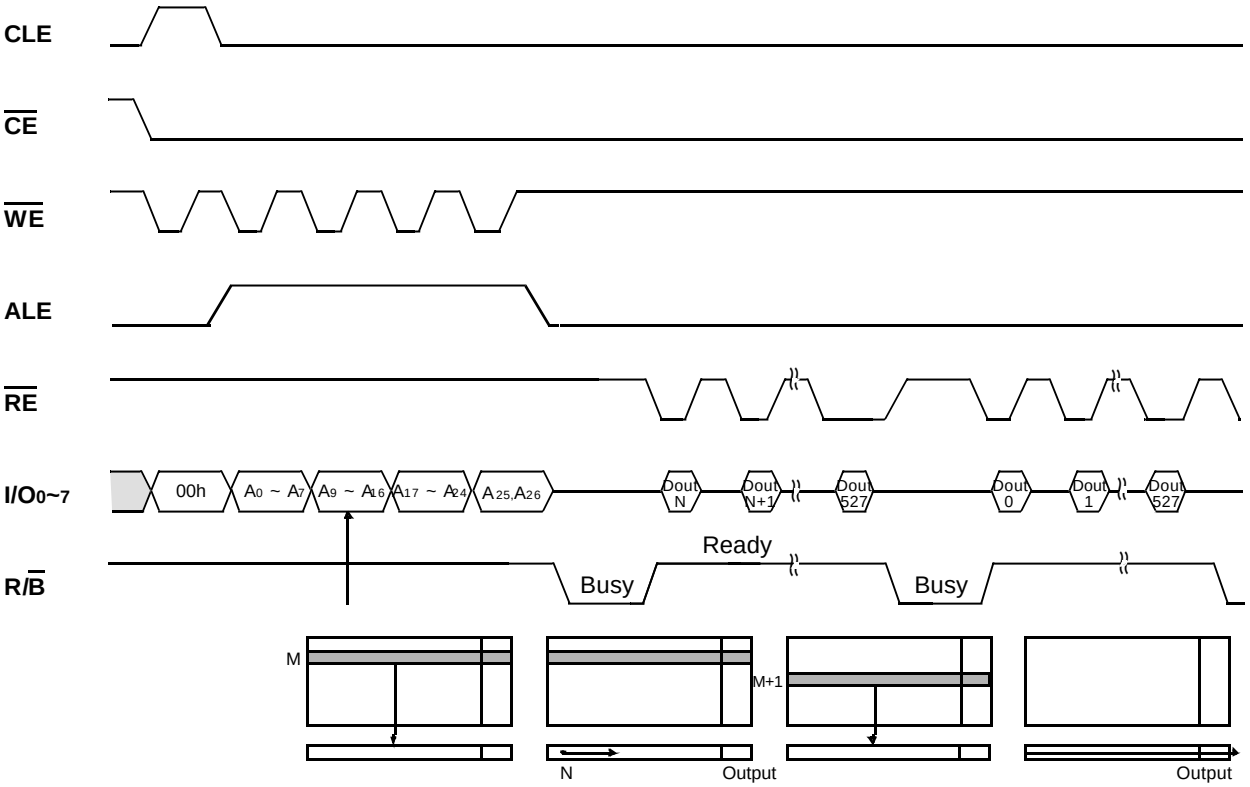
Read1 Operation(Intercepted by $\overline{CE}$)



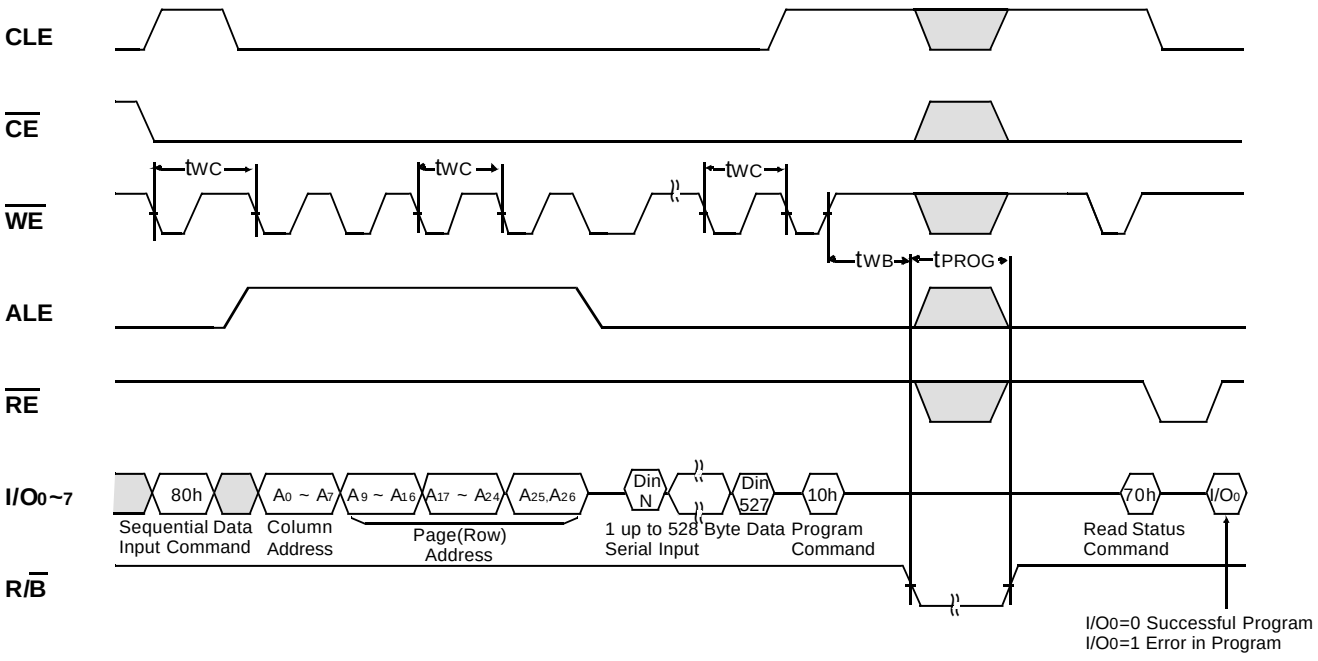
Read2 Operation (Read One Page)



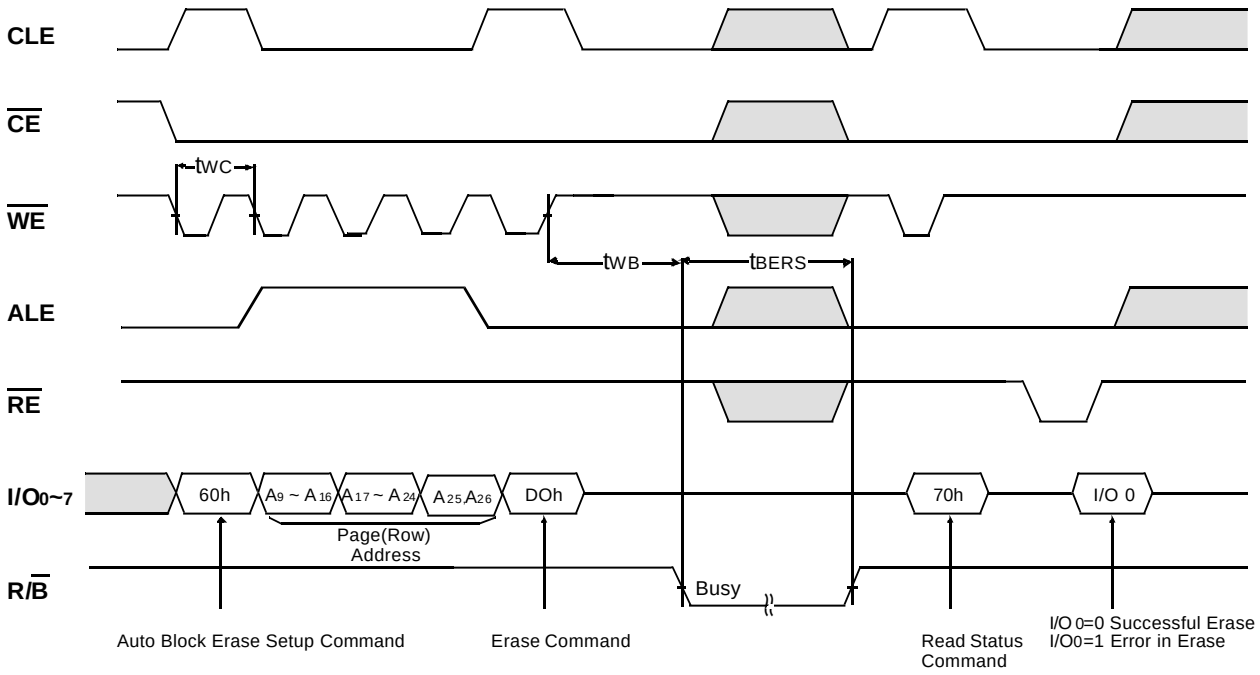
Sequential Row Read Operation (Within a Block)



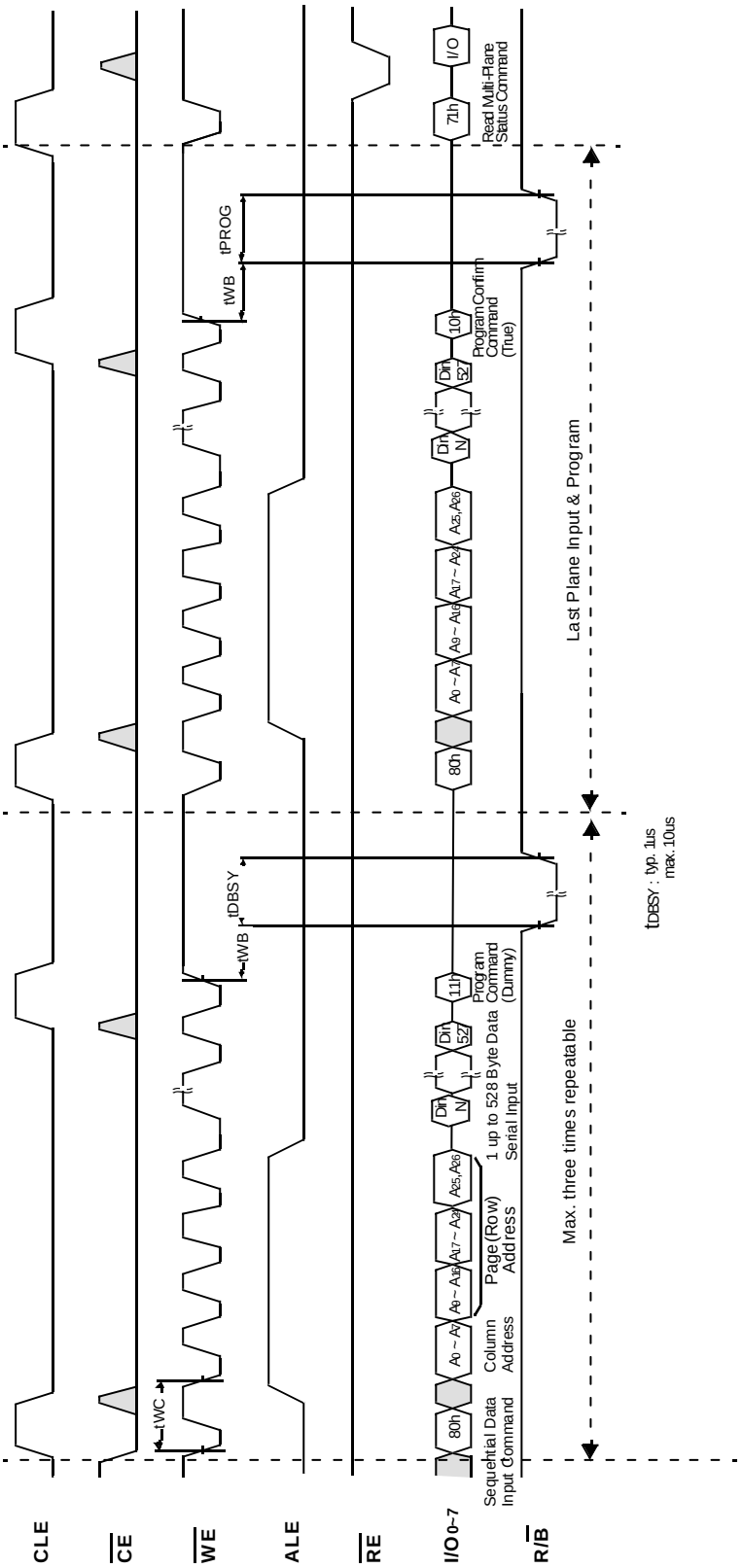
Page Program Operation



BLOCK ERASE OPERATION(ERASE ONE BLOCK)

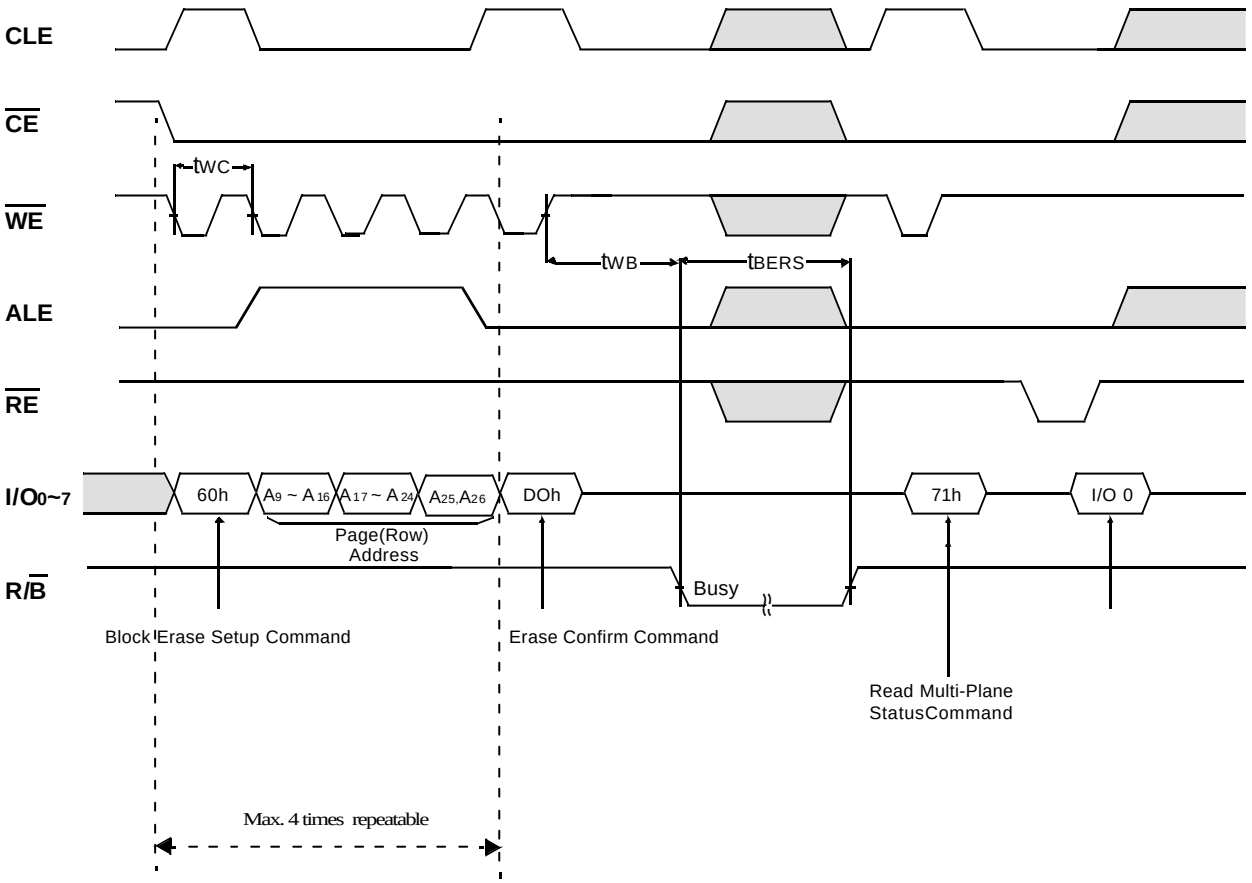


Multi-Plane Page Program Operation



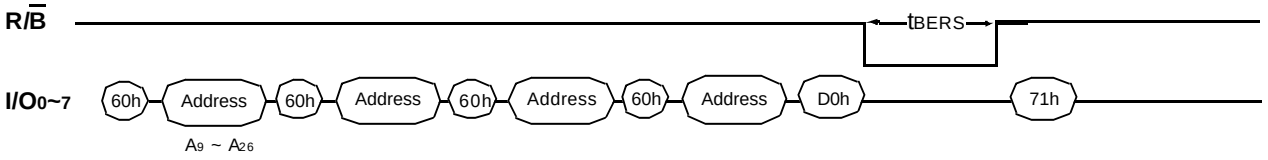
Ex.) Four-Plane Page Program into Plane 0~3 or Plane 4~7

Multi-Plane Block Erase Operation into Plane 0~3 or Plane 4~7

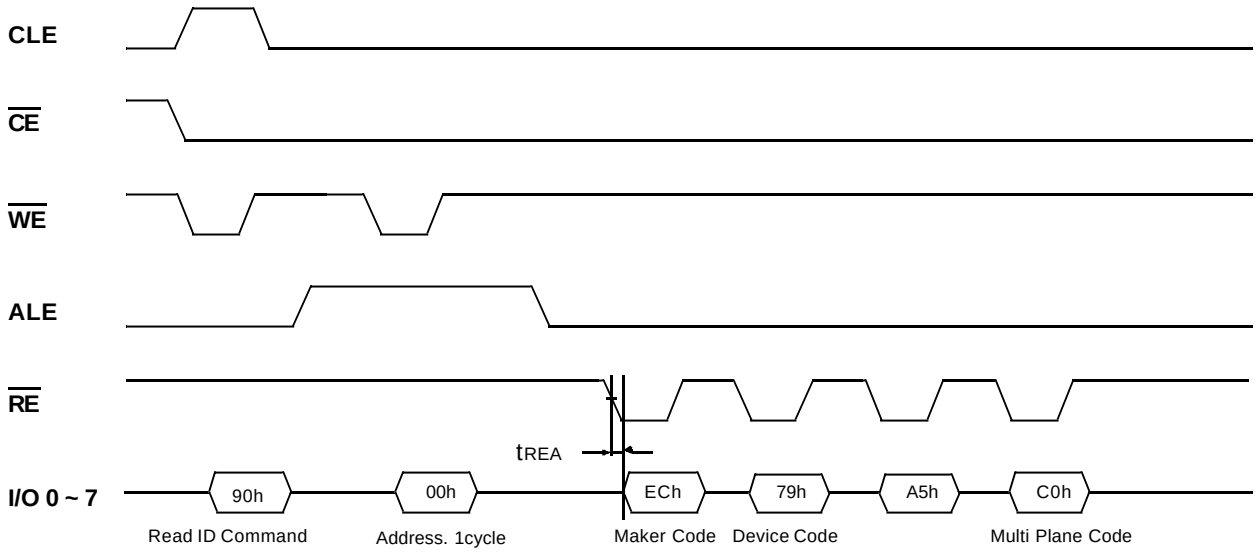


* For Multi-Plane Erase operation, Block address to be erased should be repeated before "D0H" command.

Ex.) Four-Plane Block Erase Operation



Read ID Operation

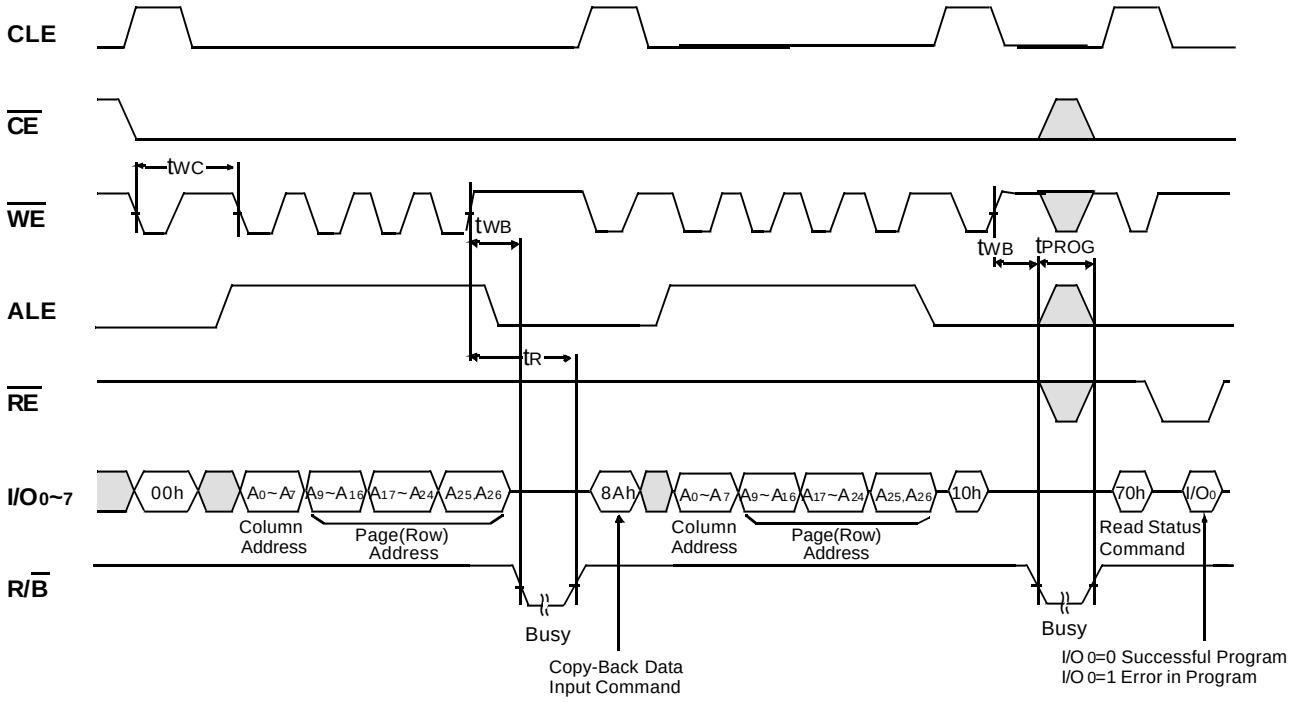


ID Defintition Table

90 ID: Access command = 90H

	Value	Description
1st Byte	ECh	Maker Code
2nd Byte	79h	Device Code
3rd Byte	A5h	Must be don' t -cared
4th Byte	**C0h**	**Supports Multi Plane Operation**

Copy-Back Program Operation



Device Operation

PAGE READ

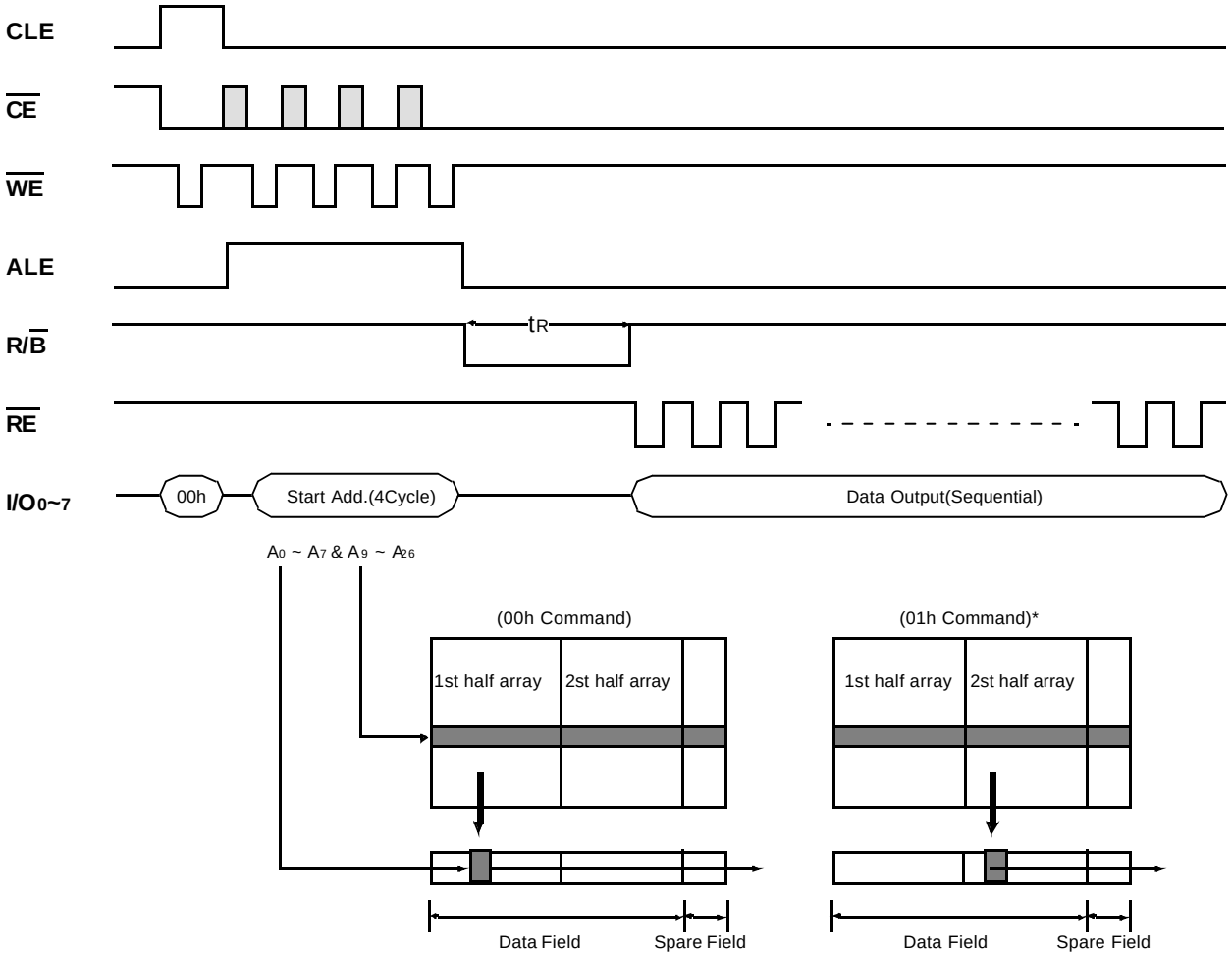
Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with four address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available : random read, serial page read and sequential row read.

The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 12µs(t_R). The system controller can detect the completion of this data transfer(t_R) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$. High to low transitions of the $\overline{RE}$ clock output the data stating from the selected column address up to the last column address.

After the data of last column address is clocked out, the next page is automatically selected for sequential row read.

Waiting 12µs again allows reading the selected page. The sequential row read operation is terminated by bringing $\overline{CE}$ high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command. Addresses A_0 to A_3 set the starting address of the spare area while addresses A_4 to A_7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command(00h/01h) is needed to move the pointer back to the main area. Figures 8 to 11 show typical sequence and timings for each read operation.

Figure 8. Read1 Operation



* After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

Figure 9. Read2 Operation

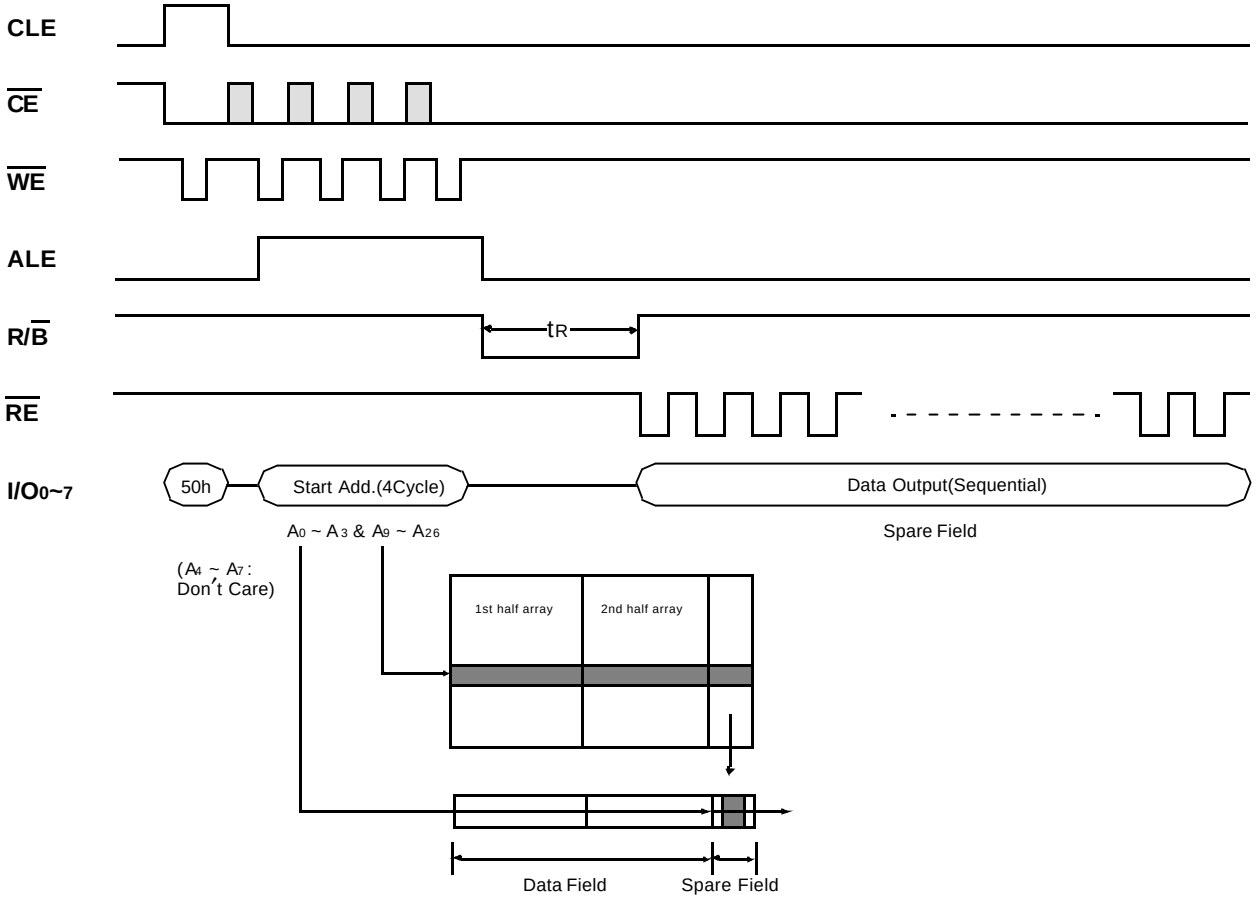
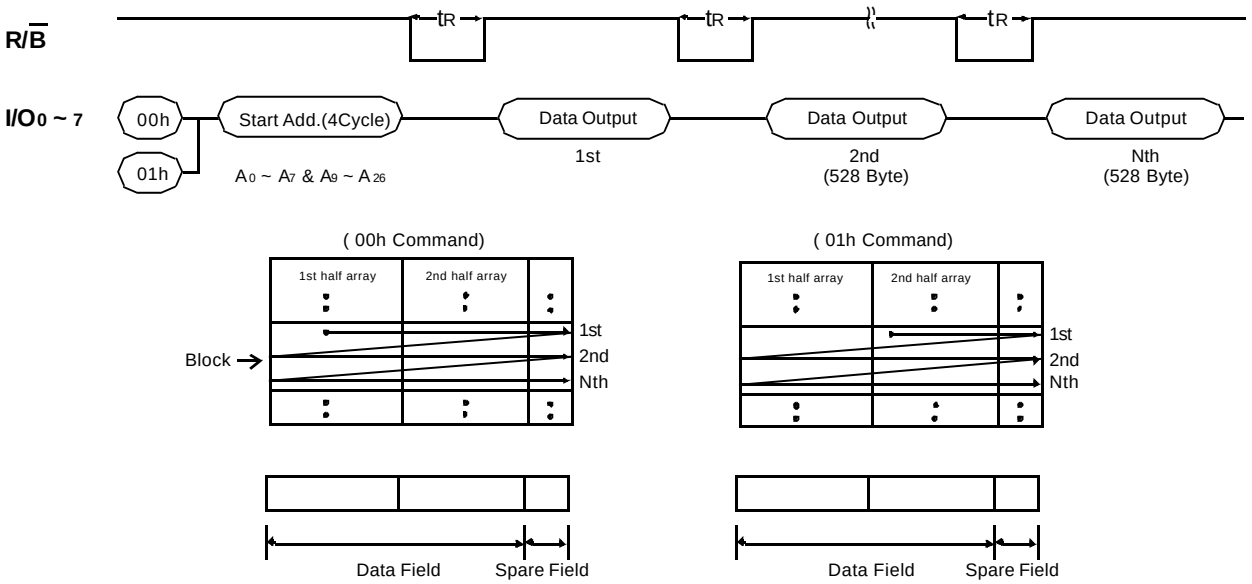
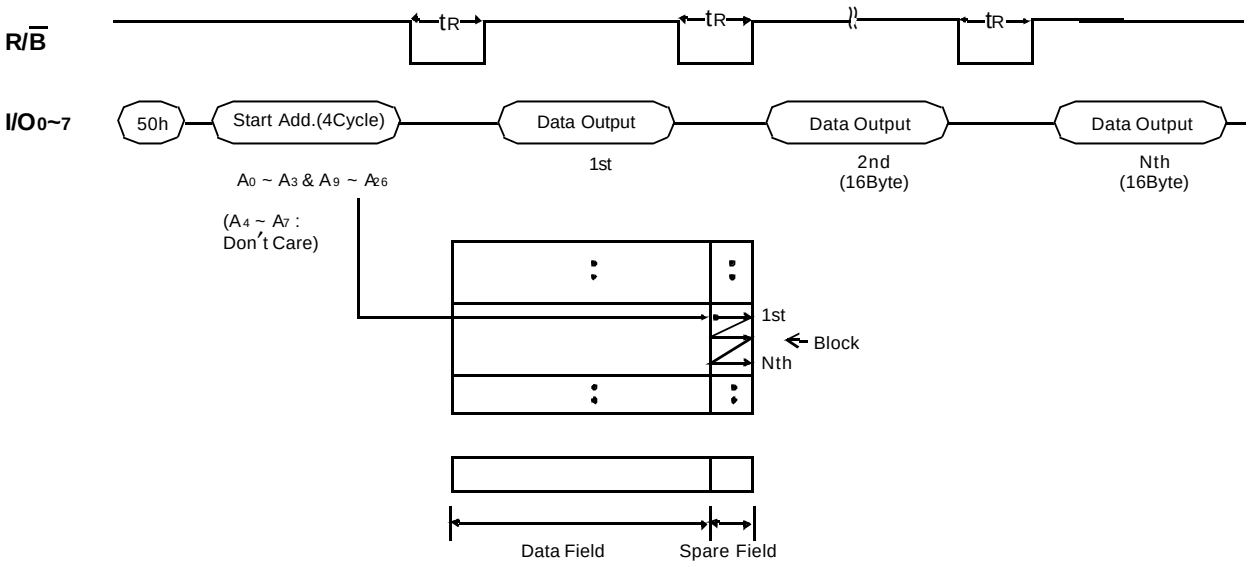


Figure 10. Sequential Row Read1 Operation



The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is read-out, the sequential read operation must be terminated by bringing $\overline{CE}$ high. When the page address moves onto the next block, read command and address must be given.

Figure 11. Sequential Row Read2 Operation

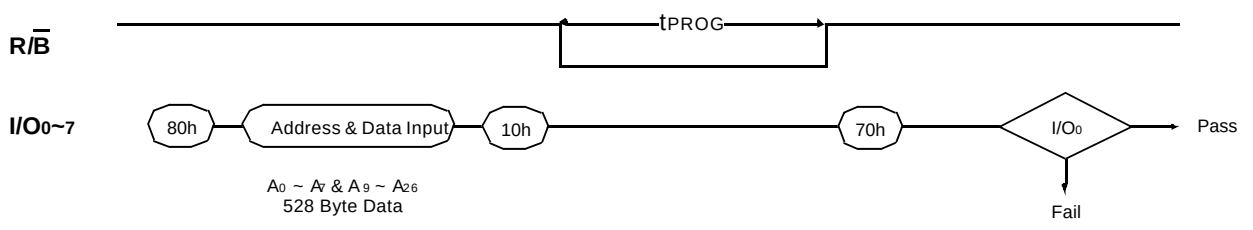


PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 for main array and 2 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the four cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded.The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state control automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 12). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

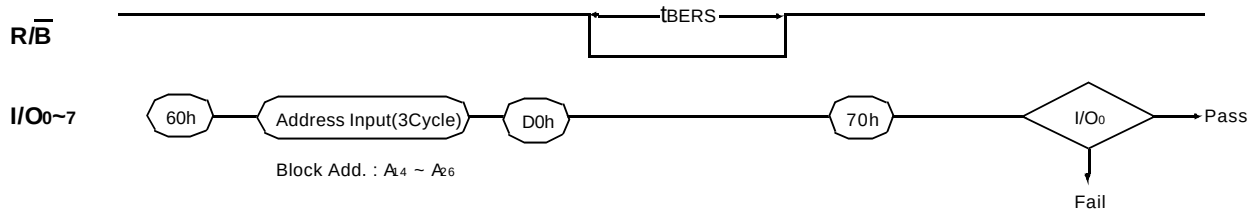
Figure 12. Program & Read Status Operation



BLOCK ERASE

The Erase operation is done on a block(16K Byte) basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A_{14} to A_{26} is valid while A_9 to A_{13} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 13 details the sequence.

Figure 13. Block Erase Operation

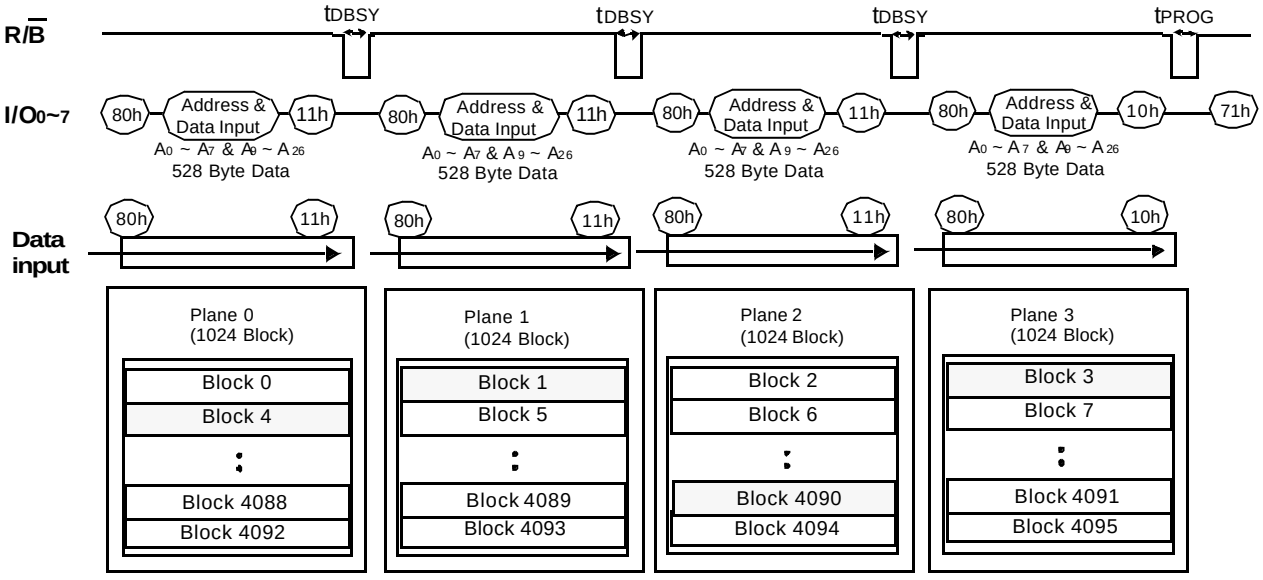


Multi-Plane Page Program into Plane 0~3 or Plane 4~7

Multi-Plane Page Program is an extension of Page Program, which is executed for a single plane with 528 byte page registers. Since the device is equipped with eight memory planes, activating the four sets of 528 byte page registers into plane 0~3 or plane 4~7 enables a simultaneous programming of four pages. Partial activation of four planes is also permitted.

After writing the first set of data up to 528 byte into the selected page register, Dummy Page Program command (11h) instead of actual Page Program (10h) is inputted to finish data-loading of the current plane and move to the next plane. Since no programming process is involved, R/$\overline{B}$ remains in Busy state for a short period of time(tDBSY). Read Status command (standard 70h or alternate 71h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit(I/O 6). Then the next set of data for one of the other planes is inputted with the same command and address sequences. After inputting data for the last plane, actual True Page Program (10h) instead of dumy Page Program command (11h) must be followed to start the programming process. The operation of R/$\overline{B}$ and Read Status is the same as that of Page Program. Since maximum four pages into plane 0~3 or plane 4~7 are programmed simultaneously, pass/fail status is available for each page when the program operation completes. The extended status bits (I/O1 through I/O 4) are checked by inputting the Read Multi-Plane Status Register. Status bit of I/O 0 is set to "1" when any of the pages fails.
Multi-Plane page Program with "01h" pointer is not supported, thus prohibited.

Figure 14. Four-Plane Page Program



Restriction in addressing with Multi Plane Page Program

While any block in each plane may be addressable for Multi-Plane Page Program, the five least significant addresses(A9-A13) for the selected pages at one operation must be the same. Figure 15 shows an example where 2nd page of each addressed block is selected for four planes. However, any arbitrary sequence is allowed in addressing multiple planes as shown in Figure16.

Figure 15. Multi-Plane Program & Read Status Operation

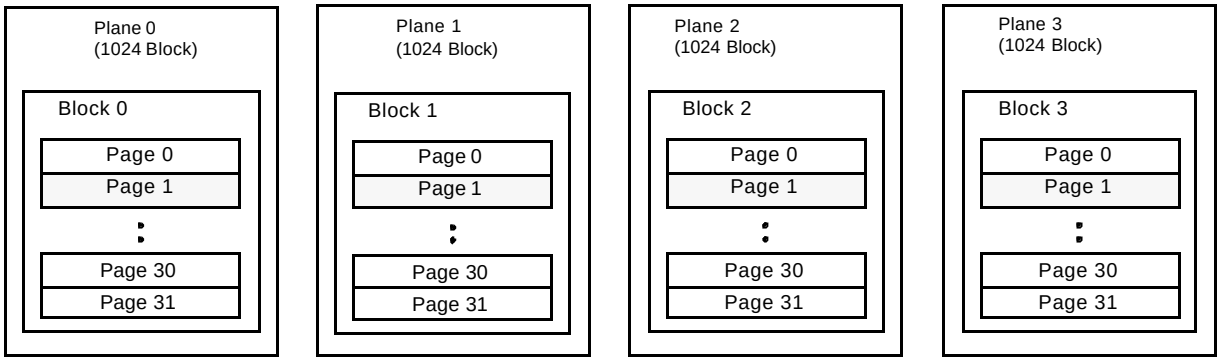


Figure 16. Addressing Multiple Planes

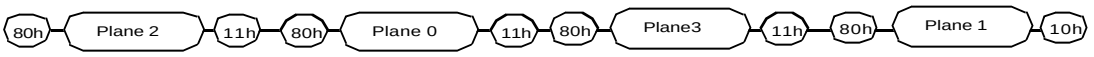
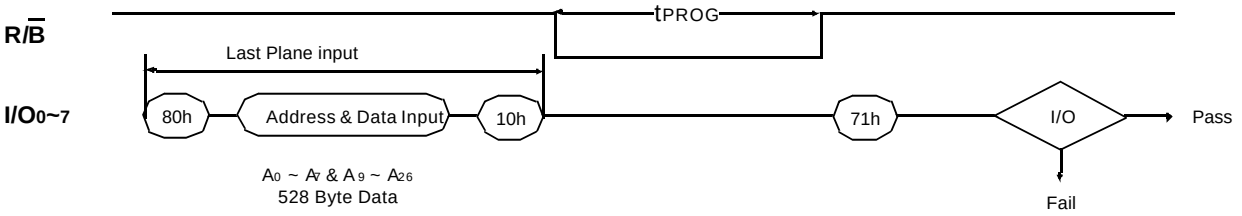


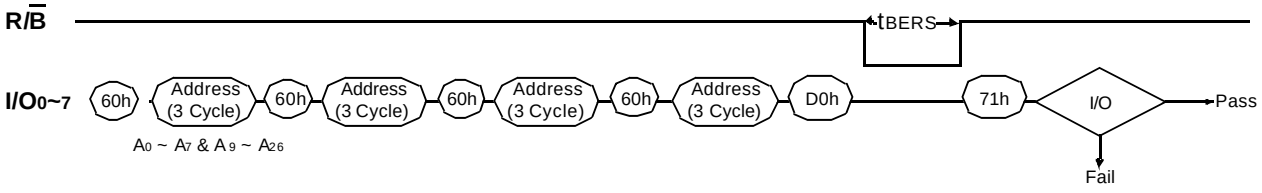
Figure 17. Multi-Plane Page Program & Read Status Operation



Multi-Plane Block Erase into Plane 0~3 or Plane 4~7

Basic concept of Multi-Plane Block Erase operation is identical to that of Multi-Plane Page Program. Up to four blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command followed by three address cycles) may be repeated up to four times for erasing up to four blocks. Only one block should be selected from each plane. The Erase Confirm command initiates the actual erasing process. The completion is detected by analyzing R/$\overline{B}$ pin or Ready/Busy status (I/O 6). Upon the erase completion, pass/fail status of each block is examined by reading extended pass/fail status(I/O 1 through I/O 4).

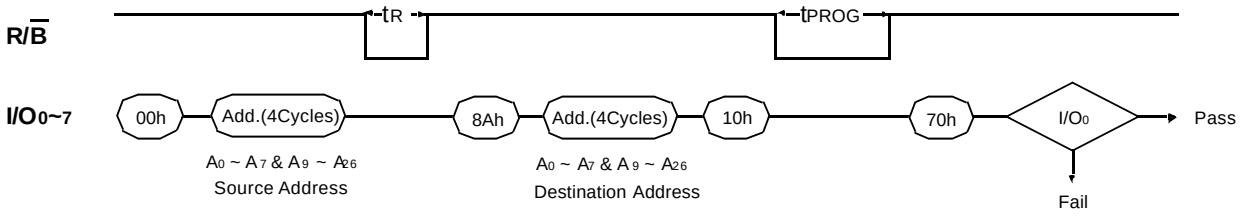
Figure 18. Four Block Erase Operation



Copy-Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page within the plane to another page within the same plane without utilizing an external memory. Since the time-consuming sequently-reading and its re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command and the address of the source page moves the whole 528byte data into the internal buffer. As soon as the device returns to Ready state, Page-Copy Data-input command (8Ah) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. A14 , A15 and A26 must be the same between source and target page. Figure19 shows the command sequence for single plane operation. **"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation."**

Figure 19. One Page Copy-Back program Operation

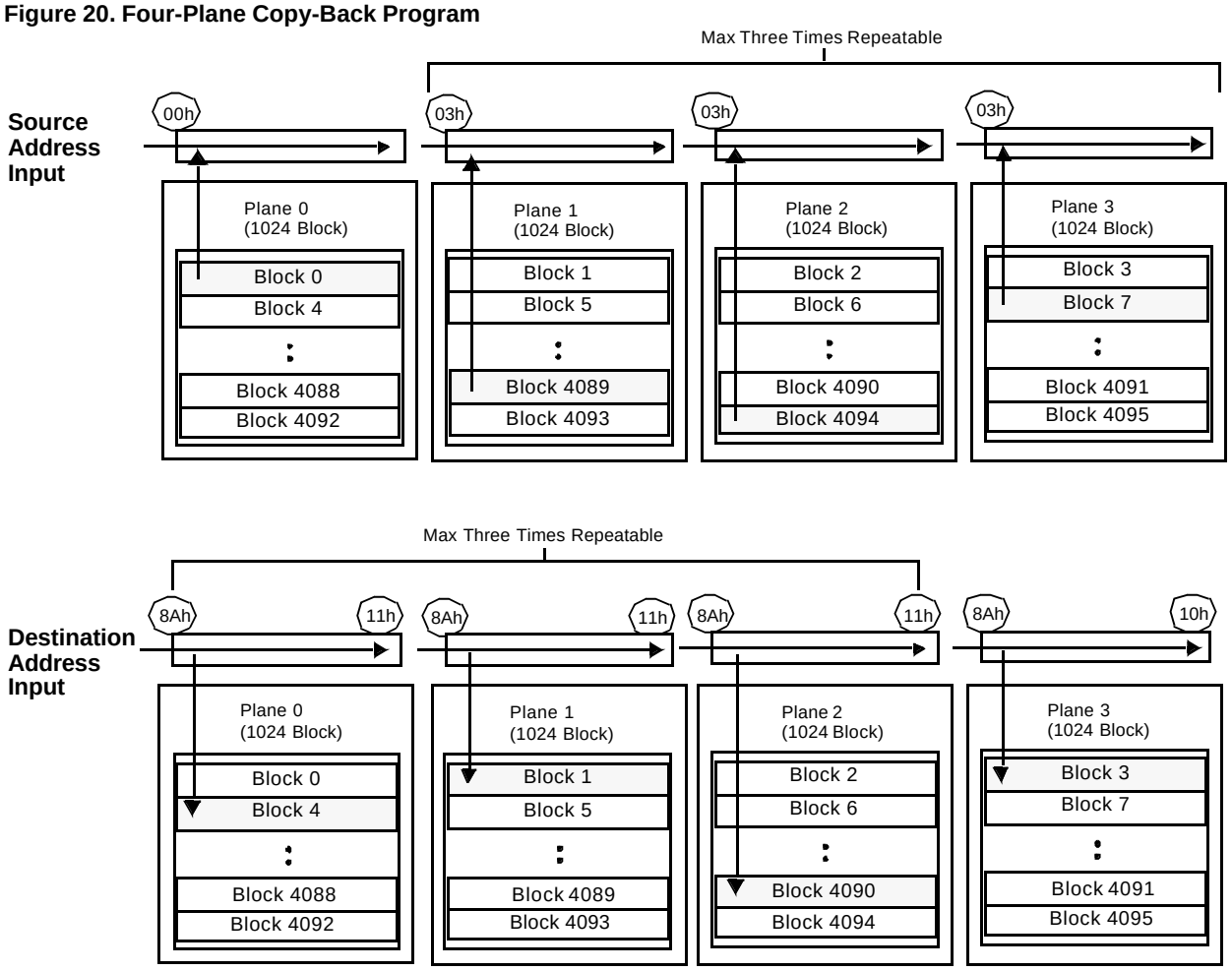


Multi-Plane Copy-Back Program

Multi-Plane Copy-Back Program is an extension of one page Copy-Back Program into four plane operation. Since the device is equipped with four memory planes, activating the four sets of 528 byte page registers enables a simultaneous Multi-Plane Copy-Back programming of four pages. Partial activation of four planes is also permitted.

First, normal read operation with the "00h"command and address of the source page moves the whole 528 byte data into internal page buffers. Any further read operation for transferring the addressed pages to the corresponding page register must be executed with "03h" command instead of "00h" command. Any plane may be selected without regard to "00h" or "03h". Up to four planes may be addressed. Data moved into the internal page registers are loaded into the destination plane addresses. After the input of command sequences for reading the source pages, the same procedure as Multi-Plane Page programming except for a replacement address command with "8Ah" is executed. Since no programming process is involved during data loading at the destination plane address , R/$\overline{B}$ remains in Busy state for a short period of time(tDBSY). Read Status command (standard 70h or alternate 71h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit(I/O 6). After inputting data for the last plane, actual True Page Program (10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/$\overline{B}$ and Read Status is the same as that of Page Program. Since maximum four pages are programmed simultaneously, pass/fail status is available for each page when the program operation completes. No pointer operation is supported with Multi-Plane Copy-Back Program. **Once the Multi-Plane Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase once the Multi-Plane Copy-Back Program is finished.**

Figure 20. Four-Plane Copy-Back Program



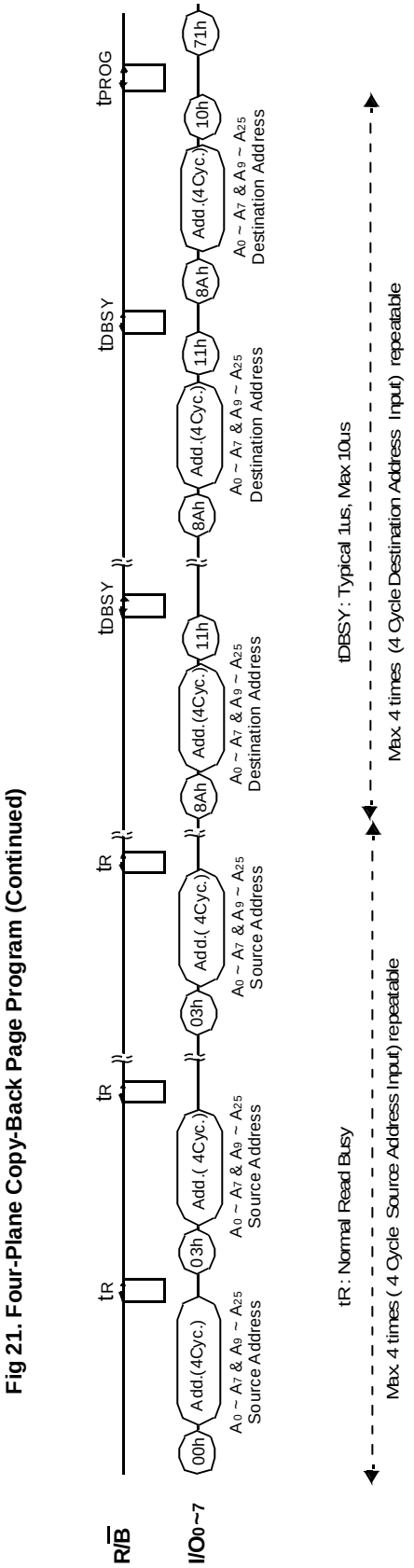


Fig 21. Four-Plane Copy-Back Page Program (Continued)

READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 4 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

For Read Status of Multi Plane Program/Erase, the Read Multi-Plane Status command(71h) should be used to find out whether multi-plane program or erase operation is completed, and whether the program or erase operation is completed successfully. The pass/fail status data must be checked only in the Ready condition after the completion of Multi-Plane program or erase operation.

Table4. Read Staus Register Definition

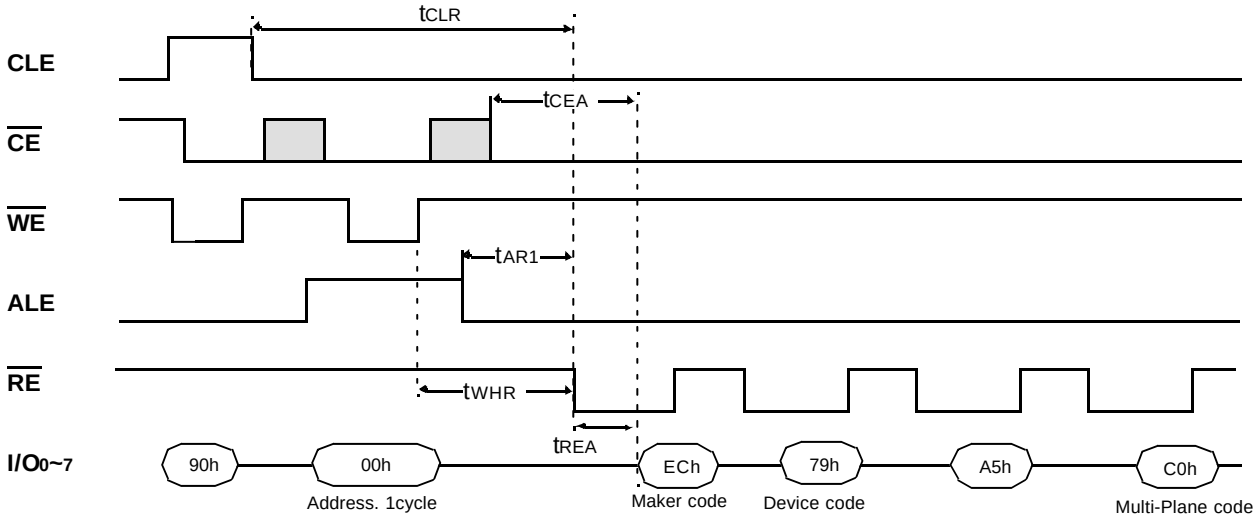
I/O No.	Status	Definition by 70h Command		Definition by 71h Command	
I/O 0	Total Pass/Fail	Pass : "0"	Fail : "1"	Pass : "0"(1)	Fail : "1"
I/O 1	Plane 0 Pass/Fail	Must be don' t -cared		Pass : "0"(2)	Fail : "1"
I/O 2	Plane 1 Pass/Fail	Must be don' t -cared		Pass : "0"(2)	Fail : "1"
I/O 3	Plane 2 Pass/Fail	Must be don' t -cared		Pass : "0"(2)	Fail : "1"
I/O 4	Plane 3 Pass/Fail	Must be don' t -cared		Pass : "0"(2)	Fail : "1"
I/O 5	Reserved	Must be don' t -cared		Must be don' t-cared	
I/O 6	Device Operation	Busy : "0"	Ready : "1"	Busy : "0"	Ready : "1"
I/O 7	Write Protect	Protected : "0"	Not Protected : "1"	Protected : "0"	Not Protected : "1"

NOTE : 1. I/O 0 describes combined Pass/Fail condition for all planes. If any of the selected multiple pages/blocks fails in Program/ Erase operation, it sets "Fail" flag.
2. The pass/fail status applies only to the corresponding plane.

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacture code(ECh), and the device code (79h), Reserved(A5h), Multi plane operation code(C0h) respectively. A5h must be don' t-cared. C0h means that device supports Multi Plane operation. The command register remains in Read ID mode until further commands are issued to it. Figure 22 shows the operation sequence.

Figure 22. Read ID Operation 1



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 5 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Refer to Figure 23 below.

Figure 23. RESET Operation

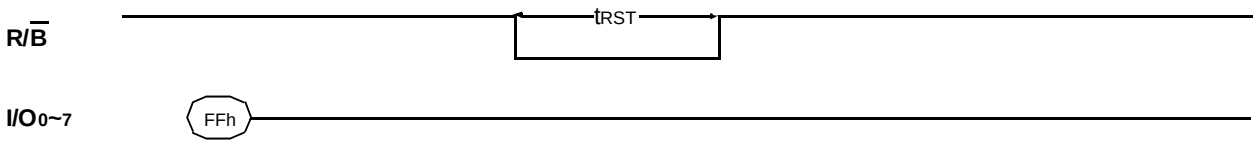


Table5. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 24). Its value can be determined by the following guidance.

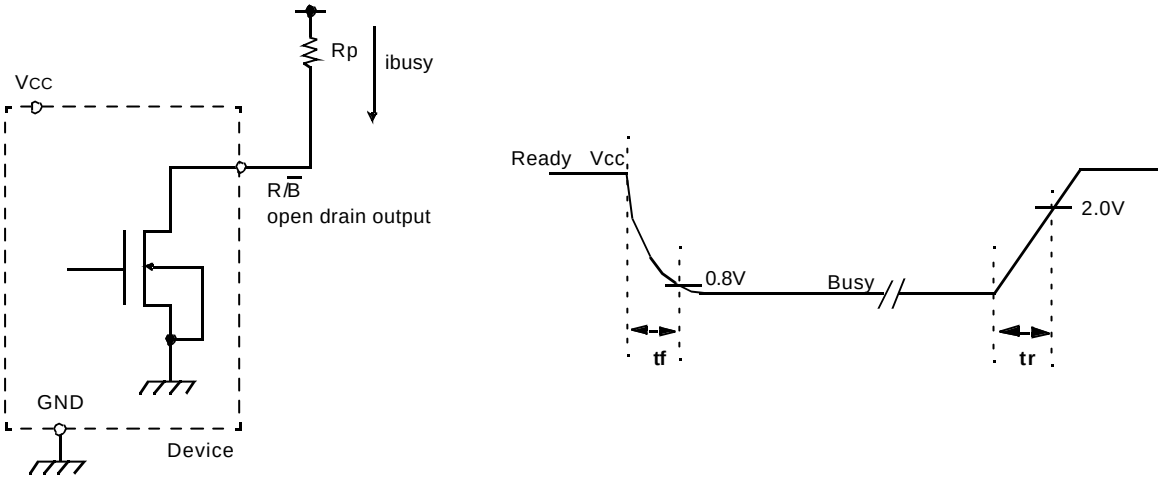
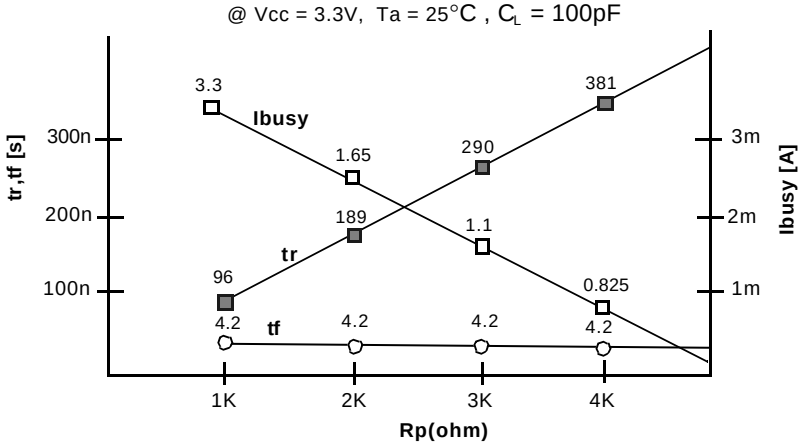


Fig 24 Rp vs tr ,tf & Rp vs ibusy

@ Vcc = 3.3V, Ta = 25°C , C_L = 100pF



Rp value guidance

$$Rp(min) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

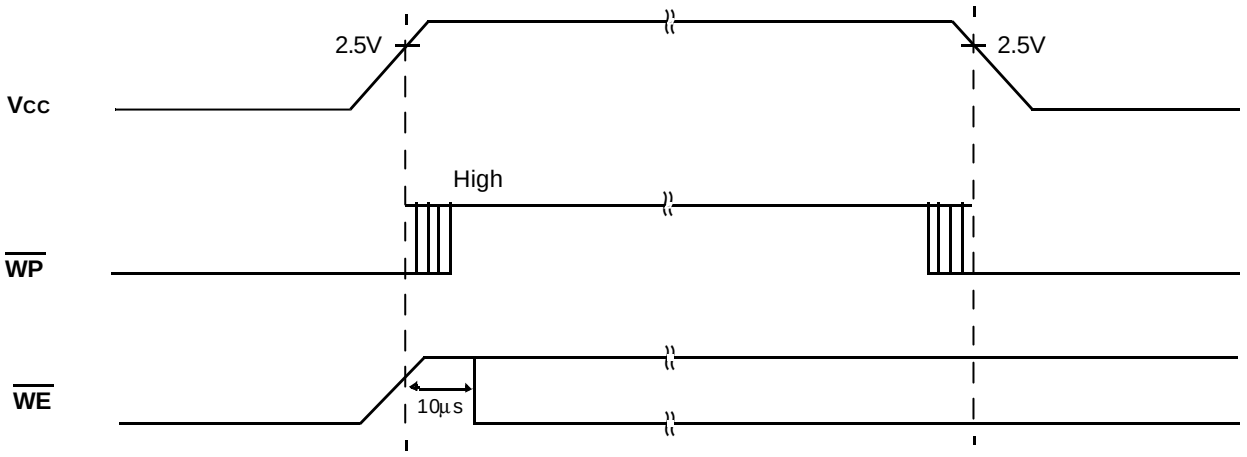
where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 10 µs is required before internal circuit gets ready for any command sequences as shown in Figure 25. The two step command sequence for program/erase provides additional software protection.

Figure 25. AC Waveforms for Power Transition



Package Dimensions

48-Pin Lead Plastic Thin Small Out-Line Package Type(I)