

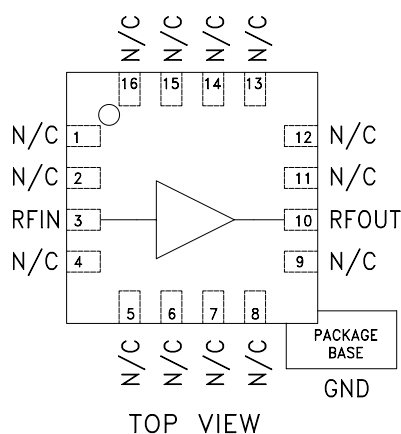
InGaP HBT GAIN BLOCK MMIC AMPLIFIER, DC - 6.0 GHz

Typical Applications

The HMC311LP3 is an ideal RF/IF gain block or LO buffer amplifier for:

- Cellular / PCS / 3G
- Fixed Wireless & WLAN
- CATV & Cable Modem
- Microwave Radio

Functional Diagram



Features

P1dB Output Power: +15.5 dBm

Output IP3: +32 dBm

Gain: 14.5 dB

50 Ohm I/O's

3 x 3 x 1 mm QFN SMT Package

General Description

The HMC311LP3 is a GaAs InGaP Heterojunction Bipolar Transistor (HBT) Gain Block MMIC SMT DC to 6 GHz amplifier. This 3x3mm QFN packaged amplifier can be used as either a cascadable 50 Ohm gain stage or to drive the LO of HMC mixers with up to +17 dBm output power. The HMC311LP3 offers 14.5 dB of gain and an output IP3 of +30 dBm while requiring only 56 mA from a +5V supply. The Darlington feedback pair used results in reduced sensitivity to normal process variations and yields excellent gain stability over temperature while requiring a minimal number of external bias components.

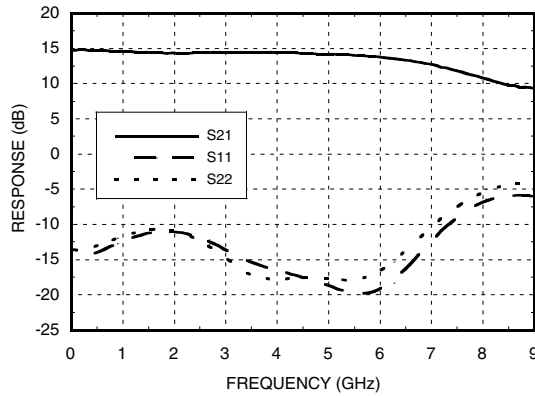
Electrical Specifications, $V_s = 5.0$ V, $R_{bias} = 22$ Ohm, $T_A = +25^\circ$ C

Parameter		Min.	Typ.	Max.	Units
Gain	DC - 1.0 GHz	13.0	14.5		dB
	1.0 - 4.0 GHz	12.5	14.3		dB
	4.0 - 6.0 GHz	12.0	14.0		dB
Gain Variation Over Temperature	DC - 2.0 GHz		0.005	0.008	dB/ °C
	2.0 - 4.0 GHz		0.008	0.012	dB/ °C
	4.0 - 6.0 GHz		0.012	0.016	dB/ °C
Return Loss Input / Output	DC - 1.0 GHz		13		dB
	1.0 - 3.0 GHz		11		dB
	3.0 - 6.0 GHz		15		dB
Reverse Isolation	DC - 6.0 GHz		18		dB
Output Power for 1 dB Compression (P1dB)	DC - 2.0 GHz	13.5	15.5		dBm
	2.0 - 4.0 GHz	12.0	15.0		dBm
	4.0 - 6.0 GHz	10.0	13.0		dBm
Output Third Order Intercept (IP3)	DC - 1.0 GHz		32		dBm
	1.0 - 2.0 GHz		30		dBm
	2.0 - 4.0 GHz		28		dBm
	4.0 - 6.0 GHz		24		dBm
Noise Figure	DC - 6.0 GHz		4.5		dB
Supply Current (Icq)			56		mA

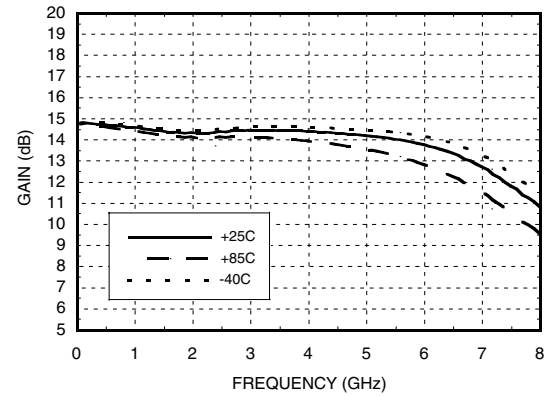
Note: Data taken with broadband bias tee on device output.

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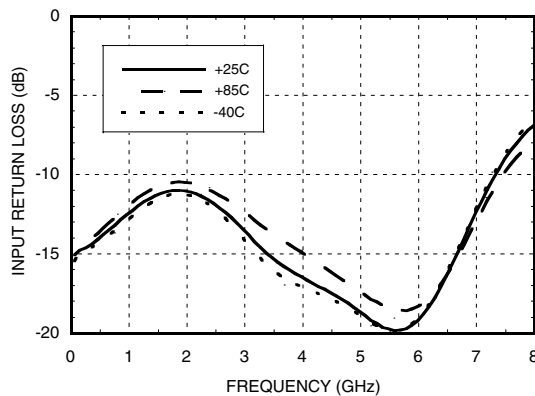
Gain & Return Loss



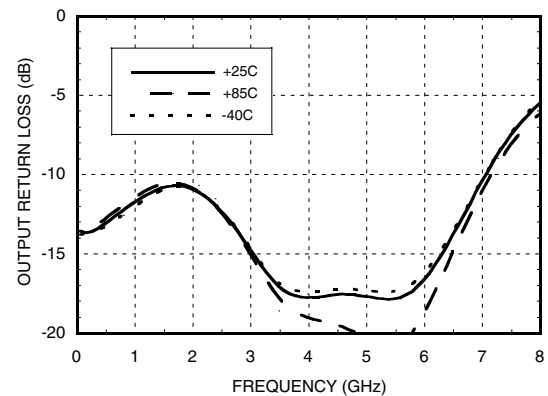
Gain vs. Temperature



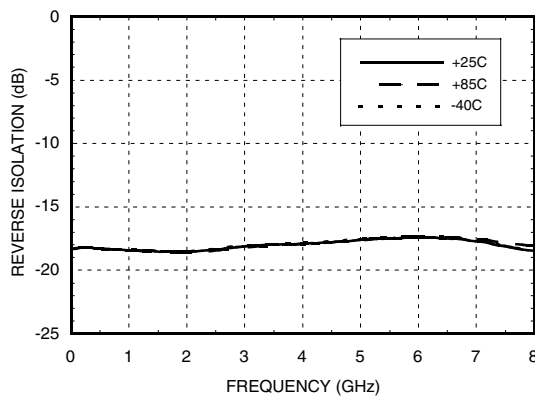
Input Return Loss vs. Temperature



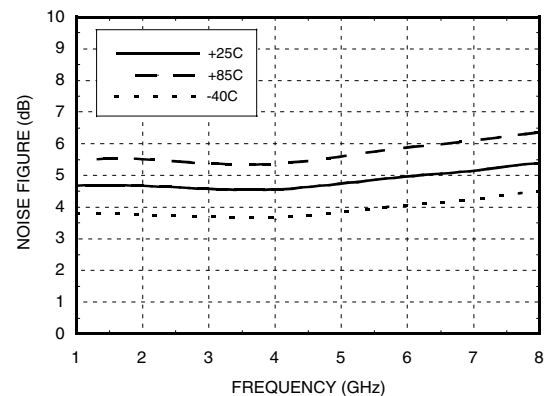
Output Return Loss vs. Temperature



Reverse Isolation vs. Temperature



Noise Figure vs. Temperature

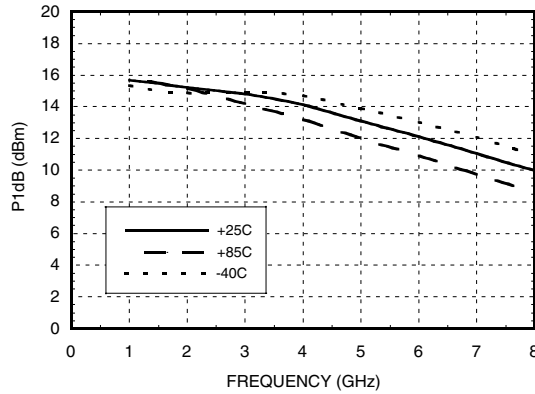


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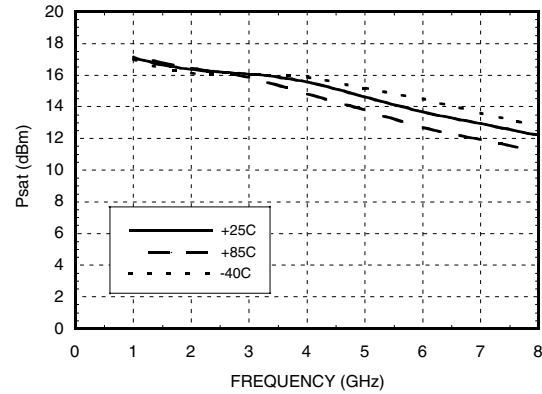
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AMPLIFIERS - SMT

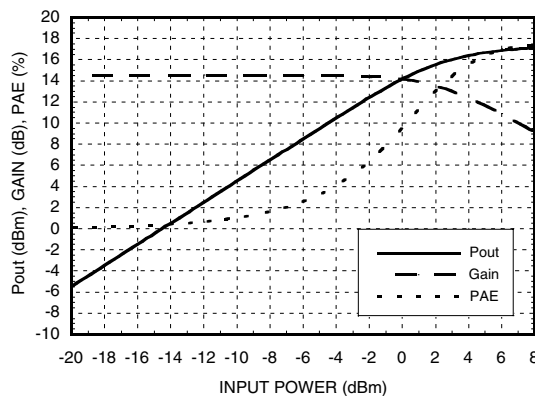
P1dB vs. Temperature



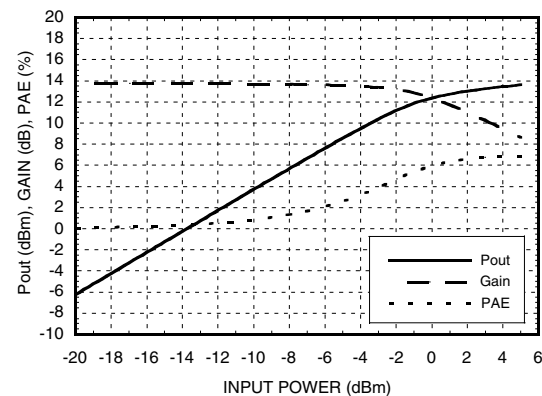
Psat vs. Temperature



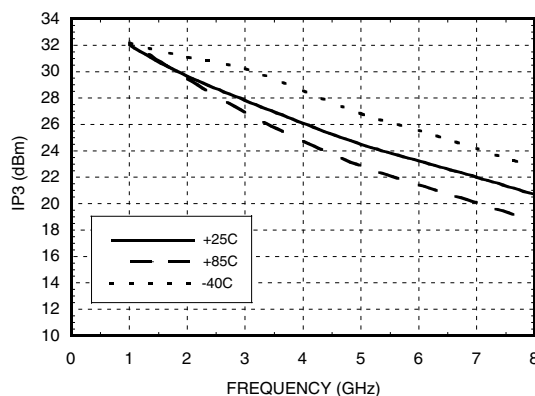
Power Compression @ 1 GHz



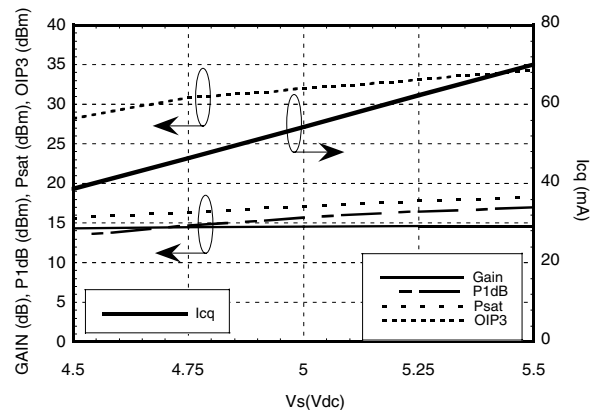
Power Compression @ 6 GHz



Output IP3 vs. Temperature



Gain, Power, OIP3 & Supply Current vs. Supply Voltage @ 1 GHz

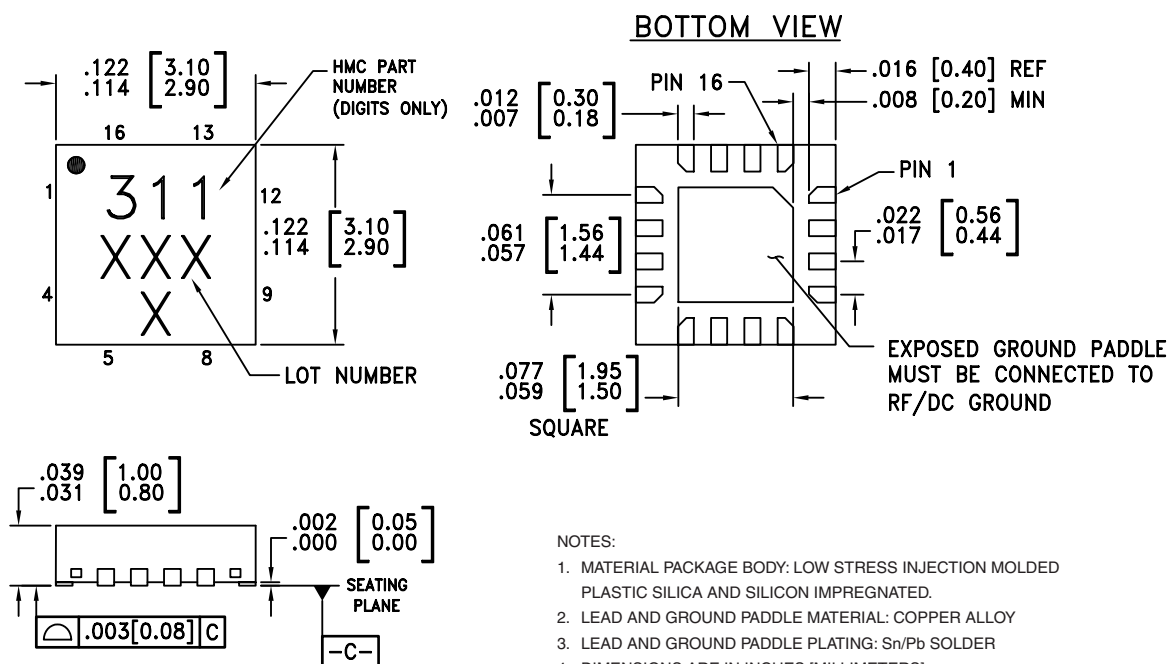


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Absolute Maximum Ratings

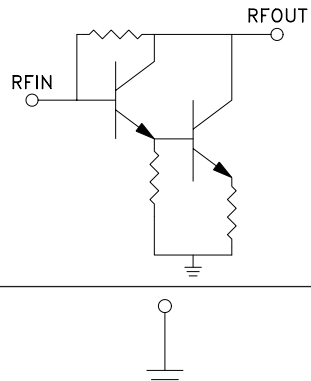
Collector Bias Voltage (Vcc)	+7.0 Vdc
RF Input Power (RFIn)(Vs = +5.0 Vdc)	+10 dBm
Junction Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 5.21 mW/°C above 85 °C)	0.339 W
Thermal Resistance (junction to ground paddle)	192 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Outline Drawing

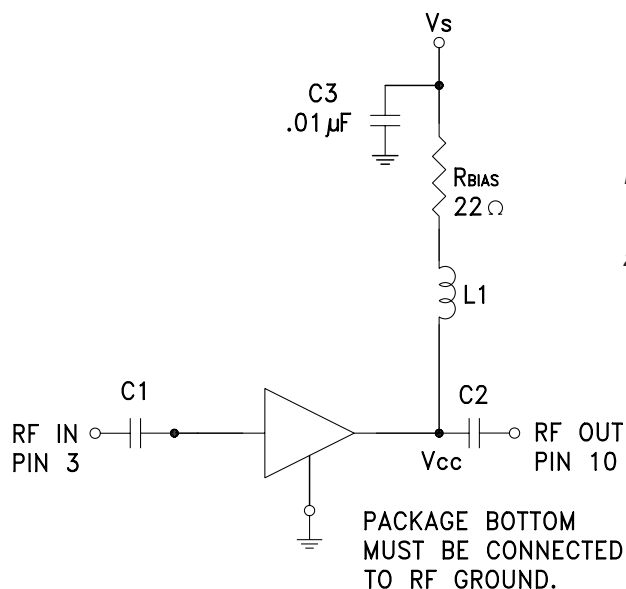


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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2, 4 - 9, 11 - 16	N/C	This pin may be connected to RF ground.	
3	RFIN	This pin is DC coupled. An off chip DC blocking capacitor is required.	
10	RFOUT	RF output and DC Bias for the output stage.	
	GND	Package bottom must be connected to RF/DC ground.	

Application Circuit



Note:

1. Select R_{bias} to achieve I_{cq} using equation below,
 $R_{bias} \geq 22 \text{ Ohm}$.
2. External blocking capacitors are required on
RFIN and RFOUT.

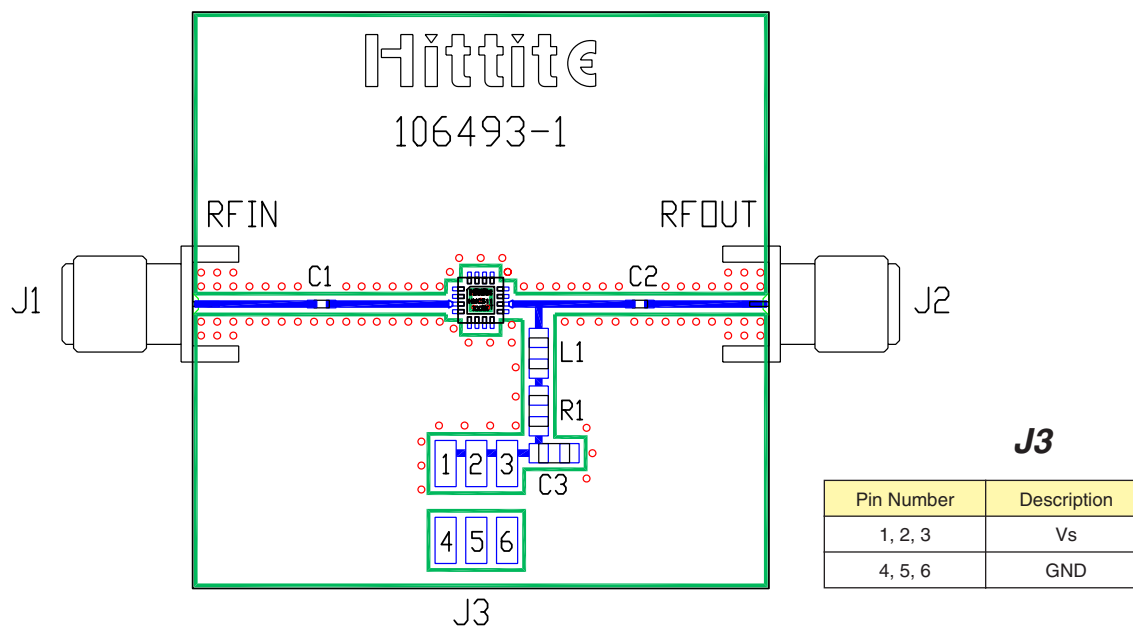
$$I_{cq} = \frac{V_s - 3.9}{R_{bias}}$$

Recommended Component Values

Component	Frequency (MHz)							
	50	900	1900	2200	2400	3500	5200	5800
L1	270 nH	56 nH	18 nH	18 nH	15 nH	8.2 nH	3.3 nH	3.3 nH
C1, C2	0.01 μ F	100 pF	100 pF	100 pF	100 pF	100 pF	100 pF	100 pF

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Evaluation PCB



List of Materials

Item	Description
J1 - J2	PC Mount SMA Connector
J3	2 mm DC Header
C1, C2	Capacitor, 0402 Pkg.
C3	10,000 pF Capacitor, 0805 Pkg.
R1	22 Ohm Resistor, 0805 Pkg.
L1	Inductor, 0805 Pkg.
U1	HMC311LP3
PCB*	106493 Evaluation PCB
* Circuit Board Material: Rogers 4350	

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.