HMC421QS16

PCS/UMTS HIGH IP3 RFIC DOWNCONVERTER, 1.4 - 2.3 GHz

Typical Applications

The HMC421QS16 is ideal for:

- GSM, GPRS & EDGE Infrastructure
- CDMA, WCDMA Infrastructure
- PHS & PDC Infrastructure

Features

+19 dBm Input IP3

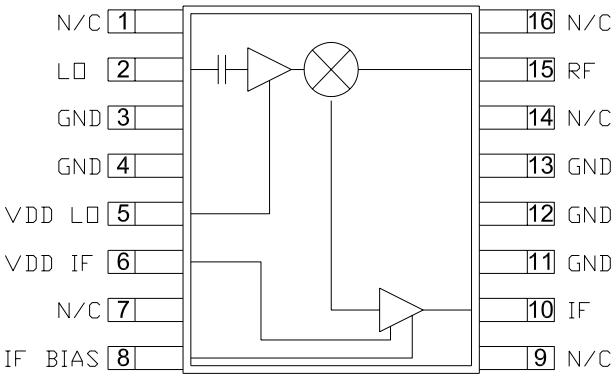
Integrated IF & LO Amps: +10 dBm LO

Conversion Gain: 9 dB

Noise Figure: 9 dB

Single Positive Supply: +5V, 60 mA

Functional Diagram



General Description

The HMC421QS16 is a high linearity down-converter receiver IC suitiable for PCS/UMTS infrastructure applications. The receiver IC is designed to support UMTS applications where a high third order intercept point (OIP3) is required. A passive mixer coupled with a high dynamic range IF amplifier achieves an Input IP3 of +19 dBm. The converter provides a gain of 8 dB and 9 dB typical single side band noise. The IC operates from positive +5V rails and consumes 60 mA of current. The design requires no external Baluns. The mixer supports IF frequencies between 50 MHz and 300 MHz.

Electrical Specifications, T_A = +25° C, LO = +10 dBm, Vdd = 5V

Parameter	IF= 100 MHz			IF= 250 MHz			IF= 250 MHz			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range, RF	1.4 - 1.6			1.7 - 2.0			2.0 - 2.3			GHz
Frequency Range, LO	1.3 - 1.55			1.4 - 1.95			1.7 - 2.25			GHz
Frequency Range, IF*	50 - 100			50 - 300			50 - 300			MHz
Conversion Gain	6	9		7	9		5	8		dB
Noise Figure (SSB)		11			9			9.5		dB
LO to RF Isolation	23	29		28	33		26	32		dB
LO to IF Isolation	35	42		42	52		50	60		dB
RF to IF Isolation	35	42		42	52		50	60		dB
IP3 (Input)	15	18		17	19		17	20		dBm
1 dB Compression (Input)	3	6		4	6.5		4	7		dBm
LO Input Drive Level (Typical)	+8 to +12			+8 to +12			+8 to +12			dBm
Supply Current (Idd for LO & IF) (IF bias resistor= 6.8 Ohms)		62			62			62		mA

** If matching must be tuned for optimal results, see application circuit herein.*

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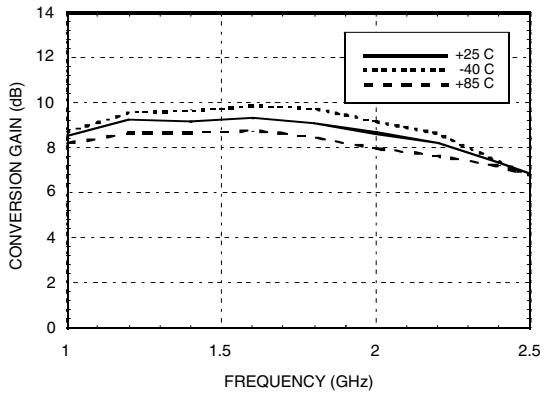
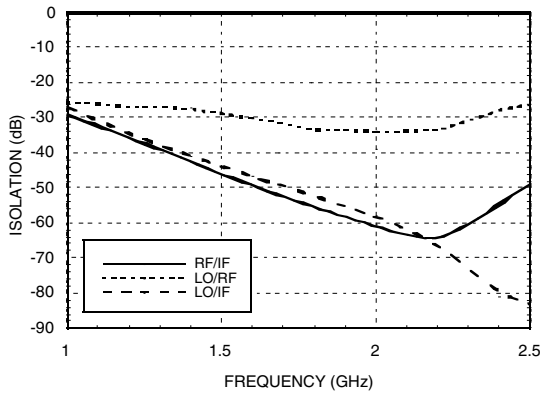
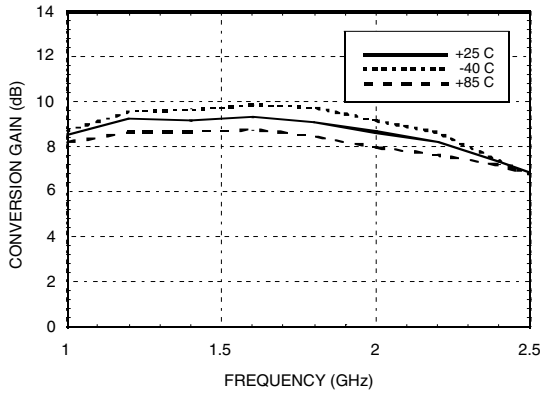
Conversion Gain vs. Temperature @ LO = +10 dBm



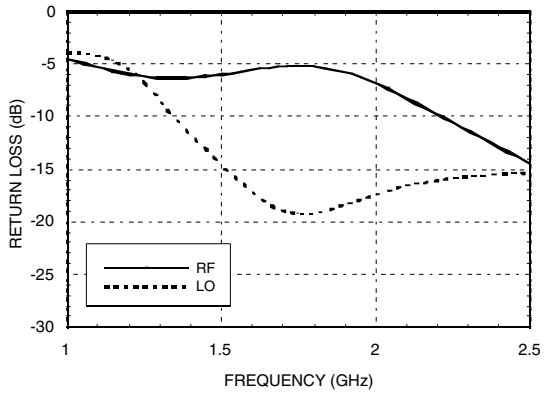
Isolation @ LO = +10 dBm



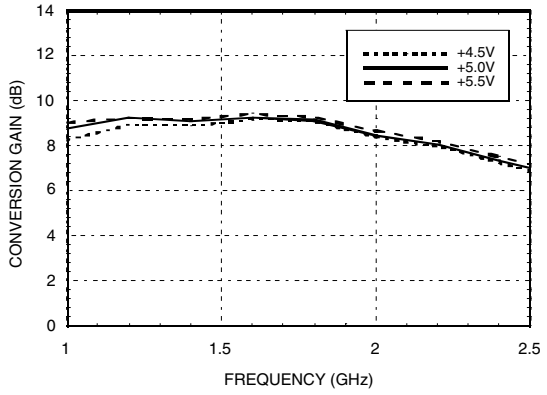
Conversion Gain vs. LO Drive



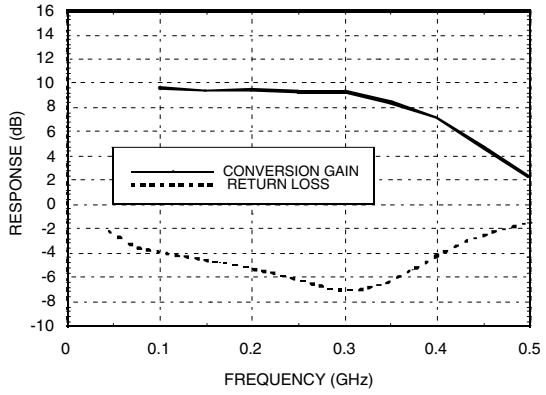
Return Loss @ LO = +10 dBm



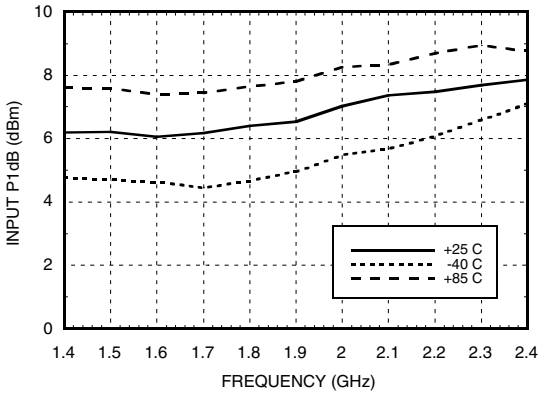
Conversion Gain vs. Vdd @ LO = +10 dBm



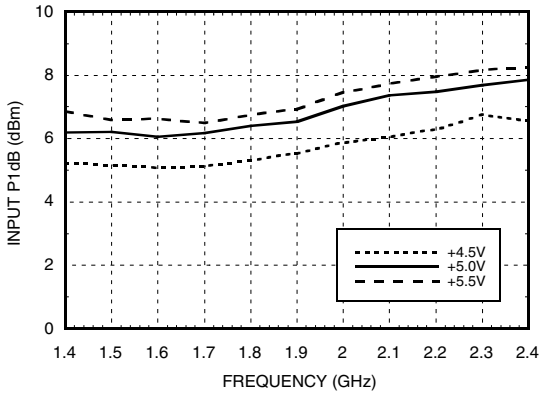
IF Bandwidth @ LO = +10 dBm



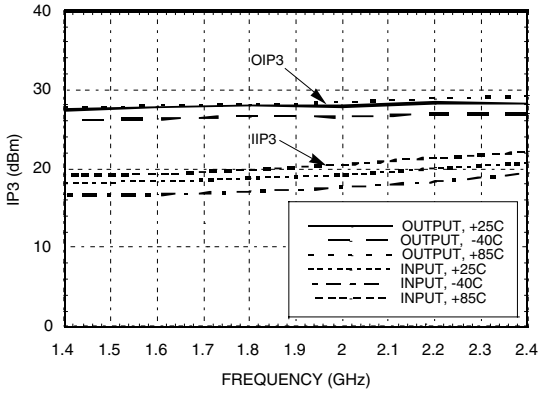
Input P1dB vs. Temperature @ LO = +10 dBm



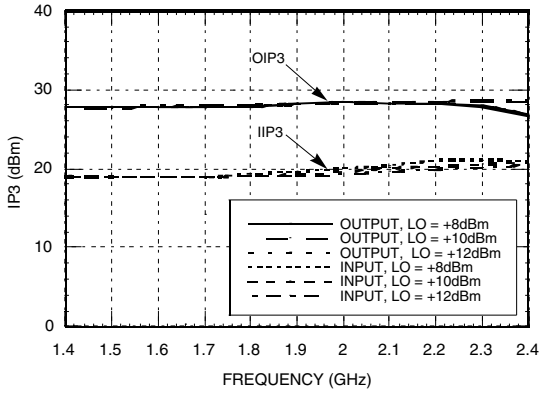
Input P1dB vs. Vdd @ LO = +10 dBm



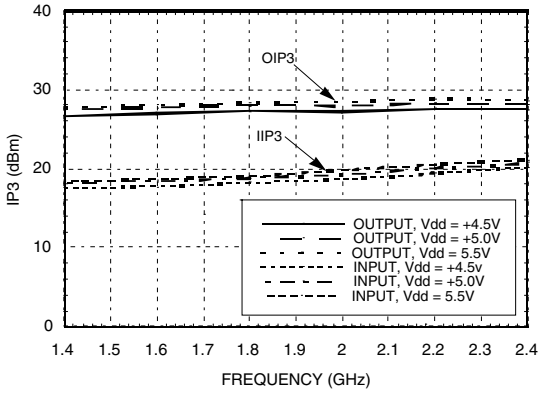
Input and Output IP3 vs. Temperature @ LO = +10 dBm*



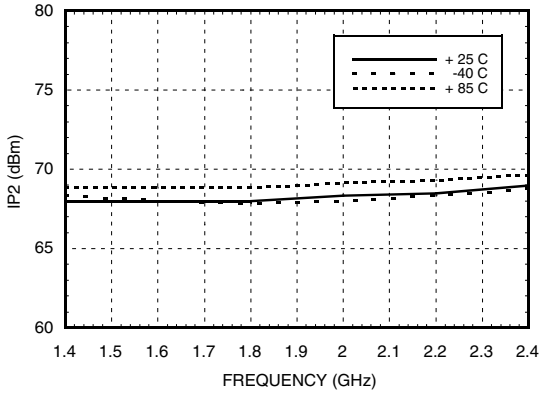
Input and Output IP3 vs. LO Drive*



Input and Output IP3 vs. Vdd @ LO = +10 dBm*

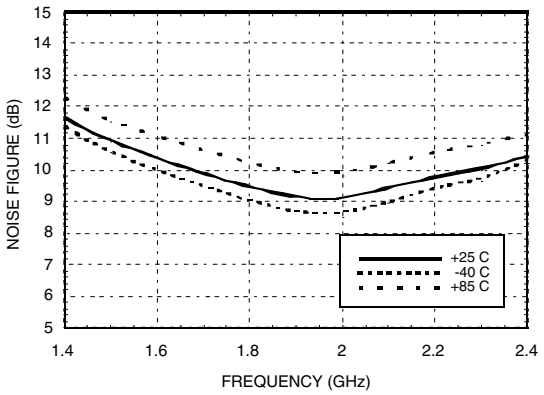


Input IP2 vs. Temperature @ LO = +10 dBm*

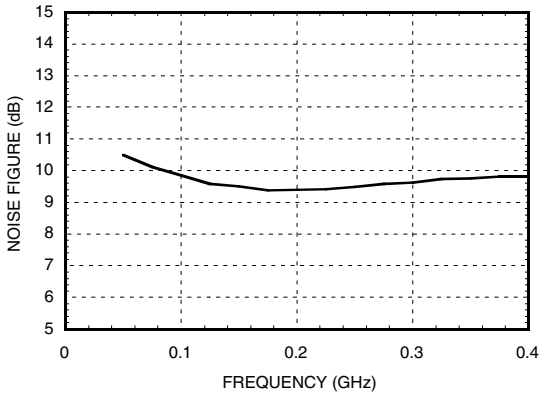


** Two-tone input power= -5 dBm each tone, 1 MHz spacing.*

Noise Figure vs. Temperature, Swept LO, Fixed IF = 250 MHz



Noise Figure Swept IF, Fixed LO = 2 GHz



MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	XX	42	55	47	52
1	65	0	66	80	89
2	>108	103	50	99	106
3	>108	>108	>108	80	>108
4	>108	>108	>108	>108	>108

RF = 2.05 GHz @ -10 dBm
LO = 1.8 GHz @ +10 dBm
All values in dBc relative to the IF power level.

Harmonics of LO

	nLO Spur @ RF Port			
LO Freq. (GHz)	1	2	3	4
1.4	27	16	33	33
1.6	30	19	33	42
1.8	32	19	29	35
2	33	19	30	49
2.2	33	20	34	45
2.4	28	20	34	42

LO = +10 dBm
All values in dBc below input LO level @ RF port.

HMC421QS16

PCS/UMTS HIGH IP3 RFIC DOWNCONVERTER, 1.4 - 2.3 GHz

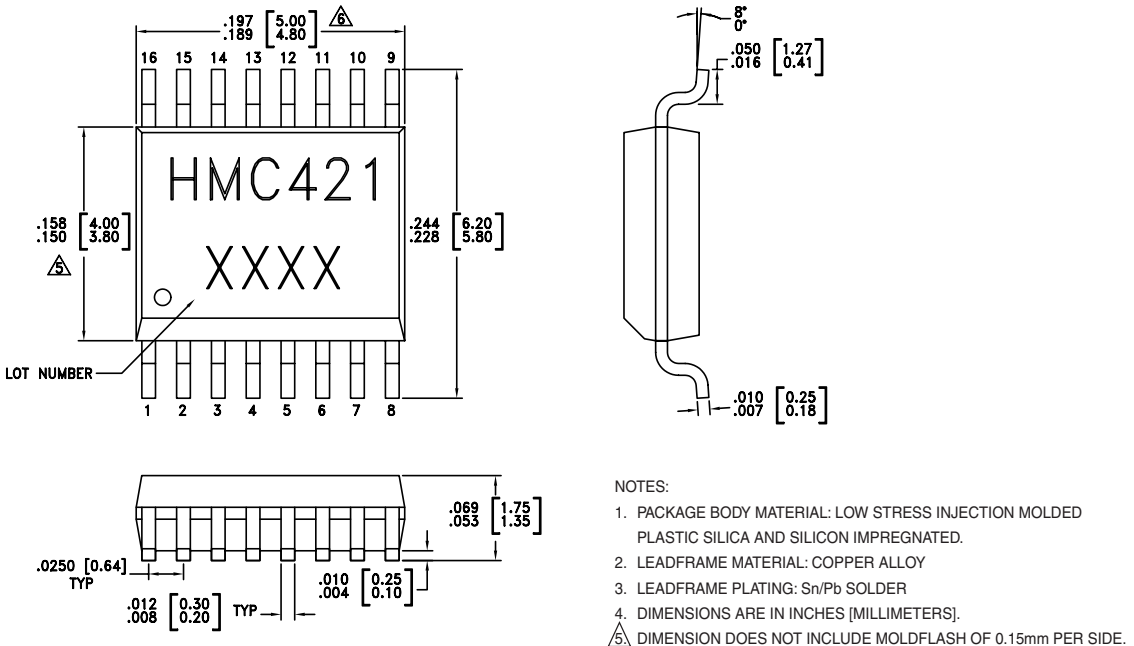
Absolute Maximum Ratings

RF / IF Input (Vdd= +5V)	+13 dBm
LO Drive (Vdd= +5V)	+15 dBm
Vdd (LO or IF)	+7 Vdc
Channel Temperature	150°C
Continuous Pdiss (T = 85°C) (Derate 6.34 mW/°C above 85 C)	0.41 W
Storage Temperature	-65 to +150°C
Operating Temperature	-40 to +85°C

Typical Supply Current vs. Vdd

Vdd (LO + IF) (Vdc)	(Idd) mA
4.5	61
5.0	62
5.5	63

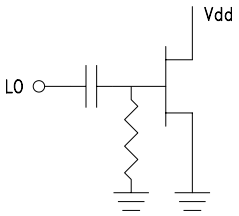
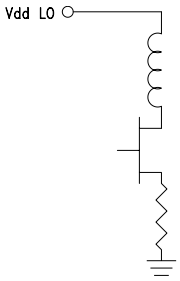
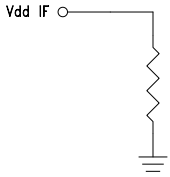
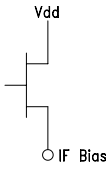
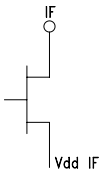
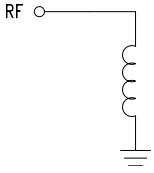
Outline Drawing



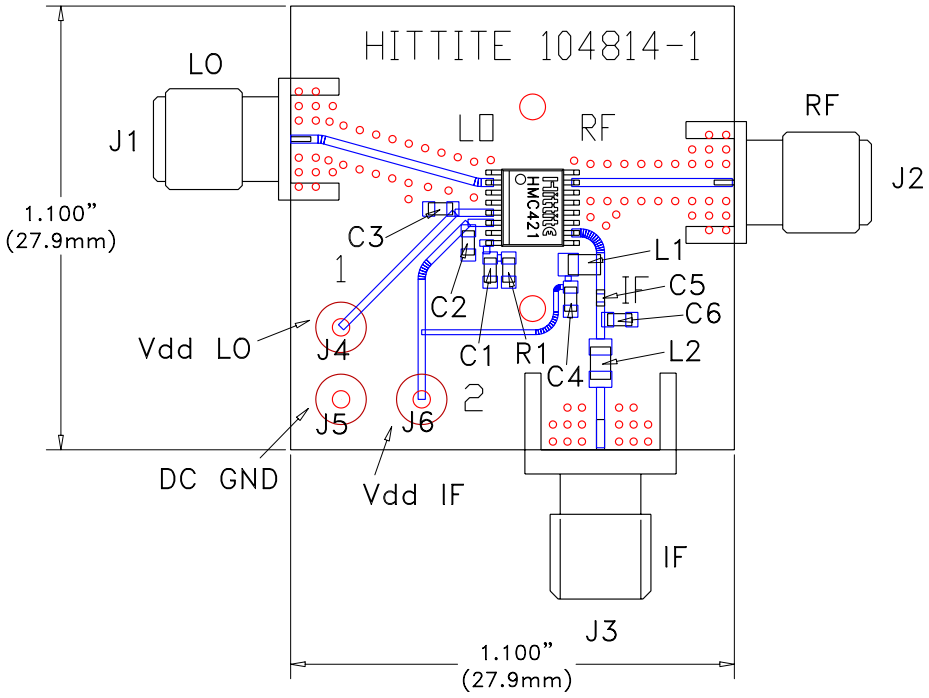
NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEADFRAME MATERIAL: COPPER ALLOY
3. LEADFRAME PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
6. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
7. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 7, 9, 14, 16	N/C	Not Connected	
2	LO Port	This pin is AC coupled and matched to 50 Ohm from 1.3 - 2.5 GHz.	
3, 4, 11, 12, 13	GND	Pin must connect to RF ground.	
5	Vdd LO	Power supply for the LO amplifier. One external RF bypass capacitor (10,000 pF) is required.	
6	Vdd IF	Bias voltage for IF amplifier. One external RF bypass capacitor (10,000 pF) is required.	
8	IF Bias	DC bias setting for IF amplifier.	
10	IF Port	Output of IF and bias port for amplifier. A pull up inductor (L1), output matching network (C5, C6, L2), and 10,000 pF bypass capacitor (C4) are required.	
15	RF Port	This pin is DC coupled and matched to 50 Ohm from 1.7 - 2.5 GHz.	

Evaluation PCB



List of Material

Item	Description
J1 - J3	PC Mount SMA RF Connector
J4 - J6	DC Pins
C1	1000 pF Chip Capacitor, 0603 Pkg.
C2, C3, C4	0.01 µF Chip Capacitor, 0603 Pkg.
C5	82 pF Chip Capacitor, 0402 Pkg.
C6	6 pF Chip Capacitor, 0603 Pkg.
L1	150 nH Chip Inductor, 0805 Pkg.
L2	27 nH Chip Inductor, 0805
R1	6.8 Ohm Resistor, 0603
U1	HMC421QS16 Mixer
PCB*	104814 Evaluation Board, 1.100" x 1.100"
* Circuit Board Material: Rogers 4350	

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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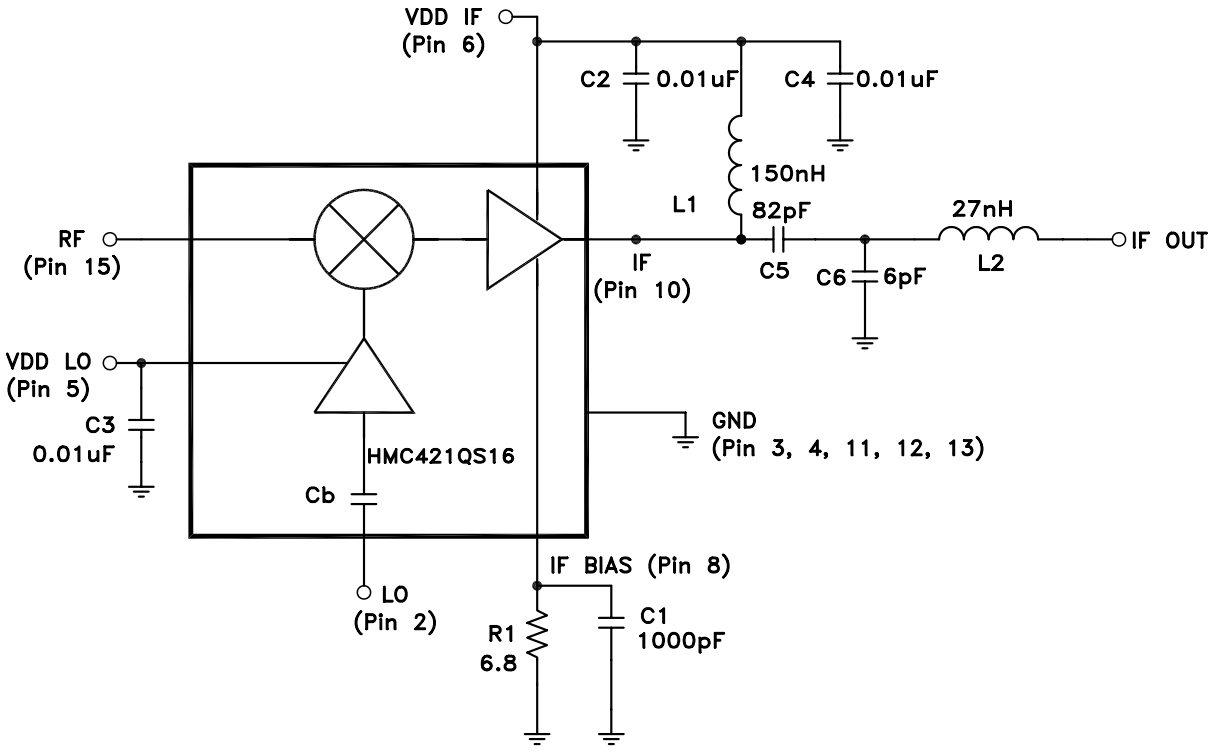
Application Circuit



Notes:

1. *Pin 5 and Pin 6 may be connected to a common Vdd supply.*
2. *Select C6 & L2 to optimize IF frequency. Values for IF = 250 MHz are shown.*