

SN55LVDS31, SN65LVDS31, SN65LVDS3487, SN65LVDS9638 HIGH-SPEED DIFFERENTIAL LINE DRIVERS

SLLS261K – JULY 1997 – REVISED MARCH 2004

- Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and 100-Ω Load
- Typical Output Voltage Rise and Fall Times of 500 ps (400 Mbps)
- Typical Propagation Delay Times of 1.7 ns
- Operate From a Single 3.3-V Supply
- Power Dissipation 25 mW Typical Per Driver at 200 MHz
- Driver at High Impedance When Disabled or With $V_{CC} = 0$
- Bus-Terminal ESD Protection Exceeds 8 kV
- Low-Voltage TTL (LVTTTL) Logic Input Levels
- Pin Compatible With AM26LS31, MC3487, and μ A9638

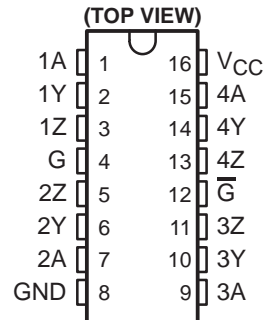
description

The SN55LVDS31, SN65LVDS31, SN65LVDS3487, and SN65LVDS9638 are differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as TIA/EIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers delivers a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

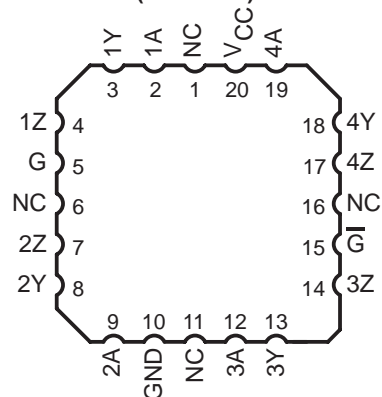
The intended application of these devices and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS31, SN65LVDS3487, and SN65LVDS9638 are characterized for operation from -40°C to 85°C . The SN55LVDS31 is characterized for operation from -55°C to 125°C .

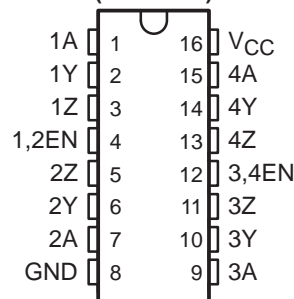
SN55LVDS31 ... J OR W
SN65LVDS31 ... D OR PW
(Marked as LVDS31 or 65LVDS31)



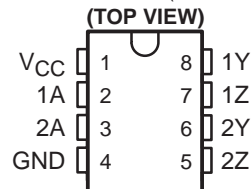
SN55LVDS31FK
(TOP VIEW)



SN65LVDS3487D
(Marked as LVDS3487 or 65LVDS3487)
(TOP VIEW)



SN65LVDS9638D (Marked as DK638 or LVDS38)
SN65LVDS9638DGN (Marked as L38)
SN65LVDS9638DGK (Marked as AXG)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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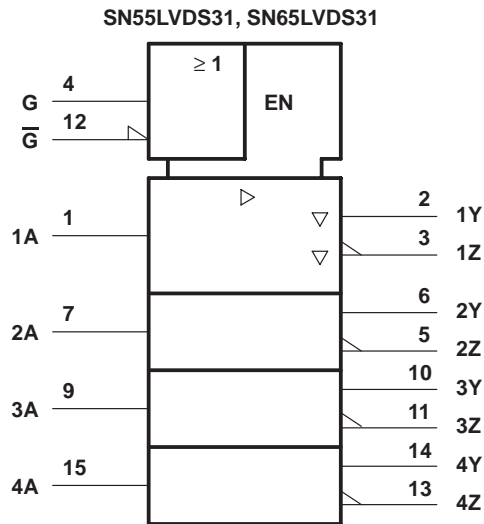
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SN55LVDS31, SN65LVDS31, SN65LVDS3487, SN65LVDS9638
HIGH-SPEED DIFFERENTIAL LINE DRIVERS

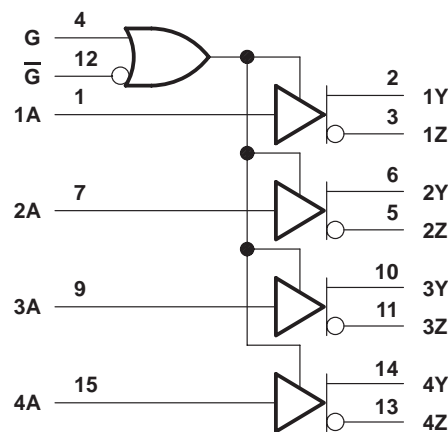
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AVAILABLE OPTIONS						
T _A	PACKAGE					
	SMALL OUTLINE		MSOP	CHIP CARRIER (FK)	CERAMIC DIP (J)	FLAT PACK (W)
	(D)	(PW)				
–40°C to 85°C	SN65LVDS31D	SN65LVDS31PW	—	—	—	—
	SN65LVDS3487D	—	—	—	—	—
	SN65LVDS9638D	—	SN65LVDS9638DGN	—	—	—
	—	—	SN65LVDS9638DGK	—	—	—
–55°C to 125°C	—	—	—	SNJ55LVDS31FK	SNJ55LVDS31J	SNJ55LVDS31W SN55LVDS31W

logic symbol†

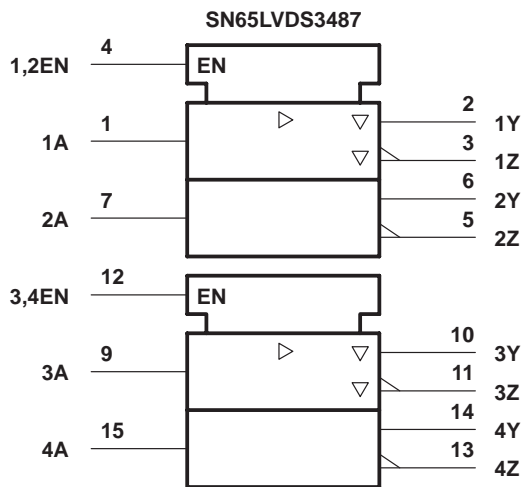


'LVDS31 logic diagram (positive logic)

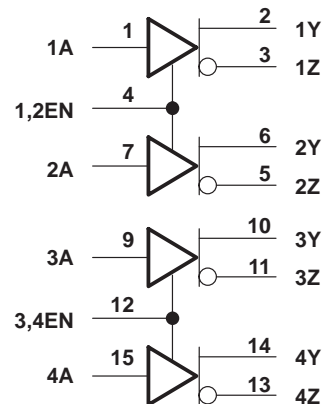


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic symbol†



SN65LVDS3487 logic diagram (positive logic)

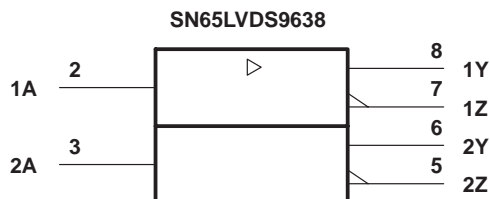


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

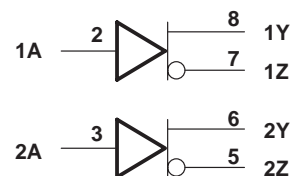
SN55LVDS31, SN65LVDS31, SN65LVDS3487, SN65LVDS9638 HIGH-SPEED DIFFERENTIAL LINE DRIVERS

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logic symbol†



SN65LVDS9638 logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Function Tables

SN55LVDS31, SN65LVDS31

INPUT A	ENABLES		OUTPUTS	
	G	G	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

SN65LVDS3487

INPUT A	ENABLE EN	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

SN65LVDS9638

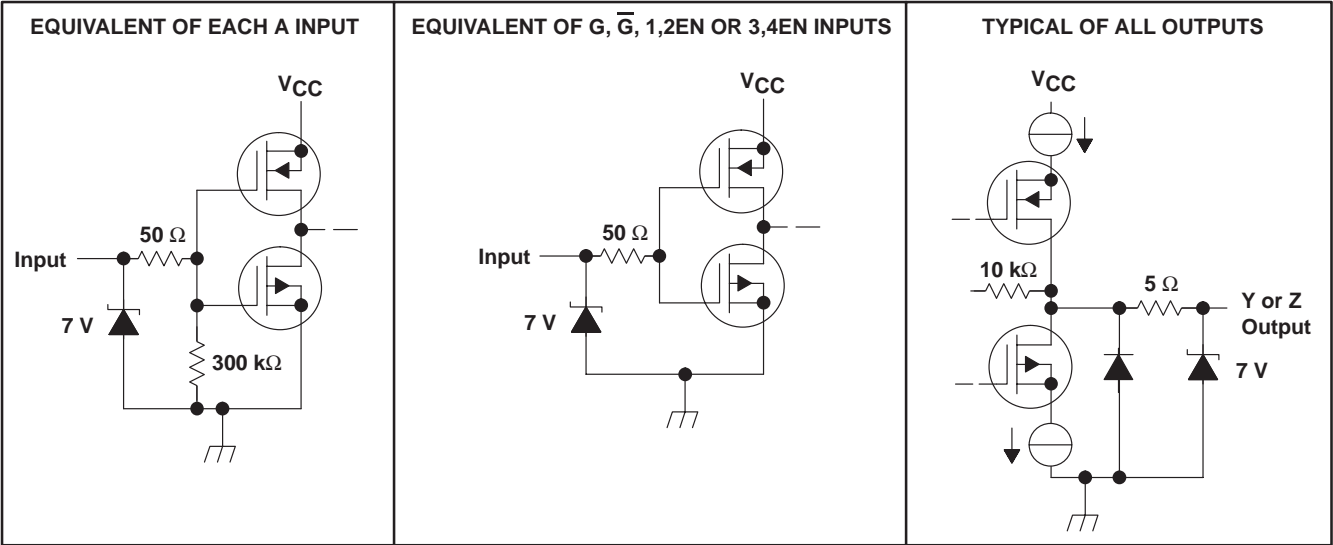
INPUT A	OUTPUTS	
	Y	Z
H	H	L
L	L	H
Open	L	H

H = high level, L = low level

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equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	-0.5 V to 4 V
Input voltage range, V_I	-0.5 V to $V_{CC} + 0.5$ V
Continuous total power dissipation	See Dissipation Rating Table
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [‡] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW	377 mW	—
D (16)	950 mW	7.6 mW/°C	608 mW	494 mW	—
DGK	425 mW	3.4 mW/°C	272 mW	221 mW	—
DGN [§]	2.14 W	17.1 mW/°C	1.37 W	1.11 W	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
PW (16)	774 mW	6.2 mW/°C	496 mW	402 mW	—
W	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

[‡] This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

[§] The PowerPAD[™] must be soldered to a thermal land on the printed-circuit board. See the application note *PowerPAD Thermally Enhanced Package* (SLMA002)

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	SN65 prefix	-40	85	°C
	SN55 prefix	-55	125	



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SN55LVDS31 electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OD} Differential output voltage magnitude	R _L = 100 Ω, See Figure 2	247	340	454	mV
ΔV _{OD} Change in differential output voltage magnitude between logic states	R _L = 100 Ω, See Figure 2	–50		50	mV
V _{OC(SS)} Steady-state common-mode output voltage	See Figure 3	1.125	1.2	1.375	V
ΔV _{OC(SS)} Change in steady-state common-mode output voltage between logic states	See Figure 3	–50		50	mV
V _{OC(PP)} Peak-to-peak common-mode output voltage	See Figure 3		50	150	mV
I _{CC} Supply current	V _I = 0.8 V or 2 V, Enabled, No load		9	20	mA
	V _I = 0.8 or 2 V, Enabled, R _L = 100 Ω		25	35	
	V _I = 0 or V _{CC} , Disabled		0.25	1	
I _{IH} High-level input current	V _{IH} = 2		4	20	μA
I _{IL} Low-level input current	V _{IL} = 0.8 V		0.1	10	μA
I _{OS} Short-circuit output current	V _{O(Y)} or V _{O(Z)} = 0		–4	–24	mA
	V _{OD} = 0			±12	
I _{OZ} High-impedance output current	V _O = 0 or 2.4 V			±1	μA
I _{O(OFF)} Power-off output current	V _{CC} = 0, V _O = 2.4 V			±4	μA
C _i Input capacitance			3		pF

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

SN55LVDS31 switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high-level output	R _L = 100 Ω, C _L = 10 pF, See Figure 2	0.5	1.4	4	ns
t _{PHL} Propagation delay time, high-to-low-level output		1	1.7	4.5	ns
t _r Differential output signal rise time (20% to 80%)		0.4	0.5	1	ns
t _f Differential output signal fall time (80% to 20%)		0.4	0.5	1	ns
t _{sk(p)} Pulse skew (t _{PHL} – t _{PLH})			0.3	0.6	ns
t _{sk(o)} Channel-to-channel output skew‡			0.3	0.6	ns
t _{PZH} Propagation delay time, high-impedance-to-high-level output	See Figure 4		5.4	15	ns
t _{PZL} Propagation delay time, high-impedance-to-low-level output			2.5	15	ns
t _{PHZ} Propagation delay time, high-level-to-high-impedance output			8.1	17	ns
t _{PLZ} Propagation delay time, low-level-to-high-impedance output			7.3	15	ns

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

‡ t_{sk(o)} is the maximum delay time difference between drivers on the same device.



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SN65LVDSxxxx electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN65LVDS31 SN65LVDS3487 SN65LVDS9638			UNIT
				MIN	TYP†	MAX	
V _{OD}	Differential output voltage magnitude	R _L = 100 Ω, See Figure 2		247	340	454	mV
ΔV _{OD}	Change in differential output voltage magnitude between logic states	R _L = 100 Ω, See Figure 2		–50		50	mV
V _{OC(SS)}	Steady-state common-mode output voltage	See Figure 3		1.125	1.2	1.375	V
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states	See Figure 3		–50		50	mV
V _{OC(PP)}	Peak-to-peak common-mode output voltage	See Figure 3			50	150	mV
I _{CC}	Supply current	SN65LVDS31, SN65LVDS3487	V _I = 0.8 V or 2 V, Enabled, No load		9	20	mA
			V _I = 0.8 or 2 V, R _L = 100 Ω, Enabled		25	35	
			V _I = 0 or V _{CC} , Disabled		0.25	1	
		SN65LVDS9638	V _I = 0.8 V or 2 V	No load	4.7	8	
				R _L = 100 Ω	9	13	
I _{IH}	High-level input current	V _{IH} = 2			4	20	μA
I _{IL}	Low-level input current	V _{IL} = 0.8 V			0.1	10	μA
I _{OS}	Short-circuit output current	V _{O(Y)} or V _{O(Z)} = 0			–4	–24	mA
		V _{OD} = 0				±12	
I _{OZ}	High-impedance output current	V _O = 0 or 2.4 V				±1	μA
I _{O(OFF)}	Power-off output current	V _{CC} = 0, V _O = 2.4 V				±1	μA
C _i	Input capacitance				3		pF

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

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SN65LVDSxxxx switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN65LVDS31 SN65LVDS3487 SN65LVDS9638			UNIT
		MIN	TYP†	MAX	
t _{PLH} Propagation delay time, low-to-high-level output	R _L = 100 Ω, C _L = 10 pF, See Figure 2	0.5	1.4	2	ns
t _{PHL} Propagation delay time, high-to-low-level output		1	1.7	2.5	ns
t _r Differential output signal rise time (20% to 80%)		0.4	0.5	0.6	ns
t _f Differential output signal fall time (80% to 20%)		0.4	0.5	0.6	ns
t _{sk(p)} Pulse skew (t _{PHL} – t _{PLH})			0.3	0.6	ns
t _{sk(o)} Channel-to-channel output skew‡			0	0.3	ns
t _{sk(pp)} Part-to-part skew§				800	ps
t _{PZH} Propagation delay time, high-impedance-to-high-level output	See Figure 4		5.4	15	ns
t _{PZL} Propagation delay time, high-impedance-to-low-level output			2.5	15	ns
t _{PHZ} Propagation delay time, high-level-to-high-impedance output			8.1	15	ns
t _{PLZ} Propagation delay time, low-level-to-high-impedance output			7.3	15	ns

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

‡ t_{sk(o)} is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

§ t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.



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PARAMETER MEASUREMENT INFORMATION

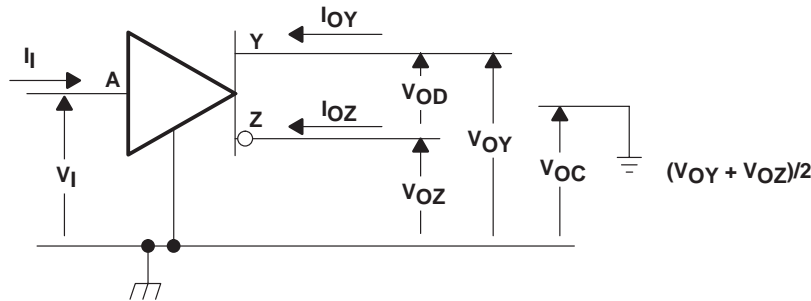
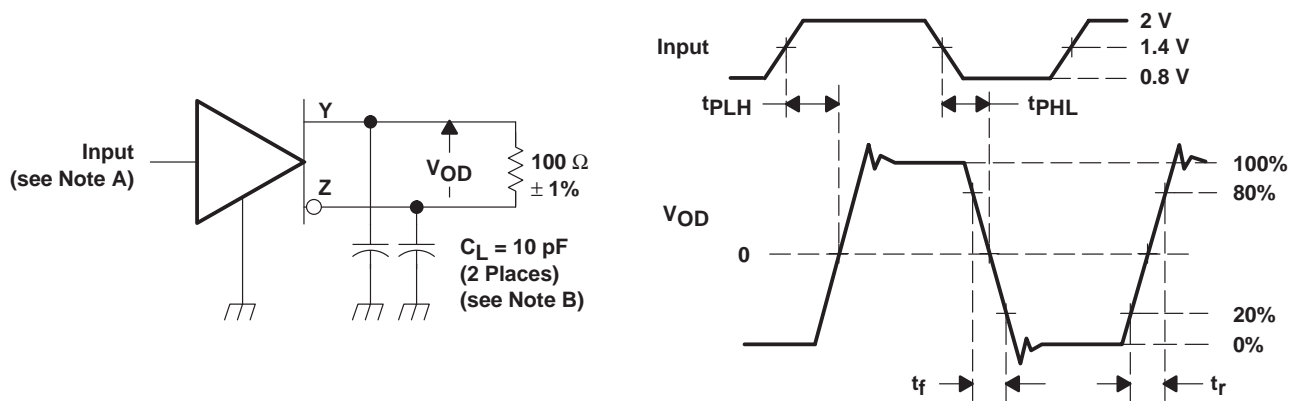
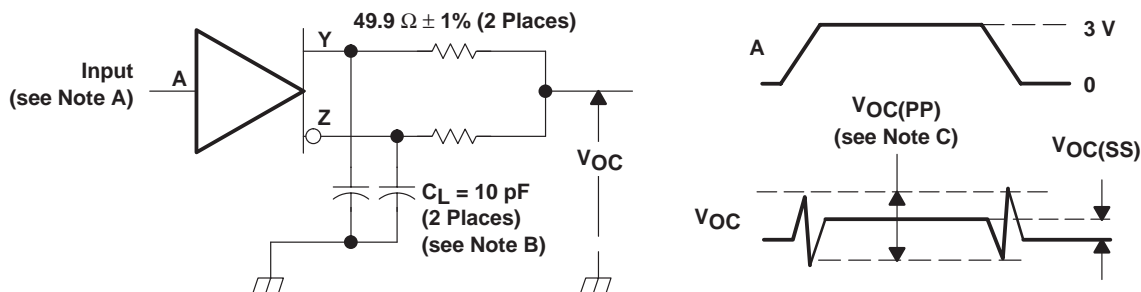


Figure 1. Voltage and Current Definitions



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.
C. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3-dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION

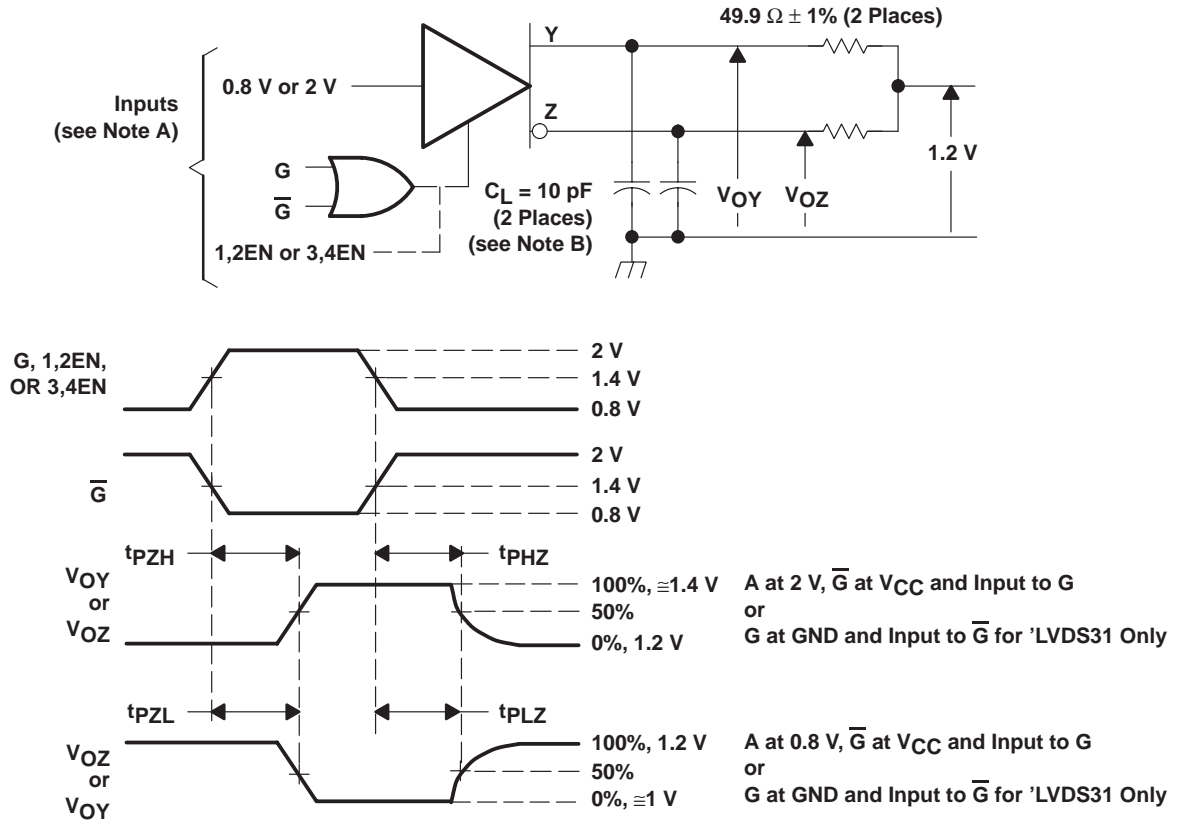


Figure 4. Enable- and Disable-Time Circuit and Definitions

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TYPICAL CHARACTERISTICS

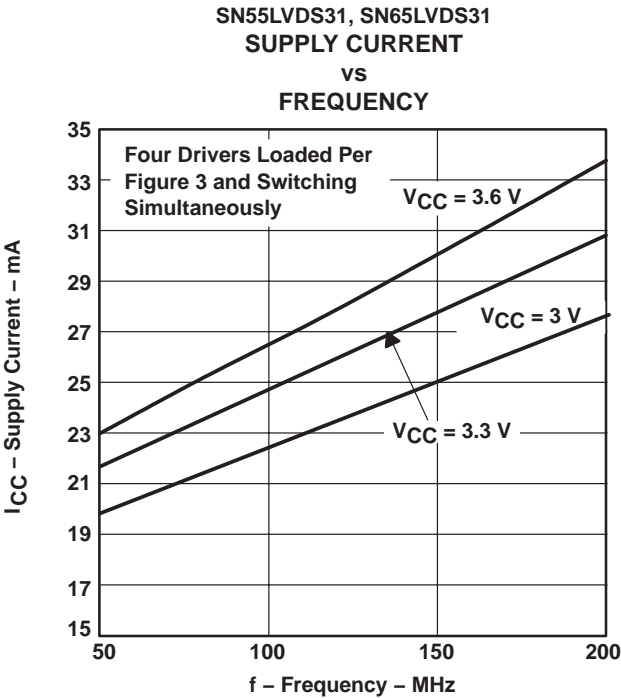


Figure 5

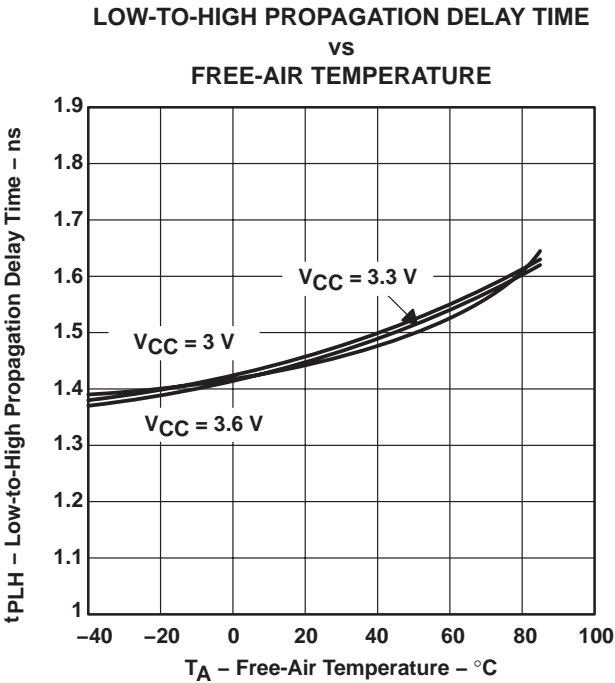


Figure 6

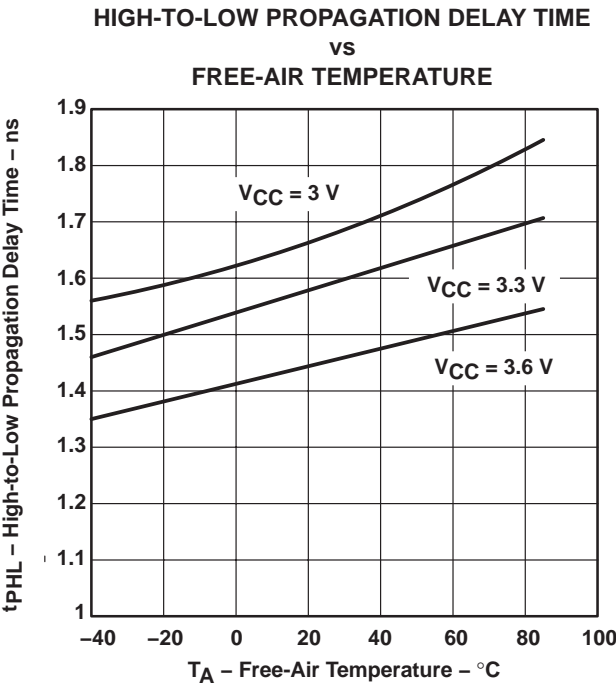
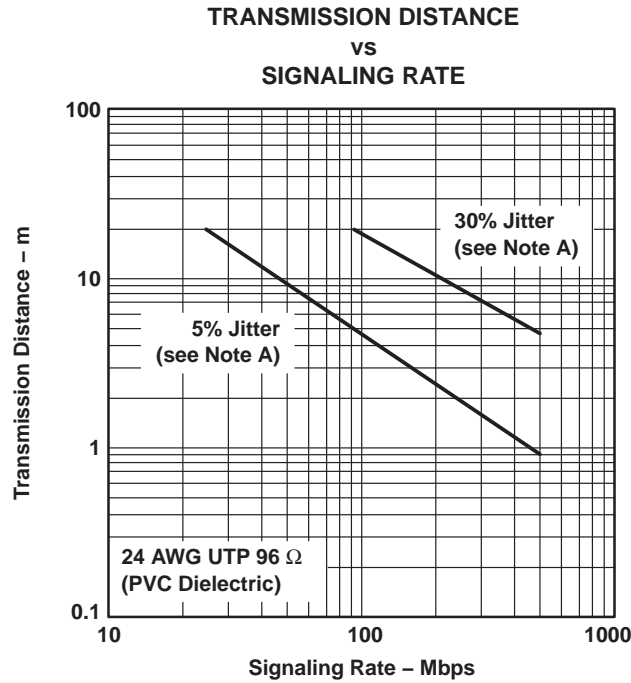


Figure 7

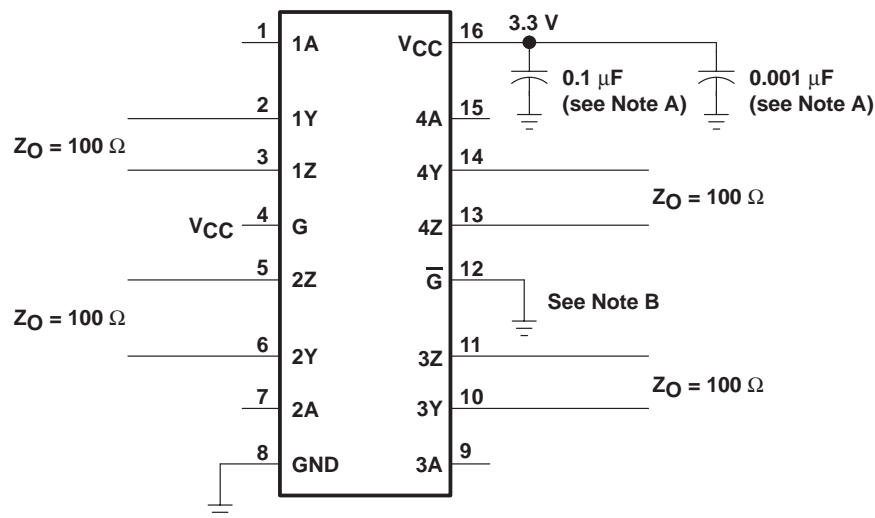
APPLICATION INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission where ground differences are less than 1 V. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual supply requirements.



NOTE A: This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

Figure 8. Typical Transmission Distance Versus Signaling Rate



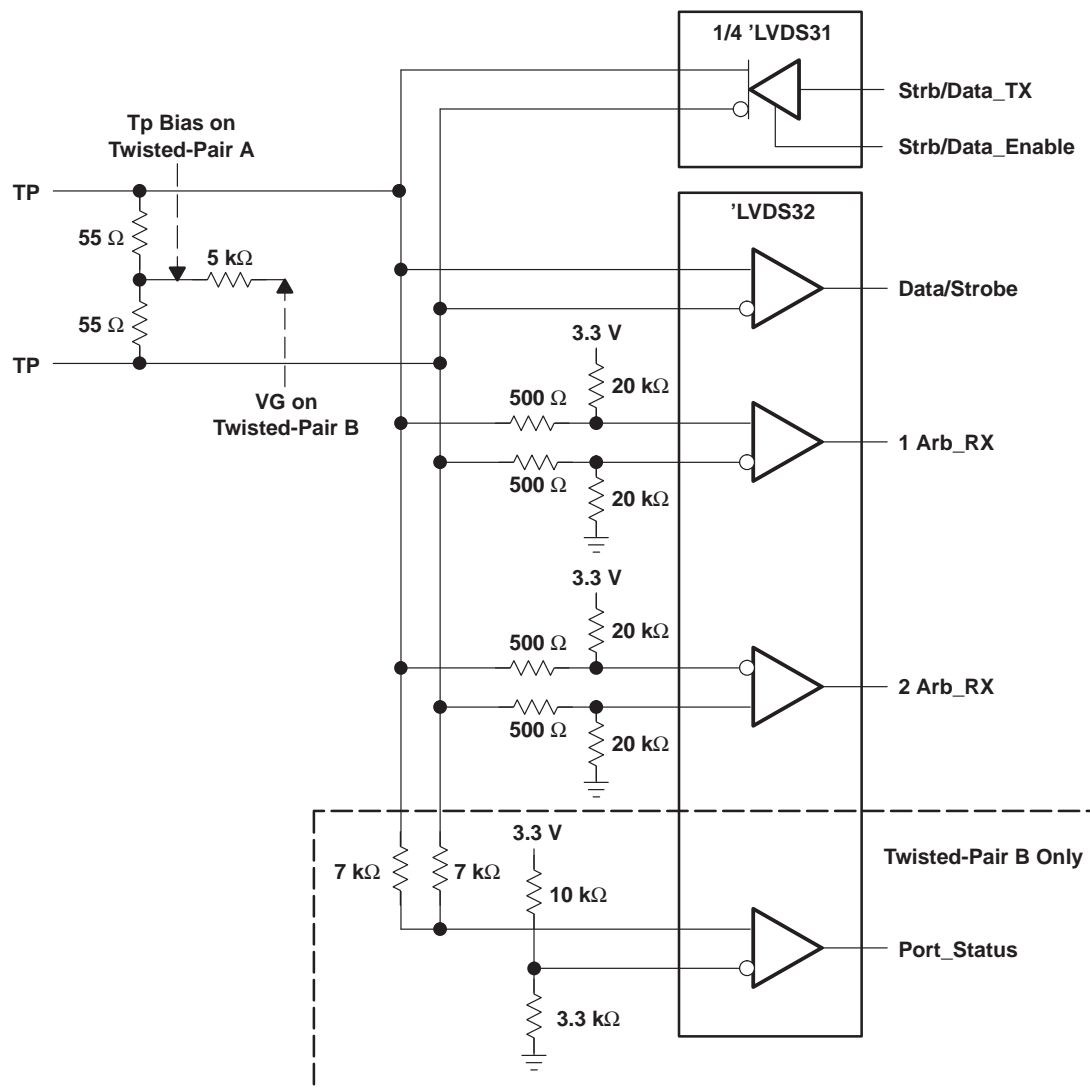
- NOTES: A. Place a 0.1- μ F and a 0.001- μ F Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.
B. Unused enable inputs should be tied to V_{CC} or GND, as appropriate.

Figure 9. Typical Application Circuit Schematic

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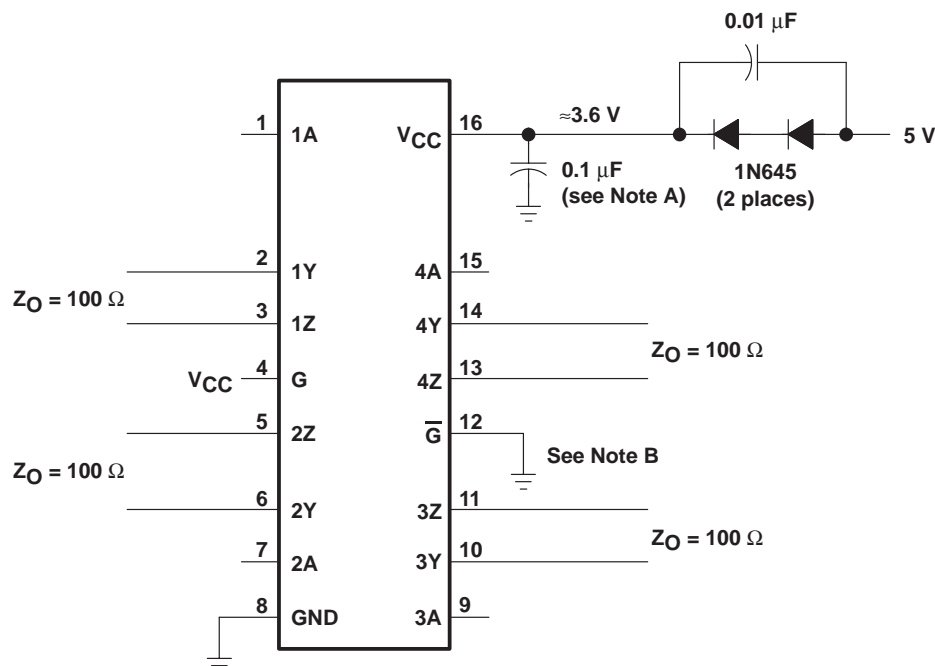
APPLICATION INFORMATION



NOTES: A. Resistors are leadless, thick film (0603), 5% tolerance.
B. Decoupling capacitance is not shown, but recommended.
C. V_{CC} is 3 V to 3.6 V.
D. The differential output voltage of the 'LVDS31 can exceed that specified by IEEE1394.

Figure 10. 100-Mbps IEEE 1394 Transceiver

APPLICATION INFORMATION



NOTES: A. Place a 0.1- μ F Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.
B. Unused enable inputs should be tied to V_{CC} or GND, as appropriate.

Figure 11. Operation With 5-V Supply

related information

IBIS modeling is available for this device. Please contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, please see the following documents:

- *Low-Voltage Differential Signaling Design Notes* (literature number SLLA014)
- *Interface Circuits for TIA/EIA-644 (LVDS)* (literature number SLLA038)
- *Reducing EMI With LVDS* (literature number SLLA030)
- *Slew Rate Control of LVDS Circuits* (literature number SLLA034)
- *Using an LVDS Receiver With TIA/EIA-422 Data* (literature number SLLA031)
- *Low Voltage Differential Signaling (LVDS) EVM* (literature number SLLA033)

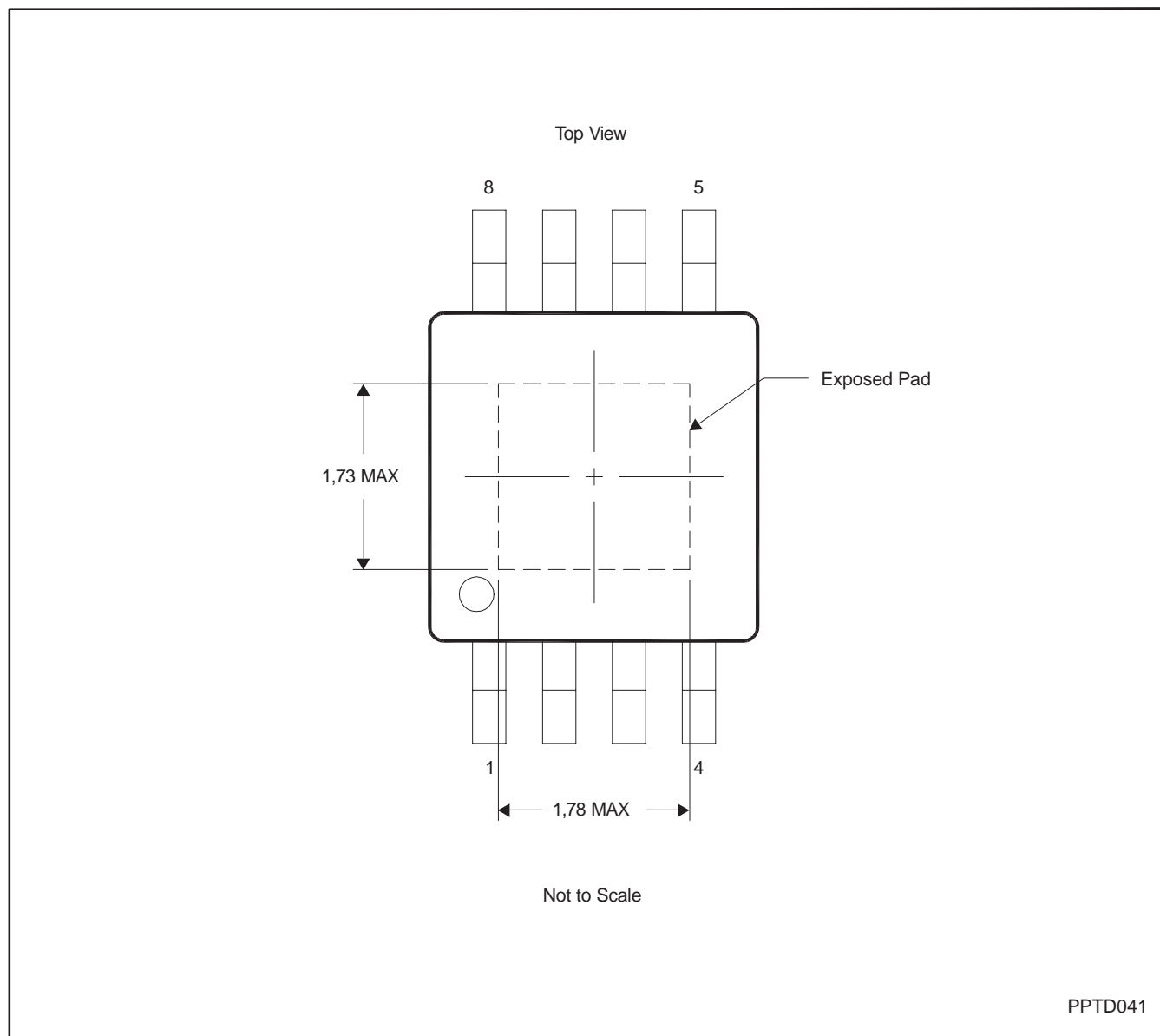
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THERMAL PAD MECHANICAL DATA

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

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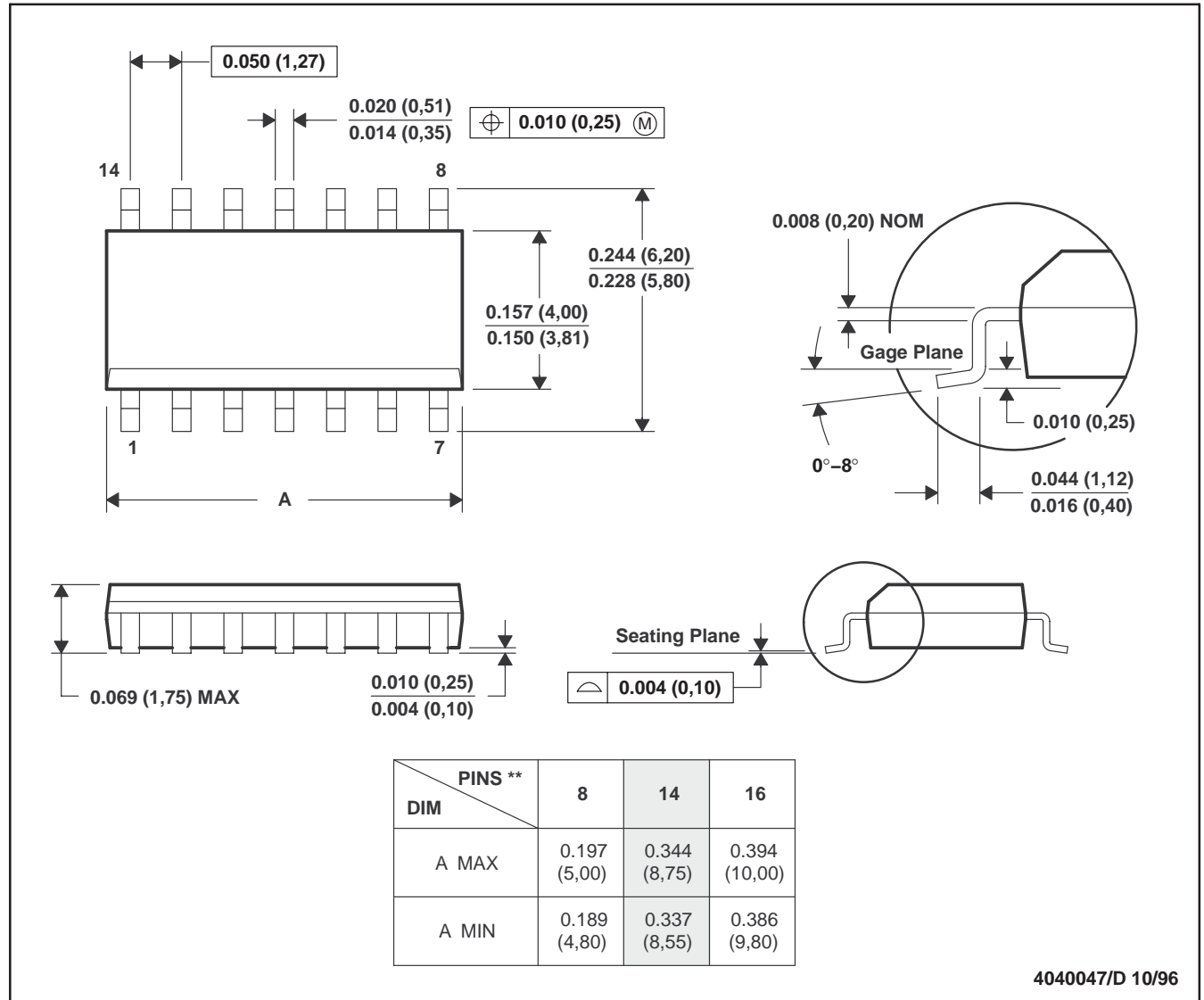
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MECHANICAL INFORMATION

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012

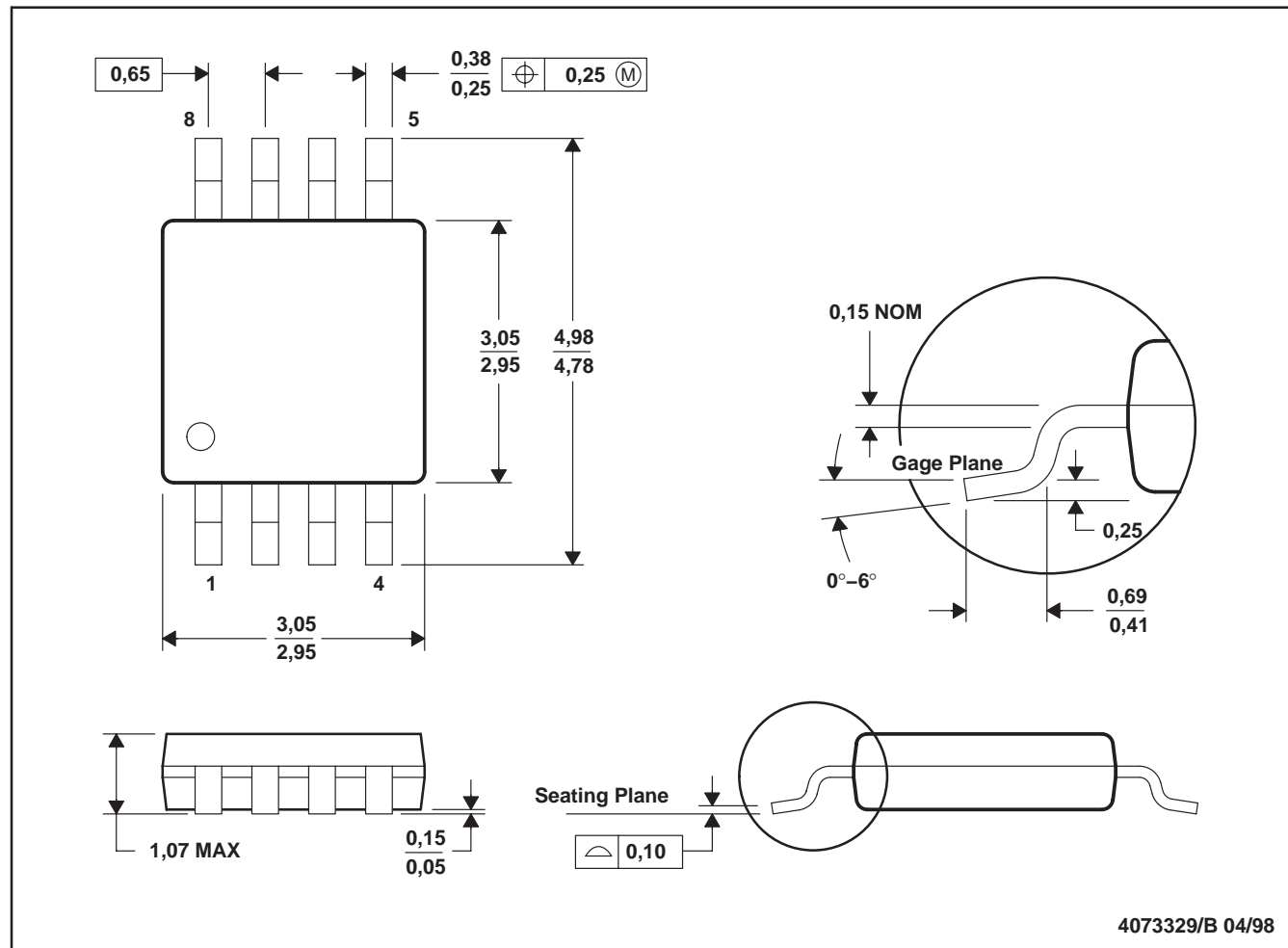
SN55LVDS31, SN65LVDS31, SN65LVDS3487, SN65LVDS9638 HIGH-SPEED DIFFERENTIAL LINE DRIVERS

SLLS261K – JULY 1997 – REVISED MARCH 2004

MECHANICAL INFORMATION

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187

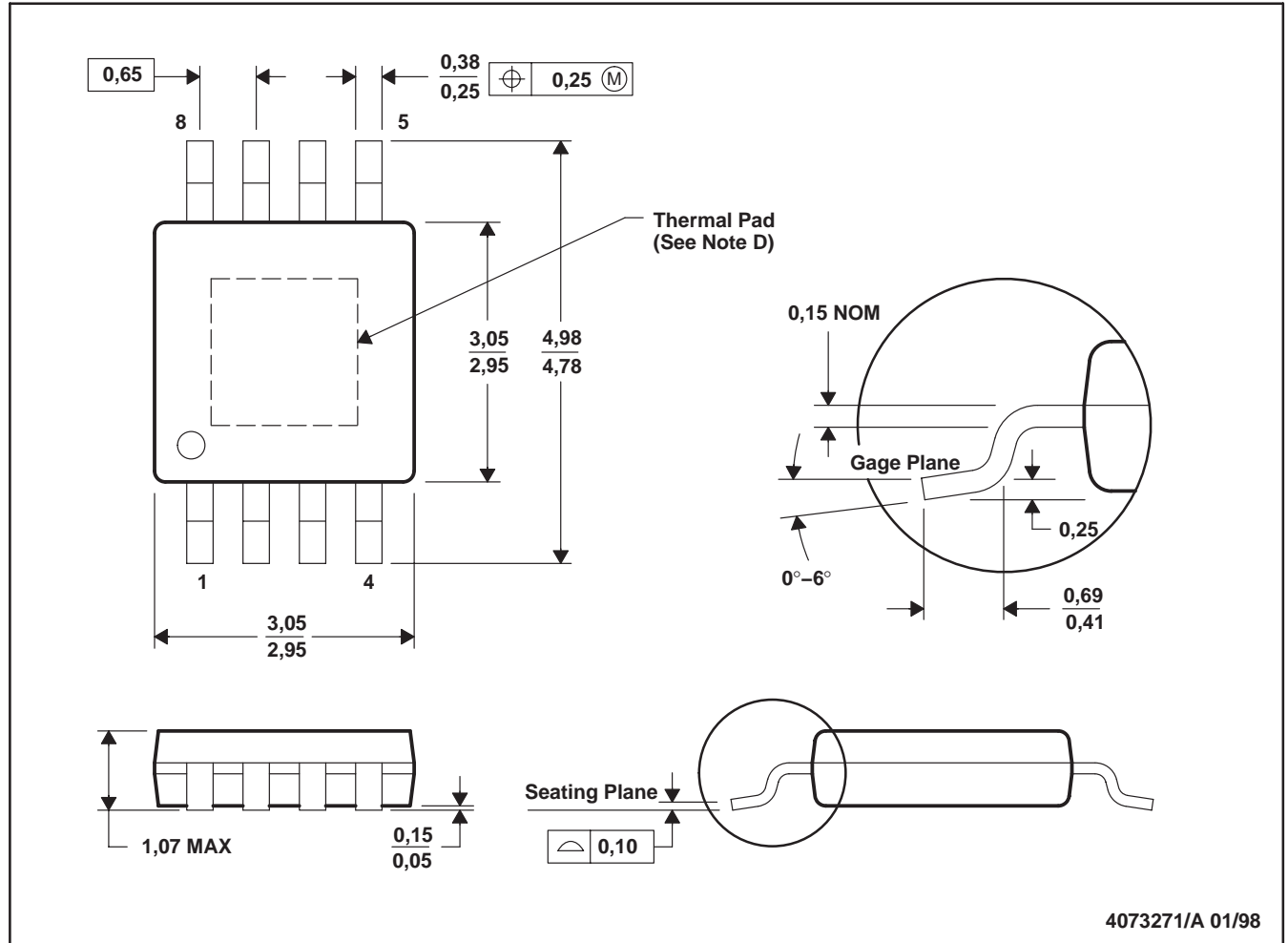
SN55LVDS31, SN65LVDS31, SN65LVDS3487, SN65LVDS9638 HIGH-SPEED DIFFERENTIAL LINE DRIVERS

SLLS261K – JULY 1997 – REVISED MARCH 2004

MECHANICAL INFORMATION

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions include mold flash or protrusions.
 - The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 - Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments.



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SN55LVDS31, SN65LVDS31, SN65LVDS3487, SN65LVDS9638 HIGH-SPEED DIFFERENTIAL LINE DRIVERS

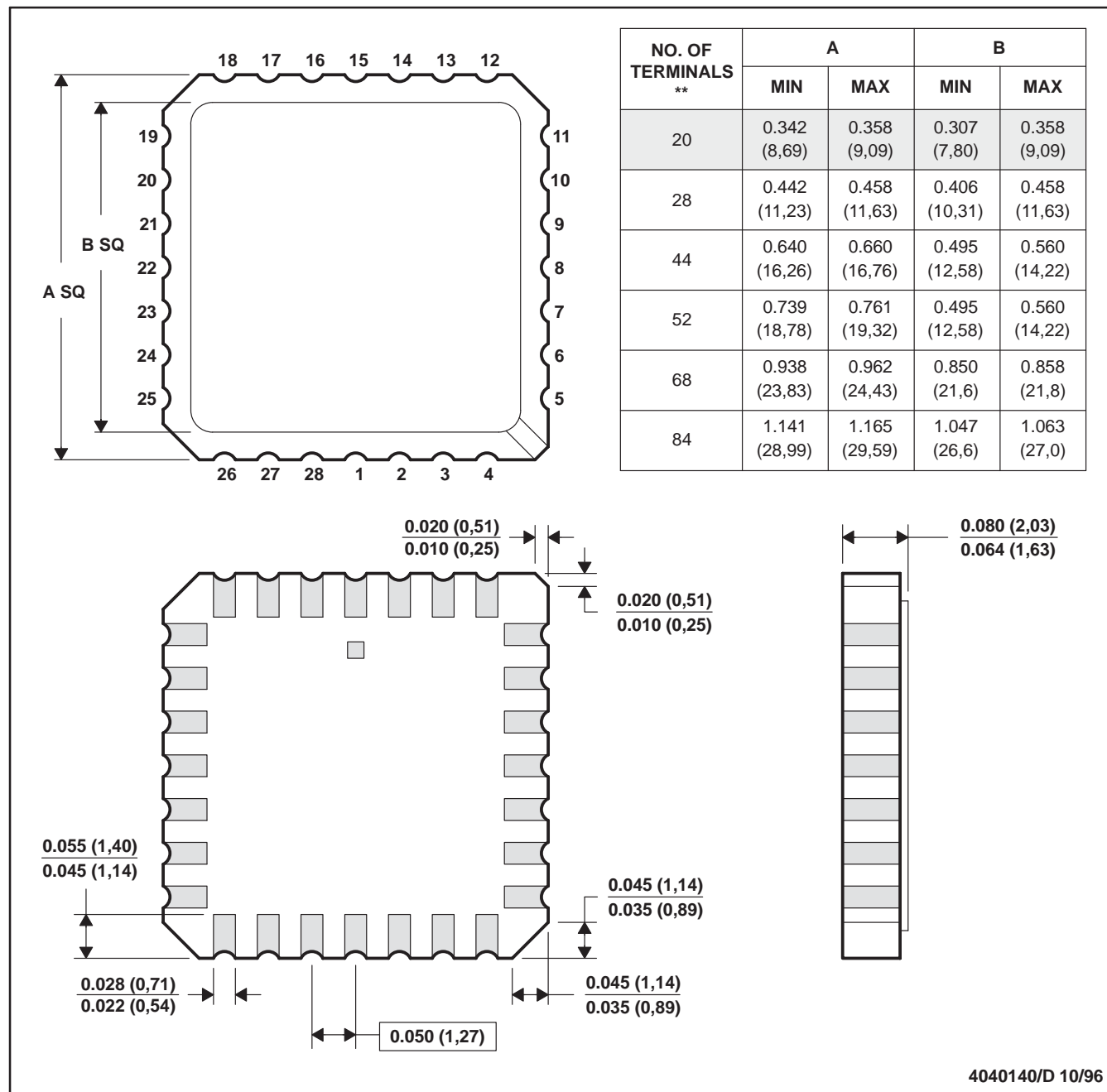
SLLS261K – JULY 1997 – REVISED MARCH 2004

MECHANICAL INFORMATION

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

SN55LVDS31, SN65LVDS31, SN65LVDS3487, SN65LVDS9638 HIGH-SPEED DIFFERENTIAL LINE DRIVERS

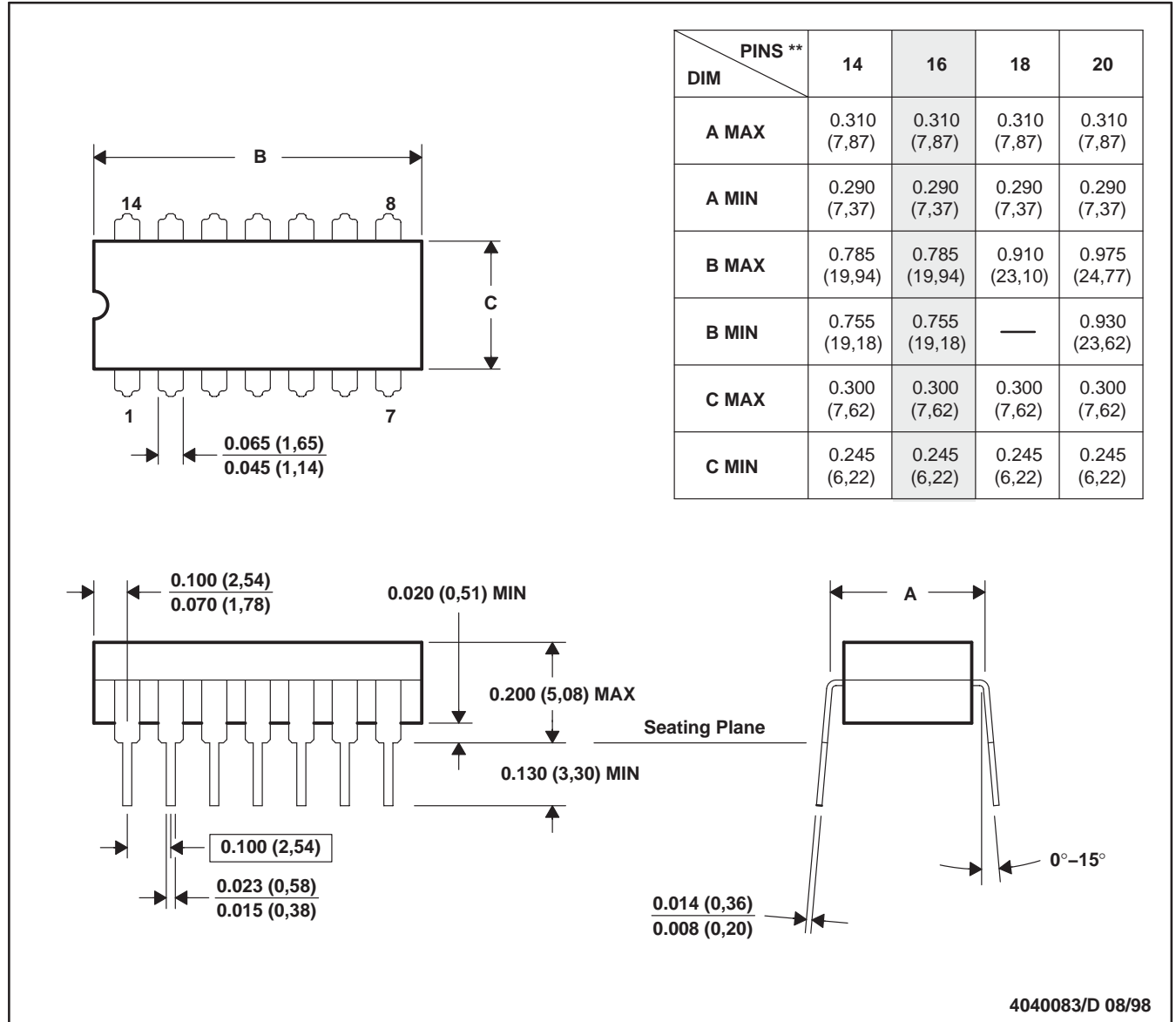
SLLS261K – JULY 1997 – REVISED MARCH 2004

MECHANICAL INFORMATION

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22.

SN55LVDS31, SN65LVDS31, SN65LVDS3487, SN65LVDS9638
HIGH-SPEED DIFFERENTIAL LINE DRIVERS

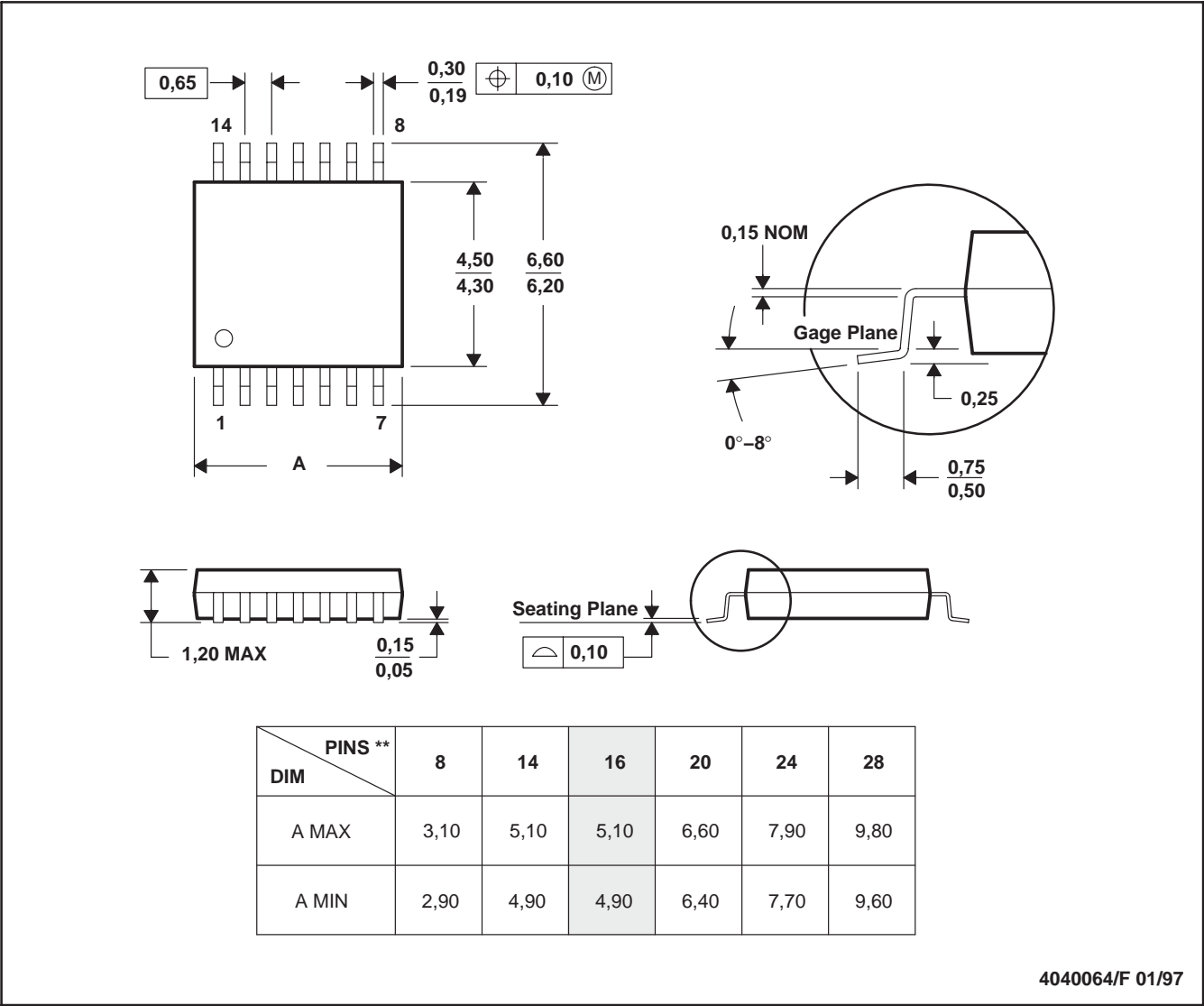
SLLS261K – JULY 1997 – REVISED MARCH 2004

MECHANICAL INFORMATION

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

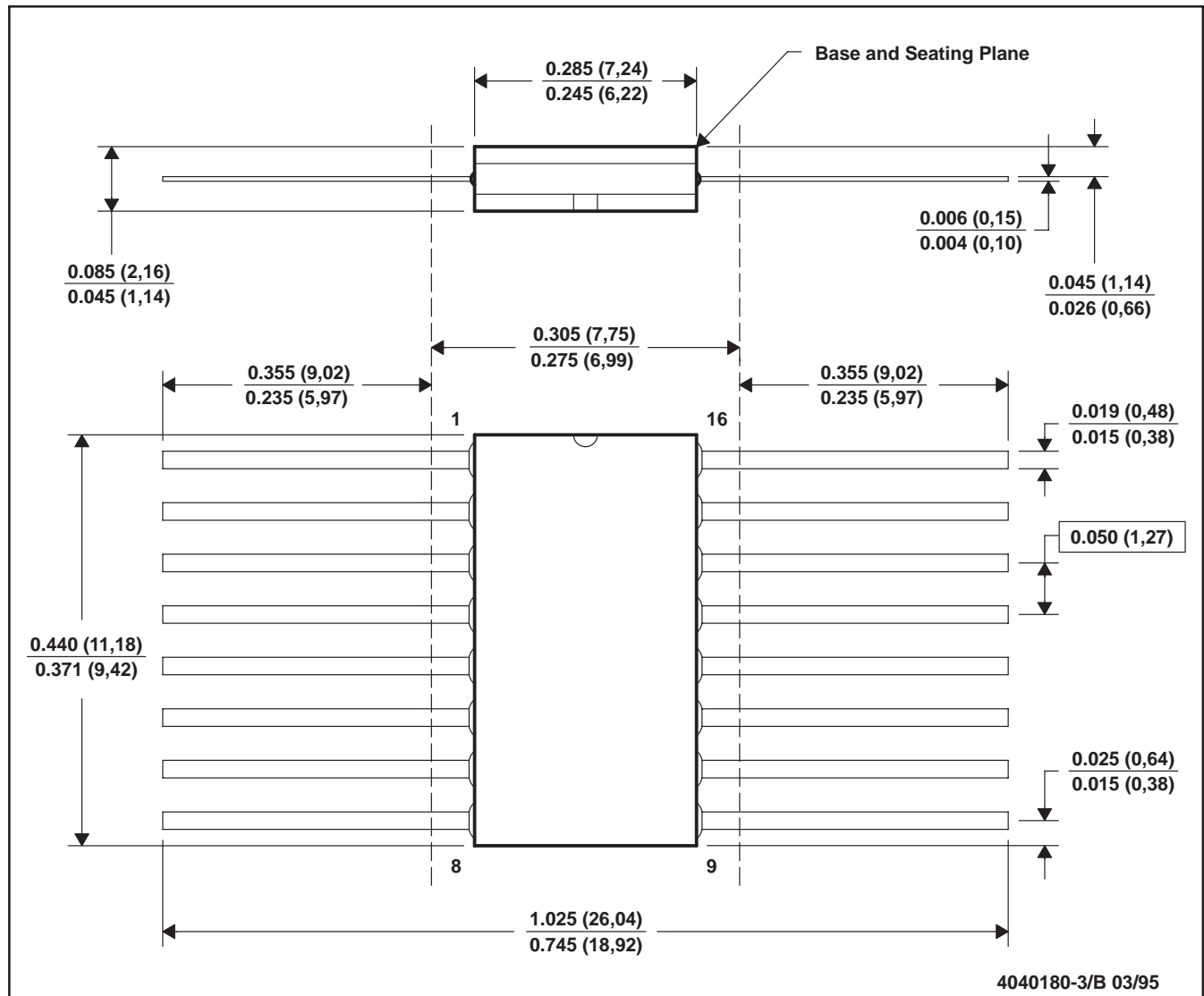
SN55LVDS31, SN65LVDS31, SN65LVDS3487, SN65LVDS9638 HIGH-SPEED DIFFERENTIAL LINE DRIVERS

SLLS261K – JULY 1997 – REVISED MARCH 2004

MECHANICAL INFORMATION

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL-STD-1835 GDFP1-F16 and JEDEC MO-092AC

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9762101Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-9762101QEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-9762101QFA	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-9762101VFA	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	Level-NC-NC-NC
SN55LVDS31W	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	Level-NC-NC-NC
SN65LVDS31D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS31DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS31DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS31NSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS31PW	ACTIVE	TSSOP	PW	16	90	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS31PWR	ACTIVE	TSSOP	PW	16	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS3487D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS3487DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS9638D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS9638DGK	ACTIVE	MSOP	DGK	8	80	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS9638DGKR	ACTIVE	MSOP	DGK	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS9638DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS9638DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS9638DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ55LVDS31FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
SNJ55LVDS31J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
SNJ55LVDS31W	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

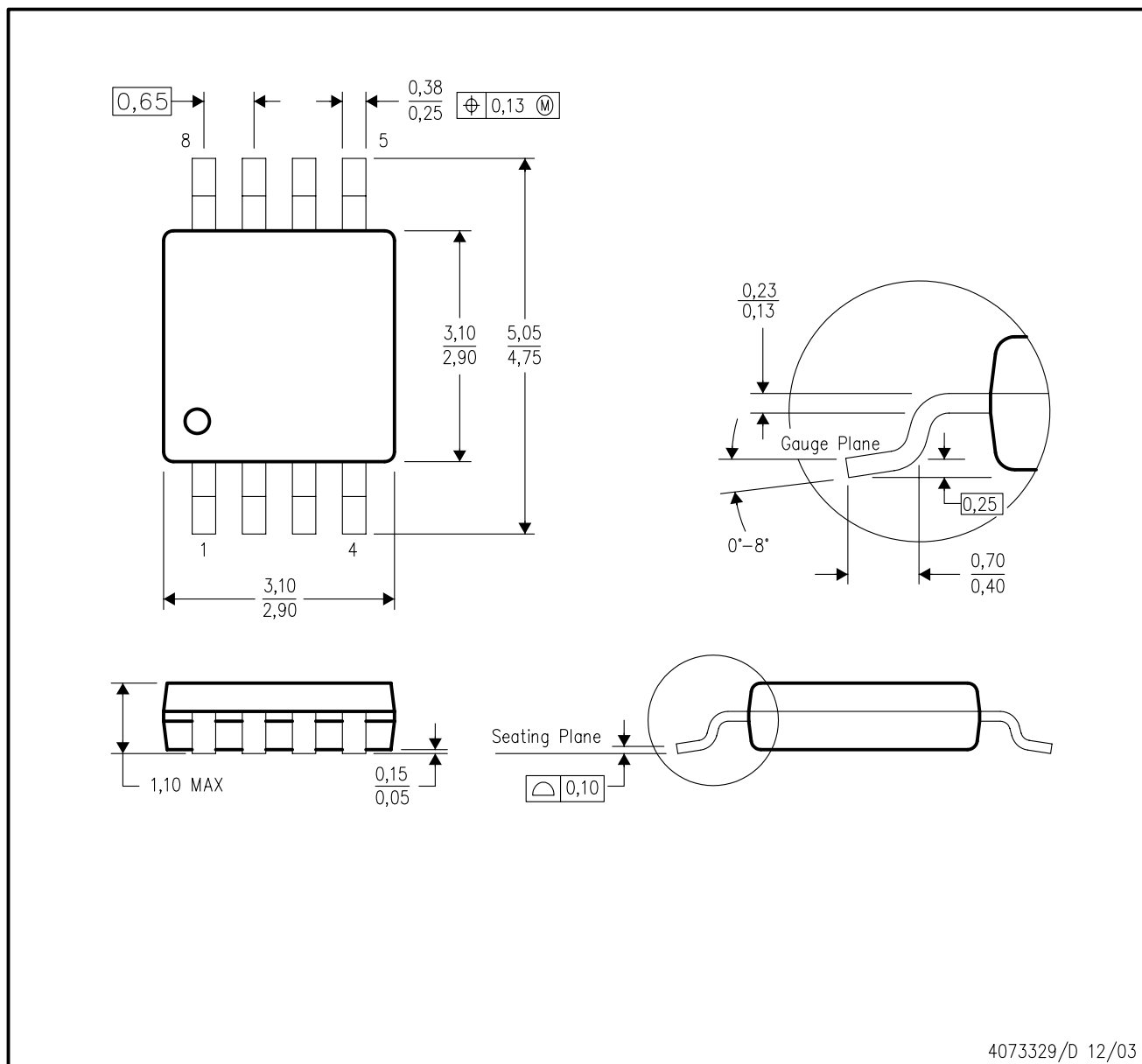
28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

DGK (S-PDSO-G8)

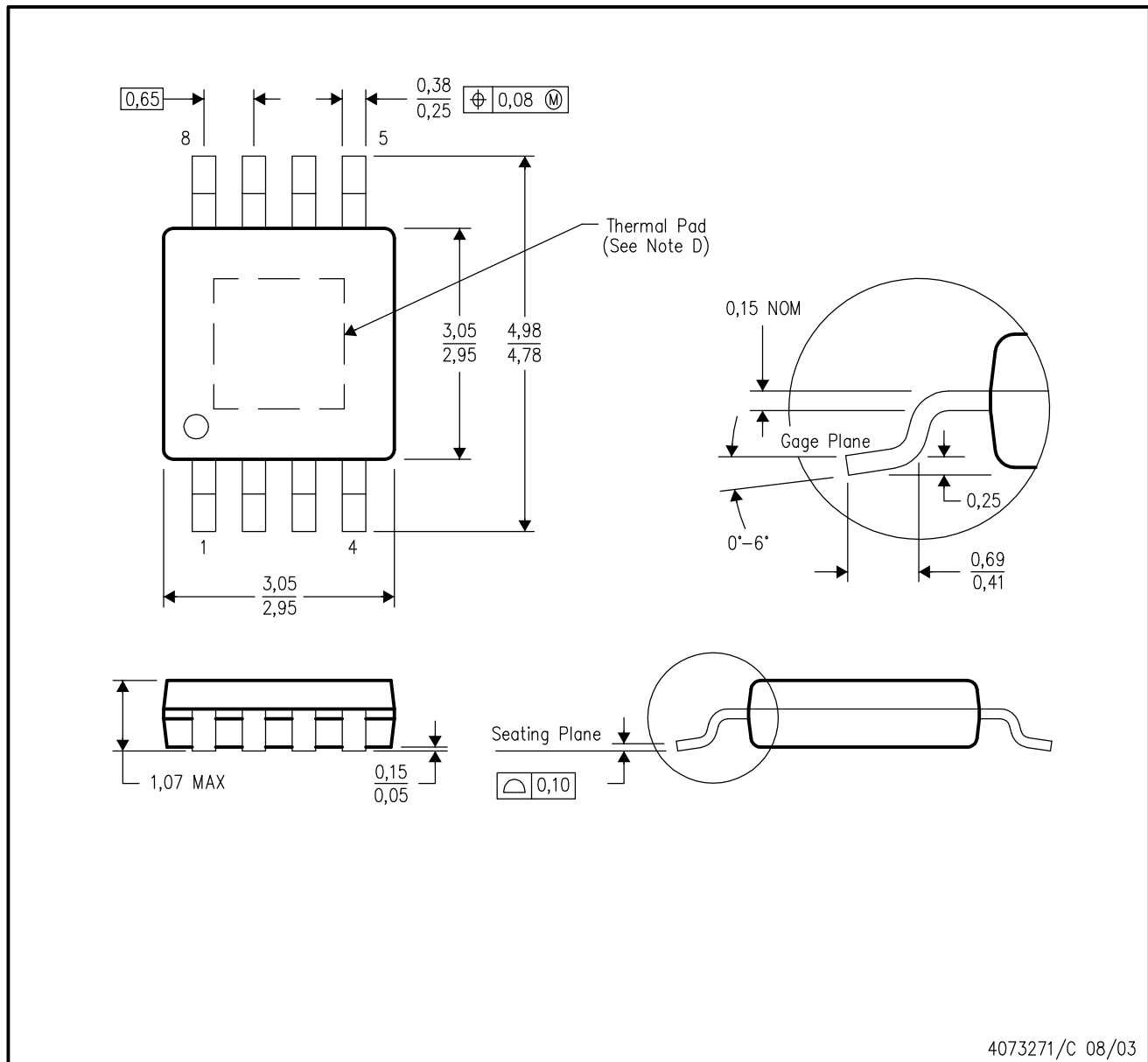
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation AA.

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

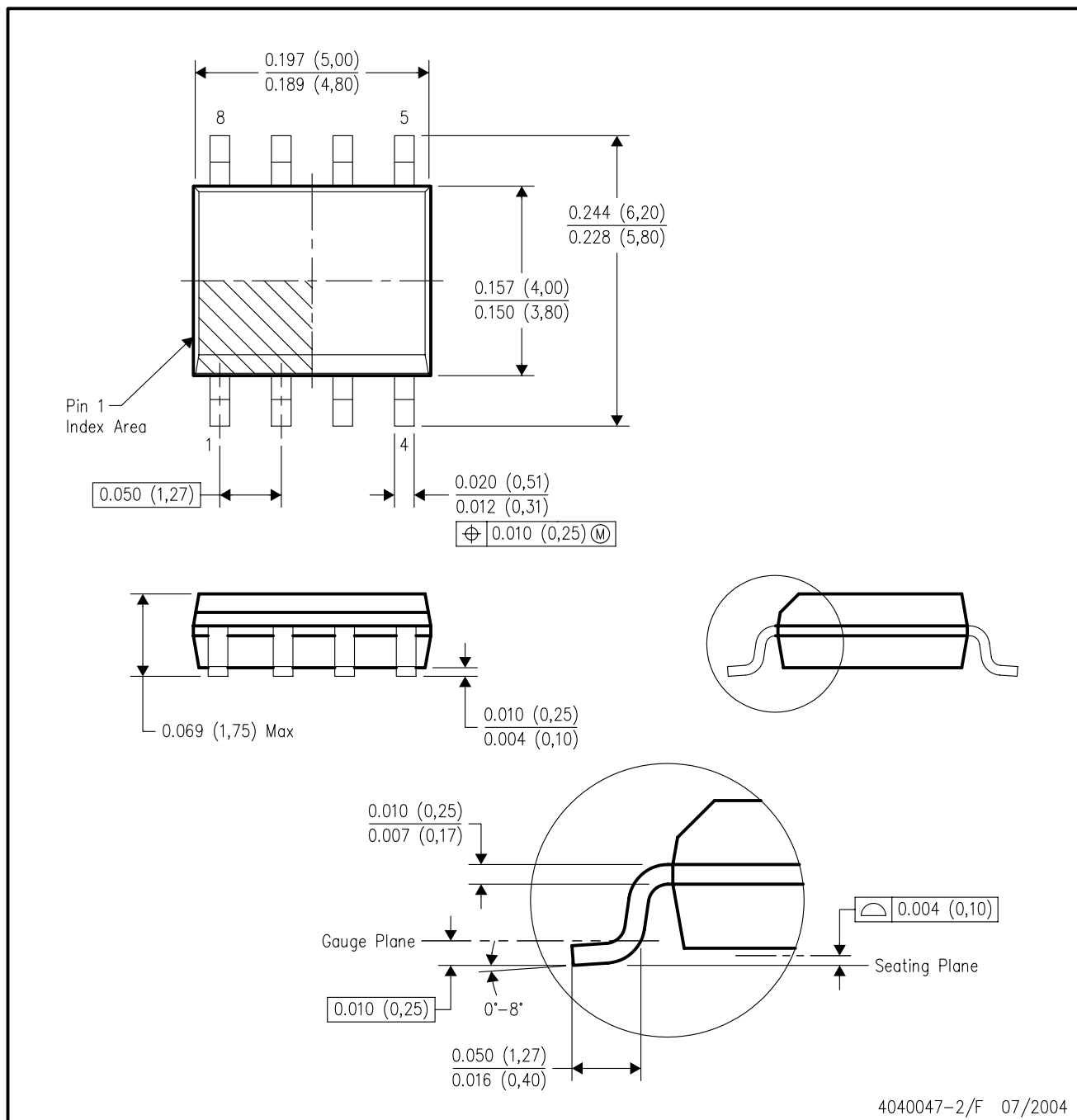


NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AC.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AA.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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