

# PowerMOS transistor

## Isolated version of PHP8N50E

**PHX5N50E****GENERAL DESCRIPTION**

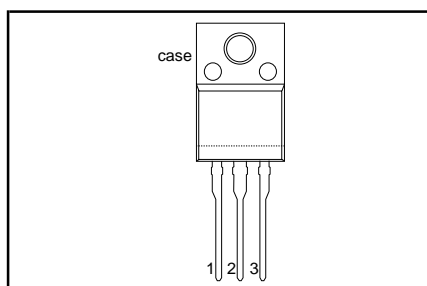
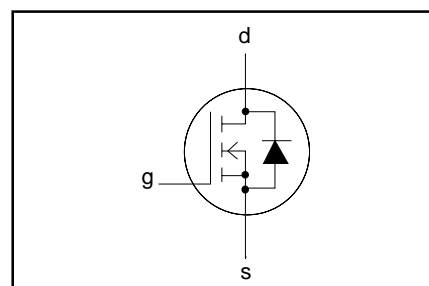
N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Drain-source voltage	500	V
$I_D$	Drain current (DC)	4	A
$P_{tot}$	Total power dissipation	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.8	$\Omega$

**PINNING - SOT186A**

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

**PIN CONFIGURATION****SYMBOL****LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage		-	500	V
$V_{DGR}$	Drain-gate voltage		-	500	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
$I_D$	Drain current (DC)	$R_{GS} = 20 \text{ k}\Omega$	-	4	A
		$T_{hs} = 25^\circ\text{C}$	-	2.5	A
		$T_{hs} = 100^\circ\text{C}$	-	16	A
$I_{DM}$	Drain current (pulse peak value)	$T_{hs} = 25^\circ\text{C}$	-	4	A
$I_{DR}$	Source-drain diode current (DC)	$T_{hs} = 25^\circ\text{C}$	-	16	A
$I_{DRM}$	Source-drain diode current (pulse peak value)	$T_{hs} = 25^\circ\text{C}$	-	30	W
$P_{tot}$	Total power dissipation	$T_{hs} = 25^\circ\text{C}$	-55	150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		-	150	$^\circ\text{C}$
$T_j$	Junction temperature		-	150	$^\circ\text{C}$

**AVALANCHE LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 8 \text{ A}$ ; $V_{DD} \leq 50 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $R_{GS} = 50 \Omega$	-	510	mJ
		$T_j = 25^\circ\text{C}$ prior to surge	-	82	mJ
		$T_j = 100^\circ\text{C}$ prior to surge	-	13	mJ
$W_{DSR}^1$	Drain-source repetitive unclamped inductive turn-off energy	$I_D = 8 \text{ A}$ ; $V_{DD} \leq 50 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $R_{GS} = 50 \Omega$ ; $T_j \leq 150^\circ\text{C}$	-		

1. Pulse width and frequency limited by  $T_{j(max)}$

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**ISOLATION LIMITING VALUE & CHARACTERISTIC** $T_{hs} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{isol}$	R.M.S. isolation voltage from all three terminals to external heatsink	$f = 50\text{--}60\text{ Hz}$ ; sinusoidal waveform; $R.H. \leq 65\%$ ; clean and dustfree	-		2500	V
$C_{isol}$	Capacitance from T2 to external heatsink	$f = 1\text{ MHz}$	-	10	-	pF

**THERMAL RESISTANCES**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

**STATIC CHARACTERISTICS** $T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 0.25\text{ mA}$	500	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ ; $I_D = 0.25\text{ mA}$	2.0	3.0	4.0	V
$I_{DSS}$	Drain-source leakage current	$V_{DS} = 500\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^{\circ}\text{C}$	-	10	100	$\mu\text{A}$
		$V_{DS} = 400\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 125\text{ }^{\circ}\text{C}$	-	0.1	1.0	mA
$I_{GSS}$	Gate-source leakage current	$V_{GS} = \pm 30\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 4\text{ A}$	-	0.67	0.8	$\Omega$
$V_{SD}$	Source-drain diode forward voltage	$I_F = 8\text{ A}$ ; $V_{GS} = 0\text{ V}$	-	1.4	2.0	V

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**DYNAMIC CHARACTERISTICS** $T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$g_{fs}$	Forward transconductance	$V_{DS} = 15\text{ V}; I_D = 4\text{ A}$	4	6	-	S
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	1500	1800	pF
$C_{oss}$	Output capacitance		-	170	270	pF
$C_{rss}$	Feedback capacitance		-	70	120	pF
$Q_{g(tot)}$	Total gate charge	$V_{GS} = 10\text{ V}; I_D = 8\text{ A}; V_{DS} = 400\text{ V}$	-	65	-	nC
$Q_{gs}$	Gate to source charge		-	8	-	nC
$Q_{gd}$	Gate to drain (Miller) charge		-	34	-	nC
$t_{d\text{ on}}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 2.8\text{ A};$ $V_{GS} = 10\text{ V}; R_{GS} = 50\text{ }\Omega;$ $R_{GEN} = 50\text{ }\Omega$	-	20	40	ns
$t_r$	Turn-on rise time		-	60	90	ns
$t_{d\text{ off}}$	Turn-off delay time		-	200	250	ns
$t_f$	Turn-off fall time		-	75	90	ns
$t_{rr}$	Source-drain diode reverse recovery time	$I_F = 8\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	500	-	ns
$Q_{rr}$	Source-drain diode reverse recovery charge	$V_{GS} = 0\text{ V}; V_R = 100\text{ V}$	-	6	-	$\mu\text{C}$
$L_d$	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
$L_s$	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

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## MECHANICAL DATA

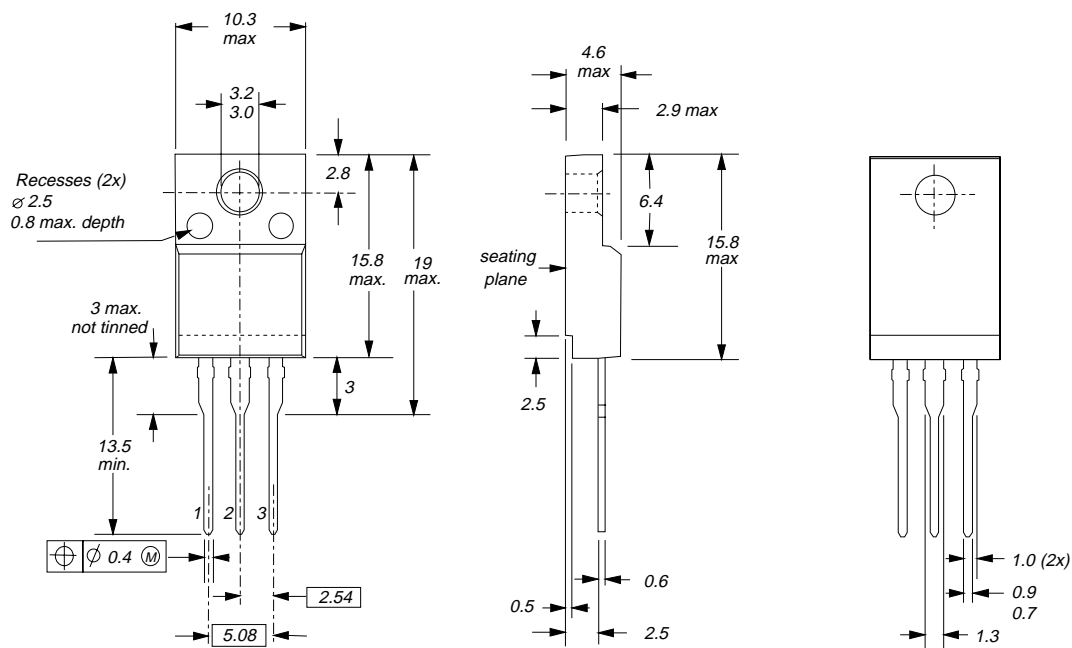
*Dimensions in mm**Net Mass: 2 g*

Fig.1. SOT186A; The seating plane is electrically isolated from all terminals.

**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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