

FAIRCHILD

A Schlumberger Company

μ A739 • μ A749

Dual Audio Operational Amplifier / Preamplifier

Linear Products

Description

The μ A739 and μ A749 consist of two identical High-Gain Operational Amplifiers constructed on a single silicon chip using the Fairchild Planar epitaxial process. These 3-stage amplifiers use Class A PNP transistor output stages with uncommitted collectors. This enables a variety of loads to be employed for general purpose applications from dc to 10 MHz, where two high performance operational amplifiers are required. In addition, the outputs may be wired-OR for use as a dual comparator or they may function as diodes in low threshold rectifying circuits such as absolute value amplifiers, peak detectors, etc.

- SINGLE OR DUAL SUPPLY OPERATION
- LOW POWER CONSUMPTION
- HIGH GAIN, 25,000 V/V
- LARGE COMMON MODE RANGE, +11 V, -13 V
- EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE
- NO LATCH-UP
- OUTPUT SHORT CIRCUIT PROTECTED

Absolute Maximum Ratings

Supply Voltage

(μ A749, μ A749C, μ A739)	± 18 V
(μ A749D)	± 12 V

Internal Power Dissipation

(Note 1)	
Metal Package	500 mW
DIP	650 mW

Differential Input Voltage

	± 5 V
Input Voltage (Note 2)	
(μ A749, μ A749C, μ A739)	± 15 V
(μ A749D)	± 12 V

Storage Temperature Range

Metal Package and Ceramic DIP	-65°C to $+150^{\circ}\text{C}$
Molded DIP	-55°C to $+125^{\circ}\text{C}$

Operating Temperature Range

	0°C to $+70^{\circ}\text{C}$
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Pin Temperature

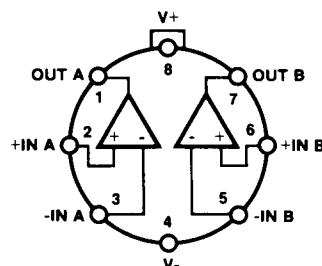
Metal Package, Ceramic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Output Short Circuit Duration,

$T_A = 25^{\circ}\text{C}$ (Note 3)	30 seconds
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Notes

- Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $8.3 \text{ mW}/^{\circ}\text{C}$ for the Ceramic DIP.
- For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to ground or either supply.

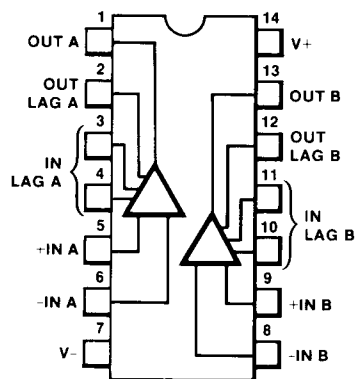
Connection Diagram
8-Pin Metal Package

(Top View)

Pin 4 is connected to case.

Order Information

Type	Package	Code	Part No.
μ A749D	Metal	5W	μ A749DHC

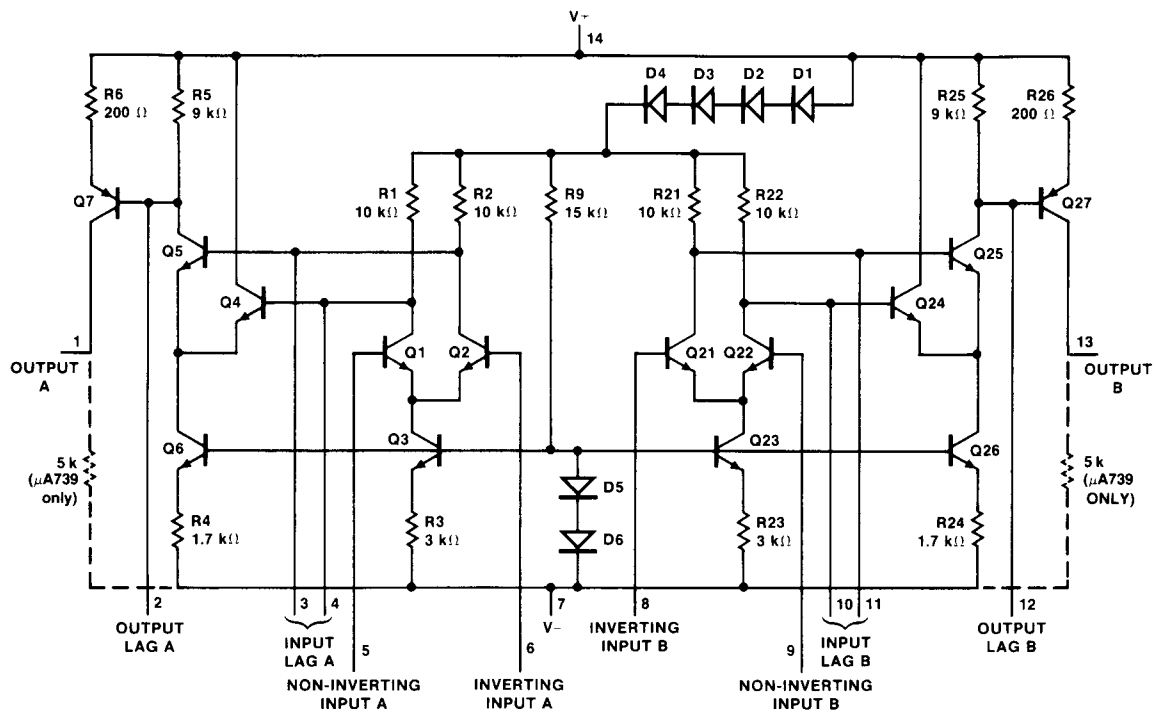
Connection Diagram
14-Pin DIP

(Top View)

Order Information

Type	Package	Code	Part No.
μ A739C	Ceramic DIP	6A	μ A739DC
μ A739C	Molded DIP	9A	μ A739PC
μ A749C	Ceramic DIP	6A	μ A749DC
μ A749C	Molded DIP	9A	μ A749PC

Equivalent Circuit



Pin numbers for DIP only.

μA749C, μA749D and μA739E

Electrical Characteristics $V_+ = \pm 15\text{ V}$, $R_L = 5\text{ k}\Omega$ to Pin 7, $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Condition
Input Offset Voltage	$R_S = 200\ \Omega$
Input Offset Current	
Input Bias Current	
Input Resistance	
Large Signal Voltage Gain	$V_{OUT} = \pm 10\text{ V}$
Positive Output Voltage Swing	
Negative Output Voltage Swing	
Output Resistance	$f = 1.0\text{ kHz}$
Common Mode Rejection Ratio	$R_S = 200\ \Omega$, $V_{IN} = +11.5\text{ V}$ to -13.5 V
Supply Voltage Rejection Ratio	$R_S = 200\ \Omega$
Input Voltage Range	
Internal Power Dissipation	$V_{OUT} = 0$
Supply Current	$V_{OUT} = 0$
Broadband Noise Figure	$R_S = 10\text{ k}\Omega$, $BW = 10\text{ Hz}$ to 10 kHz
Turn On Delay (See Figure 3)	Open Loop, $V_{IN} = \pm 20\text{ mV}$
Turn Off Delay (See Figure 3)	Open Loop, $V_{IN} = \pm 20\text{ mV}$
Slew Rate (unity gain) (See Figure 2)	$C_1 = 0.02\ \mu\text{F}$, $R_1 = 33\ \Omega$, $C_2 = 10\text{ pF}$
Channel Separation (See Figure 4)	$R_S = 1\text{ k}\Omega$, $f = 10\text{ kHz}$
The following specifications apply for $V_+ = \pm 4.0\text{ V}$, $R_L = 10\text{ k}\Omega$ to Pin 7, $T_A = 25^\circ\text{C}$	
Input Offset Voltage	$R_S = 200\ \Omega$
Input Offset Current	
Input Bias Current	
Supply Current	$V_{OUT} = 0$
Internal Power Dissipation	$V_{OUT} = 0$
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0\text{ V}$
Positive Output Voltage Swing	
Negative Output Voltage Swing	
The following specifications apply for $T_A = T_{HIGH}$ to T_{LOW} , $V_S = \pm 15\text{ V}$, $R_L = 5\text{ k}\Omega$ to Pin 7.	
Large Signal Voltage Gain	$V_{OUT} = \pm 10\text{ V}$, $T_A = \text{HIGH}$
	$V_{OUT} = \pm 10\text{ V}$, $T_A = \text{LOW}$
Positive Output Voltage Swing	
Negative Output Voltage Swing	
Input Offset Voltage	$R_S = 200\ \Omega$
Input Offset Current	$T_A = \text{HIGH}$
	$T_A = \text{LOW}$
Input Bias Current	$T_A = \text{HIGH}$
	$T_A = \text{LOW}$
Input Offset Voltage Drift	$R_S = 200\ \Omega$, $+25^\circ\text{C} \leq T_A \leq \text{HIGH}$
	$R_S = 200\ \Omega$, $\text{LOW} \leq T_A \leq +25^\circ\text{C}$

$\mu A749C$			$\mu A749D V_{CC} = \pm 6 V$ $R_L = 10 K$			$\mu A739C$			Units
Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	1.0	6.0		1.0	10		1.0	6.0	mV
	50	750		50	600		50	1000	nA
	0.3	1.5		0.3	1.5		0.3	2.0	μA
50	150		50	150		37	150		k Ω
15,000	50,000		10,000	20,000		6,500	20,000		V / V
+12	+13		+4.5	+5.0		+12	+13		V
-14	-15		-5.5	-6.0		-14	-15		V
	5.0			10			5.0		k Ω
70	90		70	90		70	90		dB
	50	350		50	100		50		$\mu V / V$
-13		+11	-4		+2.5	-10		+11	V
	180	330							mW
	9.0	14	2.0	3.0	4.5		9.0	14	mA
	2.5			2.5			2.0		dB
	.2			.2			.2		μs
	.3			.3			.3		μs
	1.0			1.0			1.0		V / μs
	140			140			140		dB
		6.0					1.0	6.0	mV
	50	600					50	1000	nA
	.3	1.5					300		μA
	2.5						2.5		mA
	20						20		mW
15,000	60,000					2,500	15,000		V / V
+2.5	+2.8					+2.5	+2.8		V
-3.6	-4.0					-3.6	-4.0		V
8,000	40,000								V / V
15,000	50,000								V / V
+12	+13								V
-14	-15								V
	1.0	9.0							mV
	.05	1.5							μA
	.05	1.5							μA
	.3	3.0							μA
	.3	3.0							μA
	3.0								$\mu V / ^\circ C$
	3.0								$\mu V / ^\circ C$

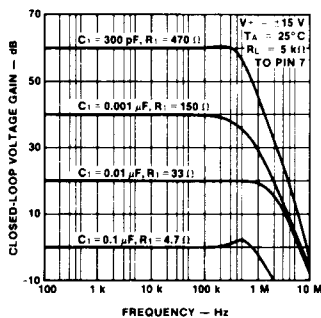
$\mu A749C$, $\mu A749D$ and $\mu A739C$

Electrical Characteristics (Cont.) $V_+ = \pm 15\text{ V}$, $R_L = 5\text{ k}\Omega$ to Pin 7, $T_A = 25^\circ\text{C}$ unless otherwise specified

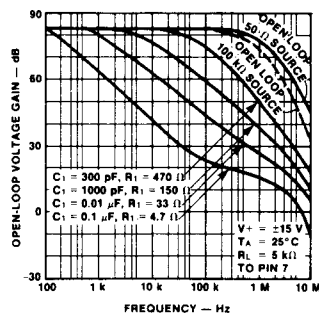
Characteristics	Condition
Input Offset Current Drift	$+25^\circ\text{C} \leq T_A$
Input Bias Current Drift	$LOW \leq T_A \leq +25^\circ\text{C}$
Supply Current	$V_{OUT} = 0$, $T_A = \text{HIGH}$
	$V_{OUT} = 0$, $T_A = \text{LOW}$
Internal Power Dissipation	$V_{OUT} = 0$, $T_A = \text{HIGH}$
	$V_{OUT} = 0$, $T_A = \text{LOW}$
The following specifications apply for T_{HIGH} to T_{LOW} , $V_S = \pm 4.5\text{ V}$, $R_L = 10\text{ k}\Omega$ to Pin 7.	
Input Offset Voltage	$R_S = 200\ \Omega$
Input Offset Current	
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0\text{ V}$, $T_A =$
	$V_{OUT} = \pm 2.0\text{ V}$, $T_A =$
Positive Output Voltage Swing	
Negative Output Voltage Swing	

Typical Performance Curves for $\mu A749C$ and $\mu A739C$

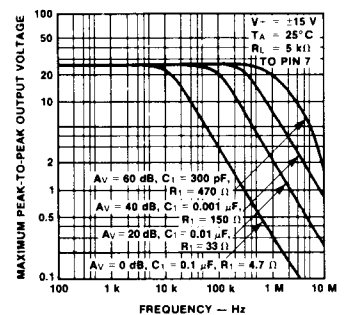
Closed Loop Gain as a Function of Frequency



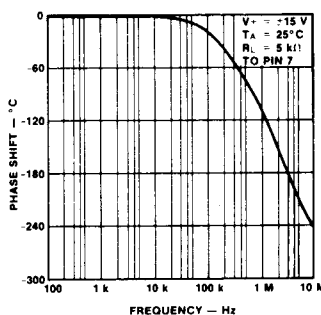
Open Loop Frequency Response Using Recommended Compensation Networks



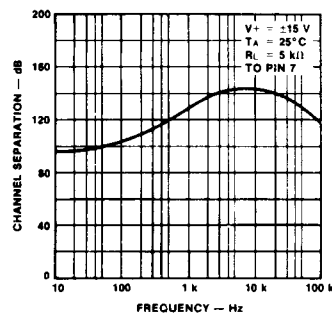
Output Capability as a Function of Frequency and Compensation



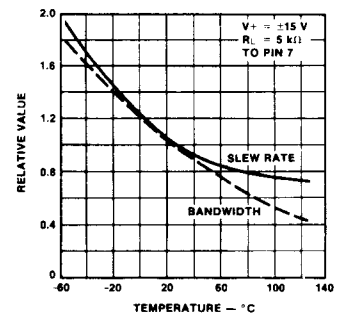
Open Loop Phase Shift Without Compensation



Channel Separation as Function of Frequency



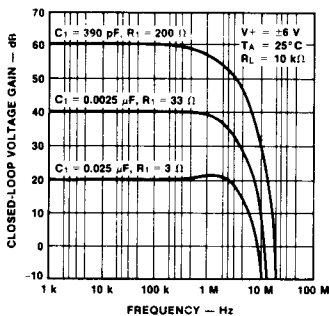
Change of AC Characteristics With Temperature



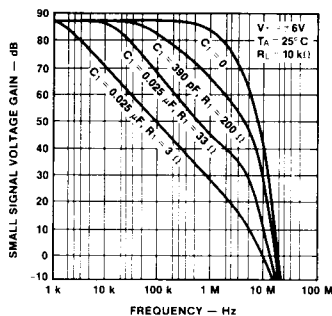
$\mu A749C$			$\mu A749D$ $V_{CC} = \pm 6V$ $R_L = 10K$			$\mu A739C$			Units
Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	.5								nA / °C
	2.0								nA / °C
	4.0								nA / °C
	10								mA
	10								mA
	100								mW
	200								mW
	1.5	7.0							mV
	50	1,000							nA
8,000									V / V
15,000									V / V
+2.5	+2.8								V
-3.6	-4.0								V

Typical Performance Curves for $\mu A749D$

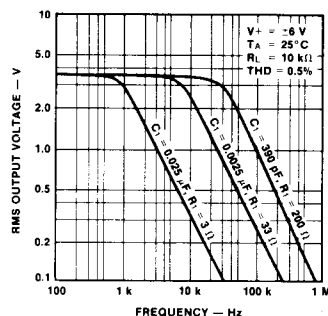
Closed Loop Gain as a Function of Frequency



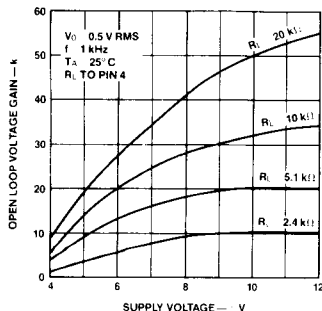
Open Loop Frequency Response Using Recommended Compensation Networks



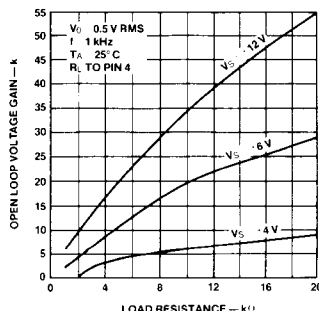
Output Voltage Swing as a Function of Frequency for Various Compensation Networks



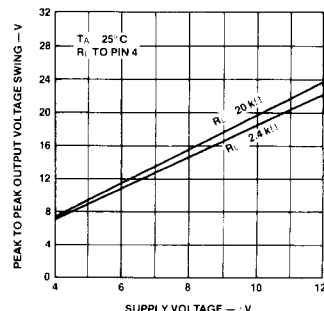
Open Loop Voltage Gain As a Function of Supply Voltage



Open Loop Voltage Gain As a Function of Load Resistance

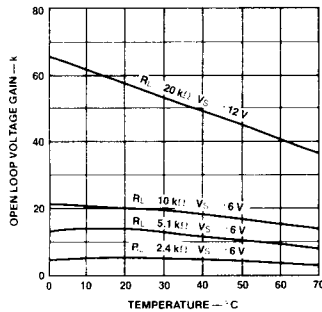


Typical Output Voltage As a Function of Supply Voltage

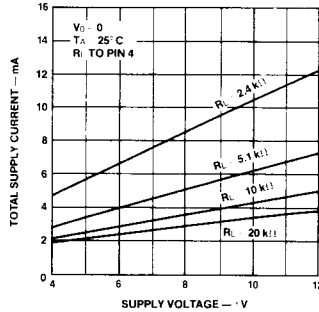


Typical Performance Curves for $\mu A749D$ (Cont.)

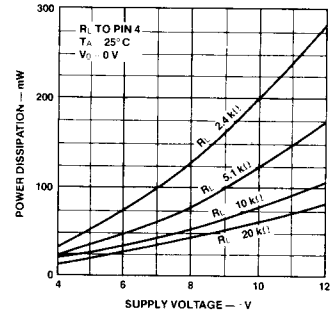
Open Loop Gain
As a Function of
Temperature



Total Supply Current
As a Function of
Supply Voltage

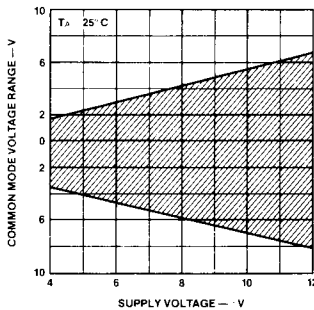


Total Power Dissipation
As a Function of
Supply Voltage and Load

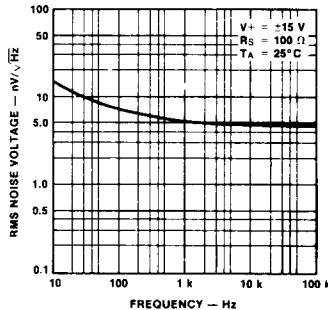


Typical Performance Curves for $\mu A749$ and $\mu A749C$

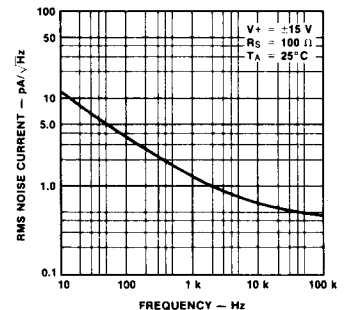
Common Mode Range
As a Function of
Supply Voltage



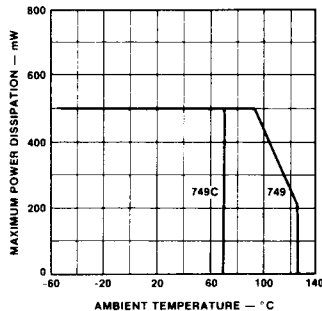
Input Noise Voltage as a
Function of Frequency



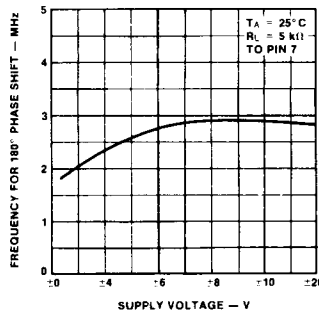
Input Noise Current as a
Function of Frequency



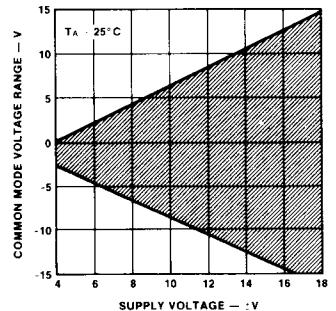
Absolute Maximum Power
Dissipation as a
Function of Temperature



Open Loop 180 $^{\circ}$ Phase
Shift Frequency as a
Function of
Supply Voltage

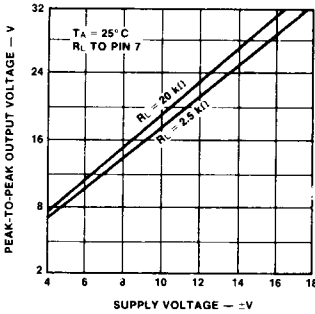


Common Mode Range as a
Function of
Supply Voltage

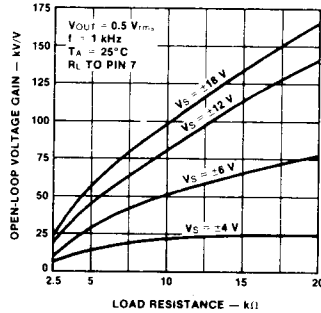


Typical Performance Curves for $\mu A749$ and $\mu A749C$ (Cont.)

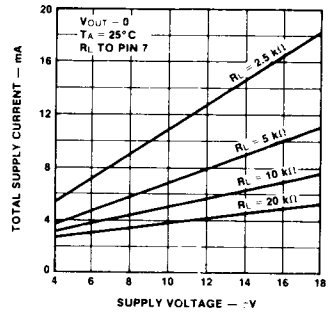
Typical Output Voltage as a Function of Supply Voltage



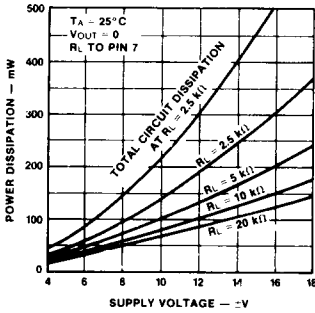
Open Loop Voltage Gain as a Function of Load Resistance



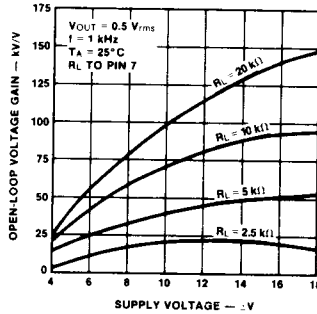
Total Supply Current as a Function of Supply Voltage



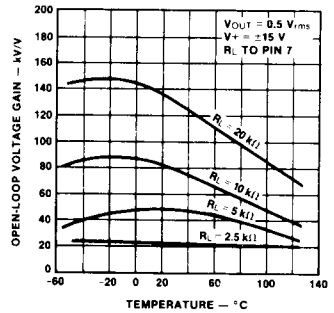
Total Power Dissipation as a Function of Supply Voltage and Load



Open Loop Voltage Gain as a Function of Supply Voltage

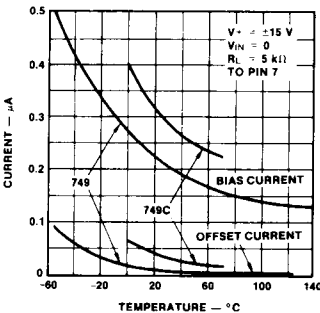


Open Loop Gain as a Function of Temperature

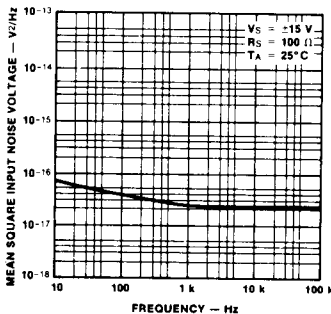


Typical Performance Curves for $\mu A739C$

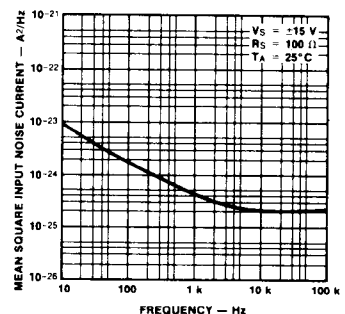
Input Offset Current and Bias Current as Functions of Temperature



Input Noise Voltage as a Function of Frequency

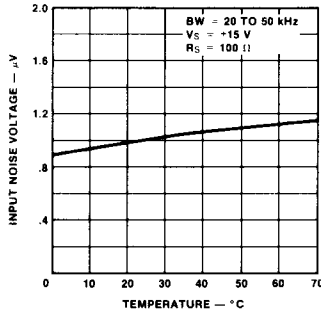


Input Noise Current as a Function of Frequency

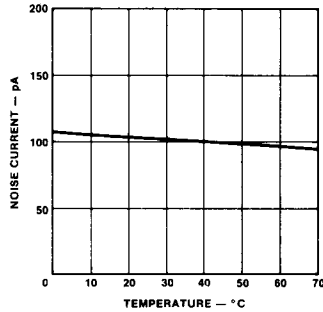


Typical Performance Curves for $\mu A739C$ (Cont.)

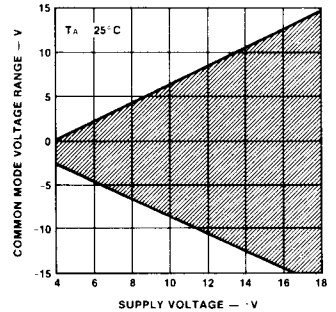
Wide Band Input Noise Voltage as a Function of Temperature



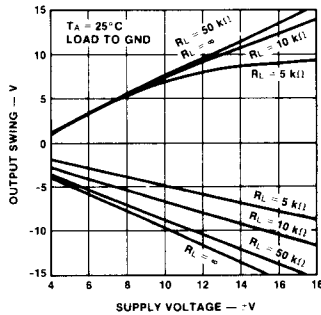
Wide Band Input Noise Current as a Function of Temperature



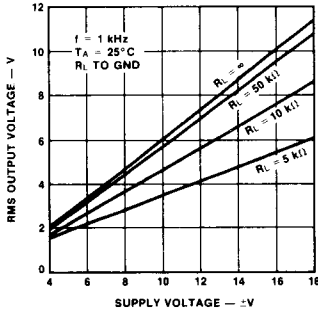
Common Mode Range as a Function of Supply Voltage



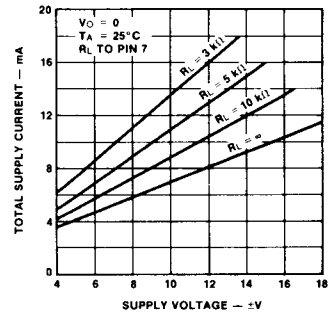
Typical Output Voltage as a Function of Supply Voltage



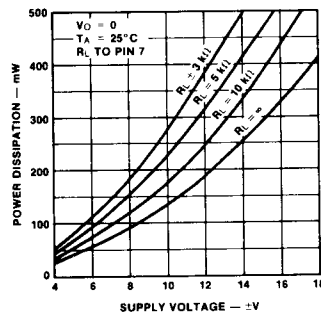
Output Capability as a Function of Supply Voltage



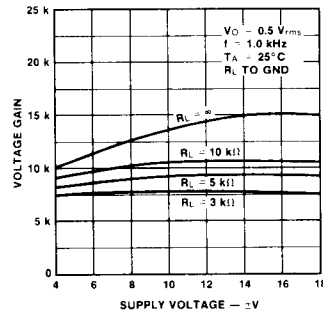
Total Supply Current as a Function of Supply Voltage



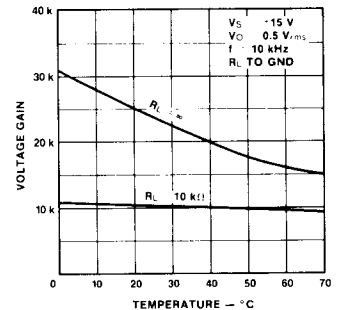
Total Power Dissipation as a Function of Supply Voltage and Load



Open Loop Voltage Gain as a Function of Supply Voltage

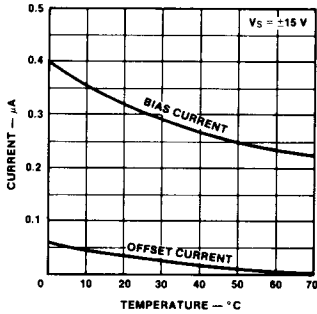


Open Loop Gain as a Function of Temperature



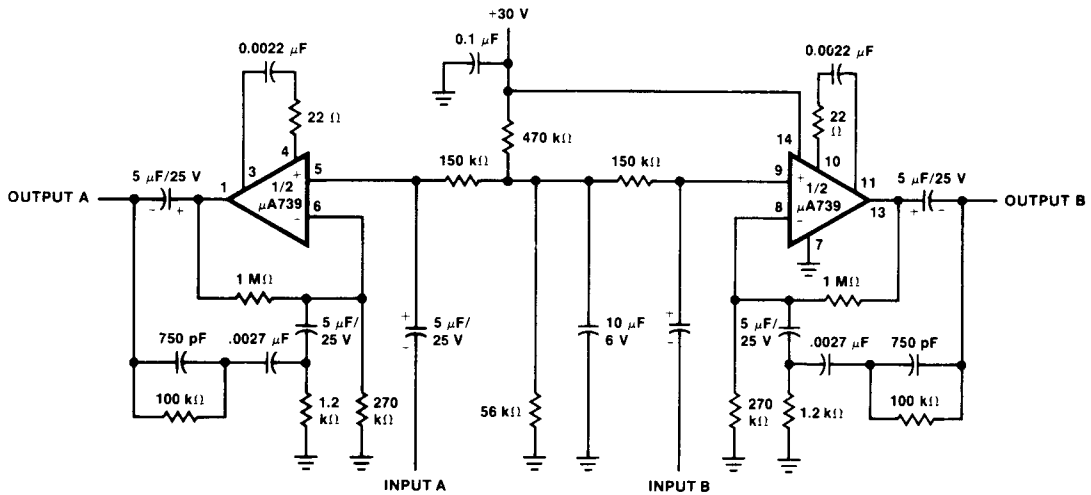
Typical Performance Curves for $\mu A739C$ (Cont.)

Input Offset Current and Bias Current as a Function of Temperature



Typical Applications

Stereo Phono Preamplifier—RIAA Equalized



Typical Performance

Gain 40 dB at 1 kHz, RIAA equalized

Input overload point, 80 mV rms

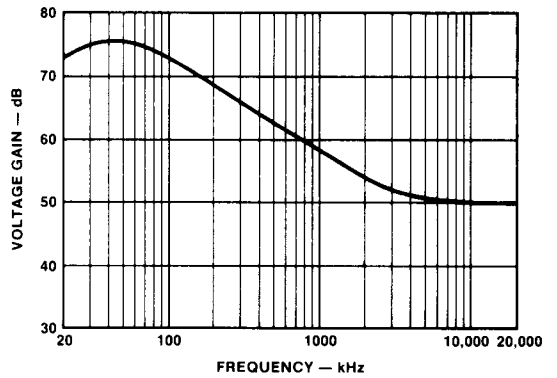
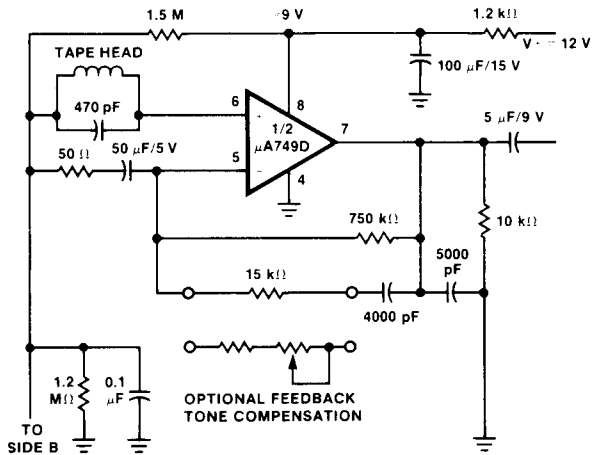
Noise Level, 2 μV referred to input

Signal to noise ratio, 74 dB below 10 mW

Channel separation @ 1 kHz, 80 dB

Typical Applications (Cont.)

Stereo Tape Preamplifier



Typical Performance

Gain at 1 kHz	60 dB
Output Voltage Swing	2.8 V rms
Power Consumption	30 mW