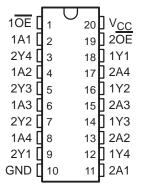
SCES274B - JUNE 1999 - REVISED JANUARY 2000

- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot) >2 V at  $V_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Ioff and Power-Up 3-State Support Hot Insertion
- **Supports Mixed-Mode Signal Operation on** All Ports (5-V Input/Output Voltage With 3.3-V V<sub>CC</sub>)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **Package Options Include Shrink** Small-Outline (DB), Plastic Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) **Packages**

#### DB, DGV, DW, OR PW PACKAGE (TOP VIEW)



#### description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V<sub>CC</sub> operation.

The SN74LVCZ244A is organized as two 4-bit line drivers with separate output-enable (OE) inputs. When OE is low, the device passes data from the A inputs to the Y outputs. When  $\overline{\sf OE}$  is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{\sf OE}$  should be tied to  $V_{\sf CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using Ioff and power-up 3-state. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN74LVCZ244A is characterized for operation from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

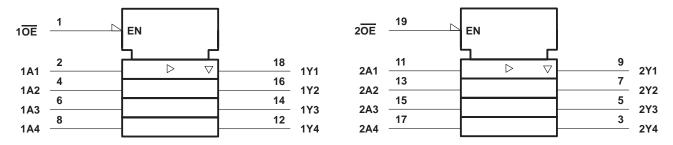
EPIC is a trademark of Texas Instruments Incorporated



### FUNCTION TABLE (each buffer)

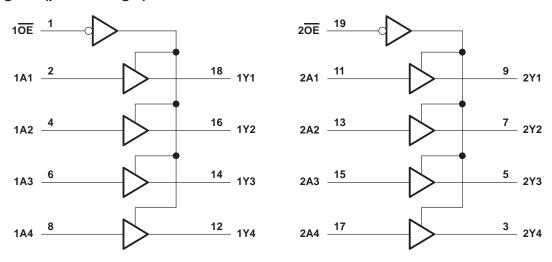
INPU	JTS	OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

### logic symbol†



<sup>&</sup>lt;sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)





#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
PW package	83°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51.

#### recommended operating conditions (see Note 4)

				MAX	UNIT
Vcc	Supply voltage			3.6	V
VIH	High-level input voltage V <sub>CC</sub> = 2	.7 V to 3.6 V	2		V
V <sub>IL</sub>	Low-level input voltage V <sub>CC</sub> = 2	.7 V to 3.6 V		0.8	V
VI	Input voltage		0	5.5	V
Va	Output voltage		0	VCC	V
Vo	Output voltage 3-state		0	5.5	V
lau	V <sub>CC</sub> = 2.7 V			-12	mA
ЮН	High-level output current $V_{CC} = 3$	V		-24	ША
lai	V <sub>CC</sub> = 2.7 V			12	mA
lOL	Low-level output current $V_{CC} = 3$	V		24	IIIA
Δt/Δν	Input transition rise or fall rate			6	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate			150	μs/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCES274B - JUNE 1999 - REVISED JANUARY 2000

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	ONDITIONS	Vcc	MIN	TYP	MAX	UNIT	
	$I_{OH} = -100 \mu\text{A}$		2.7 V to 3.6 V	V <sub>CC</sub> -0.	2			
\/	I <sub>OH</sub> = -12 mA		2.7 V	2.2			V	
VOH			3 V	2.4			V	
	I <sub>OH</sub> = -24 mA		3 V	2.2				
	I <sub>OL</sub> = 100 μA		2.7 V to 3.6 V			0.2		
VOL	I <sub>OL</sub> = 12 mA		2.7 V			0.4	V	
	I <sub>OL</sub> = 24 mA		3 V			0.55		
lį	V <sub>I</sub> = 0 to 5.5 V		3.6 V			±5	μΑ	
l <sub>off</sub>	V <sub>O</sub> = 0 to 5.5 V	$V_{O} = 0 \text{ to } 5.5 \text{ V}$				±5	μΑ	
loz	V <sub>O</sub> = 0 to 5.5 V		3.6 V			±5	μΑ	
l <sub>OZPU</sub>	$V_0 = 0.5 \text{ V to } 2.5 \text{ V},$	OE = don't care	0 to 1.5 V			±5	μΑ	
lozpd	$V_0 = 0.5 \text{ V to } 2.5 \text{ V},$	OE = don't care	1.5 V to 0			±5	μΑ	
las	$V_I = V_{CC}$ or GND		3.6 V			100		
lcc	$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{\ddagger}$	IO = 0				100	μΑ	
Δl <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			100	μΑ	
Ci	$V_I = V_{CC}$ or GND		3.3 V		3.5	·	pF	
Co	$V_O = V_{CC}$ or GND		3.3 V		5.5	·	pF	

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
	(1141 01)	(0011 01)	MIN M	AX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A		6.9	1.5	5.9	ns
t <sub>en</sub>	ŌĒ	A or B		8.6	1.5	7.6	ns
<sup>t</sup> dis	ŌĒ	A or B		6.8	1.5	6.5	ns

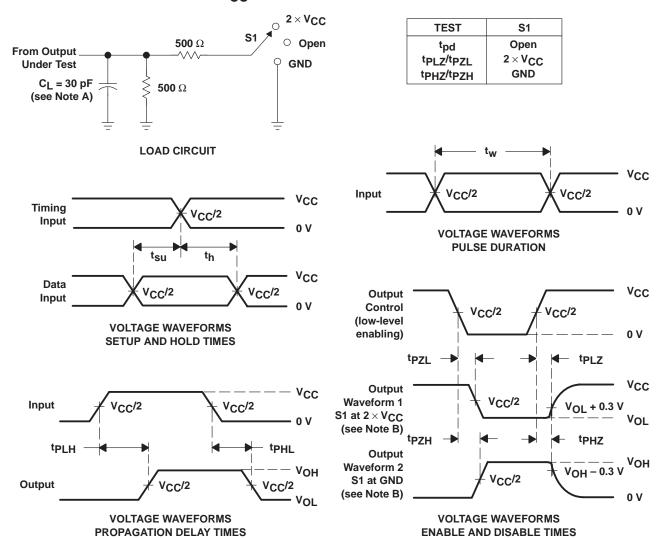
#### operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST	V <sub>CC</sub> = 3.3 V	UNIT	
	FARAMETER			TYP	ONII
<u> </u>	Down discinstian conscitones not buffer/driver	Outputs enabled	f = 10 MHz	40	pF
Cpd	Power dissipation capacitance per buffer/driver	Outputs disabled	1 = 10 MHZ	3	PΓ



<sup>‡</sup> This applies in the disabled state only.

#### PARAMETER MEASUREMENT INFORMATION $V_{CC}$ = 2.7 V AND 3.3 V $\pm$ 0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_Q = 50 \Omega$ ,  $t_r \leq$  2 ns,  $t_f \leq$  2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

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