DRAM

MT4LC8M8P4, MT4LC8M8C2

For the latest data sheet, please refer to the Micron Web site: www.micronsemi.com/mti/msp/html/datasheet.html

FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x8 pinout, timing, functions, and packages
- 12 row, 11 column addresses (C2) or 13 row, 10 column addresses (P4)
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- Extended Data-Out (EDO) PAGE MODE access
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) REFRESH distributed across 64ms
- Optional self refresh (S) for low-power data retention

OPTIONS — MARKING

OPTIONS	MARKING
• Refresh Addressing	
4,096 (4K) rows	C2
8,192 (8K) rows	P4
• Plastic Packages	
32-pin SOJ (400 mil)	DJ
32-pin TSOP (400 mil)	TG
• Timing	
50ns access	-5
60ns access	-6
• Refresh Rates	
Standard Refresh (64ms period)	None
Self Refresh (128ms period)	S*

NOTE: 1. The 8 Meg x 8 EDO DRAM base number differentiates the offerings in one place—MT4LC8M8C2. The fifth field distinguishes the address offerings: C2 designates 4K addresses and P4 designates 8K addresses.
2. The "#" symbol indicates signal is active LOW.

*Contact factory for availability

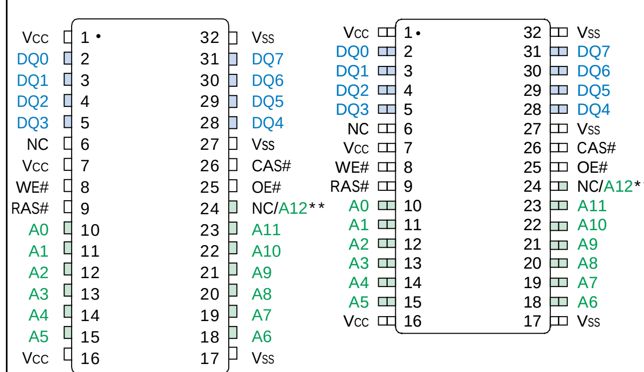
Part Number Example:
MT4LC8M8C2DJ-5

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

PIN ASSIGNMENT (Top View)

32-Pin SOJ — 32-Pin TSOP



**NC on C2 version and A12 on P4 version

8 MEG x 8 EDO DRAM PART NUMBERS

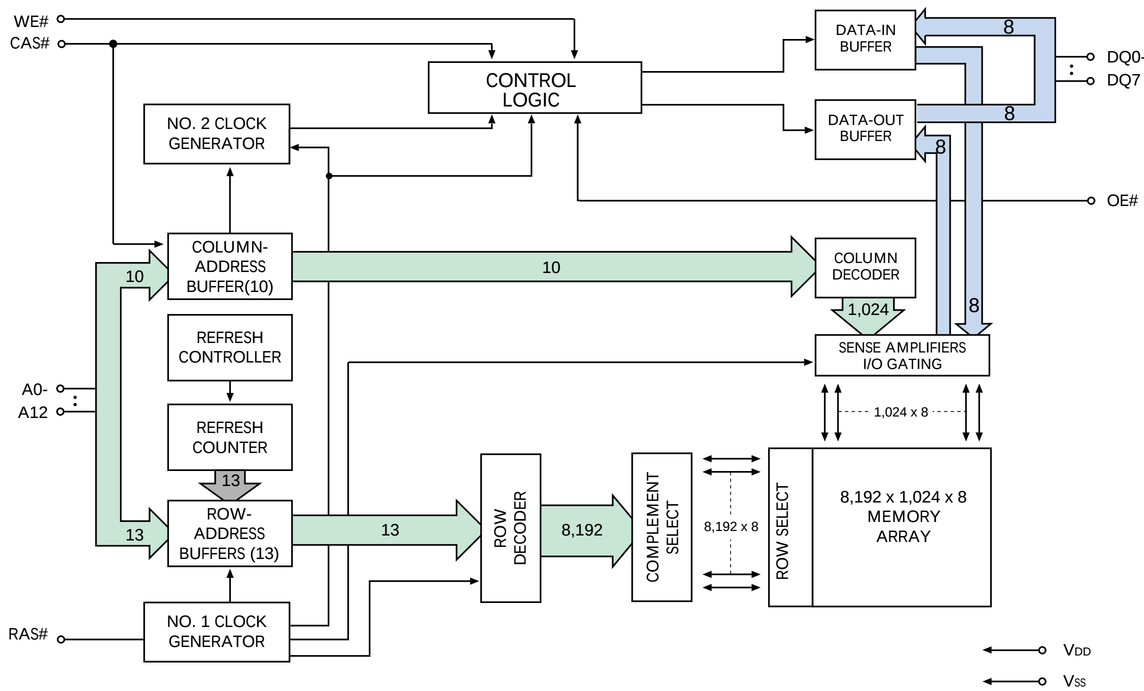
PART NUMBER	REFRESH ADDRESSING	PACKAGE	REFRESH
MT4LC8M8C2DJ-x	4K	SOJ	Standard
MT4LC8M8C2DJ-x S	4K	SOJ	Self
MT4LC8M8C2TG-x	4K	TSOP	Standard
MT4LC8M8C2TG-x S	4K	TSOP	Self
MT4LC8M8P4DJ-x	8K	SOJ	Standard
MT4LC8M8P4DJ-x S	8K	SOJ	Self
MT4LC8M8P4TG-x	8K	TSOP	Standard
MT4LC8M8P4TG-x S	8K	TSOP	Self

x = speed

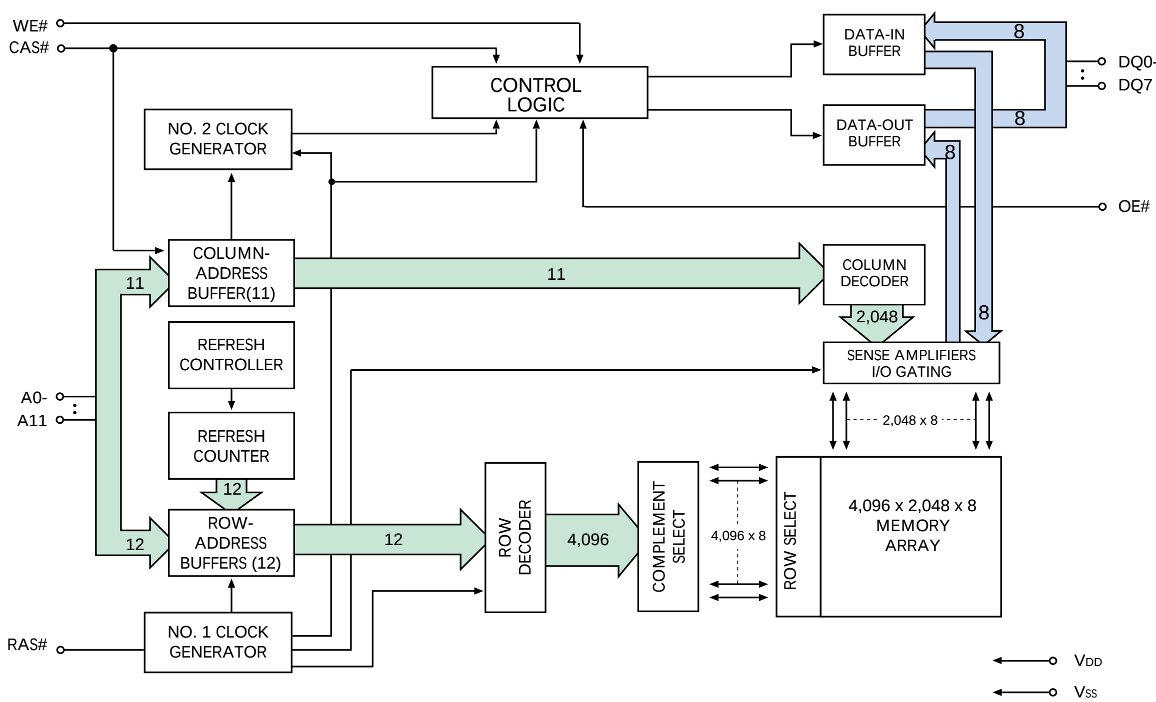
GENERAL DESCRIPTION

The 8 Meg x 8 DRAM is a high-speed CMOS, dynamic random-access memory devices containing 67,108,864 bits and designed to operate from 3V to 3.6V. The MT4LC8M8C2 and MT4LC8M8P4 are functionally organized as 8,388,608 locations containing eight bits each. The 8,388,608 memory locations are arranged in 4,096 rows by 2,048 columns on the C2 version and 8,192 rows by 1,024 columns on the P4 version. During READ or WRITE cycles, each location is

FUNCTIONAL BLOCK DIAGRAM
MT4LC8M8P4 (13 row addresses)



FUNCTIONAL BLOCK DIAGRAM
MT4LC8M8C2 (12 row addresses)



GENERAL DESCRIPTION (continued)

uniquely addressed via the address bits. First, the row address is latched by the RAS# signal, then the column address is latched by CAS#. Both devices provide EDO-PAGE-MODE operation, allowing for fast successive data operations (READ, WRITE, or READ-MODIFY-WRITE) within a given row.

The 8 Meg x 8 DRAM must be refreshed periodically in order to retain stored data.

DRAM ACCESS

Each location in the DRAM is uniquely addressable, as mentioned in the General Description. The data for each location is accessed via the eight I/O pins (DQ0-DQ7). A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z, regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no write will occur, and the data outputs will drive read data from the accessed location.

EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. If CAS# went HIGH and OE# was LOW (active), the output buffers would be disabled. The 8 Meg x 8 DRAM offers an accelerated page mode cycle by eliminating output disable from CAS# HIGH. This option is called EDO, and it allows CAS# precharge time (^{t}CP) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms in the noted appendix).

EDO operates like any DRAM READ or FAST-PAGE-MODE READ, except data is held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH. OE# can be brought LOW or HIGH while CAS# and RAS# are LOW, and the DQs will transition between valid data and High-Z. Using OE#, there are two methods to disable the outputs and keep them disabled during the CAS# HIGH time. The first method is to have OE# HIGH when CAS# transitions HIGH and keep OE# HIGH for ^{t}OEHC thereafter. This will disable the DQs, and they will remain disabled (regardless of the state of OE# after that point) until CAS# falls again. The second method is to have OE# LOW when CAS# transitions HIGH and then bring OE# HIGH for a minimum of ^{t}OEP anytime during the CAS# HIGH period. This will disable the DQs, and they will remain disabled (regardless of the state of OE# after that point) until CAS# falls again (see Figure 1). During

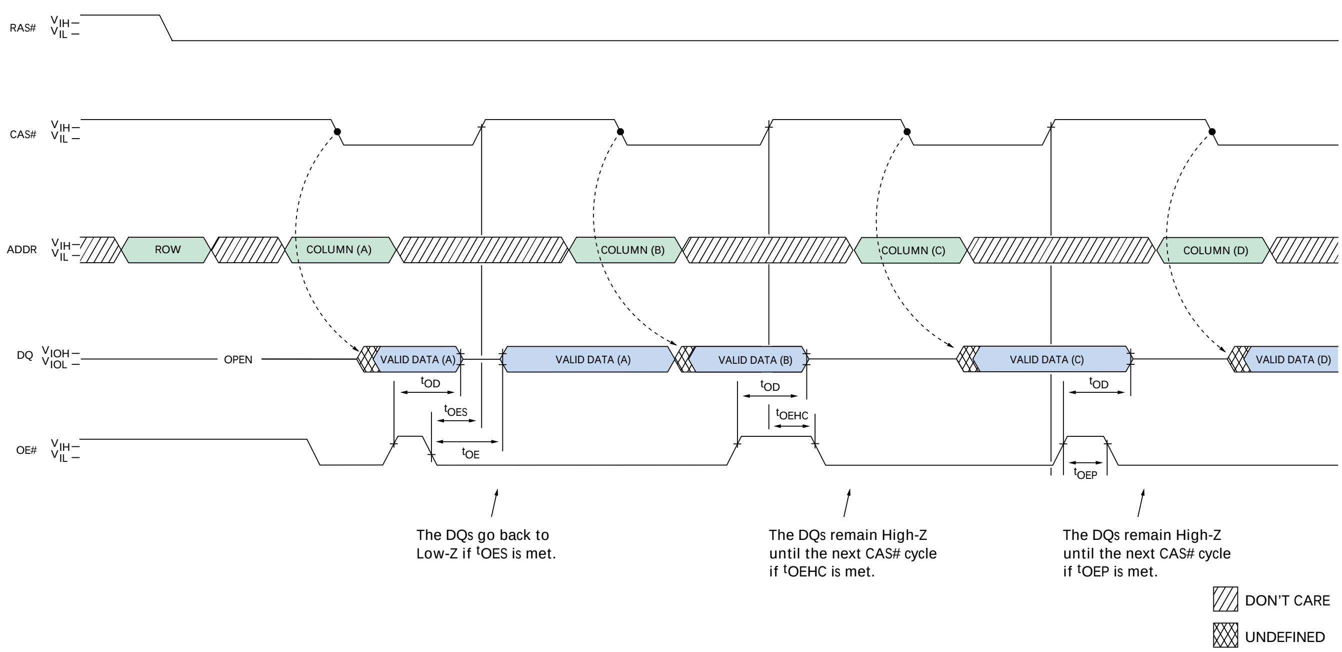


Figure 1
OE# CONTROL of DQs

EDO PAGE MODE (continued)

other cycles, the outputs are disabled at ^{t}OFF time after RAS# and CAS# are HIGH or at ^{t}WHZ after WE# transitions LOW. The ^{t}OFF time is referenced from the rising edge of RAS# or CAS#, whichever occurs last. WE# can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

EDO-PAGE-MODE operations are always initiated with a row address strobed in by the RAS# signal, followed by a column address strobed in by CAS#, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS# while holding RAS# LOW and entering new column addresses with each CAS# cycle. Returning RAS# HIGH terminates the EDO-PAGE-MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (P4) or all 4,096 rows (C2) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC8M8P4 internally refreshes two rows for every CBR cycle, whereas the MT4LC8M8C2 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing. Alternatively, RAS#-ONLY REFRESH capability is inherently provided. However, with this method, some compatibility issues may become apparent. For example, both C2 and P4 versions require 4,096 CBR REFRESH cycles, yet each requires a different number of RAS#-ONLY REFRESH cycles (C2 = 4,096 and P4 = 8,192). JEDEC strongly recommends the use of CBR REFRESH for this device.

An optional self refresh mode is also available on the “S” version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^{t}RASS. The “S” option allows for an extended period of 128ms, or 31.25µs per row for a 4K refresh and 15.625µs per row for an 8K refresh, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst CBR refresh sequence, all 1,024 rows must be refreshed using a minimum ^{t}RC refresh rate prior to resuming normal operation.

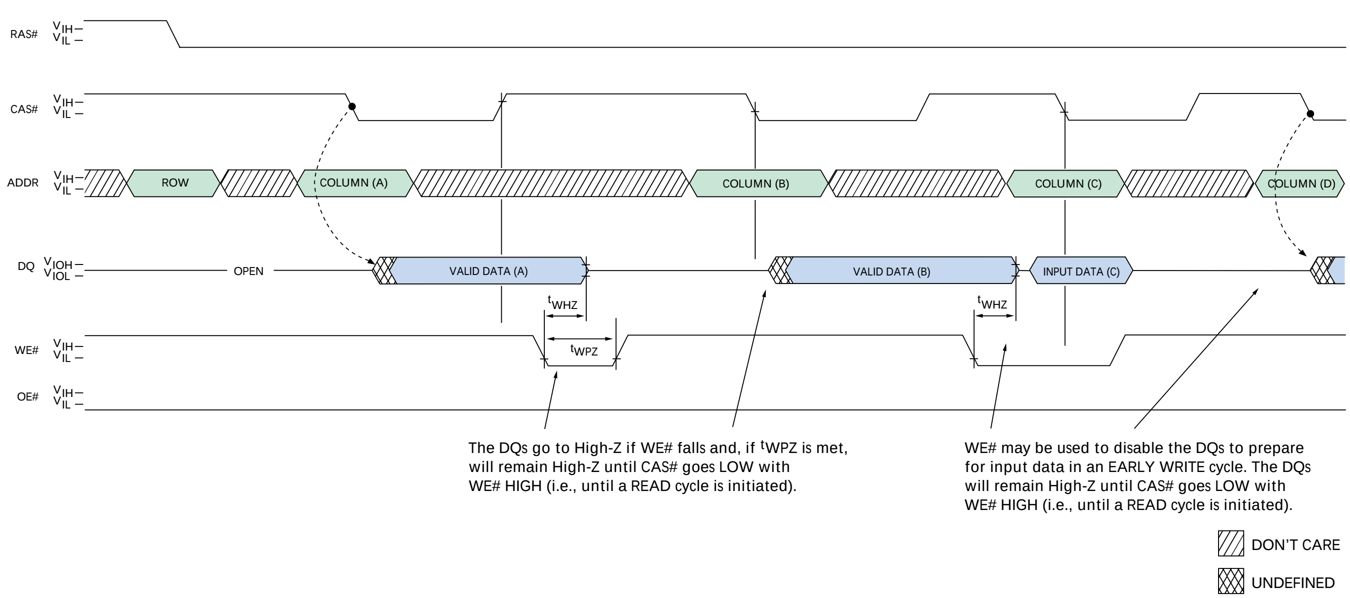


Figure 2
WE# CONTROL of DQs

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Relative to V_{SS} .... -1V to +4.6V
Voltage on NC, Inputs or I/O Pins
Relative to V_{SS} .... -1V to +4.6V
Operating Temperature, T_A (ambient) ... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Note: 1) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{CC}	3	3.6	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V_{IH}	2	V_{CC} + 0.3	V	26
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V_{IL}	-0.3	0.8	V	26
INPUT LEAKAGE CURRENT: Any input at V_{IN} (0V ≤ V_{IN} ≤ V_{CC} + 0.3V); All other pins not under test = 0V	I_I	-2	2	µA	27
OUTPUT HIGH VOLTAGE: I_{OUT} = -2mA	V_{OH}	2.4	–	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 2mA	V_{OL}	–	0.4	V	
OUTPUT LEAKAGE CURRENT: Any output at V_{OUT} (0V ≤ V_{OUT} ≤ V_{CC} + 0.3V); DQ is disabled and in High-Z state	I_{OZ}	-5	5	µA	

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 2, 3, 5, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SPEED	4K REFRESH	8K REFRESH	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{CC1}	ALL	1	1	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# ≥ V_{CC} - 0.2V; DQs may be left open; other inputs: V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V)	I_{CC2}	ALL	500	500	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	-5 -6	175 165	135 125	mA	25
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	-5 -6	155 125	155 125	mA	25
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	-5 -6	175 165	135 125	mA	22
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	-5 -6	165 155	165 155	mA	4, 7
REFRESH CURRENT: Extended ("S" version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = ^tRAS (MIN); WE# = V_{CC} - 0.2V; A0-A11, OE# and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC7}	ALL	400	400	µA	4, 7
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR with RAS# ≥ ^tRASS (MIN) and CAS# held LOW; WE# = V_{CC} - 0.2V; A0-A11, OE# and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	ALL	350	400	µA	4, 7

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance: Address pins	C_{I1}	5	pF
Input Capacitance: RAS#, CAS#, WE#, OE#	C_{I2}	7	pF
Input/Output Capacitance: DQ	C_{IO}	7	pF

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		25		30	ns	
Column-address setup to CAS# precharge	^tACH	12		15		ns	
Column-address hold time (referenced to RAS#)	^tAR	38		45		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Column address to WE# delay time	^tAWD	42		49		ns	18
Access time from CAS#	^tCAC		13		15	ns	
Column-address hold time	^tCAH	8		10		ns	
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	^tCHD	15		15		ns	
CAS# hold time (CBR Refresh)	^tCHR	8		10		ns	4
CAS# to output in Low-Z	^tCLZ	0		0		ns	
Data output hold after CAS# LOW	^tCOH	3		3		ns	
CAS# precharge time	^tCP	8		10		ns	13
Access time from CAS# precharge	^tCPA		28		35	ns	
CAS# to RAS# precharge time	^tCRP	5		5		ns	
CAS# hold time	^tCSH	38		45		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	4
CAS# to WE# delay time	^tCWD	28		35		ns	18
Write command to CAS# lead time	^tCWL	8		10		ns	
Data-in hold time	^tDH	8		10		ns	19
Data-in setup time	^tDS	0		0		ns	19
Output disable	^tOD	0	12	0	15	ns	23, 24
Output enable time	^tOE		12		15	ns	20
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	8		10		ns	24
OE# HIGH hold time from CAS# HIGH	^tOEHC	5		10		ns	
OE# HIGH pulse width	^tOEP	5		5		ns	
OE# LOW to CAS# HIGH setup time	^tOES	4		5		ns	
Output buffer turn-off delay	^tOFF	0	12	0	15	ns	17, 23

AC ELECTRICAL CHARACTERISTICS

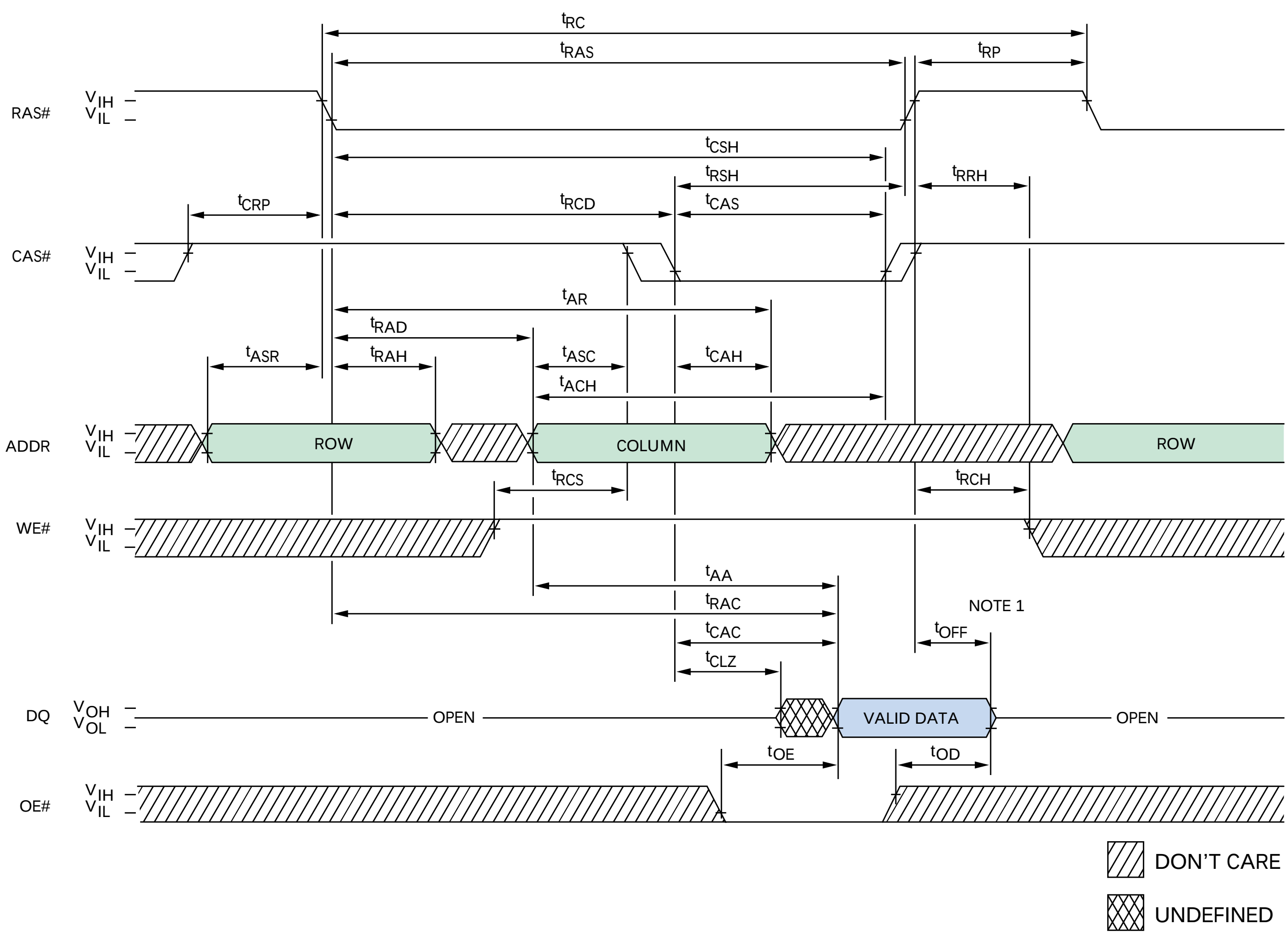
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	20		25		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^tPRWC	47		56		ns	
Access time from RAS#	^tRAC		50		60	ns	
RAS# to column-address delay time	^tRAD	9		12		ns	15
Row-address hold time	^tRAH	9		10		ns	
RAS# pulse width	^tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	^tRASP	50	125,000	60	125,000	ns	
RAS# pulse width during Self Refresh	^tRASS	100		100		µs	
Random READ or WRITE cycle time	^tRC	84		104		ns	
RAS# to CAS# delay time	^tRCD	11		14		ns	14
READ command hold time (referenced to CAS#)	^tRCH	0		0		ns	16
READ command setup time	^tRCS	0		0		ns	
Refresh period	^tREF		64		64	ms	23
Refresh period (2,048 cycles) "S" version	^tREF		128		128	ms	
RAS# precharge time	^tRP	30		40		ns	
RAS# to CAS# precharge time	^tRPC	5		5		ns	
RAS# precharge time exiting Self Refresh	^tRPS	90		105		ns	
READ command hold time (referenced to RAS#)	^tRRH	0		0		ns	16
RAS# hold time	^tRSH	13		15		ns	
READ-WRITE cycle time	^tRWC	116		140		ns	
RAS# to WE# delay time	^tRWD	67		79		ns	18
WRITE command to RAS# lead time	^tRWL	13		15		ns	
Transition time (rise or fall)	^tT	2	50	2	50	ns	
WRITE command hold time	^tWCH	8		10		ns	
WRITE command hold time (referenced to RAS#)	^tWCR	38		45		ns	
WE# command setup time	^tWCS	0		0		ns	18
WE# to outputs in High-Z	^tWHZ		12		15	ns	
WRITE command pulse width	^tWP	5		5		ns	
WE# pulse widths to disable outputs	^tWPZ	10		10		ns	
WE# hold time (CBR Refresh)	^tWRH	8		10		ns	
WE# setup time (CBR Refresh)	^tWRP	8		10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz; T_A = 25°C.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 2.5ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# and RAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF; and V_{OL} = 0.8V and V_{OH} = 2V.
13. If CAS# is LOW at the falling edge of RAS#, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
14. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC, and ^{t}CAC must always be met.
15. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD limit, ^{t}AA and ^{t}CAC must always be met.
16. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
17. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
18. ^{t}WCS, ^{t}RWD, ^{t}AWD, and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. If ^{t}WCS > ^{t}WCS MIN, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. ^{t}RWD, ^{t}AWD and ^{t}CWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.
22. RAS#-ONLY REFRESH requires that all rows be refreshed at least once every 64ms (4,096 rows for the C2 version and 8,192 rows for the P4 version). CBR REFRESH requires that at least 4,096 cycles be completed every 64ms.
23. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If CAS# stays LOW while OE# is brought HIGH, the DQs will open. If OE# is brought back LOW (CAS# still LOW), the DQs will provide the previously read data.
24. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE# is taken back LOW while CAS# remains LOW, the DQs will remain open.
25. Column address changed once each cycle.
26. V_{IH} overshoot: V_{IH} (MAX) = V_{CC} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.
27. NC pins are assumed to be left floating and are not tested for leakage.

READ CYCLE



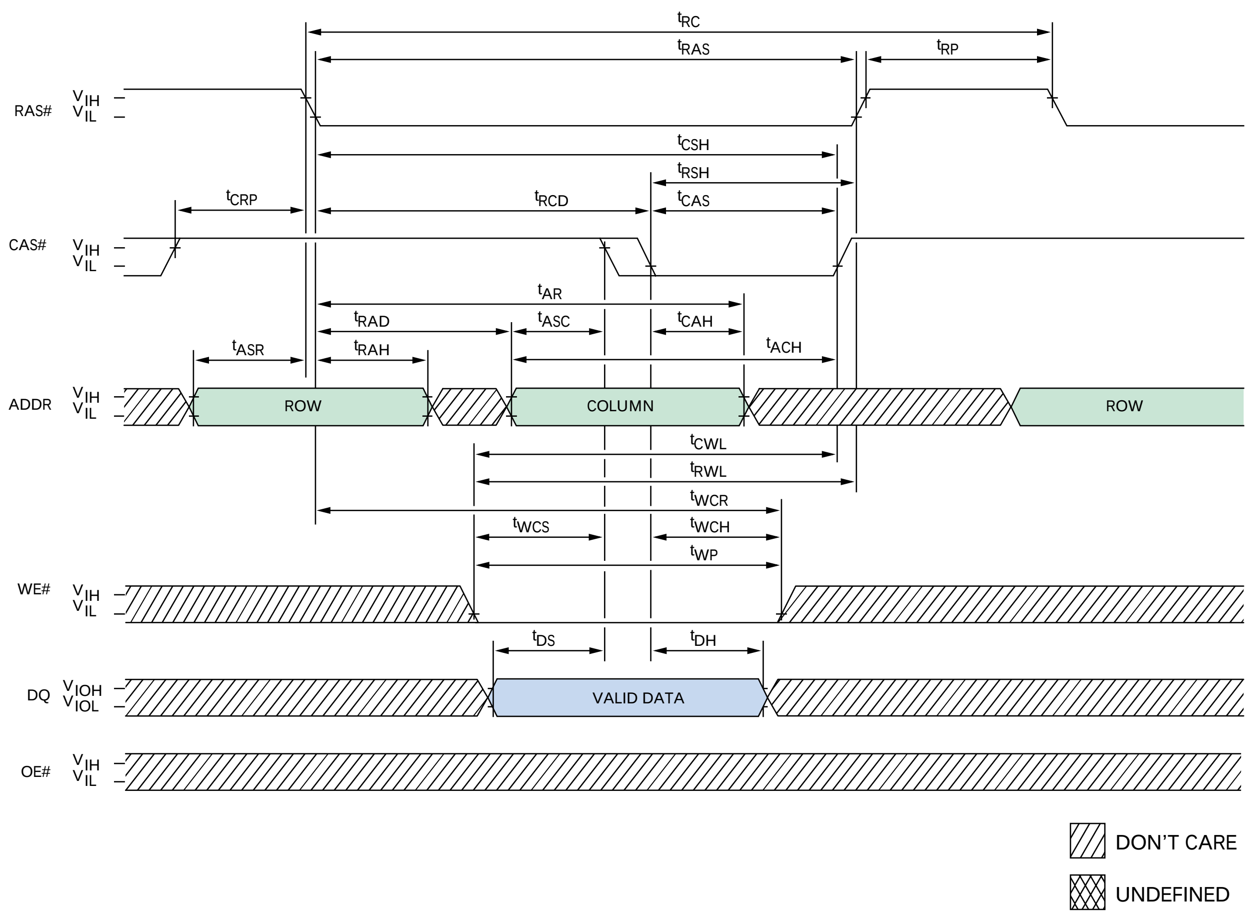
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tAA		25		30	ns
^tACH	12		15		ns
^tAR	38		45		ns
^tASC	0		0		ns
^tASR	0		0		ns
^tCAC		13		15	ns
^tCAH	8		10		ns
^tCAS	8	10,000	10	10,000	ns
^tCLZ	0		0		ns
^tCRP	5		5		ns
^tCSH	38		45		ns
^tOD	0	12	0	15	ns
^tOE		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tOFF	0	12	0	15	ns
^tRAC		50		60	ns
^tRAD	9		12		ns
^tRAH	9		10		ns
^tRAS	50	10,000	60	10,000	ns
^tRC	84		104		ns
^tRCD	11		14		ns
^tRCH	0		0		ns
^tRCS	0		0		ns
^tRP	30		40		ns
^tRRH	0		0		ns
^tRSH	13		15		ns

NOTE: 1. ^tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

EARLY WRITE CYCLE

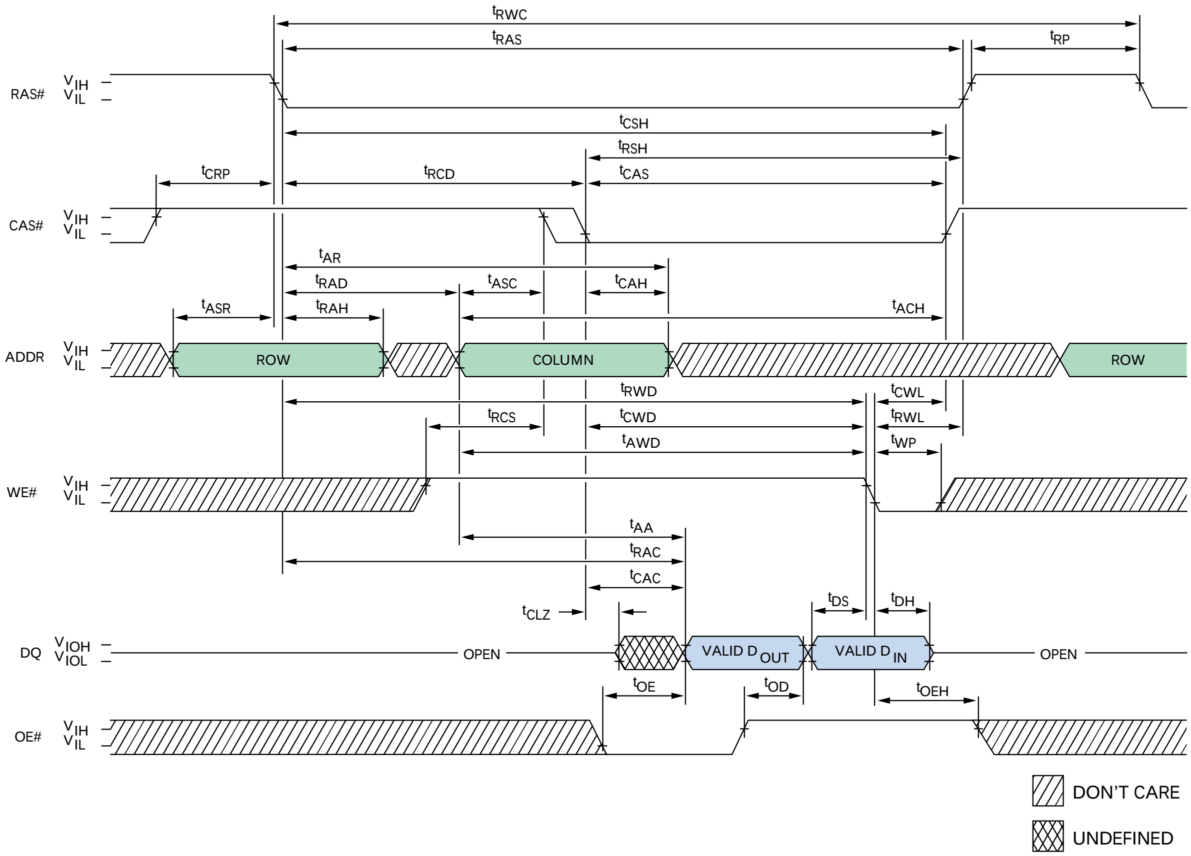


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tACH	12		15		ns
^tAR	38		45		ns
^tASC	0		0		ns
^tASR	0		0		ns
^tCAH	8		10		ns
^tCAS	8	10,000	10	10,000	ns
^tCRP	5		5		ns
^tCSH	38		45		ns
^tCWL	8		15		ns
^tDH	8		10		ns
^tDS	0		0		ns
^tRAD	9		12		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tRAH	9		10		ns
^tRAS	50	10,000	60	10,000	ns
^tRC	84		104		ns
^tRCD	11		14		ns
^tRP	30		40		ns
^tRSH	13		15		ns
^tRWL	13		15		ns
^tWCH	8		10		ns
^tWCR	38		45		ns
^tWCS	0		0		ns
^tWP	5		5		ns

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

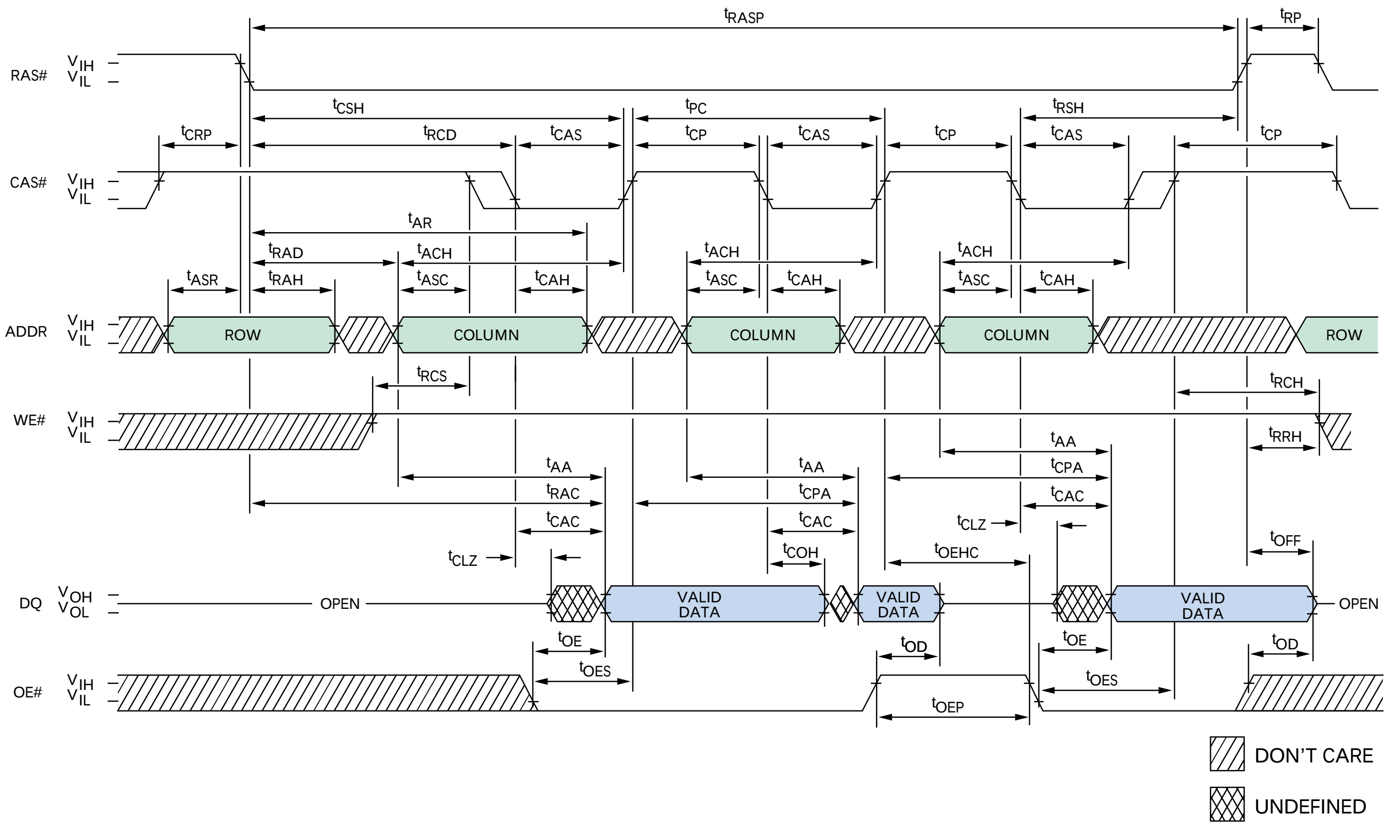


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tAA		25		30	ns
^tACH	12		15		ns
^tAR	38		45		ns
^tASC	0		0		ns
^tASR	0		0		ns
^tAWD	42		49		ns
^tCAC		13		15	ns
^tCAH	8		10		ns
^tCAS	8	10,000	10	10,000	ns
^tCLZ	0		0		ns
^tCRP	5		5		ns
^tCSH	38		45		ns
^tCWD	28		35		ns
^tCWL	8		10		ns
^tDH	8		10		ns
^tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tOD	0	12	0	15	ns
^tOE		12		15	ns
^tOEH	8		10		ns
^tRAC		50		60	ns
^tRAD	9		12		ns
^tRAH	9		10		ns
^tRAS	50	10,000	60	10,000	ns
^tRCD	11		14		ns
^tRCS	0		0		ns
^tRP	30		40		ns
^tRSH	13		15		ns
^tRWC	116		140		ns
^tRWD	67		79		ns
^tRWL	13		15		ns
^tWP	5		5		ns

EDO-PAGE-MODE READ CYCLE

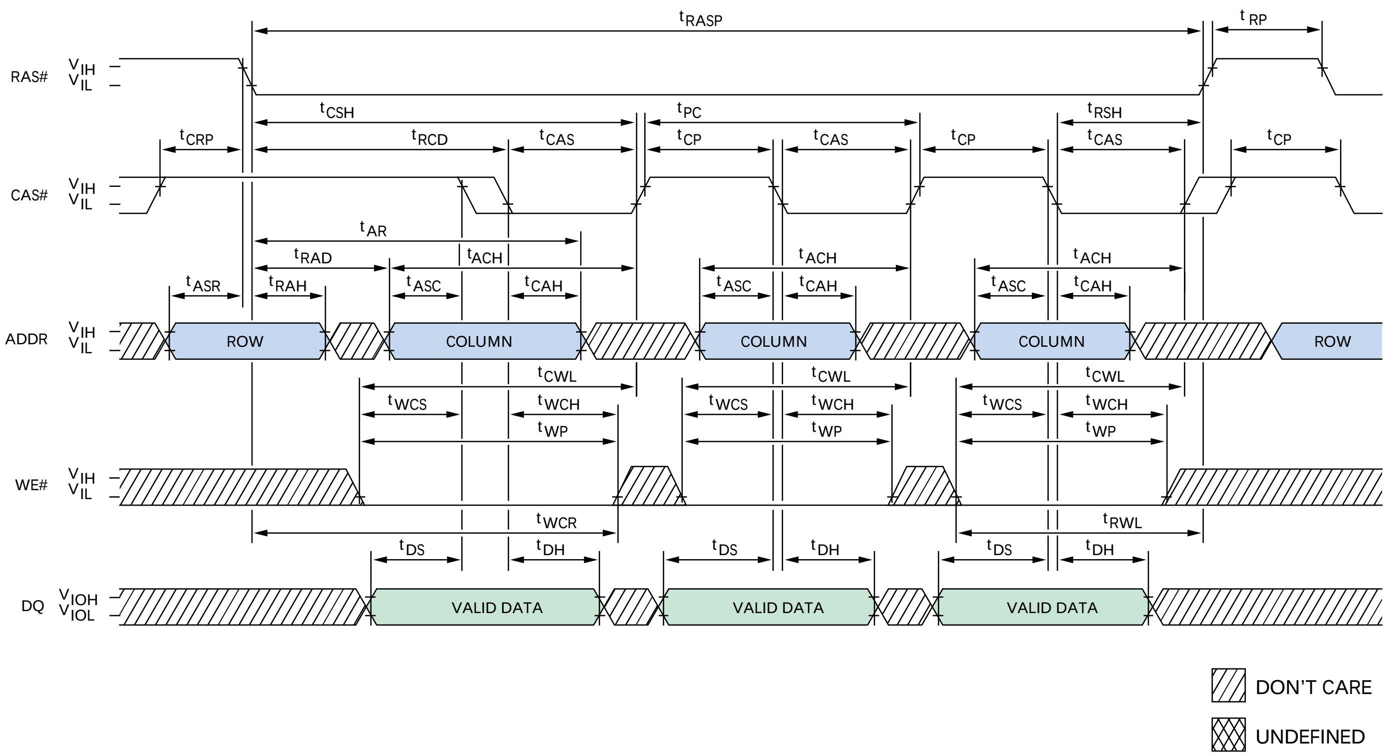


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
${}^tAA$		25		30	ns
${}^tACH$	12		15		ns
${}^tAR$	38		45		ns
${}^tASC$	0		0		ns
${}^tASR$	0		0		ns
${}^tCAC$		13		15	ns
${}^tCAH$	8		10		ns
${}^tCAS$	8	10,000	10	10,000	ns
${}^tCLZ$	0		0		ns
${}^tCOH$	3		3		ns
${}^tCP$	8		10		ns
${}^tCPA$		28		35	ns
${}^tCRP$	5		5		ns
${}^tCSH$	38		45		ns
${}^tOD$	0	12	0	15	ns
${}^tOE$		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
${}^tOEHC$	5		10		ns
${}^tOEP$	5		5		ns
${}^tOES$	4		5		ns
${}^tOFF$	0	12	0	15	ns
${}^tPC$	20		25		ns
${}^tRAC$		50		60	ns
${}^tRAD$	9		12		ns
${}^tRAH$	9		10		ns
${}^tRASP$	50	125,000	60	125,000	ns
${}^tRCD$	11		14		ns
${}^tRCH$	0		0		ns
${}^tRCS$	0		0		ns
${}^tRP$	30		40		ns
${}^tRRH$	0		0		ns
${}^tRSH$	13		15		ns

EDO-PAGE-MODE EARLY WRITE CYCLE

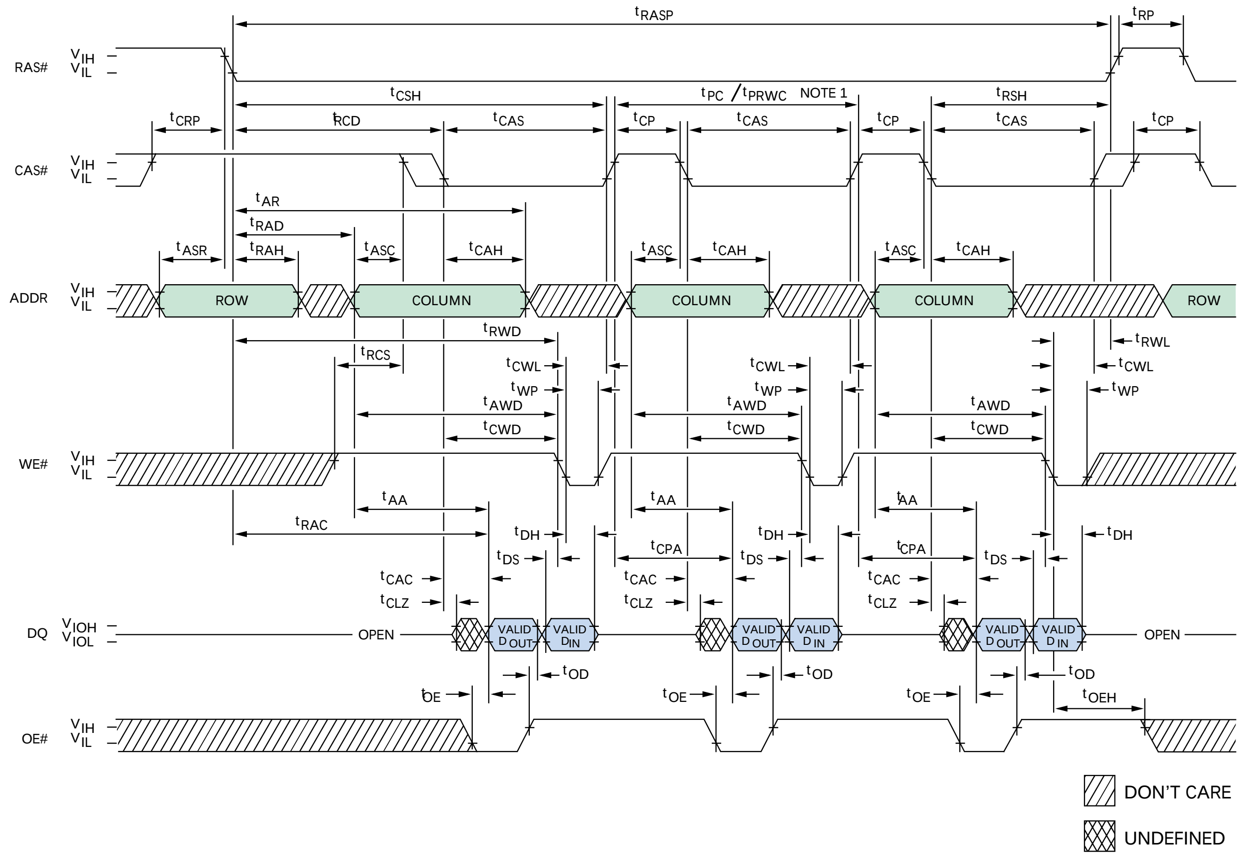


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^{t}ACH	12		15		ns
^{t}AR	38		45		ns
^{t}ASC	0		0		ns
^{t}ASR	0		0		ns
^{t}CAH	8		10		ns
^{t}CAS	8	10,000	10	10,000	ns
^{t}CP	8		10		ns
^{t}CRP	5		5		ns
^{t}CSH	38		45		ns
^{t}CWL	8		10		ns
^{t}DH	8		10		ns
^{t}DS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^{t}PC	20		25		ns
^{t}RAD	9		12		ns
^{t}RAH	9		10		ns
^{t}RASP	50	125,000	60	125,000	ns
^{t}RCD	11		14		ns
^{t}RP	30		40		ns
^{t}RSH	13		15		ns
^{t}RWL	13		15		ns
^{t}WCH	8		10		ns
^{t}WCR	38		45		ns
^{t}WCS	0		0		ns
^{t}WP	5		5		ns

EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



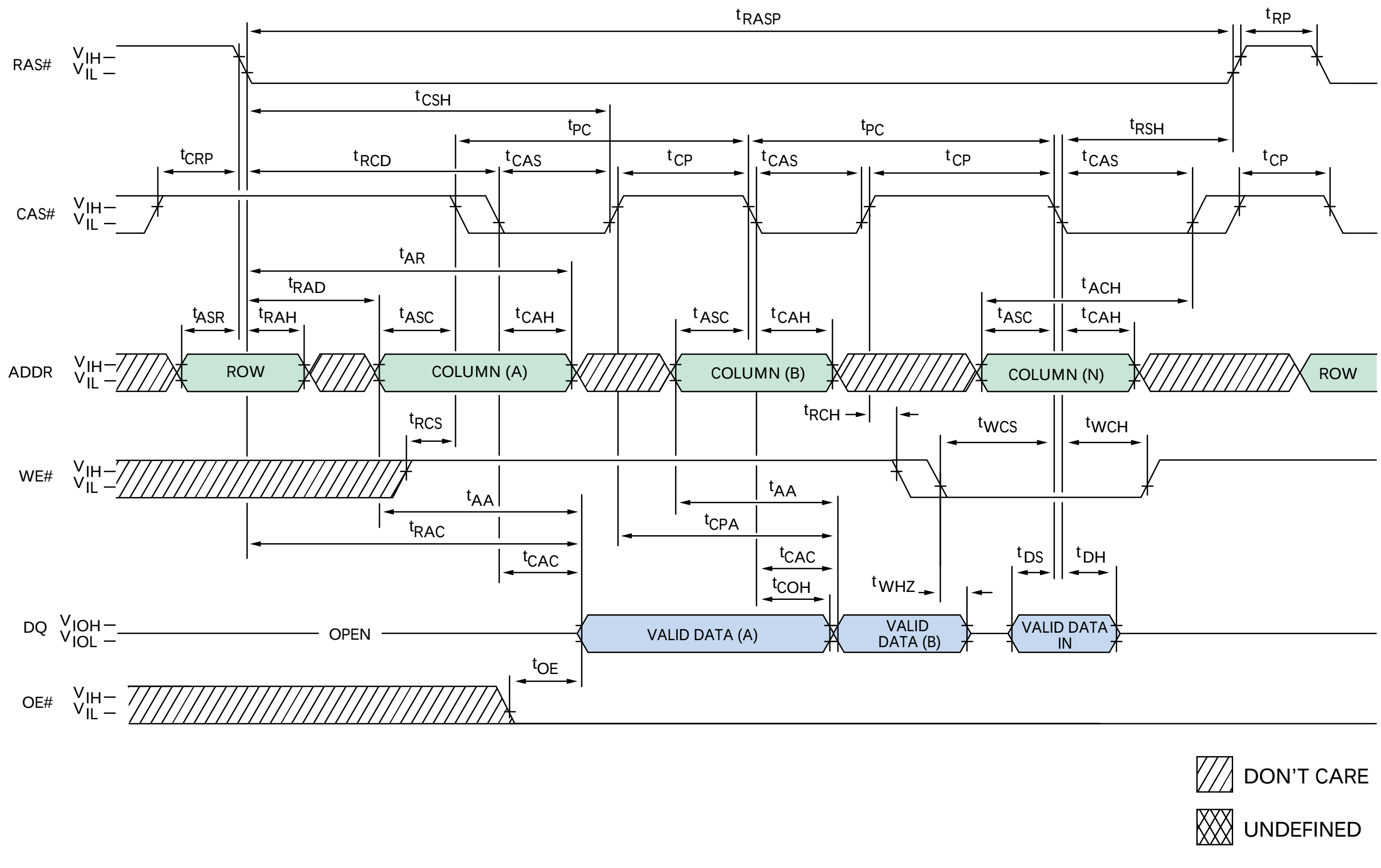
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tAA		25		30	ns
^tAR	38		45		ns
^tASC	0		0		ns
^tASR	0		0		ns
^tAWD	42		49		ns
^tCAC		13		15	ns
^tCAH	8		10		ns
^tCAS	8	10,000	10	10,000	ns
^tCLZ	0		0		ns
^tCP	8		10		ns
^tCPA		28		35	ns
^tCRP	5		5		ns
^tCSH	38		45		ns
^tCWD	28		35		ns
^tCWL	8		10		ns
^tDH	8		10		ns
^tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tOD	0	12	0	15	ns
^tOE		12		15	ns
^tOEH	8		12		ns
^tPC	20		25		ns
^tPRWC	47		56		ns
^tRAC		50		60	ns
^tRAD	9		12		ns
^tRAH	9		10		ns
^tRASP	50	125,000	60	125,000	ns
^tRCD	11		14		ns
^tRCS	0		0		ns
^tRP	30		40		ns
^tRSH	13		15		ns
^tRWD	67		79		ns
^tRWL	13		15		ns
^tWP	5		5		ns

NOTE: 1. ^tPC is for LATE WRITE cycles only.

EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

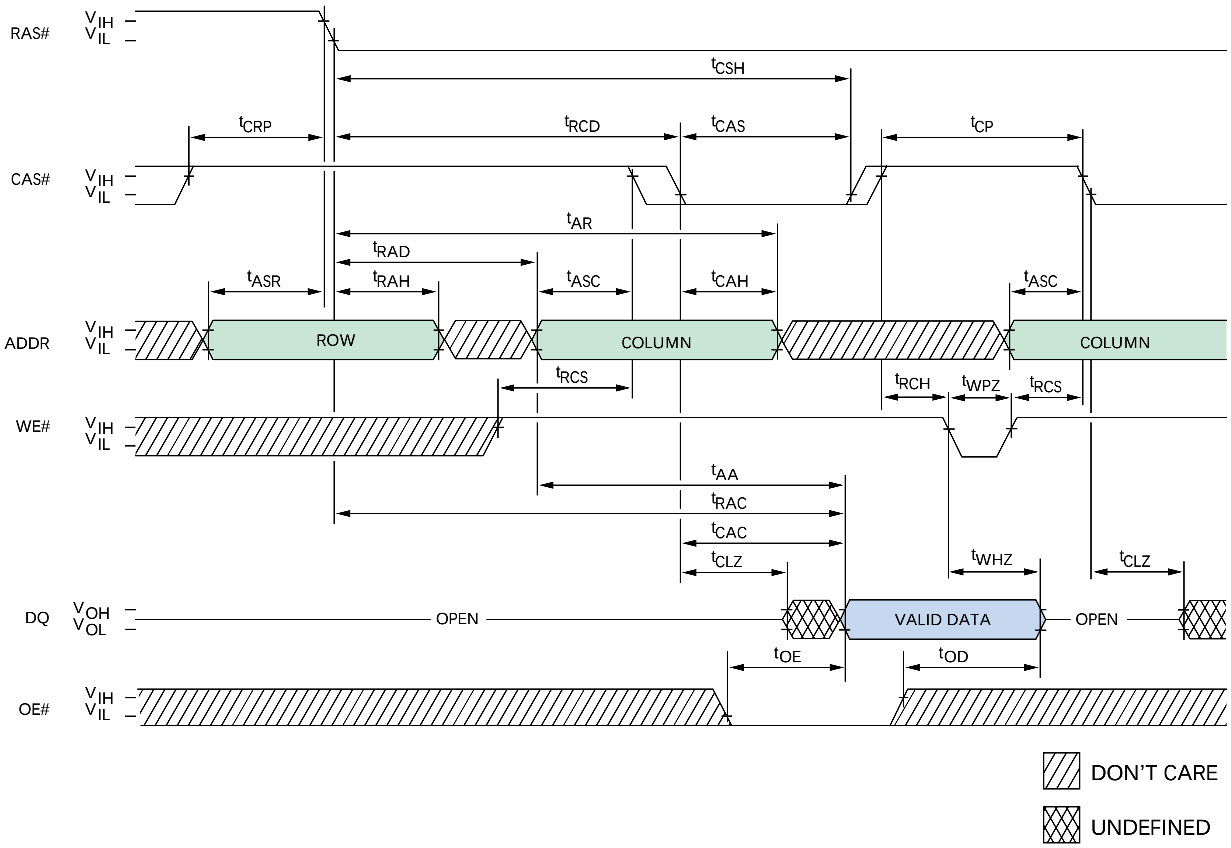


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWHZ	0	12	0	15	ns

READ CYCLE
(with WE#-controlled disable)



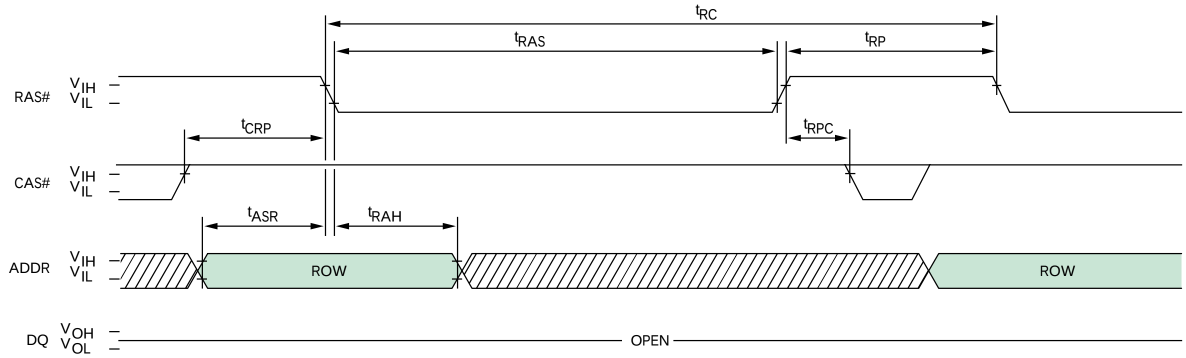
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tAA		25		30	ns
^tAR	38		45		ns
^tASC	0		0		ns
^tASR	0		0		ns
^tCAC		13		15	ns
^tCAH	8		10		ns
^tCAS	8	10,000	10	10,000	ns
^tCLZ	0		0		ns
^tCP	8		10		ns
^tCRP	5		5		ns
^tCSH	38		45		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tOD	0	12	0	15	ns
^tOE		12		15	ns
^tRAC		50		60	ns
^tRAD	9		12		ns
^tRAH	9		10		ns
^tRCD	11		14		ns
^tRCH	0		0		ns
^tRCS	0		0		ns
^tWHZ		12		15	ns
^tWPZ	10		10		ns

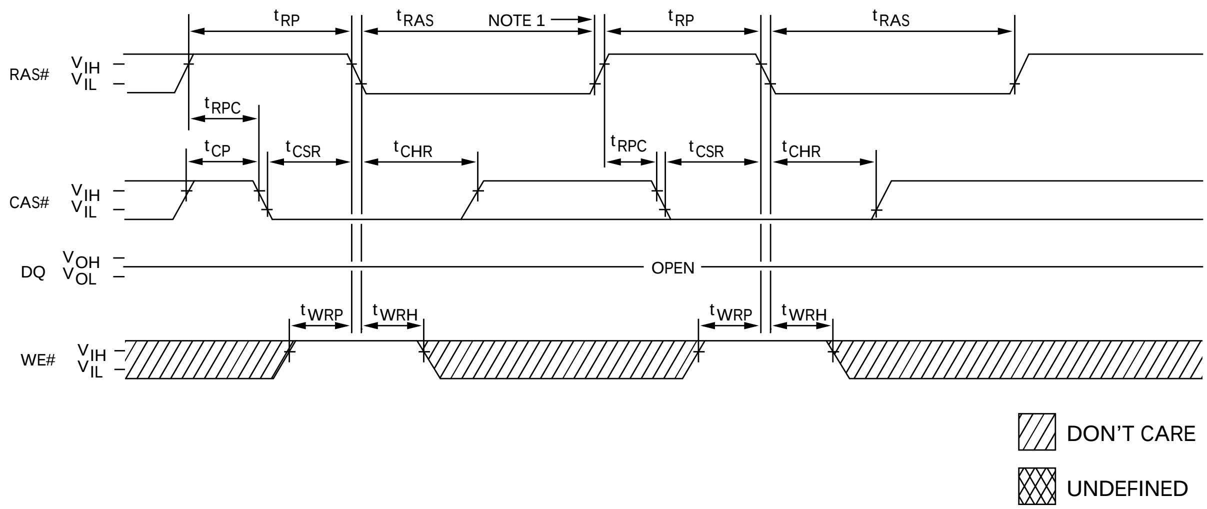
RAS#-ONLY REFRESH CYCLE

(OE# and WE# = DON'T CARE)



CBR REFRESH CYCLE

(Addresses and OE# = DON'T CARE)



TIMING PARAMETERS

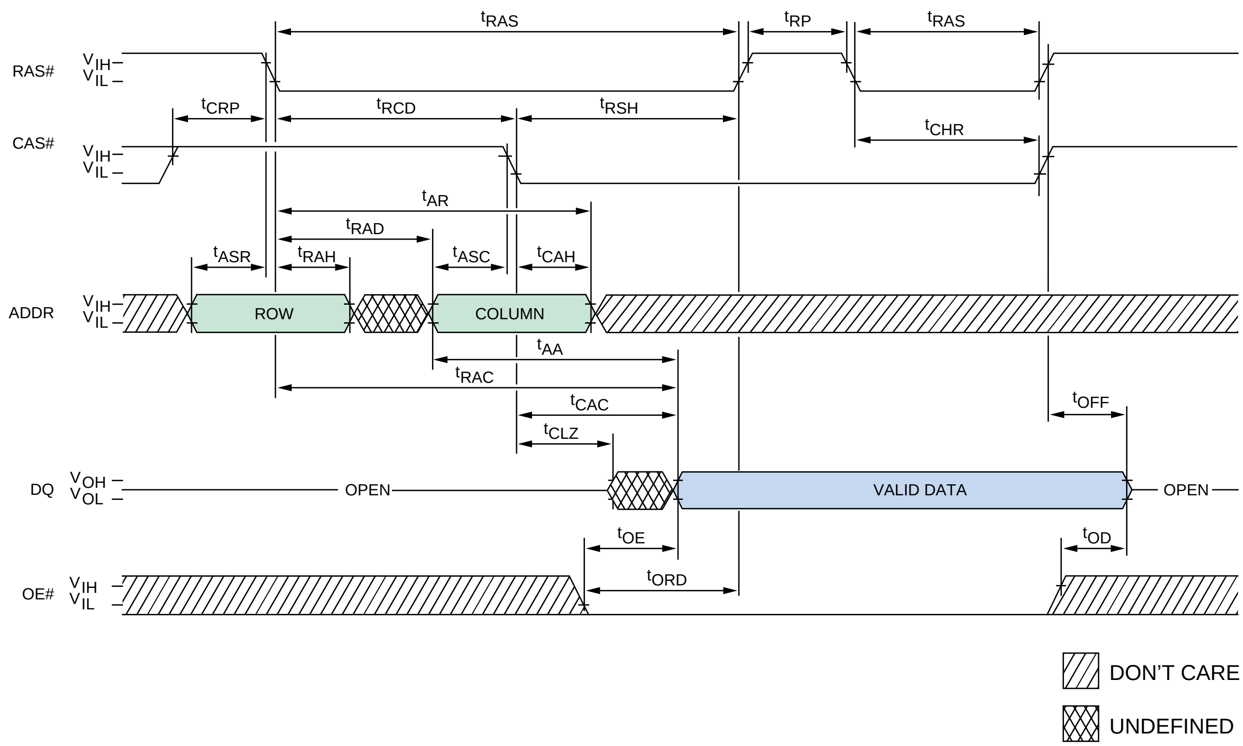
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^{t}ASR	0		0		ns
^{t}CHR	8		10		ns
^{t}CP	8		10		ns
^{t}CRP	5		5		ns
^{t}CSR	5		5		ns
^{t}RAH	9		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^{t}RAS	50	10,000	60	10,000	ns
^{t}RC	84		104		ns
^{t}RP	30		40		ns
^{t}RPC	5		5		ns
^{t}WRH	8		10		ns
^{t}WRP	8		10		ns

NOTE: 1. End of first CBR REFRESH cycle.

HIDDEN REFRESH CYCLE [1]

(WE# = HIGH; OE# = LOW)



TIMING PARAMETERS

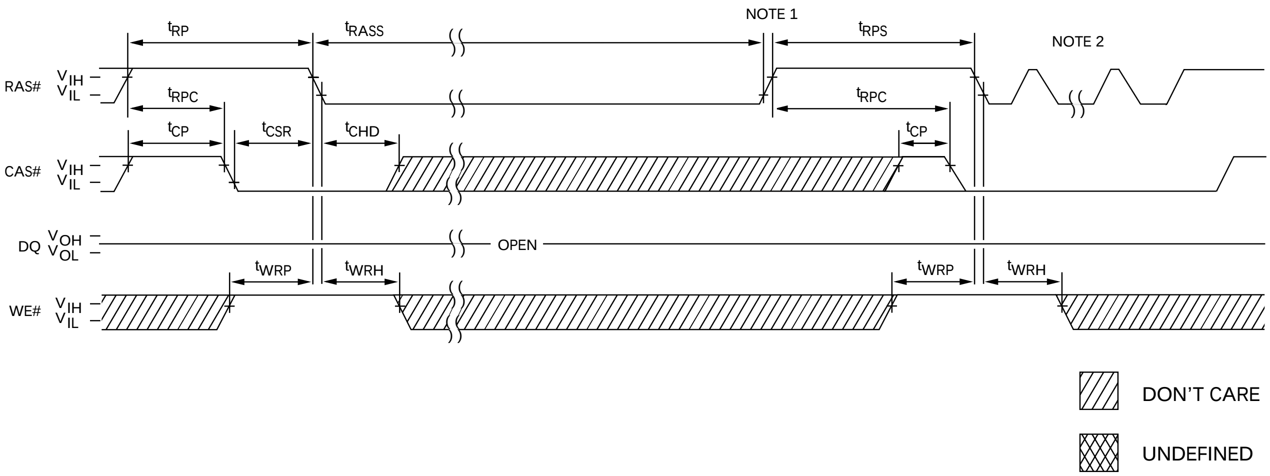
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tAA		25		30	ns
^tAR	38		45		ns
^tASC	0		0		ns
^tASR	0		0		ns
^tCAC		13		15	ns
^tCAH	8		10		ns
^tCHR	8		10		ns
^tCLZ	0		0		ns
^tCRP	5		5		ns
^tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tOE		12		15	ns
^tOFF	0	12	0	15	ns
^tORD	0		0		ns
^tRAC		50		60	ns
^tRAD	9		12		ns
^tRAH	9		10		ns
^tRAS	50	10,000	60	10,000	ns
^tRCD	11		14		ns
^tRP	30		40		ns
^tRSH	13		15		ns

NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.

SELF REFRESH CYCLE

(Addresses and OE# = DON'T CARE)



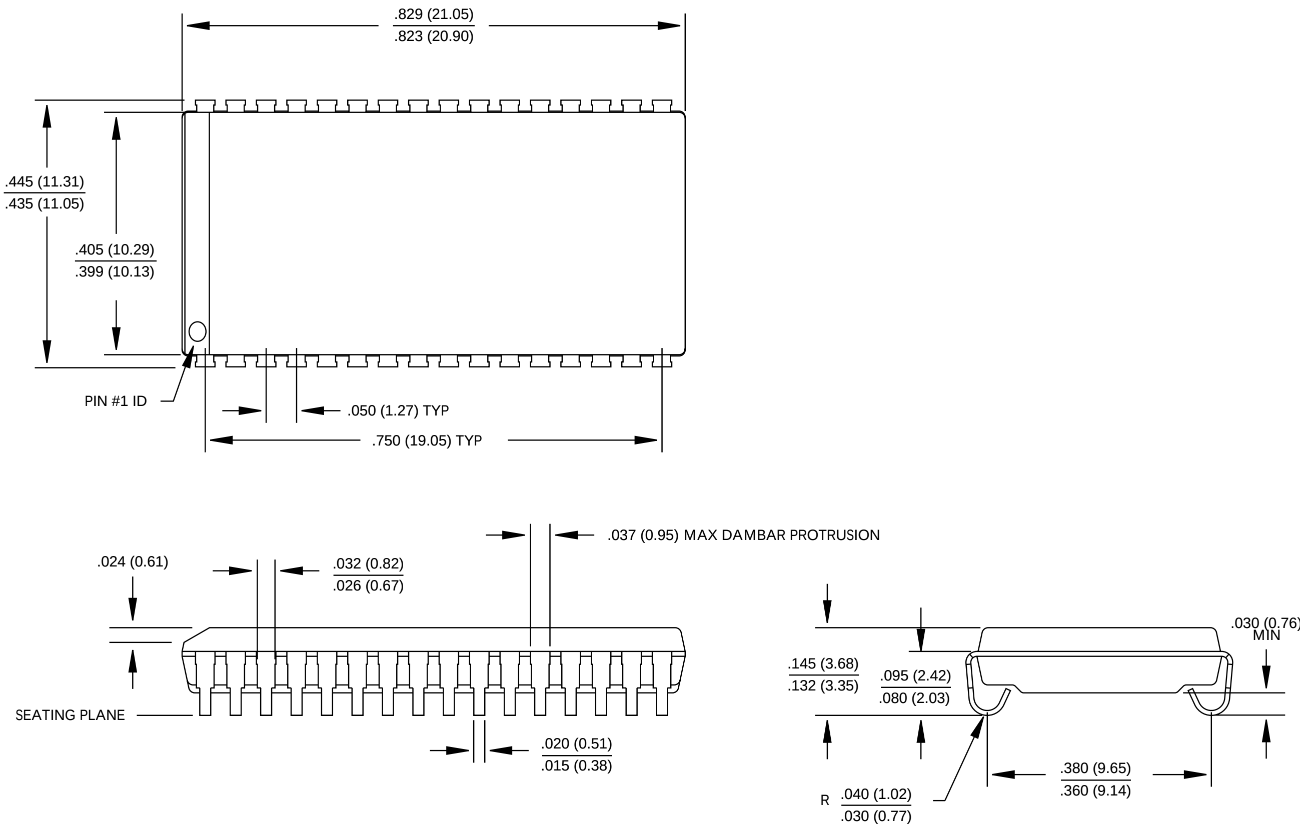
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tCHD	15		15		ns
^tCP	8		10		ns
^tCSR	5		5		ns
^tRASS	100		100		µs
^tRP	30		40		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tRPC	5		5		ns
^tRPS	90		105		ns
^tWRH	8		10		ns
^tWRP	8		10		ns

NOTE: 1. Once ^{t}RASS (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed if RAS#-only or burst CBR refresh

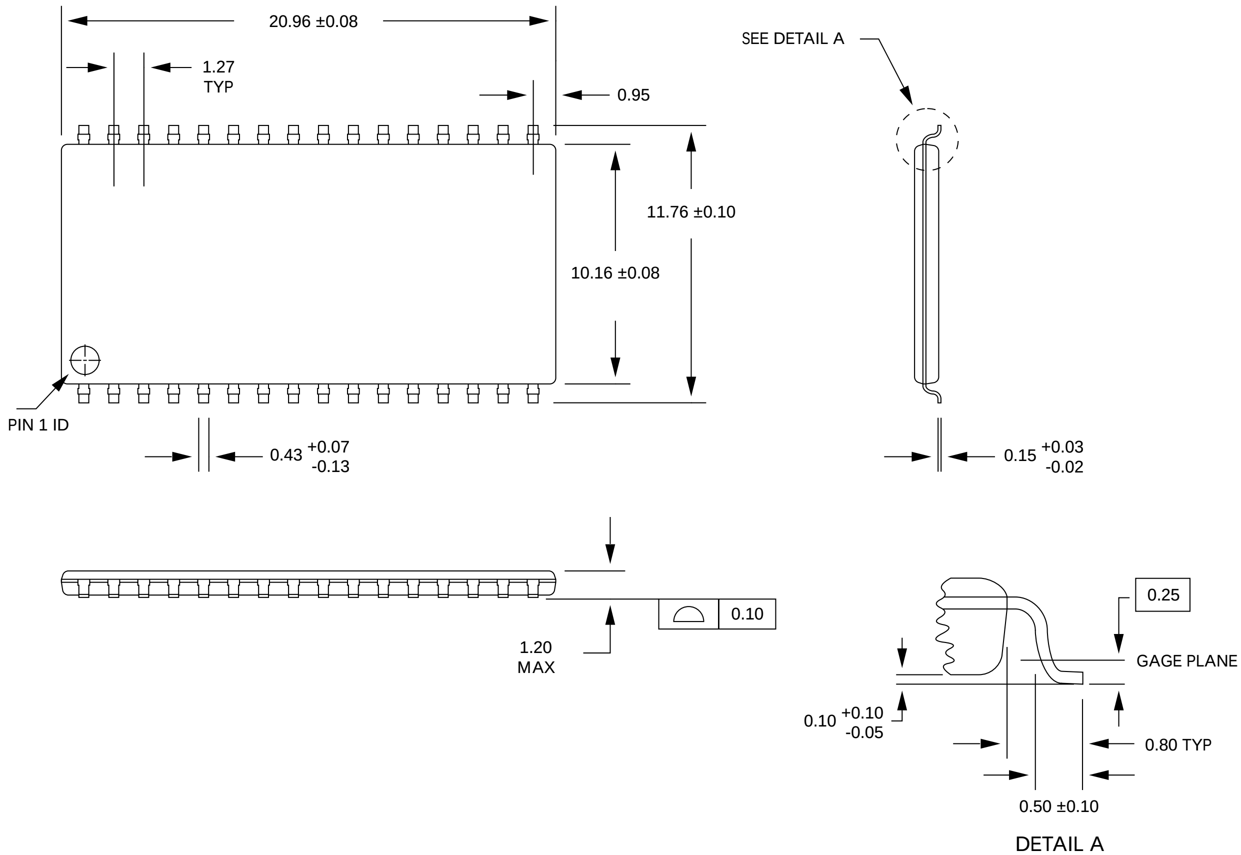
32-PIN PLASTIC SOJ (400 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC TSOP (400 mil)



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .25mm per side.

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