10 Gigabit/s Ethernet Transceiver with OC-192c Framer and XAUI Interface

The TenGiPHY™-W is a single chip transceiver IC for 10 Gbit/s Ethernet and Fibre Channel connectivity. It offers a serial, full duplex 10 Gbit/s interface to an optical sub-module. The integrated CDR and CMU operate at data rates between 9.95328 and 10.51875Gbit/s. The TenGiPHY-W provides the XGXS, PCS and PMA sublayers of the 10G Ethernet and Fibre Channel standards. For WAN applications a standard OC-192/STM-64 SONET/SDH framer together with flexible clocking modes enables a direct connection to the public network without additional components.

The networking system can control the chip via a narrow-width MDIO interface by writing and reading its control and status registers.

Applications

- Fiber optic modules according to the XENPAK multi-source agreement
- 10 Gbit/s Ethernet and Fibre Channel line cards
- Ethernet backbones in Metro Area Networks
- Terabit Routers

Features

- Complete 10 Gbit/s Ethernet and Fibre Channel PHY supporting WAN and LAN applications
- Complies with IEEE 802.3ae
- Compliant to XENPAK multi-source agreement
- Complies with ANSI 1413-D
- Embedded µController allows for control and tuning of the PMDs via analog interfaces
- Clock & data recovery and clock multiplying unit without external loop filter components
- Complies with jitter tolerance and jitter transmit requirements according to Telcordia GR-1244-CORE and ITU-T G.825
- Supports various clocking modes based on external reference clocks, loop- and external timing
- Integrated bit error rate tester (BERT) usable for multiple at-speed diagnostic scenarios
- Includes the XGXS, PCS, WIS, and PMA sublayers of the OSI protocol stack
- Synchronization and de-skewing of XAUI lanes
- Integrated standard STS-192/ STM-64 SONET/SDH framer according to GR-253-CORE, ANSI T1. 105/416, ITU-T G.707.
- Optionally maps/extracts 10 Gbit/s Ethernet packets into/ from the STS-192c/VC4-64c payload or conveys them to the serial interface directly
- Performance monitoring according to ANSI T1. 231
- Various loop back modes for system debugging
- Provides access to E²PROM via I²C interface according to XENPAK requirements; automatic E²PROM download on power-up
- Power-efficient design: <1.3W @ 1.3V

Interfaces

- Full duplex, XFI compliant serial CML line interface for data rates between 9.95 and 10.5 Gbit/s
- Quad serial Gbit/s XAUI interface with data rates between 3.1 and 3.2 Gbit/s
- MDIO interface
- I²C bus interface
- XENPAK diagnostic interface providing eight 12-bit ADCs and four 10-bit DACs
- IEEE 1149.1 JTAG boundary scan interface

UPF 01002

TenGiPHY™-W

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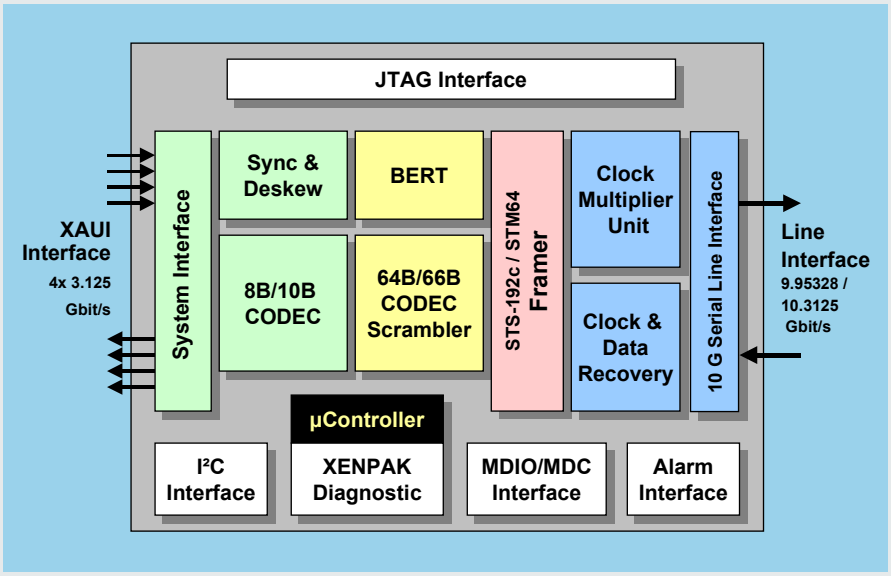
Never stop thinking.

Block Diagram

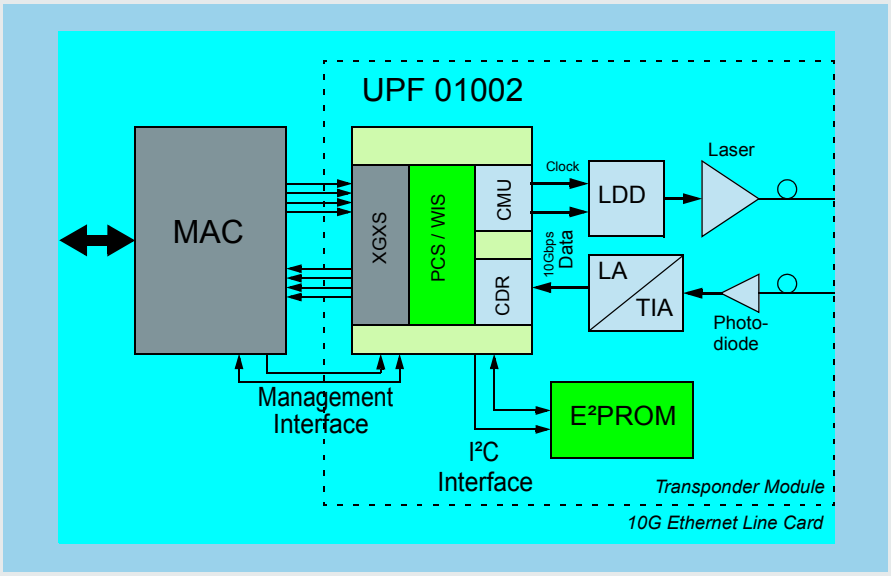


Documentation and Support Package

- Data Sheet
- **Hardware Evaluation System** includes mother- and transponder board
- **WINEASY** Software for MS Windows with graphical user interface
- **Application Assistant:** Configuration Software for MS Windows for device initialization

Type	Sales Code	Package
TenGiPHY-W	UPF 01002	P-FCHBGA-177-1

Application Example



How to reach us:
http://www.infineon.com

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