PRELIMINARY

BAND PASS FILTER FOR AUDIO SPECTRUM ANALYZER DISPLAY

■ GENERAL DESCRIPTION

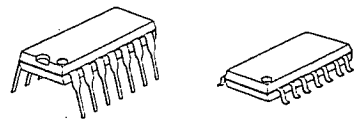
The NJU7508 is a band pass filter for spectrum analyzer display, which contains high and low band pass filter, oscillation circuit, clock generator, control circuit, Σ output circuit and DC transfer circuit.

The band pass filter consists of 11-band each for left and right channels, and used switched capacitor filter.

The data for left and right channels are output by serial, therefore it is realized in small package.

The NJU7508 is used in graphic equalizer system and other audio graphic applications.

■ PACKAGE OUTLINE

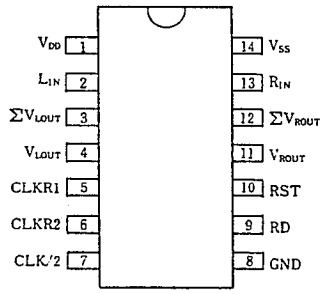


NJU7508D NJU7508M

■ FEATURES

- Band pass filter for stereo application spectrum analyzer
- Band pass filter for audio frequency band
- Left and Right Σ output circuit for each bands peak value
- DC transfer and peak hold circuit On-chip
- Switched capacitor filter Technology
- CR oscillation circuit On-chip, External R required
- Package Outline -- DIP14 / DMP14
- C-MOS Technology

■ PIN CONFIGURATION



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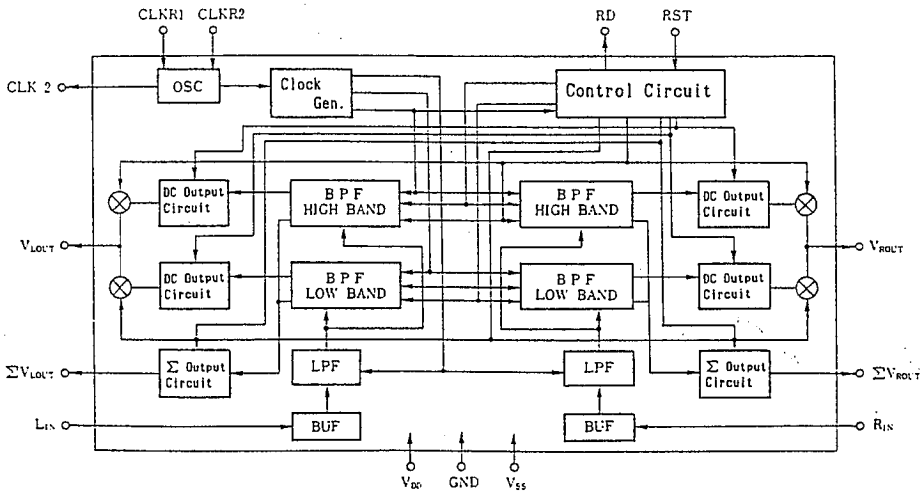
■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
1 8 14	V_{DD} GND V_{SS}	Positive power supply +5.0 V GND 0 V Negative power supply -5.0 V
2 13	L_{IN} R_{IN}	L-channel audio signal input terminal. R-channel audio signal input terminal.
4 11	V_{LOUT} V_{ROUT}	L-channel band pass filter output terminal. R-channel band pass filter output terminal.
3 12	ΣV_{LOUT} ΣV_{ROUT}	L-channel band pass filter sigma-output terminal. R-channel band pass filter sigma-output terminal.
5 6	CLKR1 CLKR2	Oscillation terminal. External Resistor or Ceramic resonator connects to these terminals.
7	CLK/2	1/2 divided clock of system clock output terminal.
9	RD	Data read enable signal output terminal to external controller.
10	RST	Initialization signal input terminal.

■ PEAK FREQUENCY Corresponding to each band

BAND	PEAK FREQUENCY(Hz)
f1	16K
f2	8K
f3	4K
f4	2K
f5	1K
f6	750
f7	500
f8	380
f9	250
f10	120
f11	60

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■ FUNCTIONAL DESCRIPTION

(1) Interface to external controller

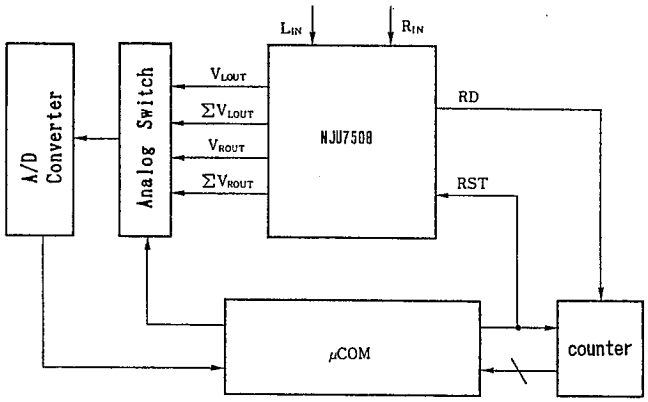
The NJU7508 outputs the filtered data for all bands of each channel by time shared serial output form to external controller.

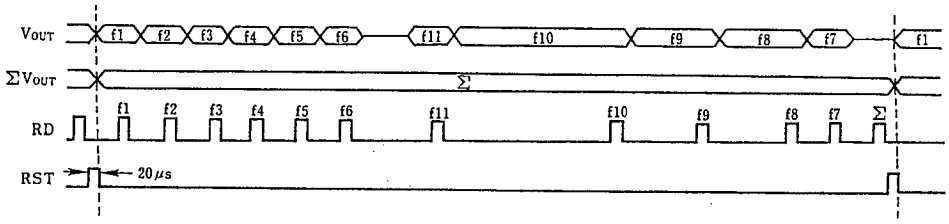
(1-1) An interface example with other micro controller and counter

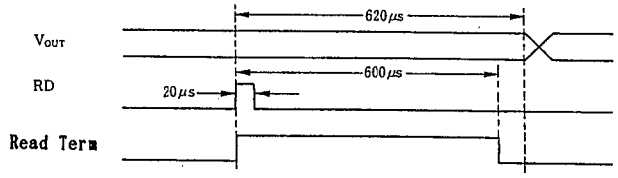
When the RST signal out from a micro controller input to the NJU7508, the internal circuits are initialized and each band data output from the NJU7508 serially as shown below time chart.

Just before the band changing, the NJU7508 outputs the RD signal to increase external counter.

A micro controller reads the output data of each band from the NJU7508 through the band judgment and analog switch which changed by 4 bit data of counter.





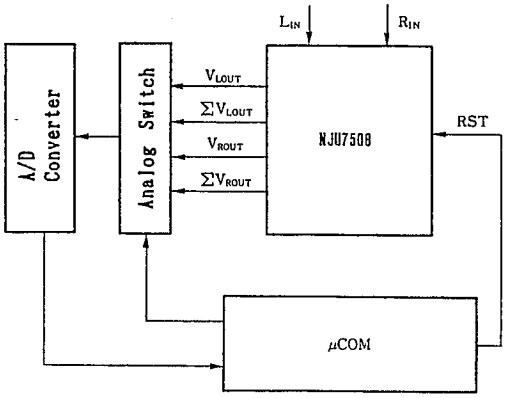


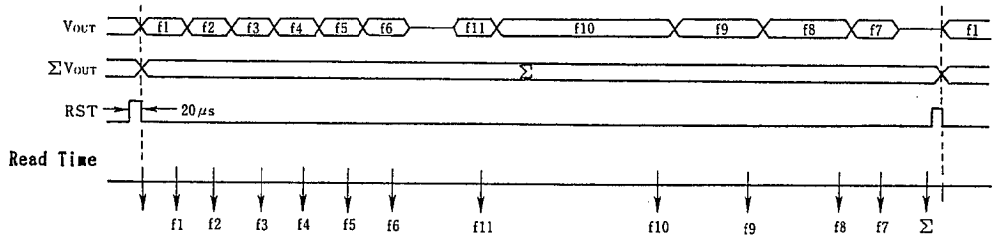
RD signal is output before 620 micro seconds to change the band of output data , then reading output data of each band should be performed within 600 micro seconds after fall edge of RD signal.

(1-2) An interface example with other micro controller

When the RST signal out from a micro controller input to the NJU7508, the internal circuits are initialized and each band data output from the NJU7508 serially as shown below time chart.

A micro controller reads the output data of each band from the NJU7508 through the analog switch which changed at the defined time (RST=0msec) of each band.





(RST=0msec)

BAND	Analog Switch Change Time(msec)
f1	9.62
f2	19.86
f3	30.10
f4	40.34
f5	50.58
f6	60.82
f11	81.30
f10	122.26
f9	142.74
f8	163.22
f7	173.46
Σ	183.70

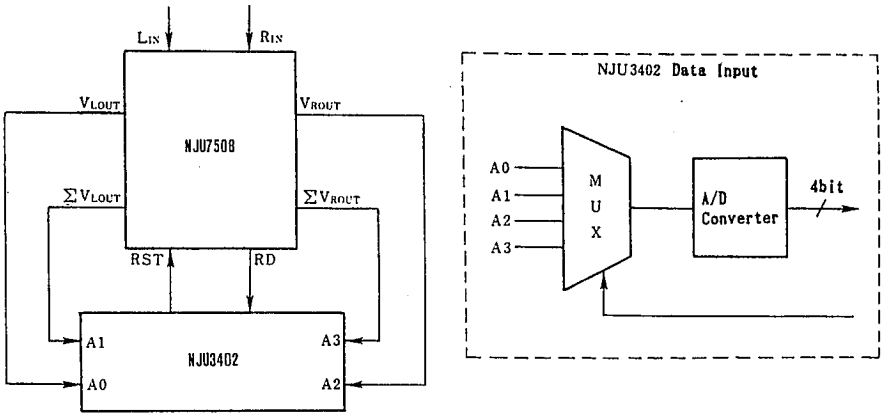
* This table shows for the 800kHz oscillation. If the oscillation frequency is changed, the time mentioned in the table also change proportionally.
The time mentioned in the table is as same as rise edge timing of the RD signal.

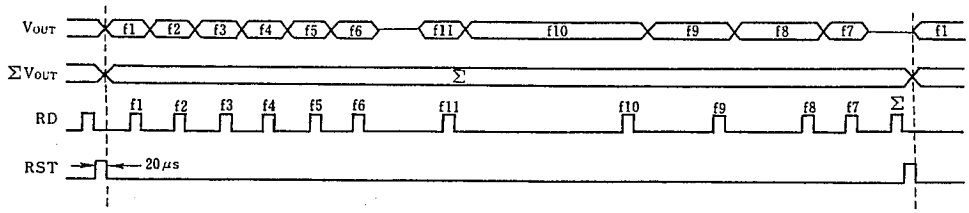
(1-3) An interface example with 4-bit micro controller NJU3402

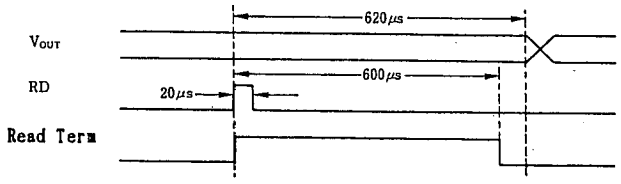
When The RST signal out from the NJU3402 input to the NJU7508, the internal circuits are initialized and each band data output from the NJU7508 serially as shown below time chart.

Just before the band changing, the NJU7508 outputs the RD signal as an interrupt signal to the NJU3402.

The NJU3402 counts the RD signal from the NJU7508, then the RST signal is output to the NJU7508 and the number of bands is determined.







RD signal is output before 620 micro seconds to change the band of output data , then reading output data of each band should be performed within 600 micro seconds after fall edge of RD signal.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	+7	V
	V_{SS}	-7	
Input Voltage	V_{IL} V_{IH}	0~V_{DD}+0.3 (RST Terminal)	V
	V_{ILC} V_{IHC}	0~V_{DD}+0.3 (CLKR Terminal)	
	V_{LIN} V_{RIN}	V_{SS}-0.3~V_{DD}+0.3 (L_{IN}, R_{IN} Terminals)	
Power Dissipation	PD	700 (DIP-14) 300 (DMP-14)	mW
Operating Temperature	T_{opr}	-30 ~ +80	°C
Storage Temperature	T_{stg}	-40 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(V_{DD}=+5V, V_{SS}=-5V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage	V_{DD}		4.5	5.0	5.5	V	
	V_{SS}		-4.5	-5.0	-5.5		
Operating Current	I_{DD}	V_{DD}=+5V, V_{SS}=-5V		10.0	20.0	mA	
Input Leak Current	I_{IL}	L_{IN}, R_{IN} Terminal	-10.0		10.0	μA	
Input Voltage	V_{IL}	RST Terminal	0		0.2V_{DD}	V	
	V_{IH}		0.8V_{DD}		V_{DD}		
Output Voltage	V_{OL}	R_L=100kΩ RD Terminal	0		0.1V_{DD}	V	
	V_{OH}		0.9V_{DD}		V_{DD}		
External Clock Input Voltage	V_{ILC}	CLKR2 Terminal	0		0.3V_{DD}	V	
	V_{IHC}		0.7V_{DD}		V_{DD}		
Clock Output Voltage	V_{OLC1}	CLKR1 Terminal	0		0.2V_{DD}	V	
	V_{OHC1}		0.8V_{DD}		V_{DD}		
Half Clock Output Voltage	V_{OLC2}	R_L=100kΩ CLK/2 Terminal	0		0.1V_{DD}	V	
	V_{OHC2}		0.9V_{DD}		V_{DD}		
Output Offset Voltage	V_{OS}	V_{IN}=0V $V_{OUT\ [L,R]}$ $\Sigma V_{OUT\ [L,R]}$ Terminal	0		500	mV	
BPF Output Voltage	V_{OUT}	f_{IN}=f1~f11 $V_{OUT\ [L,R]}$ Terminal V_{IN}=200mVpk		26.0		dB	
			3.5			V	
Σ Output Voltage	ΣV_{OUT}	f_{IN}=1kHz $\Sigma V_{OUT\ [L,R]}$ Terminal V_{IN}=200mVpk		26.0		dB	
			3.5			V	

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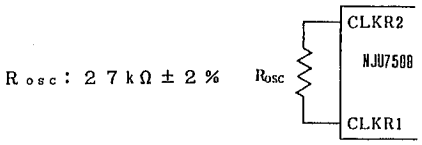
■ ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS

(V_{DD}=+5V, V_{SS}=-5V, Ta=25℃)

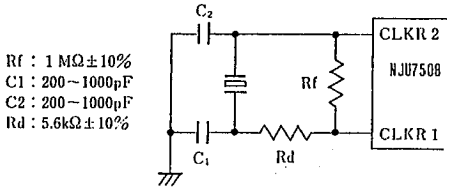
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Oscillation Clock Frequency	f_{OSC}	R_{OSC}=27kΩ±2% CLKR1 Terminal	720	800	880	kHz	1
		Ceramic Filter CLKR1,2 Terminal	770	800	830		2
External Clock Frequency	f_{CLK}	CLKR2 Terminal		800			3
RD Pulse Width	t_{PWRD}	f_{OSC}=800kHz RD Terminal		20		μs	4
RST Pulse Width	t_{PWRS}	RST Terminal	20				4
RST Rise,Fall Time	tr,tf	RST Terminal			100	ns	4
RD(Σ)→RST Time	V_{RDRS}	RD,RST Terminals	500			μs	4

NOTE 1) An example of the oscillation using a external resistor.



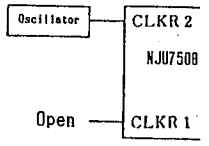
Short wiring is required to prevent a wide frequency drift by the stray capacitance of the CLKR1 and CLKR2 wiring.

NOTE 2) An example of the oscillation using a ceramic resonator.

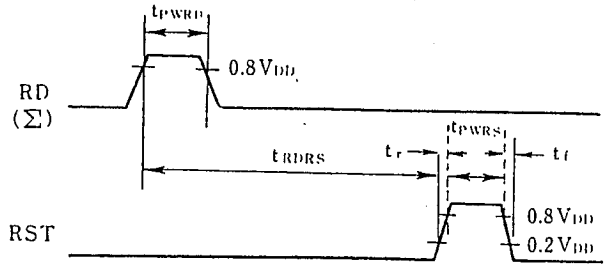


The circuit is one of the reference and it dose not guarantee the oscillation characteristic.
Optimization for external components is required.

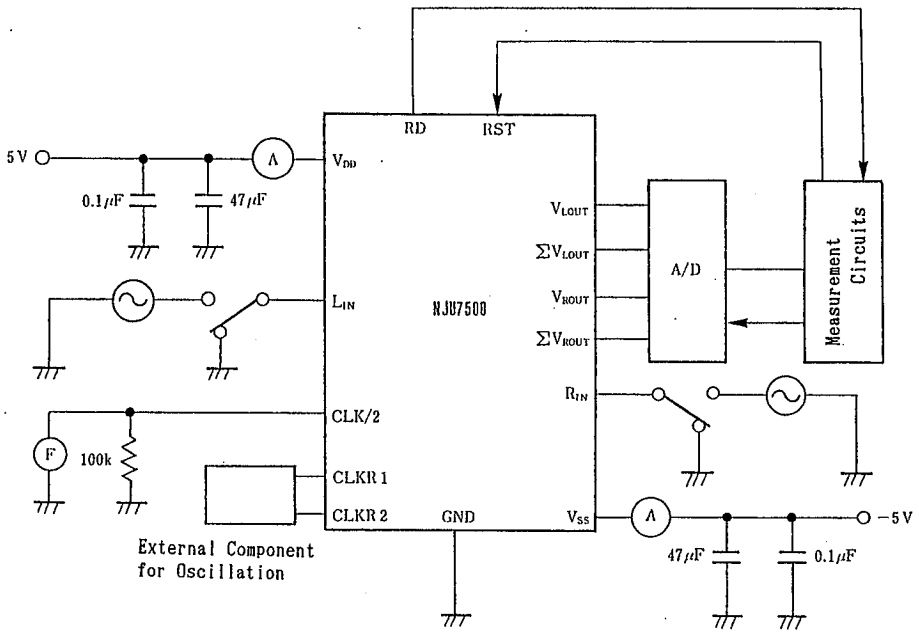
NOTE 3) An example of external clock using.



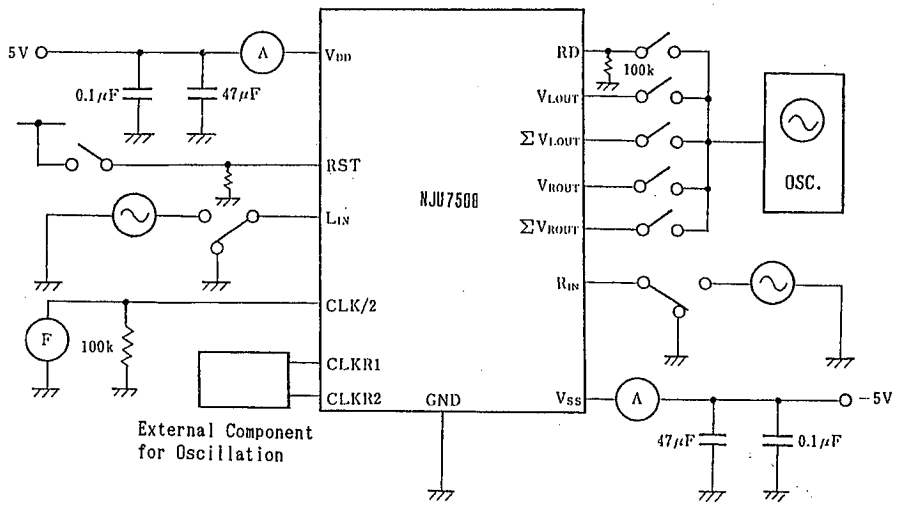
NOTE 4)



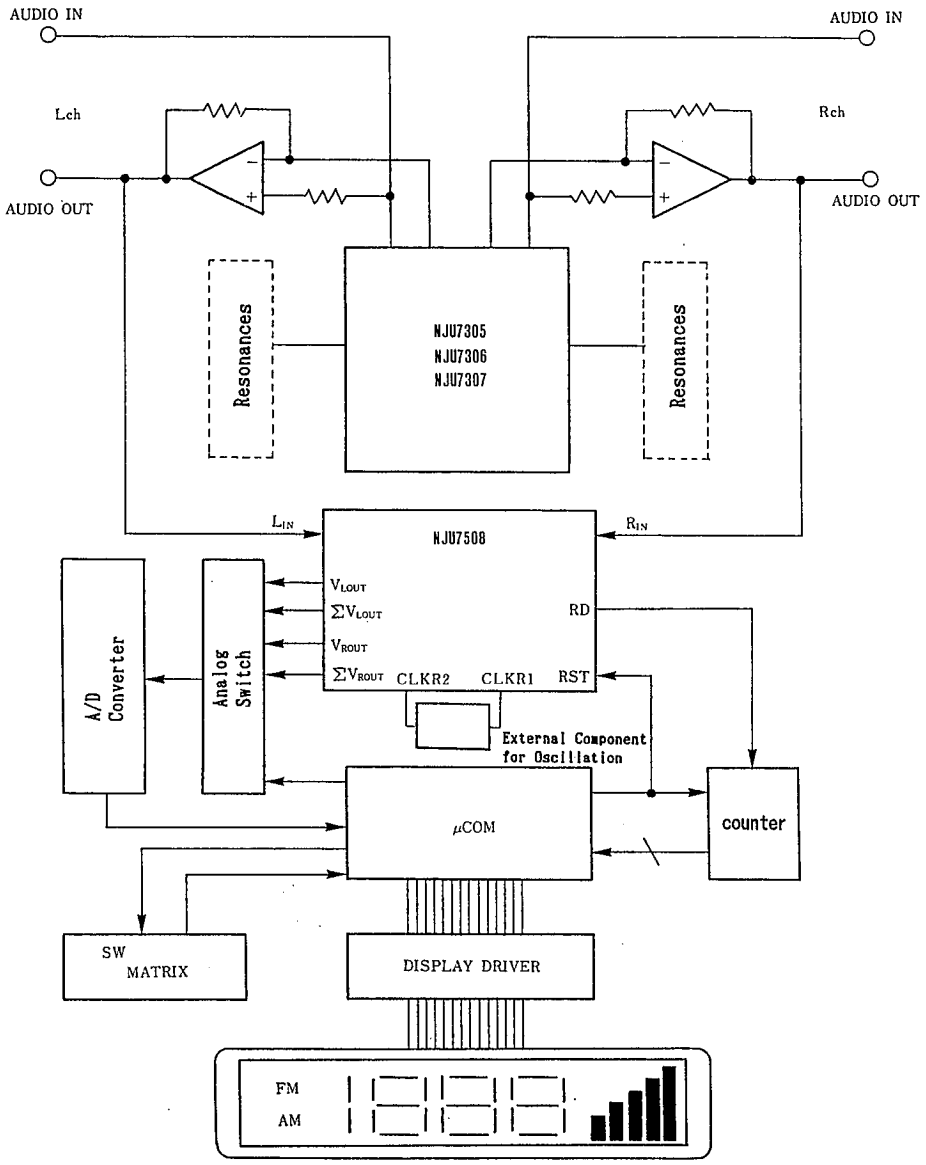
■ MEASUREMENT CIRCUIT (1)



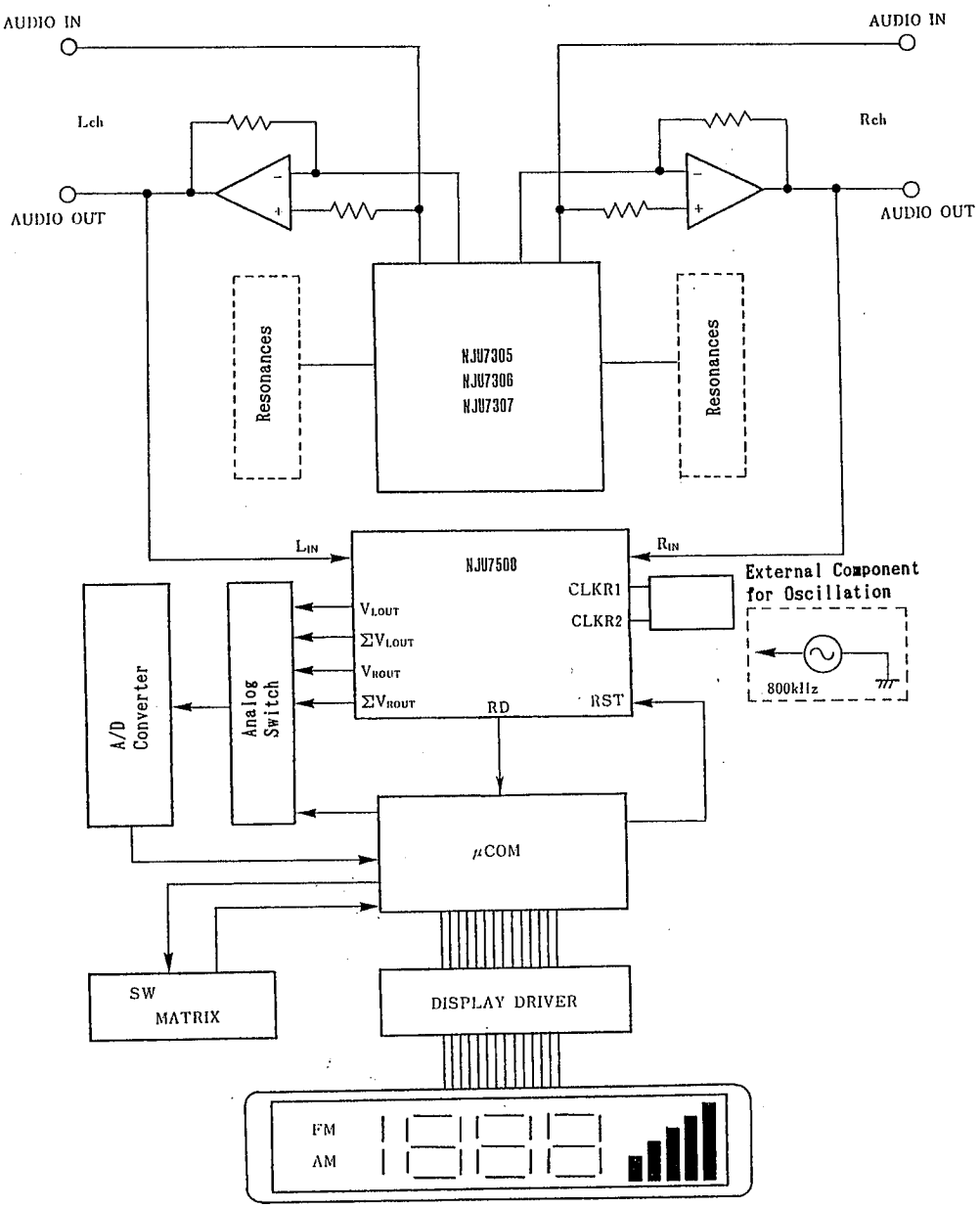
■ MEASUREMENT CIRCUIT (2)



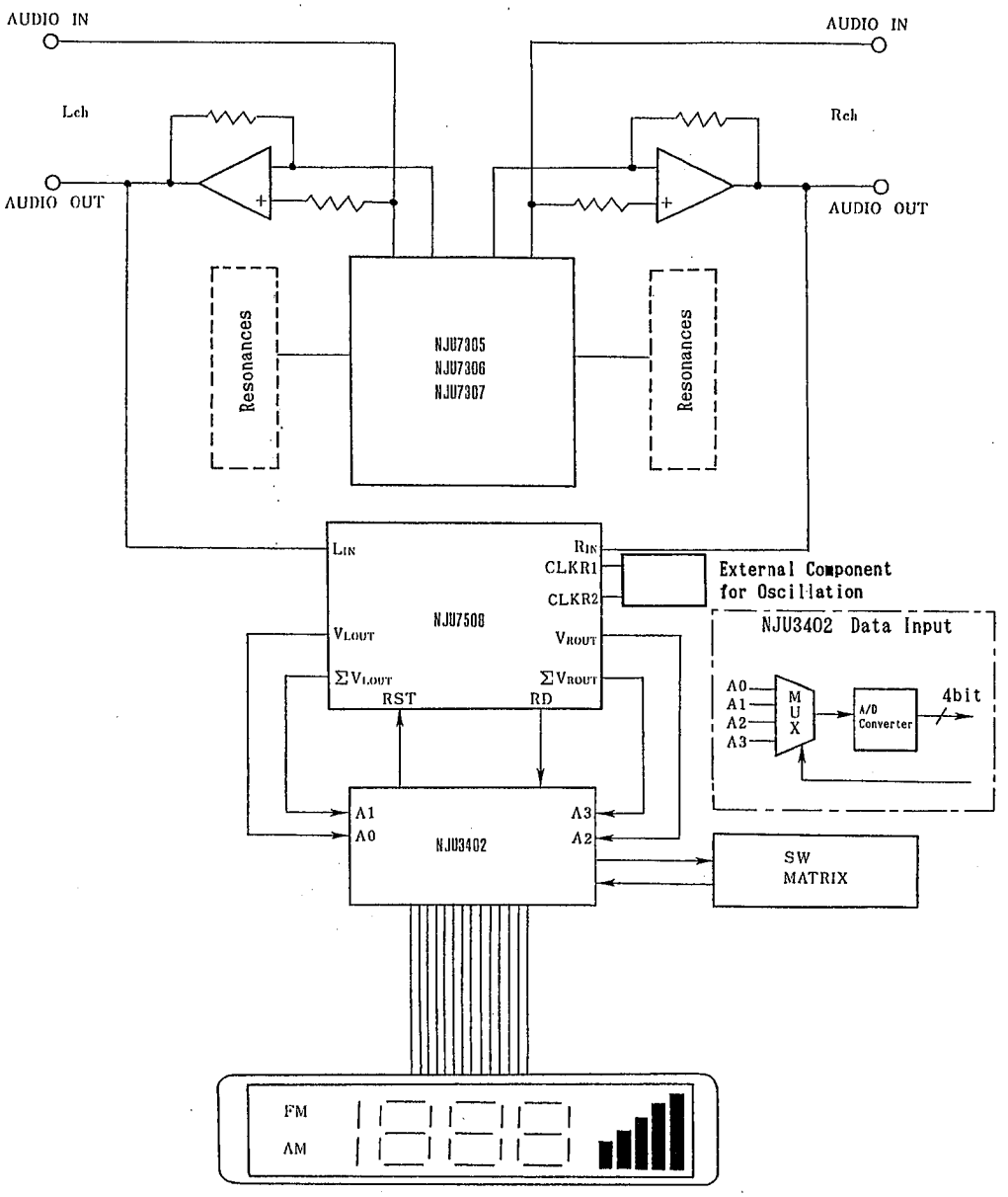
■ APPLICATION CIRCUIT (1)



APPLICATION CIRCUIT (2)



■ APPLICATION CIRCUIT (3)



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